MA 2187-09501-00
Issue 1

MAINTENANCE MANUAL

PORTABLE HF-SSB/AM RADIO SET

PRC-2200

JANUARY 1992

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont'd)

LIST OF ILLUSTRATIONS (Cont'd)

LIST OF ILLUSTRATIONS (Cont'd)

LIST OF ILLUSTRATIONS (Cont'd)

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1-1. SCOPE

a. This manual provides instructions for the maintenance of the HF Radio Set PRC-2200.

b. Detailed explanations of equipment block diagrams and circuit analysis are given in Chapter 2.

c. Chapter 3 provides maintenance instructions.

d. Equipment maintenance procedures and forms conform to standard user practice.

e. For operating, installation, and organizational maintenance instructions refer to the operator's manual.

f. Throughout this manual the following notations are used:

(1) The designations of the RT-2001/PRC-2200 and CP-2003/PRC-2200 are abbreviated as RT-2001, and CP-2003, respectively.

(2) The designations "high logic level" and "low logic level" are abbreviated as "high level" and "low level", respectively.

(3) Active-low logic lines are designated by an asterisk, *, following the name of the line.

CHAPTER 2

THEORY OF OPERATION

NOTE

The AJ, SEC, CCW, INTERNAL MODEM, FLASH, DUAL, NCW and/or AM modes are optional. Throughout this chapter refer to the circuits, performances requirements, signals, lines, tests, or measurements related to these modes as optional.

Section I. RADIO SET BLOCK DIAGRAM ANALYSIS

2-1. Functional Block Diagram

Radio Set PRC-2200 is a high-frequency (HF), single sideband (SSB), and amplitude modulation (AM), portable radio receiving/transmitting set which provides 285,000 RF channels at 100Hz spacing in the frequency range of 1.5000 to 29.9999 MHz.

a. Communication Services Provided by the PRC-2200.

(1) Signal modes. Three selections are provided:

(a) VOICE - for speech and modem signals.
(b) CW - CW telegraphy using normal receiver bandwidth.
(c) NCW - CW telegraphy using narrow receiver bandwidth for increased range and reduced interference.

The selection of a mode instructs the radio set to use the optimum parameters for the selected mode.

(2) Data transmission. Two basic selections are provided:

(a) Internal modem - for 50, 75 or 150 baud synchronous or asynchronous operation. The interface is RS-232C. This permits transmission of teletypewriter signal without additional equipment, while providing the protection of secure and anti-jamming operation, however this feature is now an option.

(b) External modem - for any data rate, as the data rate depends on modem characteristics. Usually, the maximum rate is 2400baud. Encryption/decryption must then also be provided by external equipment.

(3) Signal protection function. Three selections are provided:

(a) Clear (CLR) - radio transmits the clear input signals.

(b) Secure (SEC) - radio encrypts the transmitted signal with a key selected by the operator and decrypts the received signals, provided they were encrypted with the same key. The operator can select the key out of ten different keys that can be loaded and stored in the PRC-2200. In the SEC mode, the PRC-2200 can protect, as an option, not only voice communication, but also CW telegraphy and data transmitted by means of the internal modem.

(c) Anti-jamming (AJ) - radio transmit frequency changes rapidly during transmission, according to a random pattern determined by an operator-selected key and the receiver follows the hopping pattern, provided it uses the same key. The receiver thus remains tuned to the transmitter and can receive the transmitted signals.

Anti-jamming (AJ) operation is also called "frequency hopping".

(4) Selective calling. PRC-2200 uses digital selective calling, which means that the radio transmits an address (a digital identification code) at the beginning of each transmission. The address code is also repeated during the transmission. Each radio that receives the transmission checks the code against its receive address, and allows the received audio signal to pass to the output only when the codes match. Each address has two digits, and the operator selects both the transmitted address and its receive address.
There are a total of 31 addresses: 27 individual, 3 group and one broadcast address.

(a) The transmission of an individual address causes only the receiver loaded with that address to pass the received message.

(b) The transmission of a group address (00, 10 or 20) causes the receivers pertaining to that group (receivers with receive addresses starting with the same tens digit) to pass the received message.

(c) The transmission of the broadcast address (ALL) causes all receivers to pass the message.

The use of selective calling permits frequency reuse, greatly reduces operator fatigue (because the receiver output is muted at all times, except when receiving a message addressed to that particular receiver) and is very useful for implementing automatic retransmission stations. When using CW telegraphy, selective calling is the only way to mute audio output when desired signals are received.

(5) Speech processing. The PRC-2200 provides a standard speech processing, to increase the average transmit power.

(6) Squelch types. The PRC-2200 provides two types of squelch:

(a) Active squelch, using digital coding. This squelch is very reliable and can be used together with selective calling.

(b) Passive squelch, that is used for compatibility with existing HF radio equipment. The passive squelch is a syllabic squelch circuit that can be activated in the voice mode. The squelch circuit recognizes the syllabic structure of speech, and lets only voice messages pass to the audio outputs[other types of signals are blocked, thereby reducing noise background.

Both types of squelch circuits can be turned off.

(7) Frequency management - AUTOCALL function. The AUTOCALL function is used in the CLR and SEC modes to automatically establish a link on the quietest free channel that can support communications. This ensures that communication always takes place on the frequency that under the given conditions yields the best communication quality. The allowable frequencies are stored in two AUTOCALL frequency tables. Each table can contain up to 10 operator-selected frequencies. One of the two tables is selected by the operator (by means of the AUTO key and the associated functions), and the operating frequency is selected among the frequencies stored in the selected table. During AUTOCALL operation, the calling and called stations are identified by their selective call addresses. AUTOCALL link establishment procedure is performed as follows:

(a) The radio set continuously scans the frequencies in the selected table, and evaluates their quality (background noise, transmissions from other stations, etc) while searching for transmissions addressed to it.

(b) When a transmission is started, the calling radio set automatically selects the best free frequency, according to the conditions determined during the scan. On this frequency, the calling radio set transmits the address of the called set.

(c) When the called radio set detects this transmission, it stops on its frequency, and automatically transmits an acknowledgement to the calling station after calling transmission ends.

In response, the calling station evaluates reception quality. If quality is satisfactory, the calling station transmits an acknowledgement. If quality is not satisfactory, the calling station repeats step (b), on the next best frequency.

(d) After the acknowledgement of the selected frequency, both radio sets display a READY message and the selected frequency, and the operator can start the transmission.

(e) The radio sets continue to use the selected frequency as long as it is good enough. If quality degrades, the operators can command the radio sets to select again a frequency and continue the link on the new frequency, or disconnect the link.

(f) The link is maintained as long as there is traffic between the stations: about 40 seconds after traffic stops, the radio sets start scanning again. The operator can also press the RST button to break the link at any time and start scanning again. This action is accompanied by the message DISCONNECT in the displays of both radio sets, so that the other operator is also notified.

(g) If the link cannot be established on any of the frequencies contained in the selected frequency table, the radio set displays a NO COM message.

When making a group or a broadcast call, the AUTOCALL process is similar, except that after address transmission ends, the calling radio set does not wait for an acknowledgement before displaying READY.

b. PRC-2200 Units. The PRC-2200 comprises two main units, Receiver/Transmitter RT-2001 and Antenna Coupler, CP-2003.

Figure 2-1 shows the block diagram of the PRC-2200, and identifies the main modules.

(1) Receiver/Transmitter RT-2001 modules.

Module AUDIO - contains the analog audio signal processing circuit.

Module IF - contains the SSB and AM modulators and demodulators, the IF filters which determine transmitter and receiver bandwidth, and AGC circuit.

Module RF - contains the frequency translators of the transmitter and receiver, transmitter drivers receiver input circuits, and RCV filters.

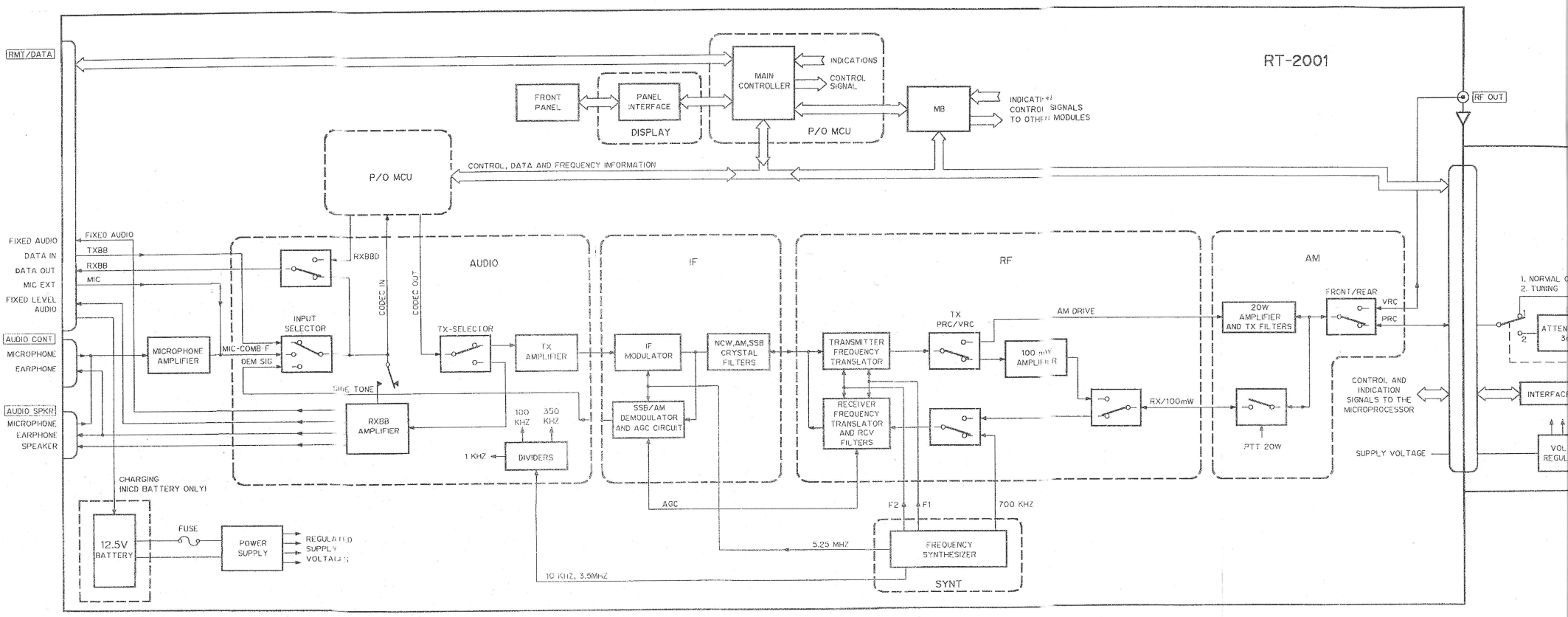
Module AM - contains the power amplifier of the transmitter, and TX filters.

Module MCU - contains a microprocessor system, which controls the operation of the radio set, in conjunction with the microprocessor in the CP-2003 and performs digital signal processing, encryption and decryption, and controls frequency hopping and AUTOCALL operation.

Module SYNT - contains the synthesizer system, which provides the various frequencies required by the RT-2001.

Module PANEL - contains the front-panel displays, and the interface to the front-panel controls. It also contains a microphone amplifier, and the AUDIO and RMT/DATA connectors.

Module PS - contains the power supply circuits of the PRC-2200.


RT-2001
RMT/DATA
FRONT PANEL
PANEL INTERFACE
DISPLAY
MAIN CONTROLLER
INDICATIONS
CONTROL SIGNAL
P/O MCU
MB
INDICATION CONTROL SIGNALS TO OTHER MODULES
RF OUT
P/O MCU
CONTROL, DATA AND FREQUENCY INFORMATION
FIXED AUDIO
DATA IN
DATA OUT
MIC EXT
FIXED LEVEL AUDIO
AUDIO CONT
MICROPHONE
EARPHONE
AUDIO SPKR
MICROPHONE
EARPHONE
SPEAKER
FIXED AUDIO
TXBB
RXBB
MIC
RXBBD
CODEC IN
CODEC OUT
AUDIO
IF
RF
AM
INPUT SELECTOR
MICROPHONE AMPLIFIER
MIC-COMB-F
DEM SIG
SIDE TONE
TX-SELECTOR
TX AMPLIFIER
RXBB AMPLIFIER
IF MODULATOR
NCW,AM,SSB CRYSTAL FILTERS
SSB/AM DEMODULATOR AND AGC CIRCUIT
100 KHZ
350 KHZ
1 KHZ
DIVIDERS
TRANSMITTER FREQUENCY TRANSLATOR
RECEIVER FREQUENCY TRANSLATOR AND RCV FILTERS
TX PRC/VRC
100 mW AMPLIFIER
AM DRIVE
RX/100mW
20W AMPLIFIER AND TX FILTERS
FRONT/REAR
VRC
PRC
PTT 20W
CONTROL AND INDICATION SIGNALS TO THE MICROPROCESSOR
SUPPLY VOLTAGE
AGC
F2
F1
700 KHZ
5.25 MHZ
10 KHZ, 3.5MHZ
FREQUENCY SYNTHESIZER
SYNT
CHARGING (NICD BATTERY ONLY)
12.5V BATTERY
FUSE
POWER SUPPLY
REGULATED SUPPLY VOLTAGES
1. NORMAL
2. TUNING
ATTEN
INTERFACE
VOL REGUL

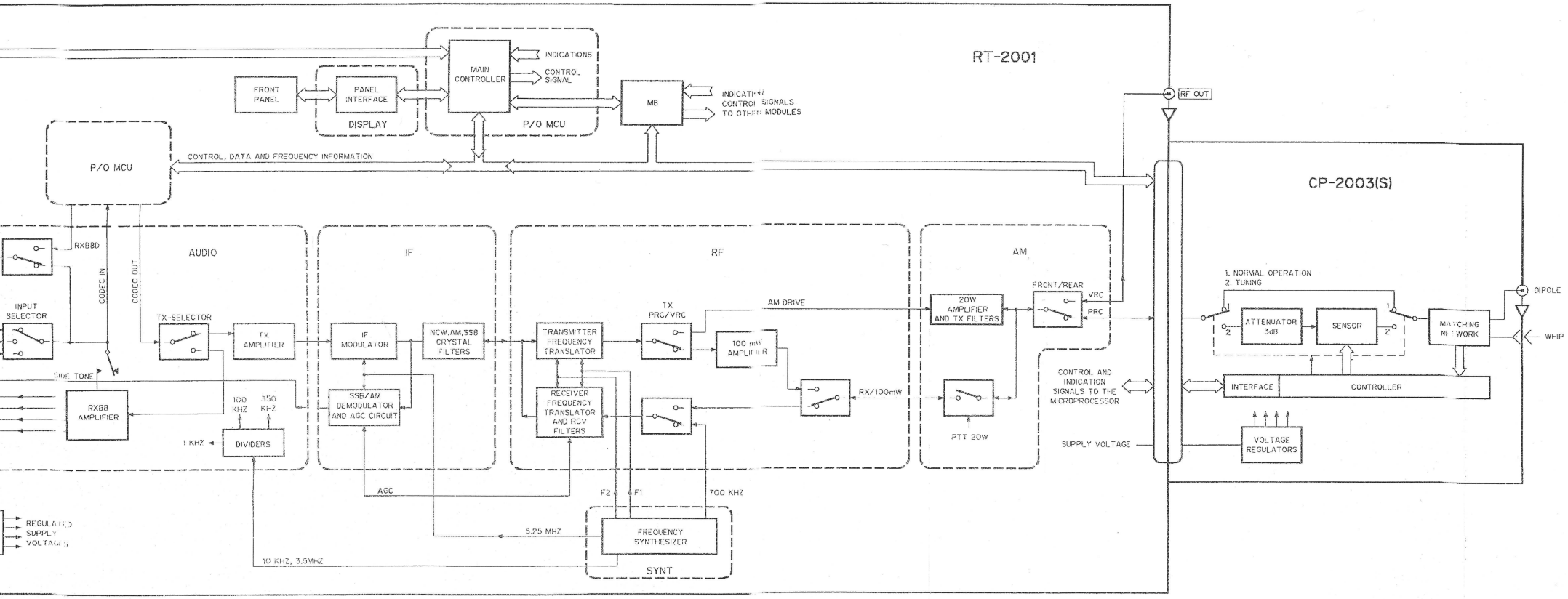


Figure 2-1. PRC-2200, Block Diagram

(2) Antenna Coupler CP-2003 modules.

Module MNC - contains a microprocessor system, which controls the operation of the CP-2003 and performs the antenna matching algorithm.

Modules RF1, RF2 and RF3 - contain the antenna matching network and various sensors required for antenna matching.

2-2. Transmit Path Block Diagram

The functional block diagram of the transmit path is shown in figure 2-2.

a. Input Signals. The transmit path can receive audio signals from the following sources:

(1) Front panel microphone signal. This signal is amplified by the microphone amplifier before being applied to the AUDIO module.

(2) Rear connector and RMT/DATA microphone signal (220mV).

(3) RMT/DATA TXBB line, for use with internal and external modems.

b. Audio Signal Processing. The input signal corresponding to the current operating mode is selected by means of the input selector of the AUDIO module. The processing applied to the selected signal depends on the operating mode:

(1) External modem: the signal applied to the TXBB line is connected directly to the TX amplifier.

(2) Analog voice: the signal is amplified and filtered, and then connected to the TX amplifier.

(3) Digital voice: whenever some type of digital voice processing is required (secure or frequency hopping operation, etc), the input signal is filtered by the variable filter 1 and applied to the codec in the MCU module. The codec converts the signal to digital data, and transfers it to the microprocessor, for processing. The processed signal is returned to the codec and converted to an analog signal. The codec output signal is filtered by the variable filter 2 and applied to the TX amplifier. The two variable filters are controlled by the MCU module.

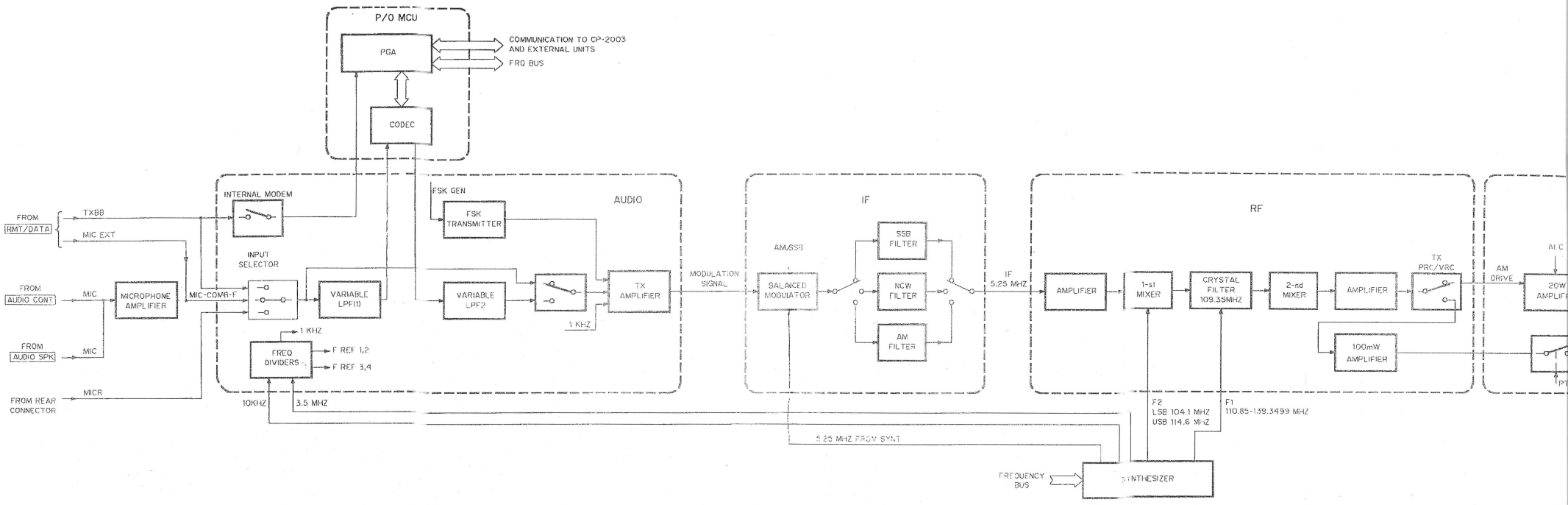
(4) Internal modem. When using the internal modem, the data applied on the TXBB line in connector RMT/DATA is directly connected to the MCU module. The processed data signal is returned via the codec.

(5) CW operation. In the CW mode, the audio inputs are disabled, and a keying tone is provided by a 1kHz signal.

(6) Transmission of signaling tones. When using selective calling, active squelch, speech enhancer, AUTOCALL, encryption or frequency hopping, the MCU module generates FSK signaling tones, which are combined with the transmit signal in the TX amplifier.

c. RF Path. The modulation signal generated by the AUDIO module is applied to the modulator in the IF module. In all operating modes except AM, the modulator output is a 5.25-MHz double sideband signal. When AM operation is selected, a conventional AM signal appears at the modulator output. The modulator output is filtered by a crystal filter which limits the frequency band occupied by the transmitter signal. There are three filters: one for SSB, DATA and CW operation, another for AM operation and the third for NCW. The filter corresponding to the selected operation mode is inserted into the signal path.

The filtered signal is applied to the transmitter frequency translator in the RF module, which converts it to the required operating frequency and sideband (LSB or USB) by a two-stage mixing process.


P/O MCU
PGA
CODEC
COMMUNICATION TO CP-2003 AND EXTERNAL UNITS
FRQ BUS
AUDIO
INTERNAL MODEM
FSK GEN
FSK TRANSMITTER
FROM RMT/DATA
TXBB
MIC EXT
INPUT SELECTOR
FROM AUDIO CONT
MIC
MICROPHONE AMPLIFIER
MIC-COMP-F
VARIABLE LPF(1)
VARIABLE LPF2
1 KHZ
TX AMPLIFIER
FROM AUDIO SPK
MIC
FREQ DIVIDERS
F REF 1,2
F REF 3,4
FROM REAR CONNECTOR
MICR
10KHZ
3.5 MHZ
MODULATION SIGNAL
IF
AM/SSB
BALANCED MODULATOR
SSB FILTER
NCW FILTER
AM FILTER
IF 5.25 MHZ
RF
AMPLIFIER
1-st MIXER
CRYSTAL FILTER 109.35MHZ
2-nd MIXER
AMPLIFIER
TX PRC/VRC
100mW AMPLIFIER
AM DRIVE
ALC
20W AMPLIFI
PT
F2
LSB 104.1 MHZ
USB 114.6 MHZ
F1
110.85-139.3499 MHZ
5.25 MHZ FROM SYNT
FREQUENCY BUS
SYNTHESIZER

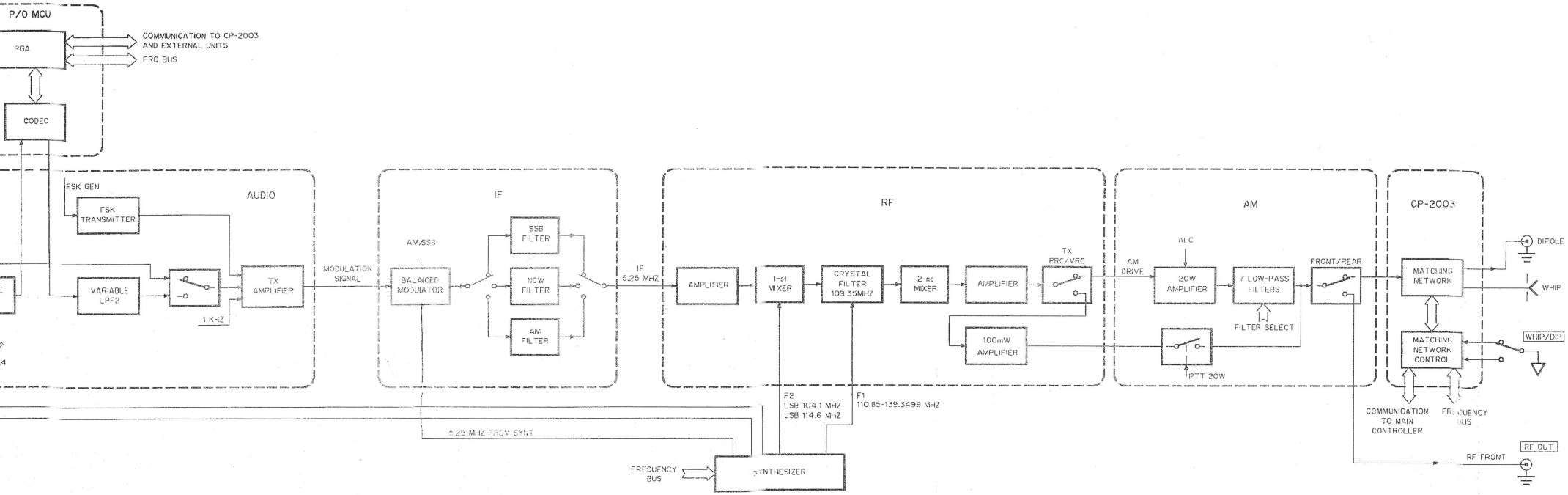


Figure 2-2. Transmit Path, Block Diagram

In the first stage, the 5.25MHz signal generated by the IF module is converted to a 109.35MHz IF signal, by mixing it with the F2 signal generated by the synthesizer. F2 frequency is 104.1MHz for LSB operation and 114.6MHz for USB and AM operation. The 109.35MHz signal is filtered by a crystal filter and then converted to the final transmit frequency by mixing with the F1 signal generated by the synthesizer. The F1 signal covers the 110.85 to 139.3499MHz range in 100Hz steps.

The transmit signal, in the 1.5000 to 29.9999MHz range, is amplified and applied to the AM module. In the AM module, the transmit signal is amplified to the required output level by the 20W power amplifier. RF output power is controlled by an ALC system, which includes the microprocessor located in the MCU module. The output power is adjusted to the desired value, while monitoring the current drawn from the battery pack.

The RF output signal of the AM module is filtered by a sub-octave bandpass filter. There are seven filters, and the filter corresponding to the operating frequency is inserted into the signal path under microprocessor control. The filtered signal is applied to the matching network located in the CP-2003.

In the CP-2003, the RF transmit signal passes through the matching network to the connector of the antenna selected by the operator.

The antenna matching process is controlled by a matching network control circuit, which includes a microprocessor. This microprocessor receives frequency information from the RT-2001 frequency bus and from the microprocessor located in the MCU module of the RT-2001, and automatically performs antenna matching, to achieve maximum sensitivity and transmit power.

(1) In fixed-frequency operation, matching occurs on the first PTT pressing. On subsequent transmissions, matching is checked again and corrected if necessary. If antenna cannot be matched (because of physical damage, or because the antenna selector on the CP-2003 shifted to an incorrect position), the operator hears an alarm tone and the message NO MATCH.

(2) When using frequency tables, such as during AJ or AUTOCALL, a special matching process, called "learning", is performed. Learning occurs when PTT is pressed. The matching is performed by the PRC-2200 without operator intervention, by transmitting on each frequency and "learning" the correct matching for each one.

2-3. Receive Path Block Diagram

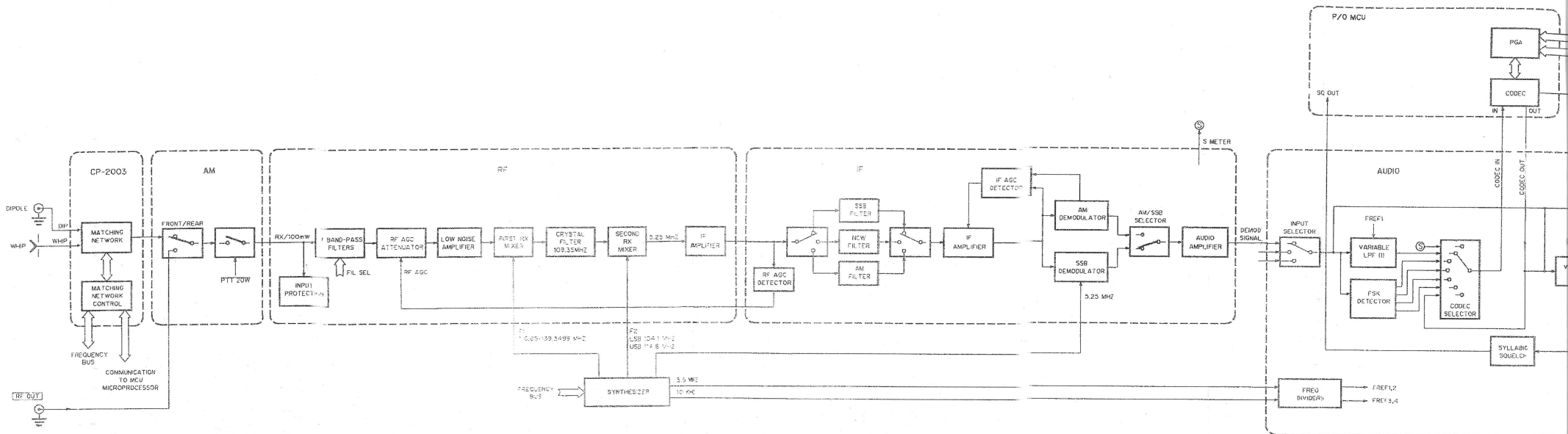
The functional block diagram of the receive path is shown in figure 2-3.

a. RF Path. The RF signal received by the antenna in use passes through the matching network in the CP-2003 to the antenna input of the RT-2001. During reception, the matching network is preset for optimal reception. In the RT-2001, the received RF signal passes through the AM module to the RF module.

The input line of the RF module is protected against excessive voltages, and then is connected to the bandpass filters. The RF module has seven sub-octave bandpass filters, and the filter corresponding to the operating frequency is inserted into the signal path by commands from the microprocessor located in the MCU module. The filtered RF output passes through the RF AGC attenuator. This attenuator starts reducing signal level when the signal measured by the RF AGC detector at the input of the IF module is too high and could cause receive overload.

The filtered signal is amplified and applied to the receiver frequency translator. The receiver frequency translator is similar to the transmitter frequency translator described in para. 2-2.c above, except that mixing is performed in the reverse order (first with the F1 signal, then with the F2 signal). The resulting 5.25MHz IF signal is amplified and applied to the IF module.

In the IF module, the IF signal is filtered by the filter corresponding to the selected operating mode, and applied to the IF amplifier. The gain of the IF amplifier is controlled by an AGC voltage, such as to obtain a constant IF


CP-2003
AM
RF
IF
AUDIO
P/O MCU
DIPOLE
DIP
WHIP
MATCHING NETWORK
MATCHING NETWORK CONTROL
FREQUENCY BUS
COMMUNICATION TO MCU MICROPROCESSOR
RF OUT
FRONT/REAR
PTT 20W
RX/100mW
INPUT PROTECTION
BAND-PASS FILTERS
FIL SEL
RF AGC ATTENUATOR
RF AGC
LOW NOISE AMPLIFIER
FIRST RX MIXER
CRYSTAL FILTER 109.35MHZ
SECOND RX MIXER
5.25 MHZ
IF AMPLIFIER
RF AGC DETECTOR
SSB FILTER
NCW FILTER
AM FILTER
IF AMPLIFIER
IF AGC DETECTOR
AM DEMODULATOR
SSB DEMODULATOR
5.25 MHZ
AM/SSB SELECTOR
AUDIO AMPLIFIER
S METER
DEMOD SIGNAL
INPUT SELECTOR
FREF1
VARIABLE LPF (1)
FSK DETECTOR
CODEC SELECTOR
CODEC IN
CODEC OUT
SYLLABIC SQUELCH
PGA
CODEC
IN
OUT
SQ OUT
FREQUENCY BUS
SYNTHESIZER
3.6 MHZ
10 KHZ
FREQ DIVIDERS
FREF1,2
FREF3,4

Figure

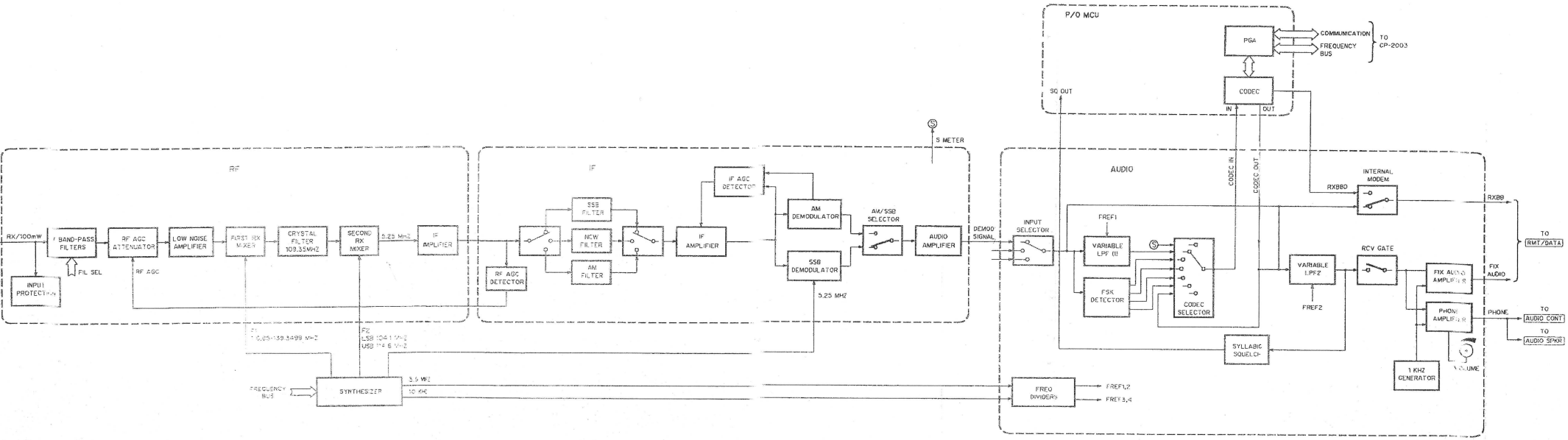


Figure 2-3. Receive Path, Block Diagram

signal level. The amplified IF signal is applied to the SSB and AM demodulators. The SSB demodulator is a synchronous detector, which receives a 5.25MHz signal from the synthesizer. The AM demodulator is an envelope detector.

The demodulated signal corresponding to the operating mode is selected by the AM/SSB selector and applied to the audio amplifier. The amplified demodulated signal is applied to the AUDIO module.

b. Audio Path.

(1) Signal processing. The audio path through the AUDIO module uses the same circuits, starting from the input selector and up to the output of the variable low-pass filter 2, that are also used by the transmit path (see para. 2-2.b):

(a) The CW signal is filtered by variable filter 2.

(b) The digital voice signal is converted by the codec to digital data, processed by the microprocessor and returned via the codec. When using the internal modem, the signal is not returned via the codec, but exits via the modem selector to the RXBB line on the RMT/DATA connector.

(c) The external modem signal passes through the internal modem selector directly to the RXBB line in the RMT/DATA connector.

The received audio signal is also applied to the syllabic squelch circuit, whose output is applied to the MCU module. The MCU module processes the syllabic squelch signal, or the active squelch information, and controls the RCV gate. When a useful signal is received, the RCV gate closes and connects the signal to the FIX AUDIO and earphone amplifiers. When operating with squelch off, the RCV gate is always closed.

The FIX AUDIO and earphone amplifiers also receive indication and alarm signals, generated by the 1kHz generator.

(2) Processing of signaling tones. The demodulated audio signal received from the IF module is also applied to the FSK BPF FILTER and detectors, which detects the presence and type of signaling tones. The signaling tones are used for active squelching, selective calling, AUTOCALL operation and secure operation modes. Four signaling tones are used. During the call establishment phase, all four tones are used. After the call is established, only two high tones remain in use.

2-4. Power Supply System (figure 2-4)

Figure 2-4 shows the power supply system of block diagram of the PRC-2200.

a. Power Source. The PRC-2200 is powered by a battery pack providing a nominal voltage of 12V. The battery pack is installed in the RT-2001 battery compartment.

b. PRC-2200 Power Sub-system.

(1) Distribution of primary power. The positive battery line is connected to module PS. Module PS contains a fuse which protects the supply line, and a resistor, connected in series with the supply line. The voltage drop across the resistor, directly proportional to the current drawn by the RT-2001, is amplified and sent to the microprocessor located in module MCU. During transmission, the microprocessor controls the RF output power, using the ALC system of module AM, such that the total current drain does not exceed the allowable limits.

The primary power line exits module PS and passes through a jumper located in the CP-2003. The jumper serves as an interlock that prevents operation without the CP-2003. The protected primary power line is connected to module PS, and to module AM.

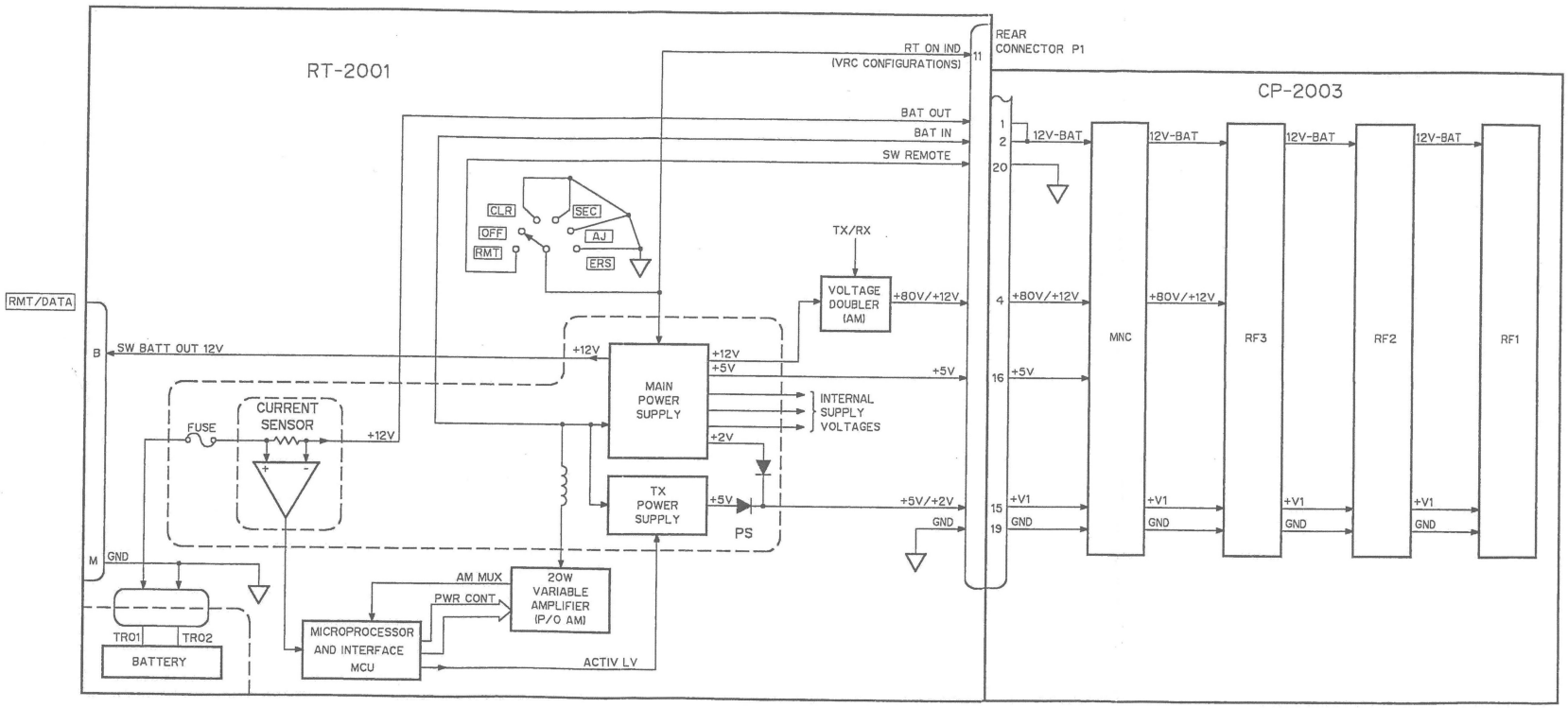


Figure 2-4. PRC-2200, Power Supply System

(2) Main power supply. The main power supply of the RT-2001 is located in module PS. Module PS converts the primary power to regulated voltages for all the RT-2001 and CP-2003 circuits.
The main power supply is turned on by grounding a control line. Ground is usually connected by setting the front-panel function selector to CLR, SEC, AJ, or ERS. With the function selector at RMT, ground can be connected via a special control line, SW REMOTE, included in the rear connector.

(3) TX power supply. The TX power supply, also located in module PS, provides to the CP-2003 a regulated voltage +5V during the transmit mode. This +5V voltage replaces the +2V voltage provides in the receive mode, by the main power supply.

(4) Voltage doubler. The voltage doubler, located in module AM, provides +12V in the receive mode, and +80V in the transmit mode. The +12V/+80V voltage is used by the CP-2003.

(5) Module AM. The 20W power amplifier in module AM is powered directly from the primary voltage line.

2-5. Control Sub-System
(figure 2-5)

a. General. The control sub-system of PRC-2200 is shown in figure 2-5.

(1) The PRC-2200 contains two microprocessors located in module MCU of the RT-2001, and in the MNC module of the CP-2003, respectively.

(a) The microprocessors in the MCU and MNC modules communicate by means of two serial data lines, TX SERIAL REAR and RX SERIAL REAR, accompanied by the communication request line COMM REQ REAR (see para. b. below).

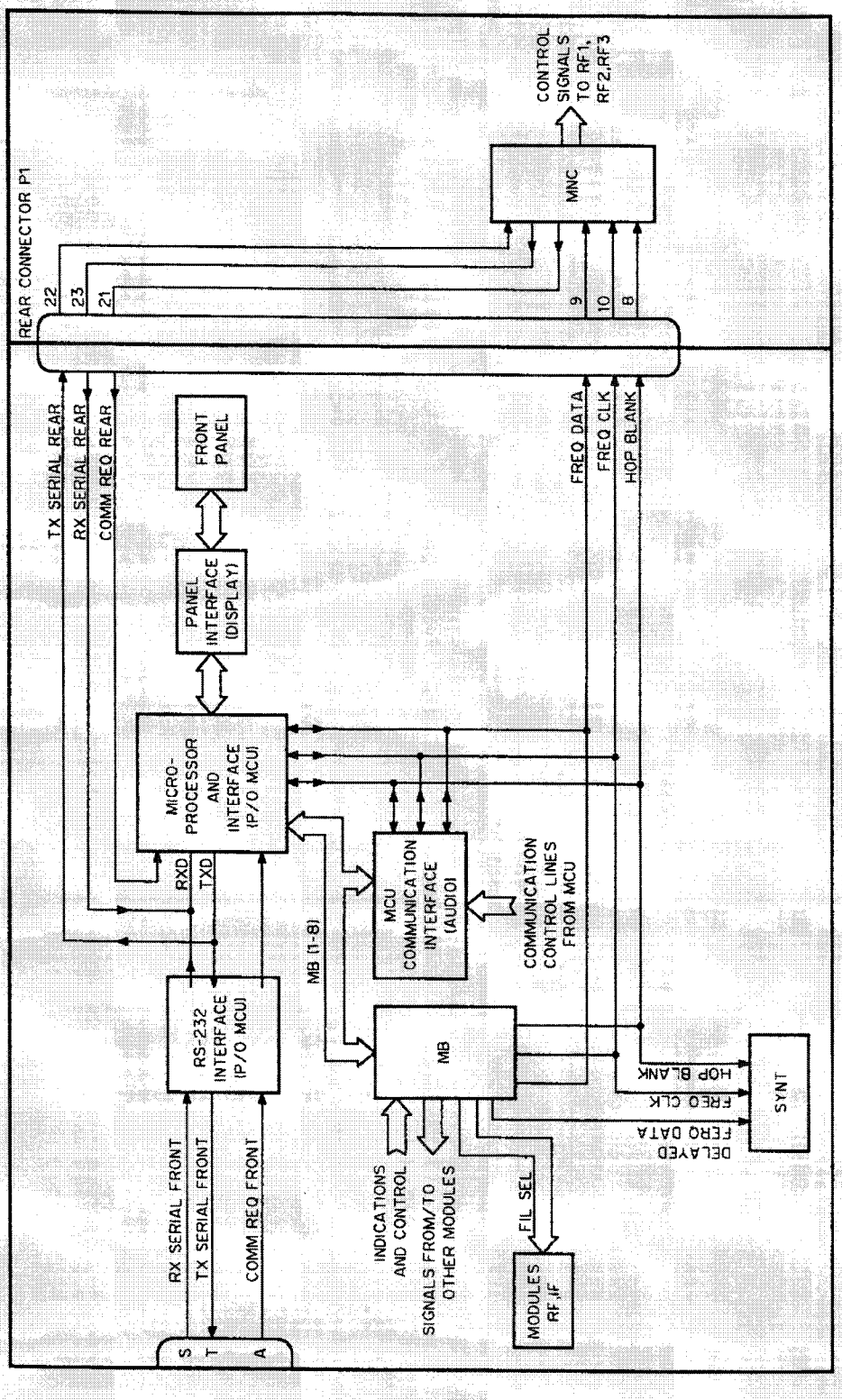


Figure 2-5. PRC-2200 Control Sub-System

The operation of the PRC-2200 is controlled by the microprocessor located in module MCU.

(2) Operator interface is via the PANEL module. The PANEL module contains an interface which monitors the front-panel controls and keypad and transfers operator inputs to the microprocessor data bus. The interface also transfers information from the microprocessor to the various displays and indicators. This microprocessor receives operator commands, entered via the front-panel controls, and converts them to control signals for the various modules. The control signals are distributed by means of the motherboard (MB), which includes interface circuits between the microprocessor bus and the controlled modules.

When a control handset is used, the microprocessor detects its presence and uses the commands entered by means of handset controls, instead of those entered via the corresponding front-panel controls.

(3) The microprocessor in the MCU module can also receive remote control commands via an RS-232 extension of the internal serial data lines (TX SERIAL FRONT and RX SERIAL FRONT lines accompanied by the communication request line COMM REQ FRONT). These lines are available in the RMT/DATA connector.

(4) In addition by commands regarding the desired operating mode, the microprocessors also determine the operating frequency. Frequency data is transferred on a separate bus, the frequency bus (see para. c. below).

b. Serial Control Communication.

(1) System configuration (fig. 2-6).

(a) The control communication uses a bus configuration, with master/slave discipline. The bus uses three lines: two data lines designated TX SERIAL, RX SERIAL, and a control line, COM REQ. All the units participating in the communication

system are connected in parallel to the bus lines. Each unit has a unique identification ("address"). System configuration is shown in fig. 2-6.

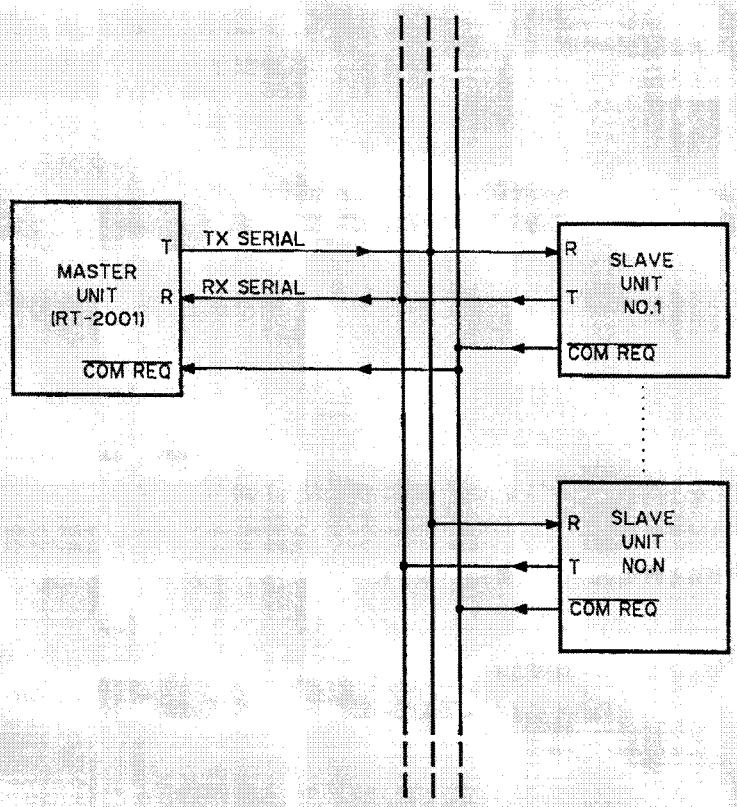


Figure 2-6. Control Communication System Configuration

In this configuration, one of the units connected to the bus is designated master. In the PRC-2200, and also in all the vehicular configurations built around RT-2001, the bus master is the microprocessor located in module MCU.

(b) Bus discipline is imposed by having the master unit address the other units, designated slaves, and requesting a specific type of response from the addressed unit. The COM REQ line is used to enable slave units to initiate communication: the slave unit activates a communication request to the master unit, and waits for the master approval. The master therefore remains in control of the bus at all times.

(c) The master unit transmits to the slaves on the TX SERIAL lines, and receives on RX SERIAL line. The slave units transmit on the RX SERIAL line, and receive on the TX SERIAL line. The bus lines extend to the rear connector of the RT-2001, and to the RMT/DATA front-panel connector. The connection to the RMT/DATA connector passes through an RS-232 interface, as shown in figure 2-5. This enables connection of external optional equipment, such as automatic test equipment, data loaders, remote control units, etc.

In the PRC-2200, the only slave unit is the microprocessor in module MNC of the CP-2003.

In the vehicular configurations, the slaves are the RF power amplifier and the antenna coupler as well as other optional equipment that may be connected by means of the vehicular mounting.

(2) Communication format.

(a) General. The communication between the RT-2001 and the other system units takes place asynchronously, at a rate of 2400baud.

The information is transferred by means of messages (frames). Each message consists of several words that are transmitted or received serially.

(b) Word format. Each word consists of 11 bits, as follows:

- 1 start bit
- 8 data bits (the last significant bit is transmitted first)
- 1 parity bit
- 1 stop bit

(c) Frame structure. The standard frame structure consists of a message header (2 words), several data words (up to 15) and one checksum word. The header contains the sending unit address field, type of command and the number of data words in the frame. The checksum word is used for error detection (para. (d) below).

When the message includes only a command, a shortened frame is used. The shortened frame consists of an one-word header, or of two header words and one checksum word.

(d) Error detection. To ensure data integrity, several error detection methods are used:

1. Parity bits - provide parity checking for each transmitted word.

2. Frame checksum - a word transmitted at the end of a frame. The checksum word is the arithmetic sum (modulo 256) of the words composing the frame.

3. Frame length check - correct reception of all the frames containing more than one word is checked by comparing the number of words actually received with the number of words indicated in the header.

4. Time-out protection - the time-out mechanism monitors critical time intervals, such as the interval between consecutive words in a frame, or the interval between the last word of a frame sent by the master and the first word of the slave response.
If any of the monitored intervals exceeds the maximum allowable duration, the time-out mechanism clears the fault and restores normal data transfer.

c. Serial Frequency Information.

(1) The serial frequency information is transmitted in frames. Each frame consists of 96 bits. The frequency information is carried on the FREQ DATA line, and is accompanied by the frequency data bus clock (FRQ CLK) and the "end of frequency hopping" (HOP BLANK) signal which is used as a strobe for the serial data. The timing and data format used on these lines are shown in figure 2-7.

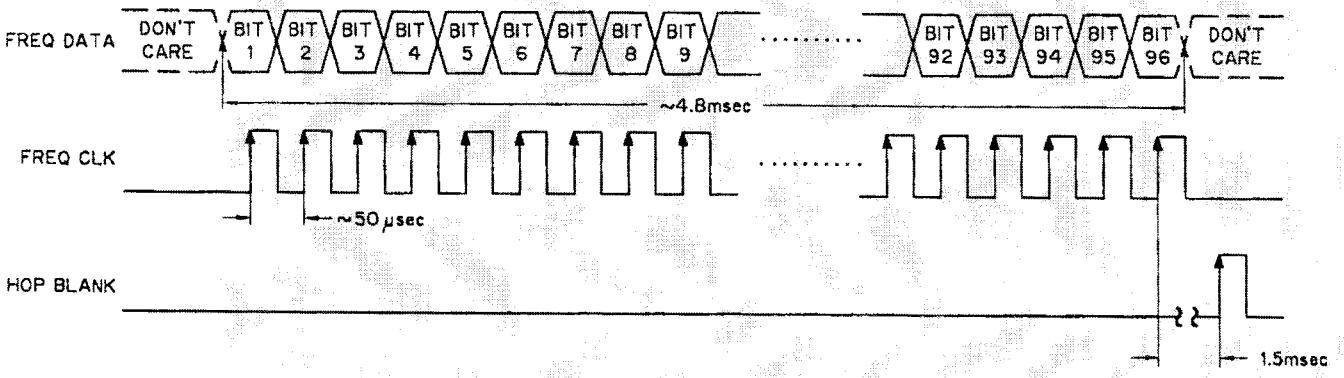


Figure 2-7. Serial Frequency Bus, Timing and Format

(2) The frequency data is provided by the microprocessor in module MCU.

(a) In the RT-2001, the frequency data is read by a control latch contained in the MB module. The control latch generates a delayed frequency word for module SYNT, and drives the filter selection lines for modules RF and AM. The data is latched into the modules upon the rising edge of the HOP BLANK signal.

(b) In the CP-2003, the microprocessor in the module MNC reads the frequency received on the frequency bus and automatically performs antenna matching.

2-6. BIT System
(figure 2-1)

a. On-line Monitoring. The microprocessor in module MCU monitors the outputs of various signal sensors, located at critical points along the various signal paths in the PRC-2200 modules. Using these sensors, the microprocessor determines if a malfunction is detected. Several alarms indications are provided in case a problem is detected, and stop after the problem is corrected. The alarm indications are as follows:

(1) Visual indication. When a malfunction is detected, the FAULT LED lights provided lighting is on. In addition, failure codes or messages are displayed (refer to b. below).

(2) Auditory indication. 1kHz beeps are heard in the earphones or in the speaker.

In addition, the relative value of the transmitter RF power, received signal strength or battery condition are indicated by the number of arrows appearing on the LEVEL display.

b. FAIL Messages. Failure codes or messages can be displayed on the message display. Only messages of interest to the operator are automatically displayed. Technical failure codes do not appear automatically on the display, but are stored in a BUG LIST. To enter the BUG LIST, press the TEST key several times until the message BUG LIST appears on the display, then press ENT. The BUG LIST contains three tables:

(1) HRD-ERR table. This table contains the hardware failure codes of malfunctions detected during the execution of the off-line self-test (initiated by the operator, or automatically performed upon turn-on).

(2) PRSNT-ERR table. This table contains the alarms or failures still present when the table is displayed. These failures are detected during the automatically-performed continuous on-line tests.

(3) PASS-ERR table. This table contains the alarms or failures that were detected during the current operating period (from the last turn-on), but were corrected and are no longer present.
These failures are detected during the automatically-performed continuous on-line tests.

To enter one of these tables, press TEST several times until the designation of the required table appears on the display (HRD-ERR, PRSNT-ERR or PASS-ERR), then press ENT. The failure codes are listed in table 3-4.

Note that some of the alarms and failure codes can be displayed only after a password has been entered (see para. 3-6.c.).

c. Self-test. Two types of tests are available:

(1) Continuous on-line tests, automatically performed by the microprocessor in the MCU module. These include continuous monitoring of battery voltage and current, RF output power, synthesizer locking and antenna matching, power supply failure, etc.

(2) Operator-initiated off-line self-test. Some of the tests covered by the self-test are listed below:

(a) Controller tests (microprocessor system self-test and testing of communication between microprocessors).

(b) Testing of power supply voltages.

(c) Front-panel operational test (display and keyboard). This test is performed interactively with the operator.

(d) Audio path testing. This test is performed by injecting audio signals and closing the loop between the transmit output and the receive input of the AUDIO module.

(e) Synthesizer lock indication test.

(f) Receiver test. An internal RF signal is injected at the input to the receive path. The microprocessor in the MCU module tunes the receiver to the test frequencies and determines the received signal level.

(g) Transmitter test. The microprocessor in the MCU module tunes the transmitter to each of the test frequencies. At each frequency, the output power level, matching capability and synthesizer functions (locking) are checked. The transmitter test is performed only upon operator request.

At the end of the self-test procedure, the system displays test results to the operator. If the radio set has failed the test, the system provides messages indicating the corrective actions to be taken in order to repair it.

(3) Initiation of off-line test. The off-line self-test is initiated in the following cases:

(a) Power-up. Part of the off-line self-test functions are automatically activated every time the PRC-2200 is turned on. If a major problem occurs, a failure message will appear on the display. To see more detailed results, check the BUG LIST (see para. b. above).

(b) BIT activation. To activate the off-line self-test, perform the following actions:

1. Press the TEST key until the message BIT appears, then press ENT. The message BIT ON appears.

2. After a few seconds, the test results: TEST-OK! or TEST FAIL will appear on the display.

*- TEST-OK! means that no failures have been detected.

*- TEST FAIL means that one or more failures have been detected.

To see the detailed BIT results, check the BUG LIST (para. b. above).

(c) Battery test. To activate the off-line battery test, perform the following actions:

1. Press the TEST key until the message BATT appears, then press ENT.

2. The test result: BATT-OK or LOW-BATT! will appear on the display.
   - BATT-OK means that battery supply voltage is within the allowable limits.
   - BATT LOW! means that the battery voltage is too low for normal operation.

   In addition, the relative battery voltage is indicated by the number of arrows appearing on the level display.

   - Five arrows indicates that the battery is full.
   - One arrow means that the battery is almost empty and should be replaced as soon as possible.

3. Enter CW mode and repeat steps 1 and 2 while pressing the PTT.

(d) Display test. To activate the display test, perform the following actions:

1. Press the TEST key until the message DISPLAY appears, then press ENT.

2. In response, all the characters should appear in a predetermined sequence on the displays.

2-7. Connectors

Tables 2-1 thru 2-4 list the pin allocations and pin functions in the RT-2001 RMT/DATA, AUDIO and rear connectors.

Table 2-1. RMT/DATA Connector

Pin	Designation	Function	To/From RT	Electrical Characteristics
S	RX SERIAL FRONT	Receive line of serial control bus	To	RS-232C
T	TX SERIAL FRONT	Transmit line of serial control bus	From	RS-232C
A	COMM REQ FRONT	Remote device identification/ request to communicate. By this line: a) The RT identifies connection of a device to the RMT/DATA connector. b) Enables the connected device to initiate communication with the RT-2001, via the control bus.	To	RS-232C
B	SW BATT OUT 12V	Filtered battery voltage, present while the RT-2001 operates	From	10.5V to 14.5V 100 mA max
M	GND	Ground	Both	0V
V	PTT D	PTT for data transmission (TTL)	To	Active: 0V Non-active: +5V or open
G	PHONE	Audio output for speaker	To	Level depends on setting of VOLUME control: minimum +3V with volume control at maximum

Table 2-1. RMT/DATA Connector (Cont'd)

Pin	Designation	Function	To/From RT	Electrical Characteristics
P	RXD	Data receive indication DCW tone is identified in the receive signal DCW tone not identified	From	RS-232C Active: +5V Non-active: -5V -5V +5V
R	RXV	Voice and DCW receive indication	From	Active: 0V Non-active: +5V or open
L	TXBB	Information input for data transmission	To	With internal modem: RS-232C With external modem: 0dBm/600ohm
F	TXBB CLK	External clock for transmitting data to internal modem	To	RS-232C
E	RXBB CLK	Internal clock for transmitting data to internal modem	From	RS-232C
H	CTS DATA	Clear to send indication from internal modem	From	RS-232C Active: +5V Non-active: -5V
D	MIC EXT FRONT	High level microphone input	To	220mVRMS across 150 ohm
C	FIX AUDIO OUT	Fixed audio output	From	220mVRMS across 150 ohm
N	CHARGE	Charge input for NiCd battery	To	10.5V to 14.5V

Table 2-1. RMT/DATA Connector (Cont'd)

Pin	Designation	Function	To/From RT	Electrical Characteristics
J	TXV FRONT	PTT for voice transmission internal modem	To	Active: 0V Non-active: +5V or open-circuit
U	TXD	PTT for data transmission	To	RS-232C Active: +5V Non-active: -5V
K	RXBB	Received information output	From	With internal modem: RS-232C (+5V="0", -5V="1") Other modes: 0dBm/600 ohm

Table 2-2. AUDIO SPKR Connector

No.	Designation	Pin	Function	To/From RT	Levels
1	GND	A	Ground	Both	0V
2	SPKR GND	E	Ground for loudspeaker	Both	0V
3	PHONE	B	Audio output for speaker or earphone	From	Depends on volume position. +3V with volume control at maximum
4	PTTV	C	Voice input PTT	To	Active: 0V Not active: Open-circuit
5	MIC	D	Microphone input	To	5mV/150ohm

Table 2-3. AUDIO CONT Connector

No.	Designation	Pin	Function	To/From RT	Levels
1	GND	A	Ground	Both	0V
2	CHANNEL CONT	E	Channel selection by handset	To	0-5V
3	PHONE	B	Audio output for speaker or earphone	From	Depends on volume position. +3V with volume control at maximum
4	PTTV	C	Voice input PTT	To	Active: 0V Not active: Open-circuit
5	MIC	D	Microphone input	To	5mV/150 ohm
6	FUNCTION CONT	F	Function (operating mode) selection by handset	To	0-5V

Table 2-4. Rear Connector

Pin	Designation	Function	To/From RT	Electrical Characteristics
1	VCC 12V IN	Supply voltage input	To	10.5 to 14.5V
2	BATT OUT	Supply voltage output	From	10.5 to 14.5V
3	SIGNAL GND	Ground for audio signals	Both	0V
4	80V/12V	Supply line for CP	From	Receive: 12V Transmit: 80V

Table 2-4. Rear Connector (Cont'd)

Pin	Designation	Function	To/From RT	Electrical Characteristics
5	FIX AUDIO REAR	FIX LEVEL audio output	From	220mV across 150ohm
6	PTT OUT	Transmit on indication	From	Transmit: 0V Receive: 5V
7	TXV REAR	Voice PTT input	To	Active: 0V Non-active: +5V or open circuit
8	HOP BLANK	Timing signal for frequency bus used to latch a new frequency data word (strobe)	From	Active: (new frequency is latched) 5V Non-active: 0V
9	FREQ DATA	Frequency bus/serial data line	From	0V or 5V
10	FREQ CLOCK	Frequency bus clock line	From	0V or 5V
11	RT ON IND	ON/OFF indication	From	ON: 0V OFF: Open circuit
12	RF GND	Ground for RF signal	Both	0V
13	RF	Transmitted or received RF signal	Both	RF signal across 50 ohm
14	MIC EXT REAR	Microphone input	To	220mV RMS/150ohm
15	5V/2V	Supply line for CP-2003 RXV line in VRC configurations	From	Transmit: 5V Receive: 2V Active reception: 5V Other condition: 2V

Table 2-4. Rear Connector (Cont'd)

Pin	Designation	Function	To/From RT	Electrical Characteristics
16	5V	Supply line for CP-2003	From	5V
17		Not used		
18	PHONE REAR	Variable volume audio output	From	0-3V across 50ohm
19	CP VRC GND	Ground for CP-2003 or VRC system	Both	0V
20	SW REMOTE	External on/off control	To	ON: 0V OFF: open circuit
21	COM REQUEST	Request to use serial control bus	To	Active: 0V Non-active: 5V
22	TX SERIAL	Transmit line of serial control bus	From	"0": 0V "1": 5V
23	RX SERIAL	Receive line of serial control bus	To	"0": 0V "1": 5
24		Not used		
25	RF GND	Same as pin No. 12	Both	0V

Section II. RT-2001 CIRCUIT ANALYSIS

2-8. Module AUDIO

(fig. 2-8 thru 2-17)

a. Block Diagram Analysis (fig. 2-8 and 2-9). Figure 2-8 shows the block diagram of the signal processing circuits of module AUDIO and figure 2-9 shows the block diagram of the interface circuits.

The operation of module AUDIO is controlled by module MCU.

(1) Signal path in the transmit mode.

(a) Input selector and amplifier. The input selector selects the signal to be processed by the transmit path (MICR/MIC COMB F/ TXBBIN), by the receive path (DEM SIG), or by the self-test sub-system (BIT 2). The transmit path signals are:

1. Front panel microphone signal (from the microphone amplifier on the PANEL module), designated MIC COMB F. This signal is received from the AUDIO connectors through a microphone amplifier located on the front panel assembly or via MIC EXT FRONT line in the RMT/DATA connector.

2. Rear microphone signal (used only on vehicular radio sets), designated MICR.

3. External signal, applied to the TXBBIN line in the RMT/DATA connector. This signal is applied to the input selector via the TXBB amplifier that matches the impedance of the signal to 3kohm/600ohm, according to the EXT MODEM or RS-232 operational modes.

The selected signal is applied to the input amplifier. The amplifier gain changes according to the selected signal, such as to obtain the same nominal level at the input of the variable low-pass filter 1 for all sources, except for the TXBBIN signal. The level of the TXBBIN signal is adjusted to half of the nominal level, to increase the dynamic range available for the modem signals.

(b) Signal path in analog voice mode. When operating in the analog voice mode, the output signal of the input amplifier is filtered by the variable low-pass filter LPF1. The filtered signal passes through the codec input selector and is applied to the codec on the MCU module, through the CODEC IN line (see para. (d) below). The processed data returns from the MCU module via the CODEC OUT line, passes via the CODEC BYPASS switch and is filtered by the low pass filter LPF II. The filtered signal is applied to the TX signal selector. The TX signal selector passes the signal to the TX adder. The TX adder is used to add the FSK tones which carry the signals required to establish and maintain calls in the selective call modes.

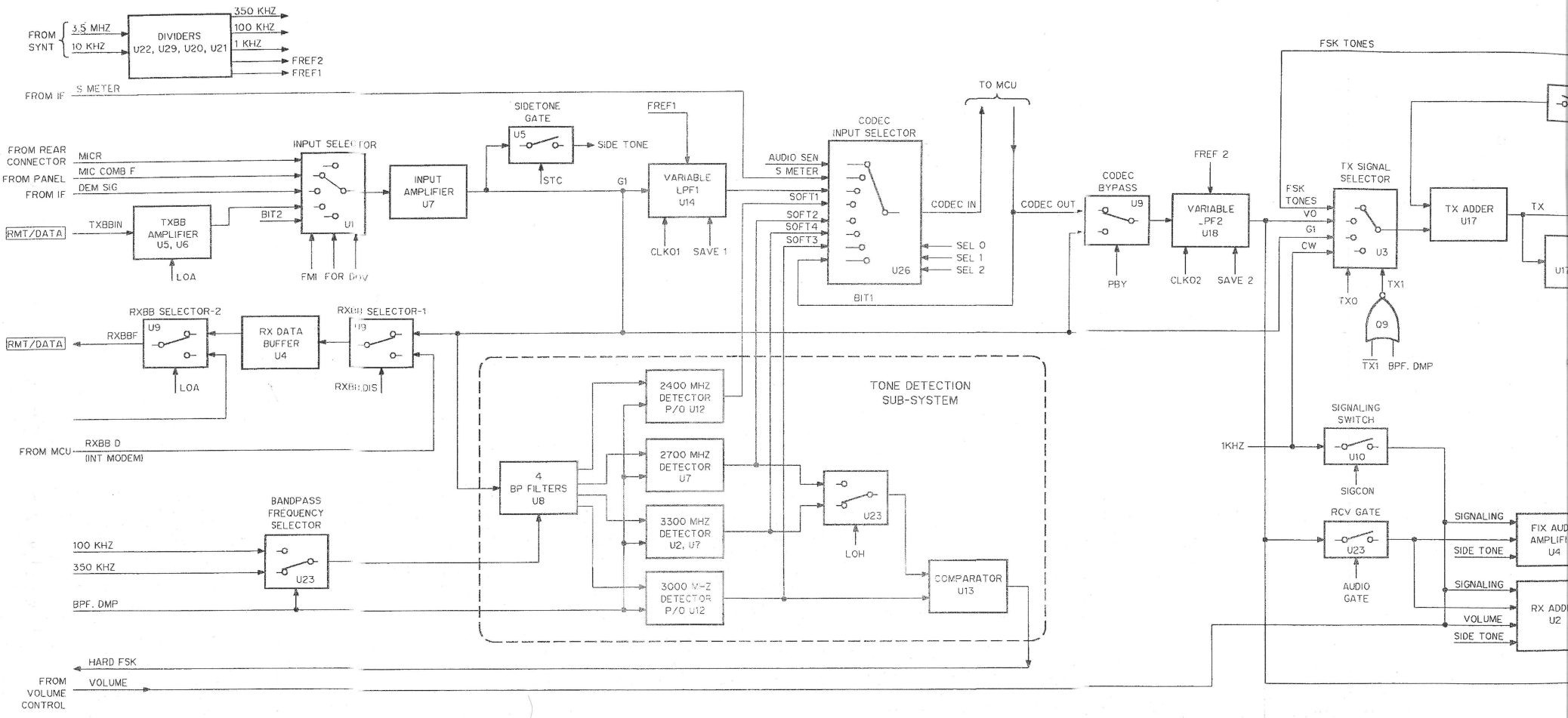


Figure 2-8. Module AUDIO,

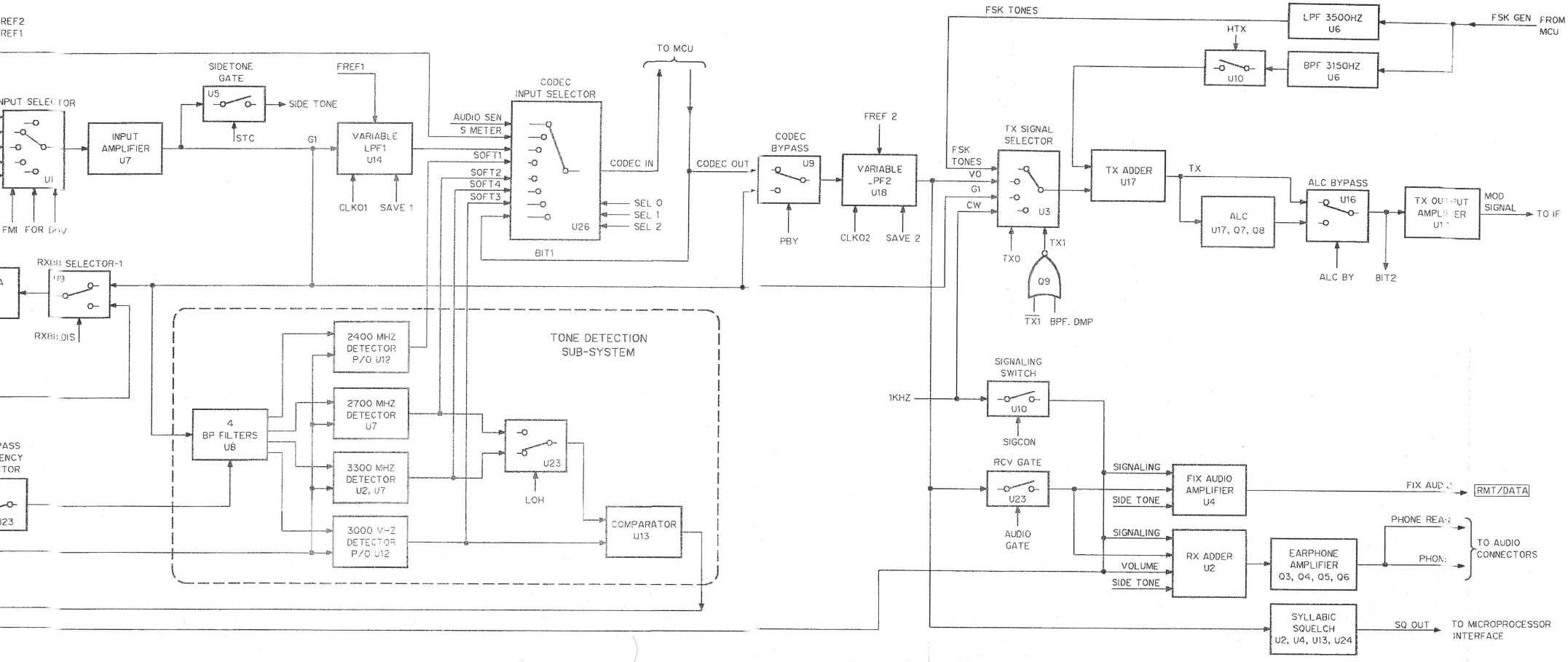


Figure 2-8. Module AUDIO, Signal Processing Circuits, Block Diagram

From the TX adder, the voice signal passes through an automatic level control (ALC) amplifier and the ALC BYPASS switch to the TX output amplifier. The output signal of the TX output amplifier is sent to the IF module. When the transmitter operates normally, a sidetone is provided by connecting the output signal of the input amplifier, via the SIDETONE gate, to the FIX AUDIO and earphone amplifiers.

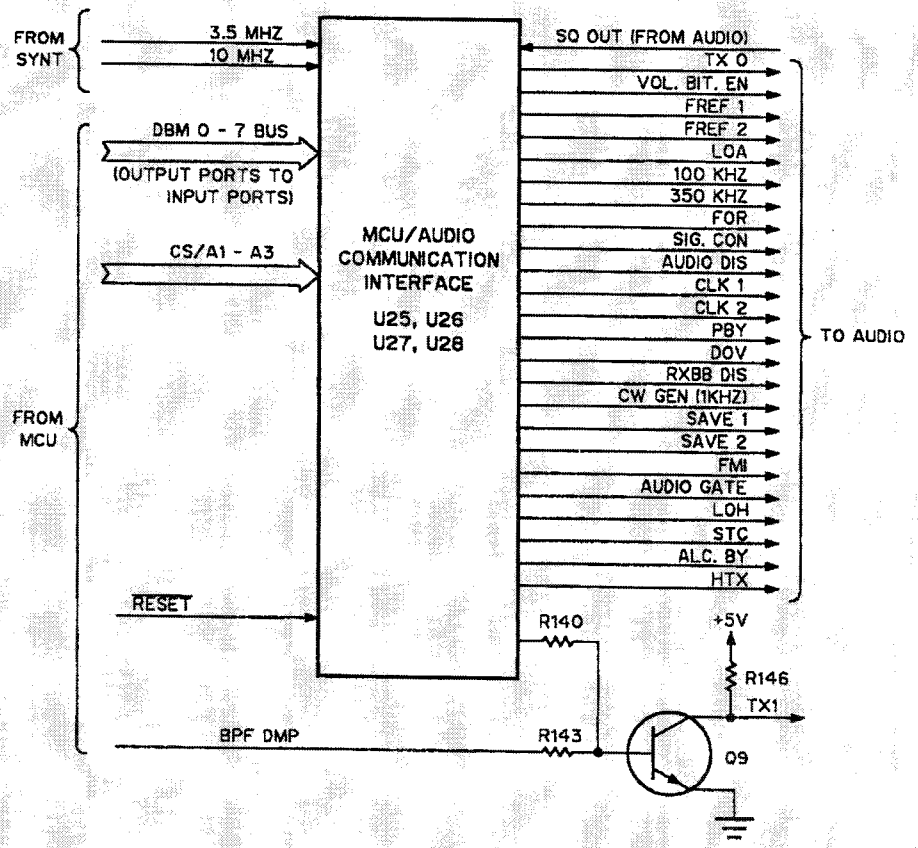


Figure 2-9. Module AUDIO, Interface Circuits, Block Diagram

(c) Signal path in external modem mode. When using an external modem, the modem signal applied to the TXBBIN line in the RMT/DATA connector is applied to the TXBB amplifier. The TXBB amplifier output signal, is directly connected to the TX signal selector. Then the signal follows the same path described in para. (b) above. No other signal is added to it, but in the AJ mode, the output signal of the TX adder passes directly via the ALC bypass switch to the TX output amplifier.

(d) Signal path with digital voice processing. When using digital voice processing, the output signal of the input amplifier is applied to the variable low-pass filter 1 (LPFI). The cut-off frequency of the low-pass filter is controlled by the MCU module, by means of the FREF1 and CLOCK-1 signals.

The filtered signal passes through the codec input selector and is applied to the codec on the MCU module, through the CODEC IN line. The codec is an analog/digital (A/D) and digital/analog (D/A) converter, especially designed for optimal processing of speech. The transmit path uses the A/D section of the codec to convert the input signal to digital data.

The processed data returns from the MCU module after it is converted back to an analog signal in the D/A section of the codec. The codec output signal is filtered by the variable low-pass filter 2 (LPFII), whose cut-off frequency is controlled by the FREF2 and CLOCK 2 signal provided by module MCU. The filtered signal passes through the TX signal selector to the TX adder, which adds the FSK tones. The resulting transmit signal can pass through the paths:

1. In all operational modes, except the AJ mode, the signal passes via the ALC amplifier and the ALC bypass switch to the TX amplifier.

2. In the AJ mode only, the signal passes through the ALC bypass switch to the TX output amplifier.

The output signal of the TX amplifier is sent to the IF module on the MOD SIGNAL line.

(e) CW operation. When operating in the CW mode, an 1kHz keying tone is generated whenever the telegraphy key is depressed. The 1kHz tone is obtained by dividing the frequency of the 10kHz signal received from module SYNT. The 1kHz CW tone is connected by the TX signal selector to the TX adder.

The output signal of the adder passes through the ALC amplifier and the ALC bypass switch to the TX output amplifier, and is then sent via the MOD SIGNAL line to module IF.

(f) FSK tone transmission. The MCU module can generate four different FSK tones. The FSK tones are generated whenever digital signal processing is being used. The four FSK tones have frequencies of 2400Hz, 2700Hz, 3000Hz and 3300Hz. The tones selected for transmission are determined according to the operating mode:

1. When operating in the digital CW mode or when using the internal modem, one of the four FSK tones is transmitted via the 3500Hz low-pass filter.

2. In the CLR, SEC, AJ and VOICE modes, only the 3000Hz or 3300Hz FSK tones are used. The appropriate tone is transmitted via the 3150Hz band-pass filter and added to the speech signals. In the CLR mode, the speech signals have a bandwidth of 300 to 2700Hz. In the SEC and AJ modes, the bandwidth is reduced to 300 to 2400Hz. The FSK tone is 8dB below the nominal speech signal level, in order to leave sufficient power for the speech transmission.

(2) Signal path in receive mode.

(a) Input selector and input amplifier. In the receive mode, the input selector and input amplifier always pass the demodulated receive signal, DEM SIG, received from the IF module.

(b) External modem signal path.

(1) When operating with an external modem, the output signal of the input amplifier is routed by the RXBB selector-1 to the RXBB buffer, and applied to the RXBBF line in the RMT/DATA connector through the RXBB selector-2.

(2) When operating with an RS-232 system, the RXBB D signal (±5V) from module MCU is applied to the AUDIO module and passes through the RXBB selector-3, the RXBB F line and the MCU module to the RMT/DATA connector.

(c) Signal path in analog voice mode. In the analog voice mode (SQ OFF), the output signal of the input amplifier is connected by the codec bypass switch to the variable low-pass filter 2. The filtered signal is connected by means of the RCV gate to the FIX AUDIO amplifier and to the RX adder. The RCV gate is always open in the transmit mode, and closes during active reception. The FIX AUDIO amplifier drives the FIX AUDIO line in the RMT/DATA connector. The output signal of the RX adder is amplified by the earphone amplifier and applied to the PHONE lines in the front-panel AUDIO connectors and in the rear connector. The level of the PHONE output signal is controlled by the front panel VOLUME control.

The two audio paths also receive the signaling generated by the 1kHz generator. Signaling type (continuous tone, beeps or no signaling at all) is controlled by means of the signaling switch. In the PHONE path, the signaling level is controlled by the volume potentiometer.

(d) Detection of FSK tones. When using AUTOCALL, selective squelch and/or any other form of digital signal processing, the signal transmitted by the remote radio set also includes four FSK tones, having frequencies of 2400Hz, 2700Hz, 3000Hz and 3300Hz (when using SQ OFF without SELECTIVE CALL, no FSK tones are added to the signal). The tone detection sub-system receives the output signal of the input amplifier and passes it through a four-channel band-pass filter (one for each tone) the filter center frequencies are controlled by the MCU module, by means of 100KHz and 350KHz frequencies, selected by a bandpass frequency selector controlled by the BPF. DMP signal.

1. Before active reception starts, the detection sub-system continuously searches for the four tones (transmitted for a short time when the PTT is pressed at the transmitter). To increase detection probability and improve response times, digital processing techniques are used: the output signals of the four tone detectors are applied to the codec input selector, via the SOFT1 thru SOFT4 lines. The information is sent to the MCU module and digitized by the codec. The MCU module compares the energy of the four tones and determines which tone is received. When the MCU module establishes that active reception should start, it generates the AUDIO GATE signal, which closes the RCV gate, and commands the input selector to disconnect the SOFT1 thru SOFT4 lines and connect instead the output signal of the LPF-1 input selector to the CODEC IN line.

2. After active reception starts, only the 3000Hz and 3300Hz tones are used. Therefore, a different detection method is used: the output signals of the 3000Hz and 3300Hz detectors are applied to a comparator, whose output signal, HARD, FSK is processed by the MCU module. The MCU module determines that active reception continues as long as the HARD FSK signal changes between low and high logic levels.

   The HARD FSK signal is used during reception because the codec performs speech processing and cannot digitize the SOFT signals.

   In other cases, the SOFT signals would be transferred to the MCU module, because they contain more information and can lead to better decisions.

(e) Signal path with digital voice processing. When using any form of digital signal processing, the output signal of the

input amplifier is routed to the MCU module and returned, as explained in para. (1).(d) above with respect to transmit signal processing. The analog signal appearing at the codec output is filtered by the variable low-pass filter 2 and connected to the receive path by means of the RCV gate.

(f) Internal modem operation. When using the internal modem, the signal returning from the MCU module on the RXBBD line is routed by means of the RXBB selector-2 to the RXBBF line, in the RMT/DATA connector.

(g) Squelch operation. Squelching is performed by controlling the RCV gate. The squelch is controlled by the digital signal processing circuits in the MCU module. When using syllabic squelch, the processing of the received signal is performed by analog circuits on the AUDIO module, and the result is sent for evaluation to module MCU by means of the SQ out control signal.

(3) MCU/AUDIO communication interface (figure 2-9). The communication between the microprocessor in the MCU module and the ports in the AUDIO module takes place via an interface circuit located on the AUDIO module.

This interface transfers control signals to and from the microprocessor located on the MCU module and the various control line of the AUDIO module.

(4) Self-test sub-system. During self-testing, the microprocessor on the MCU module initiates the following tests:

(a) Audio path test, by closing the loop between the transmit output and the receive input via the BIT2 line.

(b) Codec operational test, via the BIT1 line.

(c) Audio and earphone amplifier test.

b. Transmit Path Circuit Analysis (fig. 2-10 thru 2-16)

(1) TX data buffer (fig. 2-10.D and 2-11). The TX data buffer is built around amplifier U6-8 and the analog switch U5. The simplified diagram of the circuit is shown in fig. 2-11.
The TXBBIN signal from the RMT/DATA connector is applied to the inverting input of U6 (pin 9). Zener diodes CR7 and CR9 protect the switch U5-4 against excessive voltage.

The TXBBIN signal is routed according to the operating mode:

(a) When using an external modem, the control input (pin 9) of switch U5 receives a low level from the MCU/AUDIO interface via the LOA line. As a result, the switch closes and the output U6-8 is connected to its inverting input (pin 9) via feedback resistor R69.

The TXBBIN signal is amplified according to the ratio of R69 to R64, and applied to the input selector (pin 15 of U1).

In this case, there is a virtual ground at the junction of R74 and R64, therefore, the input impedance is determined by R64 (600 ohms).

(b) When using the internal modem, line LOA is at a high level, the feedback loop of amplifier U6-8 is disconnected and U6-8 operates as a comparator.

In this case, the input impedance is very high as long as the input voltage does not exceed the breakdown voltage of the Zener diodes CR7 and CR9.

(2) Input selector (fig. 2-10.D). The various audio signals are applied to pins 12 thru 15, 1 and 4 of the input selector U1. U1 passes the audio signal corresponding to the selected operating mode, according to the control signals DOV, FOR and FMI. These control

signals are applied from the MCU/AUDIO interface (fig. 2-10.A) to pins 10,11 and 9, respectively.

Table 2-5 lists the selected input signal ording to the binary code applied to the control inputs of U1.

Table 2-5. Input Selector U1

Control Signal			Selected Input	Selected Signal
FMI (Pin 9)	DOV (Pin 10)	FOR (Pin 11)		
0	0	0	Pin 13	Rear-panel microphone signal - MICR
0	0	1	Pin 14	Front panel microphone signal - MIC COMB F
0	1	0	Pin 15	TXBB signal from the TX data buffer U6-8
0	1	1	Pin 12	Demodulated receive signal DEM SIG
1	0	0	Pin 4	Test signal BIT2
1	1	1	Pin 1	Demodulated receive signal DEM SIG

(3) Input amplifier (fig. 2-10.D). The audio signal passed by the input selector is amplified by the input amplifier built around U7-8. The gain of each audio signal is determined by the feedback resistor R20 and by the resistors connected in series with U1 inputs.

(4) SIDETONE gate. The SIDETONE gate U5-14 is controlled by the STC line from module MCU. When the STC line rises to a high level, the output signal of amplifier U7-8 is transferred to the FIX AUDIO and earphone amplifiers, via the SIDETONE line.

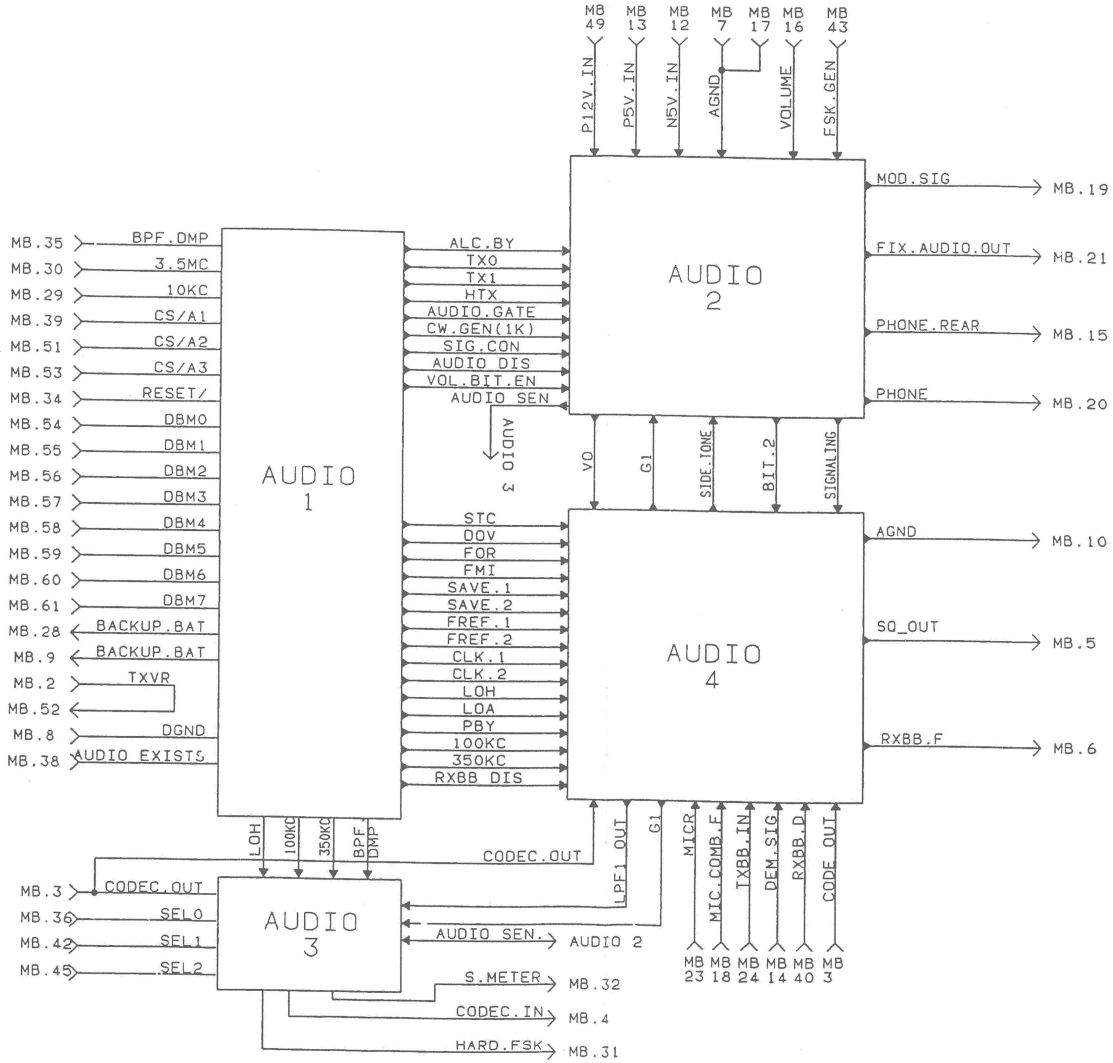


Figure 2-10.A. Module AUDIO, Schematic Diagram (Sheet 1 of 5)

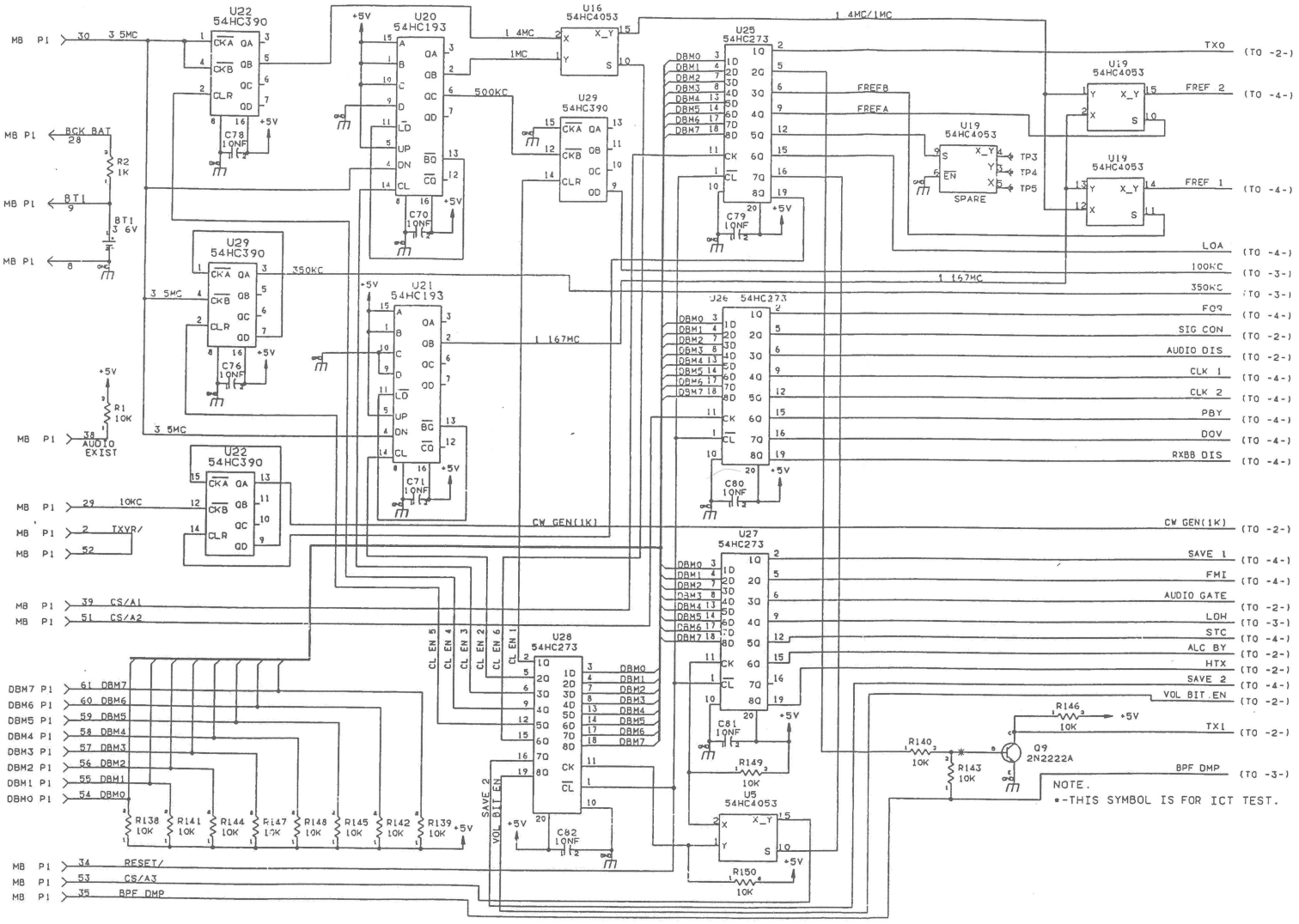


Figure 2-10.B. Module AUDIO, Schematic Diagram (Sheet 2 of 5)

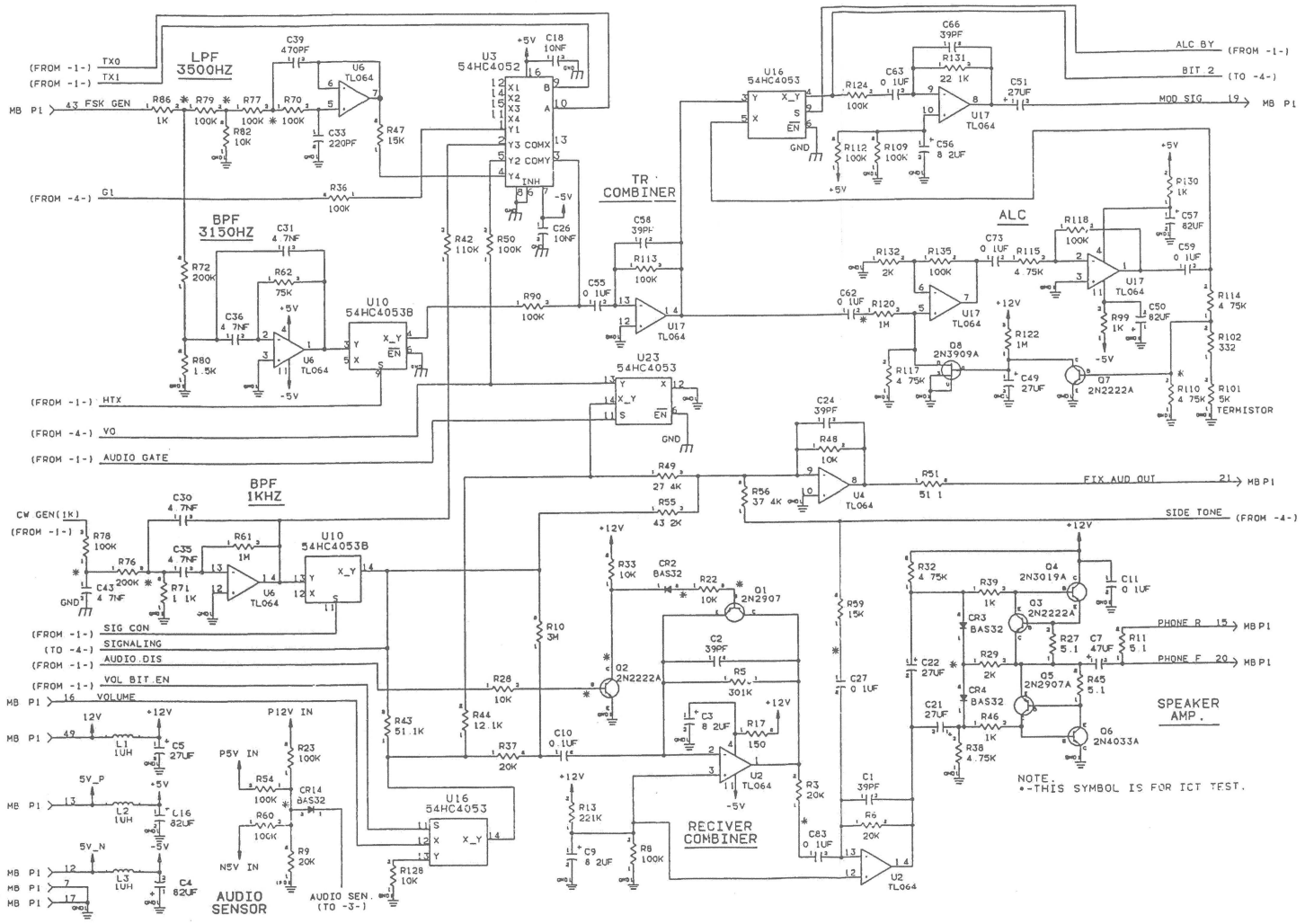


Figure 2-10.C. Module AUDIO, Schematic Diagram (Sheet 3 of 5)

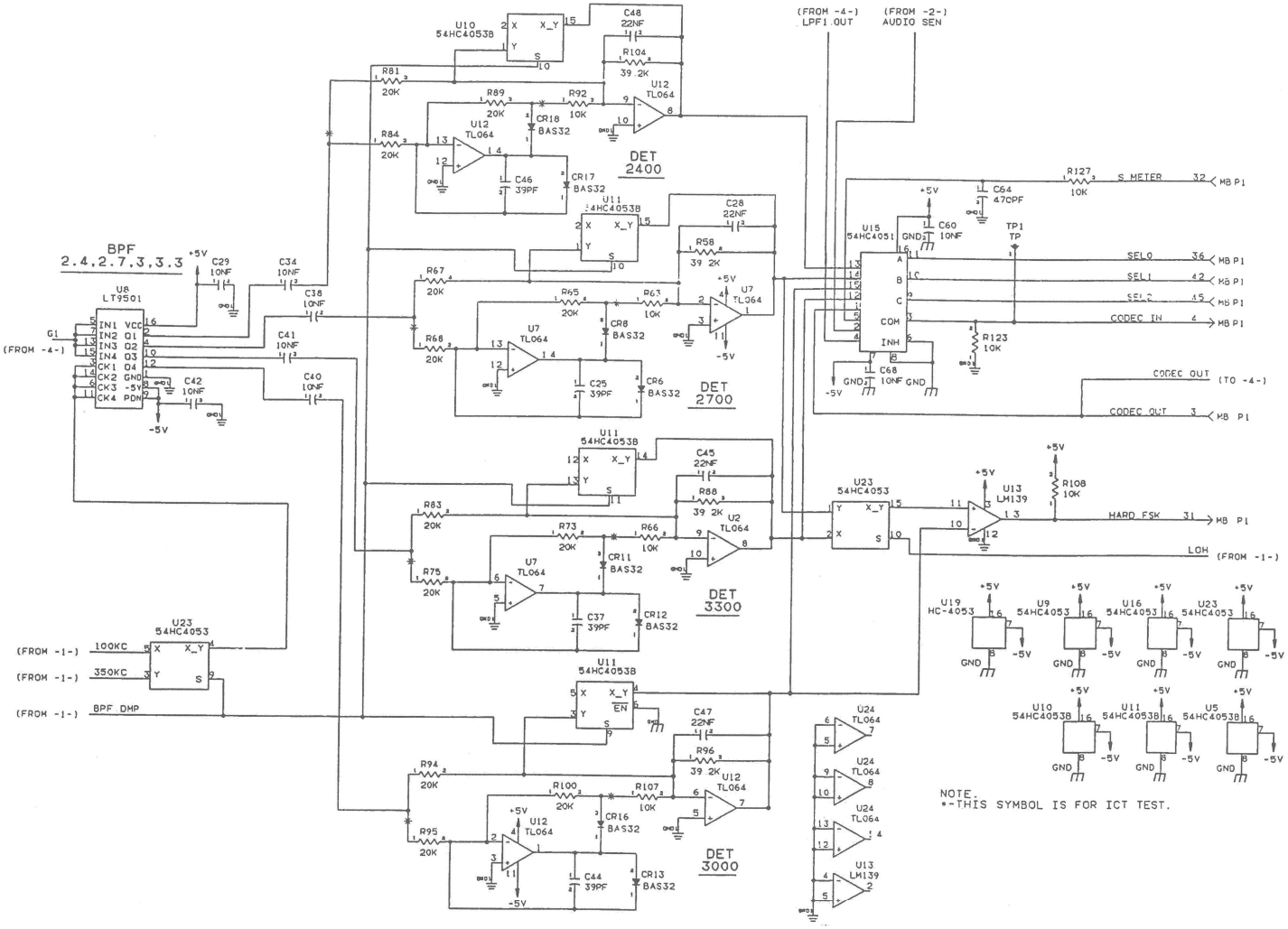


Figure 2-10.D. Module AUDIO, Schematic Diagram (Sheet 4 of 5)

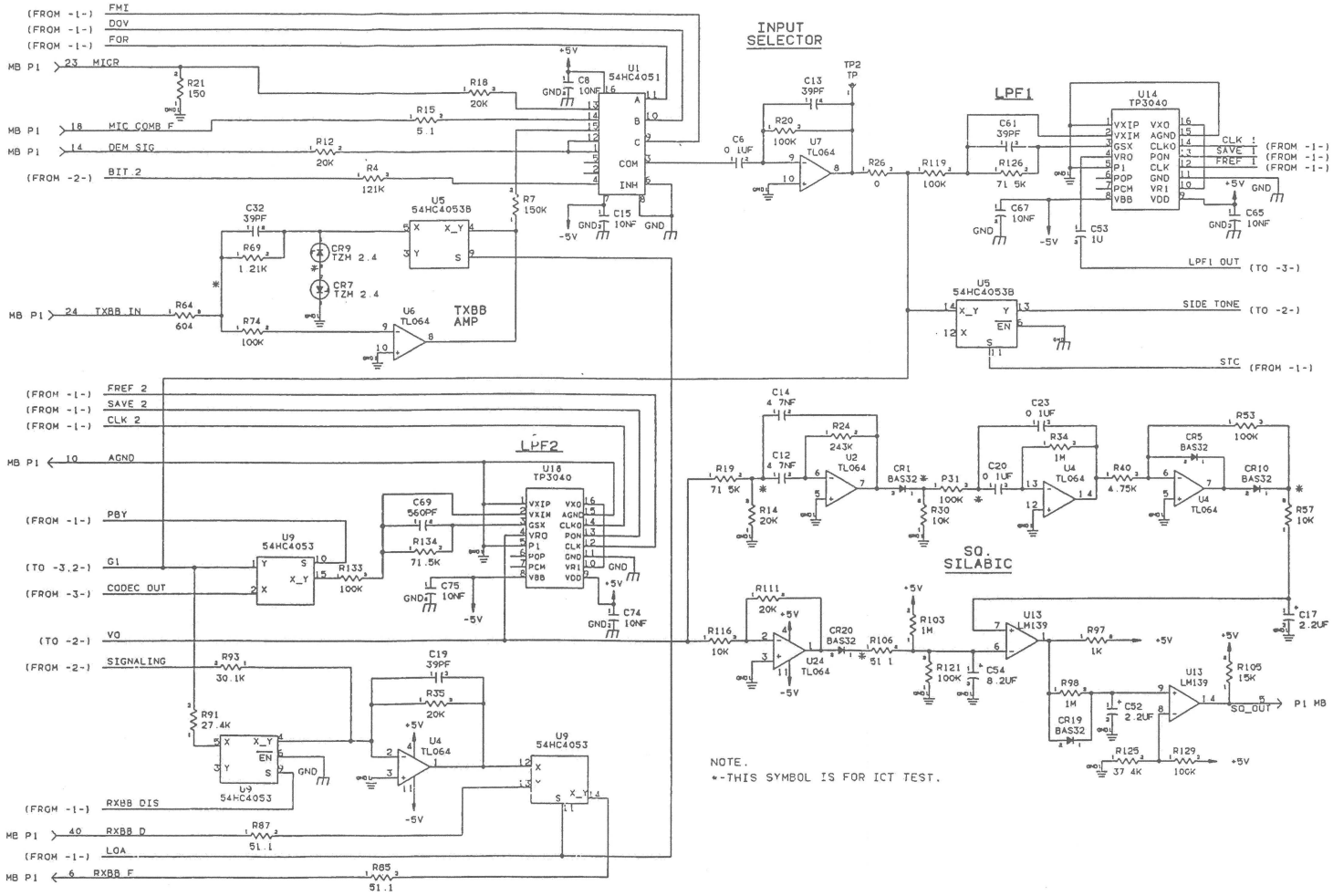


Figure 2-10.E. Module AUDIO, Schematic Diagram (Sheet 5 of 5)

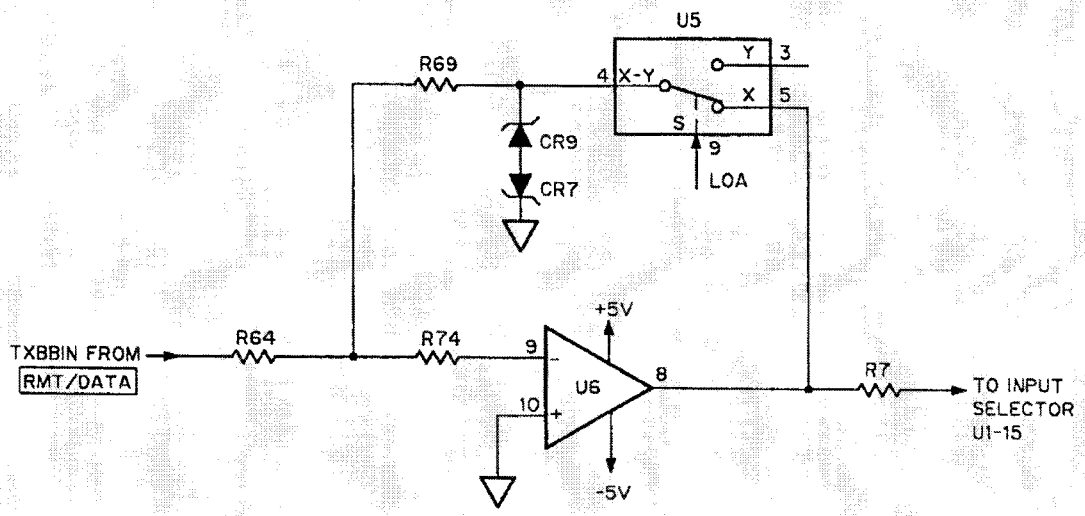


Figure 2-11. TX Data Buffer, Simplified Circuit

(5) Variable low-pass filter 1 (fig. 2-10.D). The variable low-pass filter 1 is built around the PCM monolithic filter U14. When using digital voice processing, the output signal of amplifier U7-8 is applied to pin 2 of U14. U14 is controlled by the CLK01 signal, received from the MCU/AUDIO interface (pin 9 of U26). The cut-off frequency of the low-pass filter is controlled by the MCU module, by means of the FREF1 signal applied to pin 12 of U14. U14 is disabled when a high level is received from MCU/AUDIO interface U27-2 to pin 13, via the SAVE-1 Line.

(6) Codec input selector (fig. 2-10.C.). The codec input selector U15 selects the signal to be processed by the codec (in module MCU) according to the binary code applied to the control inputs (pins 11, 10, 9) via the SEL0, SEL1 and SEL2 lines, respectively.

Table 2-6 lists the selected signal according to the operating mode.

Table 2-6. Input Signals of the Codec Input Selector

Operating Mode	Selected U15 Input	Selected Signal
Searching for FSK tones	Pin 13	SOFT1 from 2400Hz detector
	Pin 14	SOFT2 from 2700Hz detector
	Pin 15	SOFT4 from 3300Hz detector
	Pin 12	SOFT3 from 3000Hz detector
Self-test	Pin 1	BIT1 signal from the CODEC OUT signal
AUTOCALL function	Pin 5	S-METER received signal level
DC voltages testing	Pin 2	AUDIO SEN signal of AUDIO SENSOR
Voice transmission or reception	Pin 4	Output of low-pass filter 1, U14-4

(7) Variable low-pass filter 2 (fig. 2-10.D). The variable low-pass filter 2 is built around monolithic PCM filter U18. The analog output signal from the CODEC OUT line is applied through switch U9-15 to pin 2 of U18. U18 is controlled by the CLK02 signal applied from the MCU/AUDIO interface (pin 12 of U26). The cut-off frequency of the low-pass filter is controlled by means of the FREF2 signal applied to pin 12. U18 is disabled when a high level is received from MCU/AUDIO interface U28-16 to pin 13, via the SAVE-2 line.

(8) TX signal selector (fig. 2-10.B). The TX selector U3 (fig. 2-10.B) selects the signal to be transmitted. U3 is controlled by the control lines TX0 and TX1. TX0 is received directly from module MCU and TX1 is the output of NOR gate Q9 (fig. 2-10.A). Table 2-7 lists the selected TX signal according to the operating mode.

Table 2-7. Selected TX Signal

Operating Mode	Selected U3 Input	Selected Signal
Analog voice	Pin 1	G1 - output signal of input amplifier U7-8
External modem		
Digital voice processing	Pin 5	VO - output signal of low-pass filter 2
Internal modem		
CW operation	Pin 2	1kHz CW signal
Transmission of FSK tones	Pin 4	Output signal of 3500Hz low-pass filter

(9) TX adder (fig. 2-10.B). The TX adder is built around operational amplifier U17-14. The amplifier combines the following two signals:

(a) The output signal of the TX selector U3-3.

(b) The output signal of the 3150Hz band-pass filter, via resistor R90.

The level of each signal is determined by the ratio of R113 to R90 and the resistors connected in series to U3 inputs.

(10) ALC amplifier (fig. 2-10.B, 2-12). The ALC amplifier comprises the voltage-controlled attenuator built around Q8, the amplifiers U17-7, U17-1 and the rectifier built around Q7.

(a) The attenuation of the voltage-controlled attenuator depends on the drain-source resistance of the JFET Q8. This resistance is direct proportional to the gate voltage.

(b) The output voltage of the attenuator is amplified by U17-7 and U17-1. The voltage at the output of U17-1 is applied via C59 and R114 to the base of Q7. Q7 operates as a rectifier. R101 is a temperature compensation thermistor.

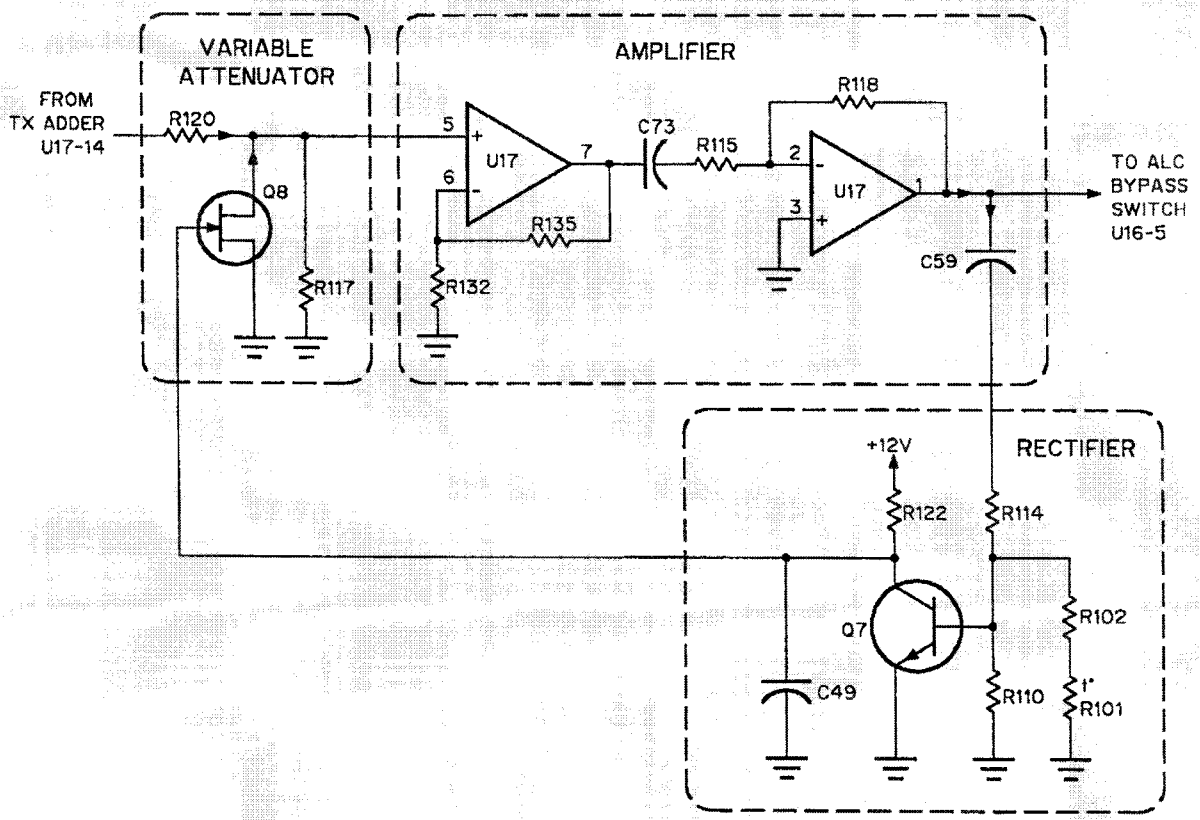


Figure 2-12. ALC Amplifier, Simplified Circuit

(c) As long as the input voltage is low, the peak-to-peak voltage appearing at the output of U17-1 is not enough to cause Q7 to conduct. Under these conditions, the voltage applied to the gate of Q8 is maximal.

The resulting drain-source resistance is also maximal, and the input signal is essentially not attenuated.

When the voltage increases beyond the ALC threshold (determined by the bias applied to Q7), Q7 starts to conduct on positive signal peaks, capacitor C49 discharges and the voltage across it decreases. The dynamic resistance of Q2 decreases and the attenuation of the input signal increases.

As a result, the output voltage of U17-1 remains at a constant level, in spite of increases in the input voltage.

(11) ALC bypass switch U16-4 (fig. 2-10.B, 2-12). In the AJ mode, since the ALC periods are too long, the control input of U16 (pin 9) receives a high level from the MCU/AUDIO interface U27-15, via the ALC BY line. As a result, the switch connects the output of the TX adder U17-14 (input Y of U16) to the TX output amplifier U17-8 and the ALC circuit is bypassed.

(12) TX output amplifier (fig. 2-10.B). The TX output amplifier is built around operational amplifier U17-8. The transfer function of U17-8 is determined by C66, R131 and R106. The output signal of the amplifier is sent to the IF module, via the MOD SIGNAL line.

(13) Transmission of FSK tones (fig. 2-10.B). The transmission of the FSK tones is performed as follows:

(a) 3500Hz low-pass filter. This low-pass filter is built around amplifier U6-7. When using the internal modem or in DCW mode, one of the four FSK tones received from module MCU via FSK GEN line, is filtered by U6-7 and then applied to pin 4 of the TX signal selector U3.

(b) 3150Hz band-pass filter. This band-pass filter comprises amplifier U6-1 and switch U10-4. In the CLR, SEC or AJ modes, a high level is applied to the control input of the switch (pin 9), from the MCU/AUDIO interface U27-19 via the HTX line. As a result, the 3000Hz or 3300Hz FSK tone passes through the band-pass filter to the TX adder U17-14.

(14) Frequency dividers (fig. 2-10.A). The dividers receive two reference frequencies (3.5 MHz and 10 KHz) from the SYNT module.

(a) When operating in the CW mode. U22-13 operates as divider-by-10 to obtain 1 KHz from 10 KHz.

(b) U22-5 operates as a divider by 2.5 to obtain 1.4 MHz from 3.5 MHz.

(c) U20-2 operates as a divider by 3.5 to obtain 1 MHz from 3.5 MHz.

(d) U21-2 operates as a divider by 3 to obtain 1.167 MHz from 3.5 MHz.

(e) U29-3 operates as a divider by 10 to obtain 350 KHz from 3.5 MHz.

(f) U20-6 operates as a divider by 5, and U29-9 operates as a divider by 7 to obtain 100 KHz from 3.5 MHz.

(g) The signals FREF1 and FREF2 determine the upper cutoff frequency of the variable low-pass filters 1 and 2. The required clock frequency is 1.00 MHz for a cut-off frequency of 2.2 KHz, 1.167 MHz for 2.7 KHz, and 1.40 MHz for 2.4 KHz. The appropriate clock signal is selected by the selectors U16 and U19, in accordance with the control signals received from module MCU via the ports (U25, U26, U27, U28).

(15) RXBB selector-1 and 2 and RX data buffer (fig. 2-10.D). The RXBB selector-1, U9-4, is controlled by the RXBB DIS line, and the RXBB selector-2 U9-14 is controlled by the LOA line, received from the MCU/AUDIO interface U25-15 and U26-19, respectively.

(a) When lines LOA and RXBB DIS are both at a low level, U9-14 and U9-4 select the received signal, applied from the input amplifier U7-8 to their X inputs (pins 5 and 12).

(b) When line LOA is at a high level, U9-14 selects the RXBB.D signal applied from MCU module to its Y input (pin 13).

The output signal of U9-4 is applied to the RX data buffer built around U4-1. The output signal of U4-1 is sent via U9-14 and the RXBBF line to the RMT/DATA connector.

(16) FSK tone detection circuits (fig. 2-10.C).

(a) Band-pass filters. U8 contains four band-pass filters. The center frequency of each band-pass filter is turned to one of the four FSK tones. The four filters have a common input (G1 line) and a common clock input. The clock input can receive two frequencies: 100 KHz for normal filter operation and 350 KHz for quick discharging of filter energy. These frequencies are applied from the selector U23-4 (controlled by module MCU, by means of the BPF. DMP signal).

The output signals of U8 (pins 2, 4, 10, 12) are applied via coupling capacitors to 4 identical detectors. The operation of the 2400Hz detector is described in para. (b) below. The operation of the other detectors detailed in para. (c), (d) and (e) below is similar.

(b) 2400Hz detector. This detector is built around amplifiers U12-14, U12-8 and switch U10-15. The output signal of the 2400Hz band-pass filter (pin 2 of U8) is rectified by the full-wave rectifier comprising U12-14, CR17 and CR18. The rectified signal is filtered by the circuit comprising U12-8, C48 and R104. The switch U10-15 is connected in parallel to C48, in order to reduce the discharge time of C48 during frequency hopping (or when operating in the AUTOCALL mode). In these modes, the switch can be closed by the band-pass filter command (BPF.DMP) received from the MCU module: when the switch is closed, C48 discharges rapidly.

(c) 2700Hz detector. This detector is built around amplifiers U7-14, U7-1, switch U11-15 and rectifiers CR8 and CR6.

(d) 3300Hz detector. This detector is built around amplifiers U7-7, U2-8, switch U11-14 and rectifiers CR11 and CR12.

(e) 3000Hz detector. This detector is built around amplifiers U12-1, U12-7, switch U11-4 and rectifiers CR16 and CR13.

(f) Switch U23-15. This switch is controlled by the LOH line from U27-9. Usually, LOH is at a low level, and the switch passes the output signal of the 3300Hz detector to the non-inverting input (pin 11) of the comparator U13.

When using the narrow bandwidth option, LOH rises to a high level and the output signal of the 2700Hz detector is applied to the non-inverting input of U13. The inverting input of U13 receives the output signal of the 3000Hz detector. U13 compares the two signals and generates a low level for 3000Hz detection and high level for 3300Hz (or 2700Hz) detection. The output signal of U13 is sent via the HARD FSK line to the MCU module.

(17) Sidetone path. When the transmitter operates normally, the STC control line rises to a high level and the SIDETONE gate U5-13 (fig. 2-10.D) connects the output signal of the input amplifier U7-8 to the RX adder U2-14 and to the FIX AUDIO amplifier U4-8 (fig. 2-10.B.), via the SIDETONE line.
In other cases, the STC line falls to a low level and SIDETONE transfer is disabled.

(18) Signaling switch (fig. 2-10.B). In the CW mode, the 1kHz signal is applied to the Y input (pin 13) of the signaling switch U10. The switch is controlled by the SIGCON line. A high level on this line connects the 1kHz signal to the RX adder U2-1 and to the FIX AUDIO amplifier U4-8.

(19) RCV gate (fig. 2-10.B). The RCV gate U23-14 is controlled by the AUDIO GATE line applied from the MCU/AUDIO interface U27-6 to the control input (pin 11) of U23. When a speech signal is detected by the squelch circuits (active reception), the AUDIO GATE line rises to a high level and the output signal of the variable low-pass filter 2 is applied to the RX adder U2-1 and the FIX AUDIO amplifier U4-8. In other cases, the line is at a low level and the path is blocked.

(20) RX adder (fig. 2-13). The RX adder is built around the amplifier U2-1 and U2-14. The simplified diagram of the circuit is shown in fig. 2-14.

(a) Usually, the transistors are cut-off and the transfer function of U2-1 is determined by R5 and C2.

(b) When operating with active squelch, then if no signal is received, the control line (AUDIO DIS.) from the MCU/AUDIO interface (pin 6 of U26) rises to a high level, Q1 and Q2 conduct and the gain is reduced.

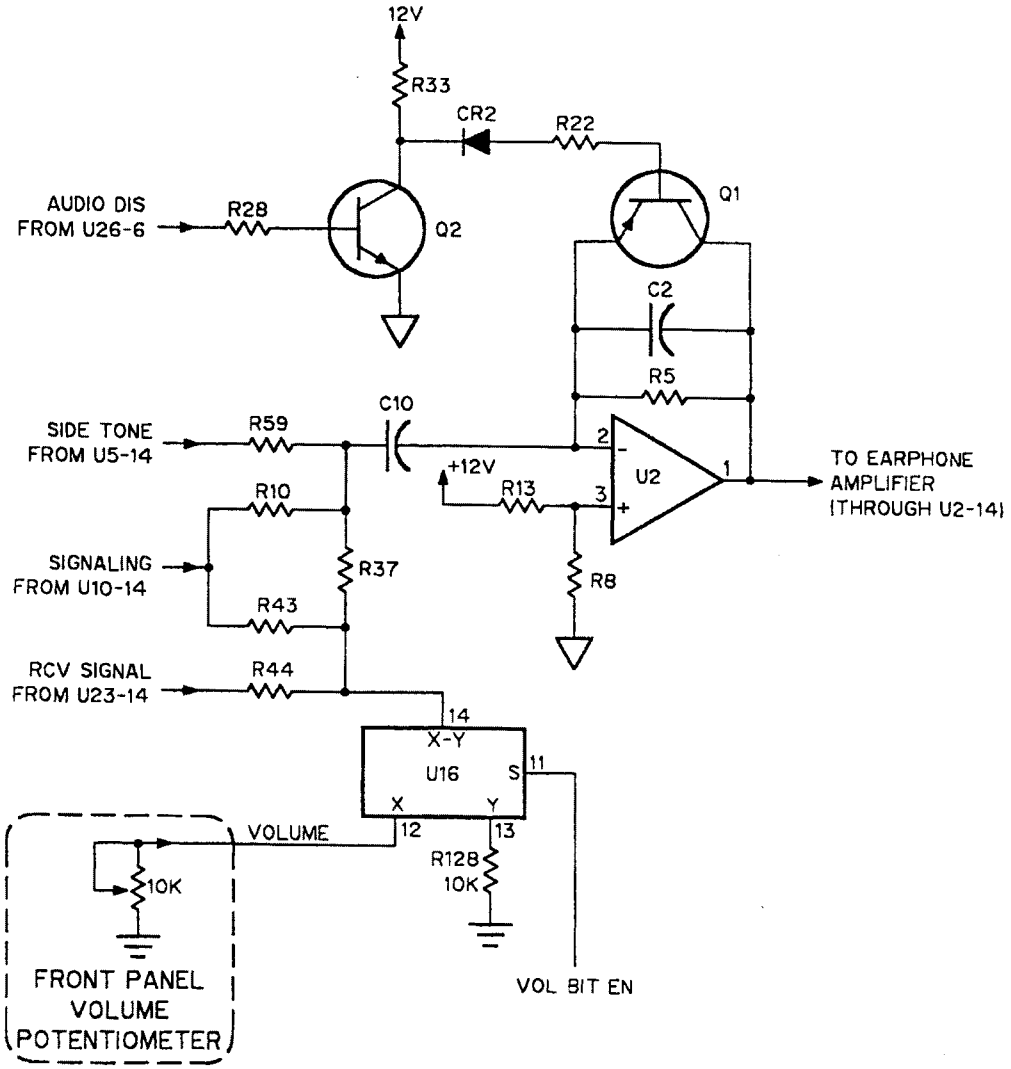


Figure 2-13. RX Adder, Simplified Diagram

(c) U2-1 combines the following signals:

1. SIDETONE signal from U5-14. The level of this signal is fixed and cannot be changed by the volume control.

2. Received signal from RCV gate U23-14. The level of the received signal is controlled by the volume control on the front panel.

3. Signaling from U10-14. This signal is applied to the amplifier via two resistors, R43 and R10. Only the level of the signal applied via R43 is controlled by the volume control signal, reached from selector U16-14. R10 provides a path that ensures the signaling would be heard even with the volume control at the minimum position.

   The built-in-test (BIT) mode needs maximum signaling amplitude, irrespective of the volume potentiometer position. Therefore, during B10, the resistor, R128 is applied from selector U16-14, controlled by the VOL.BIT.EN signal.

(21) Earphone amplifier (fig. 2-10.B). The earphone amplifier comprises the power transistors Q4 and Q6, connected in a push-pull configuration, and the transistors Q3 and Q5, used for current limiting. Diodes CR3 and CR4 reduce cross-over distortion.

(a) The output signal of the RX adder U2-14 is coupled by C21 and C22 and applied via R118 and R119 to the bases of Q5 and Q7, respectively. The signal appearing at the emitters of Q5 and Q7 passes through current-sensing resistors R39, R46 and via coupling capacitor C7 to the AUDIO connectors.

(b) Current limiting under overload.

1. During normal operation, the voltage across current sensing resistors R39 and R46 is low, therefore Q3 and Q5 are cut-off.

2. When the power consumption exceeds above the limit, the voltage across R39 or R46 causes the corresponding transistor to conduct. Consequently, the current applied to the bases of power transistors Q4 and Q6 is reduced.

(c) Bias to Q4 and Q6 is provided from the +12V line through R32, CR3, CR4 and R38. The bias holds the transistors at the conduction threshold, to reduce cross-over distortion.

(22) FIX AUDIO amplifier (fig. 2-14). The FIX AUDIO amplifier U4-8 combines the SIDETONE signal from U5-14, the received signal from RCV gate and the signaling from U10-14. U4-8 gain is determined by R48. The output signal of U4-8 is sent to the RMT/DATA connector, via the FIX AUDIO line.

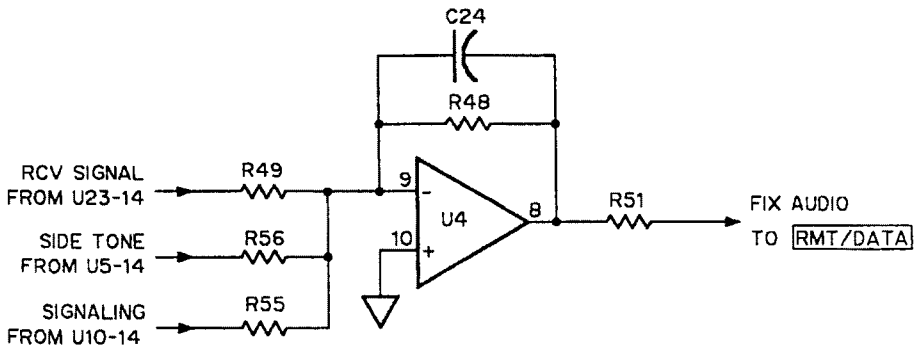


Figure 2-14. FIX AUDIO Amplifier, Simplified Diagram

(23) Syllabic squelch circuits (fig. 2-10.D, 2-15, 2-16).

(a) Principle of operation (fig. 2-15, 2-16). The squelch circuit sends the SQ. OUT command to the MCU module to turn the RCV gate off, unless a speech signal is detected in the receive signal. In order to detect the characteristic speech waveforms, the received signal is applied to two parallel paths, one processing the signal to extract the speech waveform, and another for setting an adaptive threshold.

The block diagram of the syllabic squelch is shown in fig. 2-15.

1. Signal processing path. The received signal is attenuated and then filtered by a 500Hz band-pass filter. The filtered signal is rectified by an envelope detector, whose output is filtered again by a band-pass filter centered on 5Hz. This filter passes the amplitude variations caused by the syllables. The output filter of this band-pass filter is rectified and filtered to obtain a DC voltage proportional to the syllabic modulation in the received signal. This DC voltage-is applied to one of the squelch comparator inputs.

2. Threshold generation. The rectified received signal is amplified and then rectified by a peak rectifier. The resulting DC signal is applied to the other input of the squelch comparator. The integrators located at the end of the two paths provide the required timing for the comparison of the two signals. The squelch comparator sends a command to turn the RCV gate on whenever the processed signal exceeds the threshold. To prevent gate chattering, a delay circuit delays the turn off of the gate for a short time, thereby bridging across short interruptions. This prevents interruption of the received signal between words. Fig. 2-16 shows typical waveforms in the squelch circuits.

(b) Squelch circuit operation (fig. 2-10.D). The filtered audio signal appearing at pin 4 of the low-pass filter 2, U18, is simultaneously applied to the inputs of the signal processing path and to the threshold-generation path.

1. Signal processing path. The input voltage passes through a voltage divider, composed of R14 and R19, and is then filtered by a 500Hz band-pass filter, built around U2-7. The output signal of U2-7 (B in fig. 2-16) is applied to an envelope detector, built around CR1.

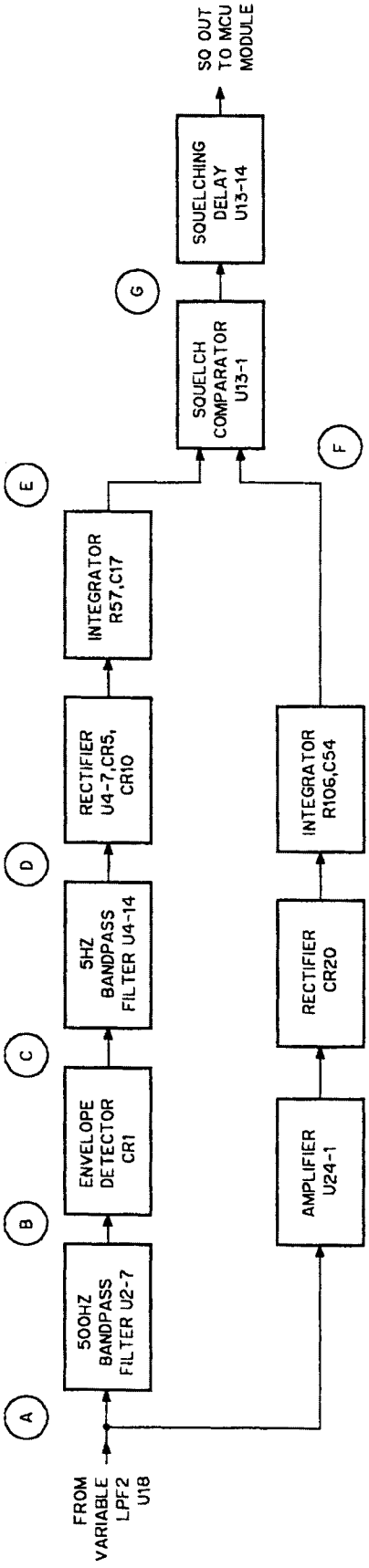


Figure 2-15. Syllabic Squelch Circuits, Simplified Block Diagram

The rectified voltage (C in fig. 2-16) is filtered by a 5Hz band-pass filter, built around U4-14. The output signal of U4-14 (D in fig. 2-16), which is the envelope of the received signal, is again rectified by the full-wave rectifier composed of U4-7, CR5 and CR10, and then filtered by the integrator R57, C17 (E in fig. 2-16).
The voltage across C33 is applied to the non-inverting input (pin 7) of the squelch comparator, U13-1.

2. Threshold generation. The input voltage is amplified by amplifier U24-1, according to the ratio of R116 to R111. The output voltage of U24-1 is rectified by CR20, filtered by the integrator R106, C54 and then applied to the inverting input (pin 6) of the squelch comparator, U13-1. A small DC bias is applied to the inverting input of U13 from the voltage divider comprising R103 and R121.

When the received signal contains speech, the voltage at the non-inverting input of U13-1 exceeds the voltage at its inverting input. Consequently, the output of U13-1 (G in fig. 2-16) rises to a high level and capacitor C52 charges rapidly through CR19 and R98. When the voltage across C52 exceeds the voltage applied to the inverting input of the squelching delay U13-14 (pin 8) via the voltage divider comprising R125 and R129, the output of U13-14 rises to a high level. The high level is sent to the MCU module via the SQ-OUT line. In response, the MCU module sends a command to close the RCV gate (para. (19) above), allowing the received signal to pass to the audio amplifiers.

When the received signal does not contain speech, the voltage applied to the inverting input of U13-1 exceeds the voltage applied to its non-inverting input.

Consequently, the output U13-1 falls to a low level and C52 slowly discharges through R98. When the voltage across C52 decreases below the voltage at the inverting input of U13-14 the output of U13-14 falls to a low level. This level is sent to the MCU module, that opens the RCV gate so the received signal cannot pass to the audio amplifiers. The slow discharge time constant of C52 ensures that short negative pulses appearing at the output of U13-1 do not change the state of the RCV gate.

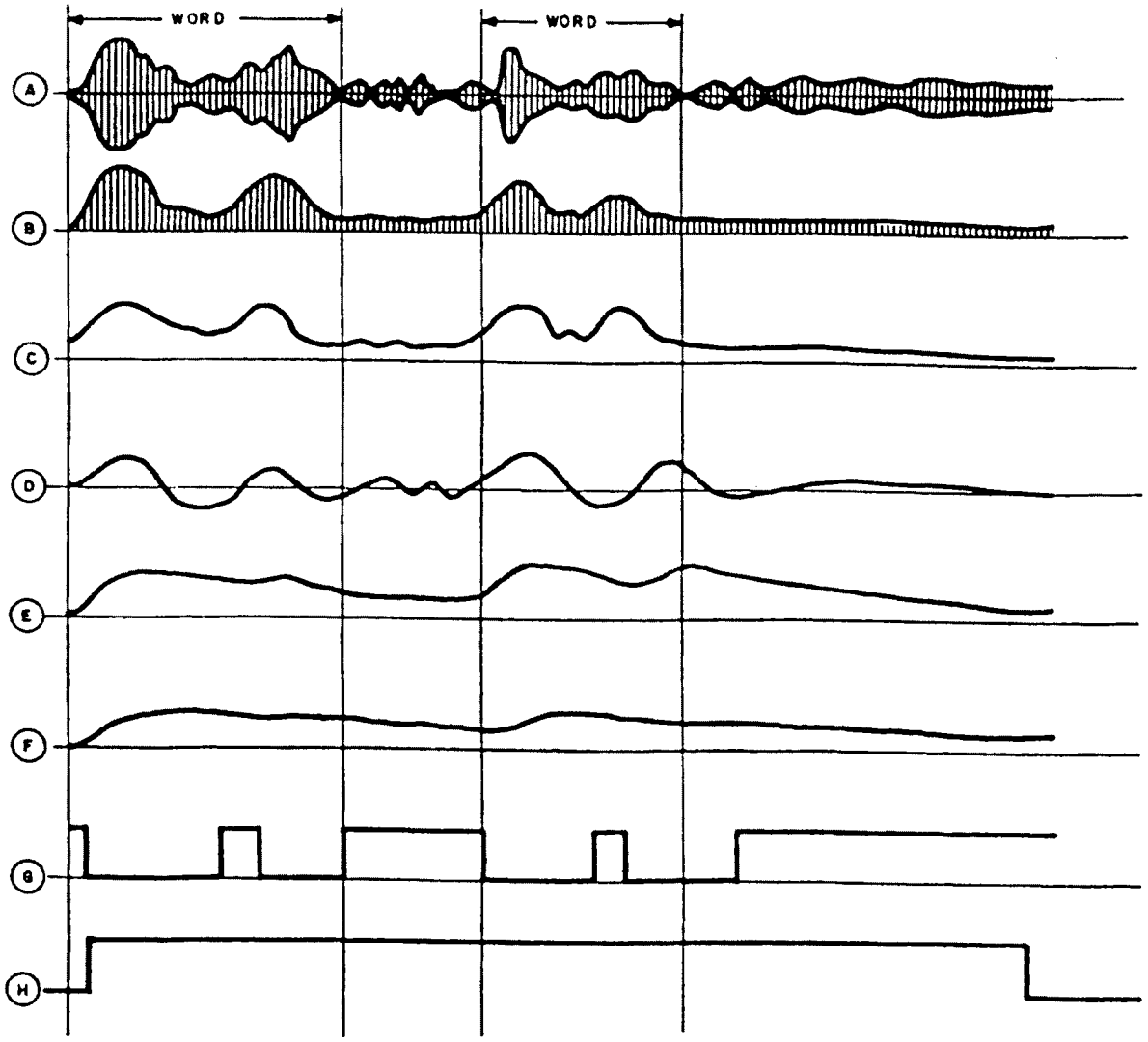


Figure 2-16. Typical Waveforms in the Squelch Circuit

(24) Audio sensor. This sensor adds the following voltages: 12V, 5V-P, 5V-N, and provides a signal, AUDIO SEN (approx. +2.5V), on the anode of CR14, when all the voltages appears correctly. This signal is applied to pin 2 of the codec input selector U15.

(25) MCU/AUDIO interface (fig. 2-10.A). This interface comprises four latches, U25, U26 and U27 and U28. The latches are used to transfer control signals from the microprocessor located in the MCU module to the internal control lines of module AUDIO. The syllabic squelch output signal (SQ OUT) is transferred to the MCU module.
The microprocessor writes data to the latches via the bidirectional bus lines, DBM0 to DBM7. Since the data bus is connected to all the latches, a chip select signal is used to select the desired latch (CS/A1 selects U25, CS/A2 selects U26 and CS/A3 selects U27 and U28 through the selector U5). The microprocessor sets each bit of the data byte according to the desired function. Upon the rising edge of the chip-select signal, the data byte is latched into the selected latch.
All the four latches can be reset by the RESET* line: a high on the RESET* line enables the four latches, and a low level disables them.

(26) Self-test sub-system. During self-test, the following tests are performed in the AUDIO module:

(a) Codec test. The microprocessor in the MCU module tests the operation of the codec U4 as follows:

1. The microprocessor sends a known data stream to the digital input of the codec. This data stream is the digital representation of the desired test signal.

2. The codec converts the data to an analog signal and transfers it, via the BIT1 line and the selector U26, back to the analog input of the codec.

3. The codec converts the analog signal to digital data and sends it back to the microprocessor.

4. The microprocessor compares the received data with the previously-sent data, and determines whether the test is passed or failed.

(b) Audio path test. The microprocessor in the MCU module tests the transmit and receive path circuits by closing a loop from the output of the transmit path to the input of the receive path, via the BIT 2 line.
This test is performed in a similar way to the codec test described above.

(c) Receive path test. A 1kHz sinusoidal signal is applied via the DEM SIG line to the receive path circuit. The output signal of the earphone amplifier is sent to a detector located on the MCU module, which checks the signal level.

2-9. Module IF
(fig. 2-17 thru 2-23)

This paragraph covers the theory of operation of module IF. Module IF has two versions:

- A full version that enables operation of PRC-2200 in the AM, NCW and SSB modes.

- A downgraded version, that enables operation of PRC-2200 only in the SSB mode.

The version actually installed in the PRC-2200 determines the manufacturer catalog number of the PRC-2200.

This paragraph covers the theory of operation of the full version.

Details on circuits that are specific for the versions of the module are given in Note 6 of figure 2-18.

a. Block Diagram Analysis (fig. 2-17). Figure 2-17 shows the block diagram of module IF.

(1) Transmit path.

(a) Transmit signal path. The transmit path receives the modulation signal from module AUDIO and modulates it onto the 5.25MHz carrier signal, supplied by the synthesizer. The modulation is performed by a double-balanced modulator. The operation of the modulator is controlled by the AM/SSB* line:

1. In the SSB mode, the modulator generates a double-sideband signal.

2. In the AM mode, the modulator adds a carrier to the output signal, to obtain an amplitude-modulated signal.

The modulator output signal is buffered and applied to the filter corresponding to the selected mode: SSB filter, NCW filter or AM filter. The required filter is inserted into the signal path by electronic switches, controlled by the filter control circuit. The filter control circuit converts the SSB and AM/SSB* control signals, received from the MCU module, to drive signals for the filter switches.

The filtered signal passes through a buffer which provides impedance matching and is then sent to the RF module.

(b) Control of transmit path. The transmit path is powered only in the transmit mode, under control of the PTT OUT* line. The PTT OUT* line controls the transmit path supply switch.

(2) Receive path.

(a) Signal path. The 5.25MHz RF signal received from the RF module passes through a matching circuit to the filter bank.

The filtered signal is applied to the IF amplifier. The gain of the IF amplifier is controlled by the AGC voltage provided by the IF AGC time constant control circuit (see para. (2) below). The IF amplifier provides an IF signal of constant amplitude, which is applied to the demodulation circuits:

1. In the SSB and CW modes, the received signal is demodulated by a synchronous SSB demodulator. The demodulator receives a 5.25MHz signal from the synthesizer. The demodulated SSB signal is applied to the AM/SSB selector.

2. In the AM mode, the received signal is amplified by an additional IF amplifier, and then applied to an envelope detector. The demodulated AM signal is amplified by an audio amplifier and applied to the AM/SSB selector.

3. AM/SSB selector. The AM/SSB selector selects the appropriate demodulated signal, under control of the AM/SSB* line. The selected signal is amplified by an audio amplifier and sent via the DEMOD SIG line to the audio processing circuits in the AUDIO module.

(b) IF AGC sub-system. The IF AGC sub-system generates an AGC signal which controls the gain of the IF amplifiers. The dynamic response of the IF AGC signal depends on the selected operating mode.

1. IF AGC detector. The IF AGC detector rectifies the IF signal and converts it to a DC voltage which follows the envelope of the IF signal.

2. IF AGC time constant control circuit. This circuit processes the output signal of the IF AGC detector, to obtain the AGC control voltage.

The processing parameters depends on the operating mode, as indicated by the state of the VOICE/DATA* and NORMAL/FAST* lines.

a. Voice modulation. When using the squelch-off voice mode or CW modulation, in fixed-frequency operation, the AGC attack time is normal, but the release time is long (approximately one second), to maintain constant gain when the received signal changes abruptly, such as during short pauses occurring between words. When using at data modulation, the release time is shorter, about 0.1 second.

When using frequency hopping, the attack time is made shorter, under control of the NORMAL/FAST* line, to allow rapid acquisition of received signal after hopping. During hopping (while the actual frequency transition takes place), a RESET AGC pulse is applied to the AGC control circuit. The RESET AGC pulse resets the AGC voltage to the value corresponding to a signal at the sensitivity threshold. When a signal-appears, the rapid attack time of the circuit allows rapid acquisition and adaptation to the signal level received on the new frequency.

b. Data modulation. During active-squelch voice transmission or data transmission, the release time is made much shorter, because no pauses are expected in the modem signal.

(c) RF AGC sub-system. To increase the dynamic range of the receiver, RF AGC is used. Under strong signal conditions, the RF AGC circuit attenuates the signal applied to the receive amplifier located in module RF, to prevent IF amplifier overloading.

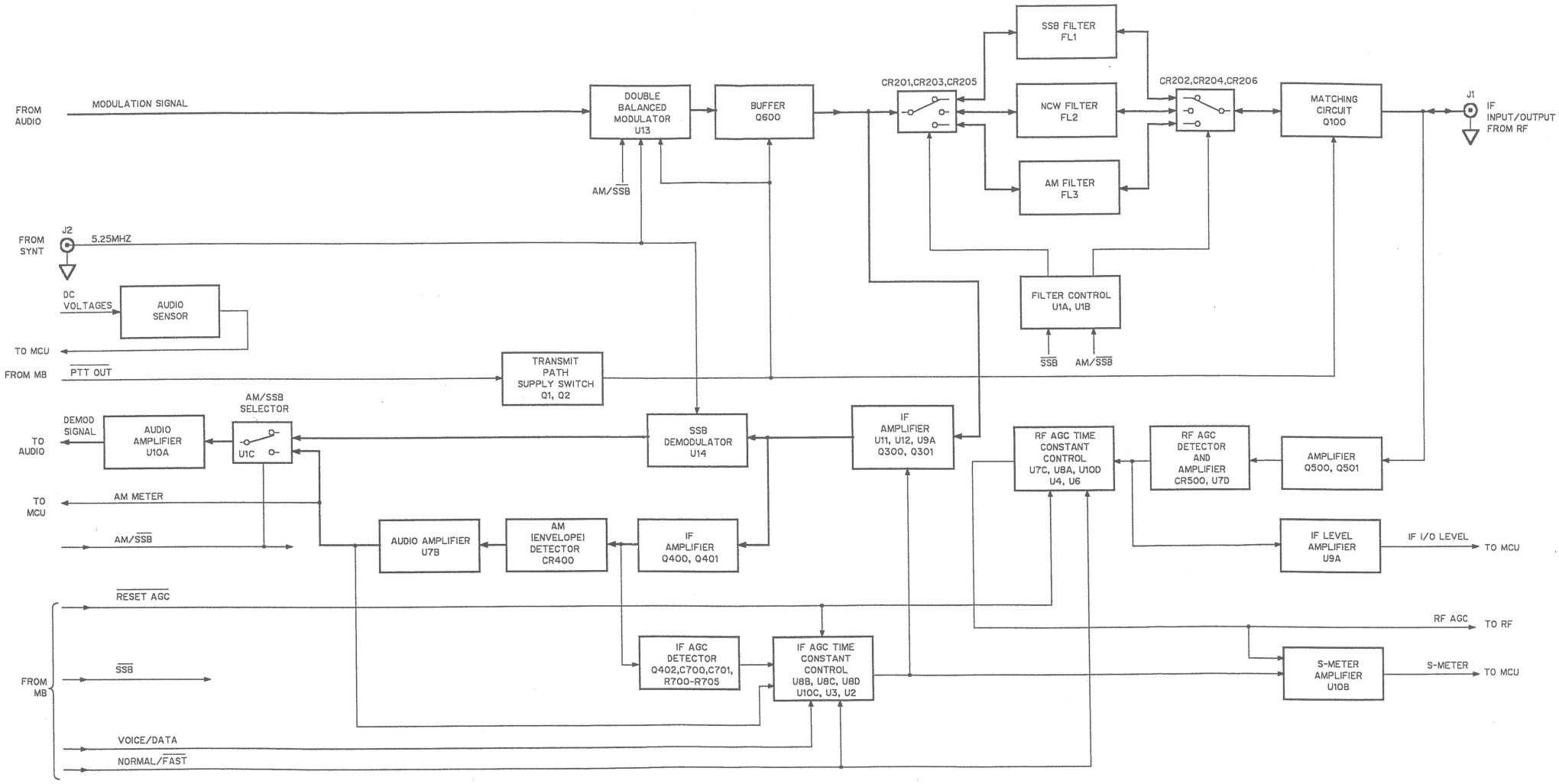


Figure 2-17. Module IF, Block Diagram

The output of U9A in the RF AGC sub-system is also used in the transmit mode, to monitor the output signal of the IF module.

The IF signal appearing at the J1 connector is amplified and applied to a RF AGC detector. The RF AGC detector provides a DC voltage proportional to the envelope of the RF signal. The output signal of the RF AGC detector is processed by the RF AGC time constant control circuit, which provides processing functions similar to those of the IF AGC time constant control circuit (para (2) above). The RF AGC signal is sent via the RF AGC line to the RF module.

(d) Indications.

1. IF I/O LEVEL indication. In the transmit path, the output signal is amplified by the IF I/O LEVEL amplifier and sent to the MCU module, for monitoring.

2. S-METER indication. The S-METER amplifier combines the IF AGC and RF AGC voltages, and generates a DC voltage proportional to the received signal level over a wide range of input signals. The S-METER signal is sent to the MCU module, where it is used to display the received signal level. The S-METER signal is also sent to modules AUDIO, and MCU where it is used as an input for the AUTOCALL algorithm, because it indicates the background level on the various frequencies used by the AUTOCALL procedure.

3. IF SENSOR indication. A resistor network provides an indication of the condition of the supply voltages of module IF to the MCU module.

b. Transmit Path Circuit Analysis (fig. 2-18). The transmit path is activated when the PTT OUT* line is grounded. Current then flows from the emitter of Q2 to the base of Q1, and Q1 saturates. As a result, the -5VF

supply voltage is transferred to the -5V IF TX line, connected to the transmit path components.

(1) Double-balanced modulator. The modulator built around mixer U13 is a double-sideband modulator which performs the modulation of the 5.25MHz carrier in all operating modes.

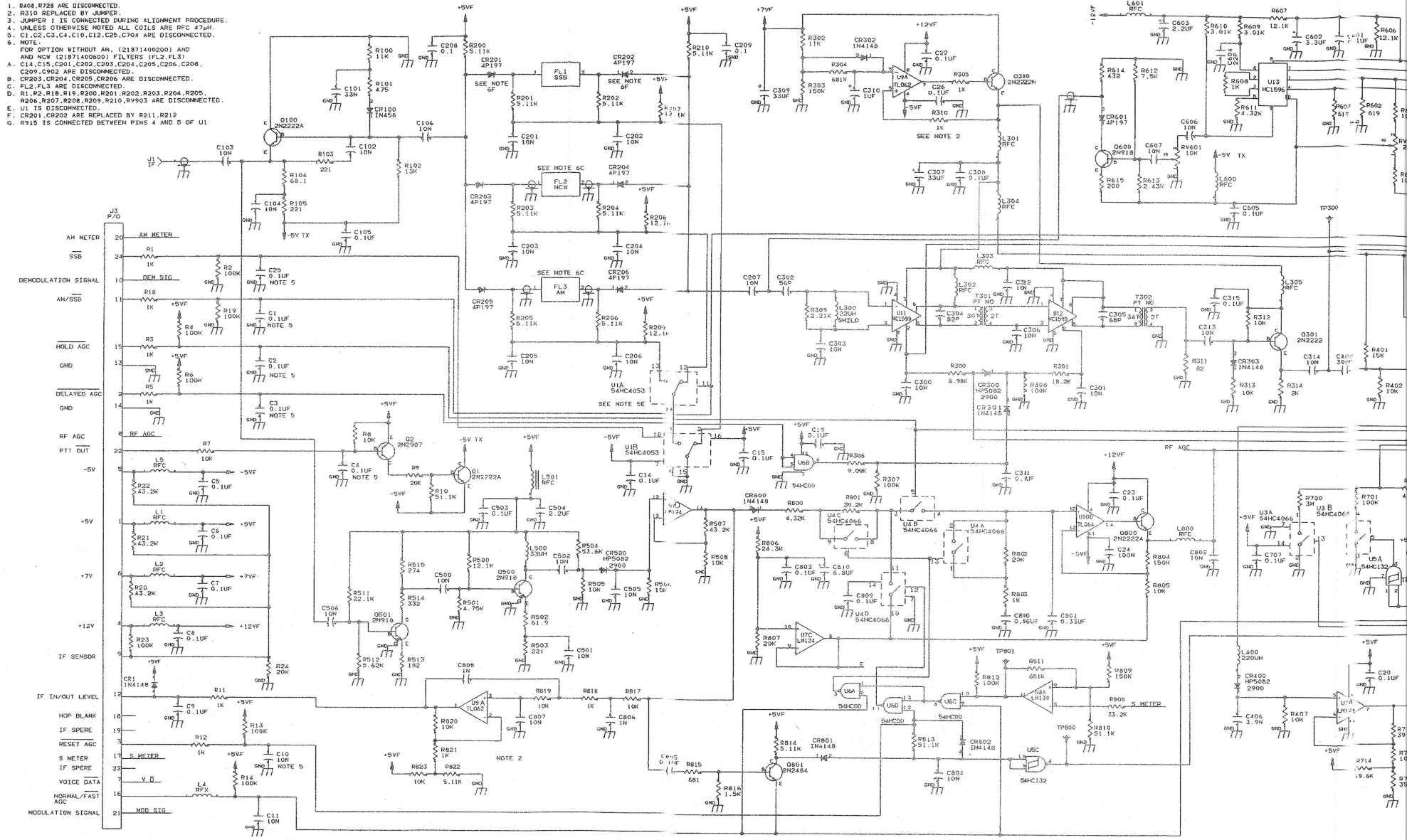
The mixer is powered by the +12VF voltage (filtered by L601 and C603), and by the -5V IF TX voltage (filtered by L600 and C605). The -5V IF TX voltage is present only during transmission.

The 5.25MHz carrier signal arriving from module SYNT is coupled through C600 and R604 to the carrier input (pin 7) of U13. Bias to the carrier inputs is provided by means of resistors R605 and R606.
The modulated signal, arriving from module AUDIO, is applied to the signal input (pin 1). The network comprising R600, RV600 and R601 is used to apply a small offset voltage for obtaining maximum carrier suppression at the output of U13 (pin 9). This is done during SSB operation. When operating in the AM mode, a carrier must be added to the output signal. Therefore, a high level is applied from the AM/SSB* line via CR600 and R616, causing the modulator to be unbalanced, thereby a carrier is added to its output signal.
Modulator gain is determined by the ratio of the load resistor R610 and the gain-setting resistor R608. The double-sideband signal appears across load resistor R610 and is coupled through capacitor C606 to potentiometer RV601.

(2) Buffer, Q600. The signal appearing at the wiper of the potentiometer RV601 is coupled via capacitor C607, to the base of Q600. Q600 bias is applied via resistor R613 and R612. The value of the collector load resistor R614 is selected to match the input impedance of the three IF filters FL1, FL2 and FL3. PIN diode CR601 is reverse-biased in the transmit mode, to prevent the 5.25MHz RF signals to leak to the receive path. The output signal of Q600 is applied to the three IF filters, via capacitor C207.

NOTES:

1. R408,R728 ARE DISCONNECTED.
2. R310 REPLACED BY JUMPER.
3. JUMPER 1 IS CONNECTED DURING ALIGNMENT PROCEDURE.
4. UNLESS OTHERWISE NOTED ALL COILS ARE RFC 47μH.
5. C1,C2,C3,C4,C10,C12,C25,C704 ARE DISCONNECTED.
6. NOTE:
   FOR OPTION WITHOUT AM, (21871406200) AND
   AND NCW (21871406600) FILTERS (FL2,FL3)
A. C14,C15,C201,C202,C203,C204,C205,C206,C208,
   C209,C902 ARE DISCONNECTED.
B. CR203,CR204,CR205,CR206 ARE DISCONNECTED.
C. FL2,FL3 ARE DISCONNECTED.
D. R1,R2,R18,R19,R200,R201,R202,R203,R204,R205,
   R206,R207,R208,R209,R210,RV903 ARE DISCONNECTED.
E. U1 IS DISCONNECTED.
F. CR201,CR202 ARE REPLACED BY R211,R212
G. R915 IS CONNECTED BETWEEN PINS 4 AND 5 OF U1



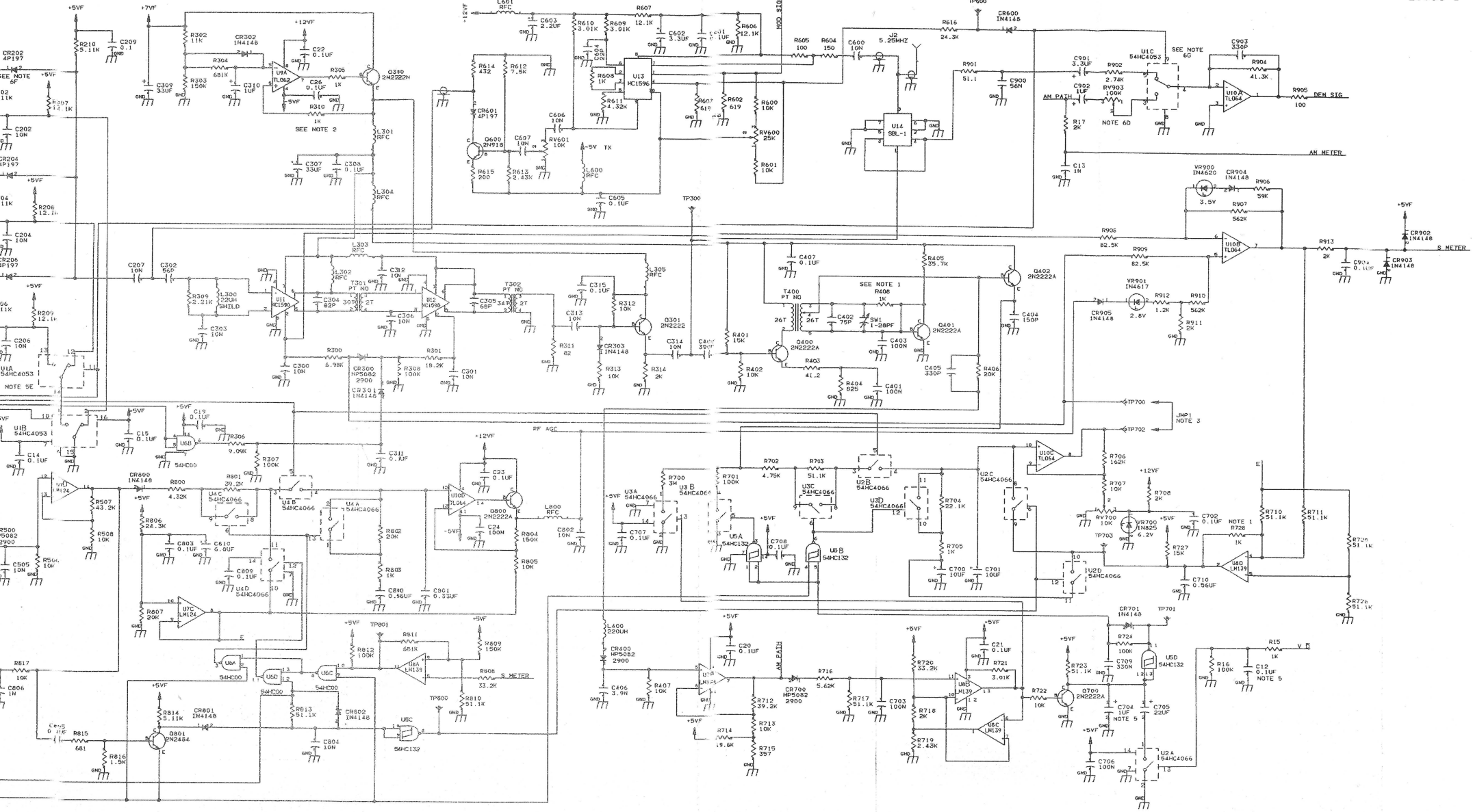


Figure 2-18. Module IF, Schematic Circuit Diagram

(3) Crystal filters and associated control switches. Three crystal filters FL1, FL2 and FL3 are inserted into the signal path by PIN diode switches. The switches are controlled by the SSB* and AM/SSB* lines applied to the control inputs of analog switches U1A and U1B.
In the down graded version of the module, FL1 and FL2 are disconnected (see note No. 6 on figure 2-18).

(a) The SSB filter, FL1, passes the upper sideband of the 5.25MHz IF signal (+350 to +3300Hz above the IF frequency). This filter is inserted into the signal path when the AM/SSB* line, connected to the control input of U1B (pin 10) falls to a low level. As a result, DC current flows from the +5VF line through R210, CR202, R202 and through R200, CR201 and R201 into pin 2 of U1B and to ground.
The remaining PIN diodes are reverse-biased, thereby blocking signal transfer to the other filters. Capacitors C201 and C202 shunt the RF voltages, appearing across R201 and R202, to ground.

(b) The NCW filter FL2 has a passband of 250Hz, centered on a frequency of 5.25MHz +1kHz. The filter is inserted into the signal path when the AM/SSB* line falls to low level and the SSB* line rises to a high level. As a result, DC current flows from the +5VF line through R210, CR204, R204 and through R200, CR203, R203 into pin 12 of U1A, and via U1B (pins 1,15) to ground.

(c) The AM filter FL3 has a passband of $\pm$3kHz. The filter is inserted into the signal path when the AM/SSB* and SSB* lines rise to a high level. As a result, DC current flows from the +5VF line through R210, CR206, R206 and through R200, CR205, R205 into pin 13 of U1A and via U1B (pins 1, 15) to ground.

(4) Matching circuit, Q100. The filtered IF signal from the selected crystal filter is applied to the base of Q100, via capacitor C106. During transmission, Q100 receives bias from the -5V IF TX line, via

R100, R101, CR100 and R102. The value of the emitter resistor R104 is selected to match the input impedance of module RF transmit path.
The output signal of Q100 is applied to module RF, via C103 and coaxial connector J1.

c. Receive Path Circuit Analysis (fig. 2-18 and 2-19). When operating in the receive mode, the PTT OUT* line rises to a high level. Transistors Q2 and Q1 are cut-off and the -5V IF TX supply voltage is disconnected from the transmit path circuits.

(1) Matching circuit. The received 5.25MHz IF signal arriving from module RF is coupled through C103 to the matching circuit. In the receive mode, the -5V IF TX line is disconnected, therefore transistor Q100 and diode CR100 are cut-off. Capacitors C102, C104 and C105 are practically short-circuits at RF frequencies, so the matching circuit comprises now resistor R104.

(2) Crystal filter and associated control circuit. The received signal 5.25MHz, attenuated by R103 is coupled by C106 to the three crystal filters FL1, FL2 and FL3, which provide the required selectivity for the receive path. The filters are inserted into the receive path according to the same AM/SSB* and SSB* commands used in the transmit path (para. b.(3) above).
In the down graded version of the module, FL1 and FL2 are disconnected (see note 6 on figure 2-18).

(3) IF amplifier.

(a) The filtered IF signal is coupled through C207 and C302 to pin 1 of U11. U11 is a differential input, differential output RF amplifier with AGC capability. C303 decouples the second input of U11 (pin 3). L300 and R309 provide a bias path to pin 3. U11 gain is controlled by the AGC voltage applied from U10C-8 (see para. (7) below) to pin 2 of U11, via resistor R300. The output voltages appearing at pins 5 and 6 of U11 are coupled by transformer T301 to U12, which is identical to U11. U12 gain is controlled by the IF AGC

voltage applied from U10C-8 to pin 2 of U12, through diode CR300 and resistor R301. The output load of U12 is the tuned-primary transformer T302, adjusted together with C305 to a resonance frequency of 5.25MHz.

(b) There is an option to limit the maximum gain of the amplifier. This option can be performed by applying a low level at the DELAYED AGC* line. The low level is inverted by U6B. CR301 is forward-biased and CR300 is reverse-biased, thereby blocking the AGC voltage provided to pin 2 of U12.

(c) The +7VF supply voltage for the IF amplifier is filtered by an active filter, built around U9A and Q300.

(d) The IF voltage appearing at the secondary of T302 is coupled through C313 to a buffer stage built around Q301. Bias for Q301 is supplied via resistor R312 and R313. CR303 is a temperature-compensation diode.

(4) SSB demodulator. The SSB demodulator is built around the mixer U14, which operates as a product detector. The IF signal appearing across the emitter resistor R314 is coupled via C314 to the signal input (pin 1) of U14, and the 5.25MHz signal is connected to its carrier input (pin 8). The audio output voltage appearing at pin 4 of U14 is filtered by R901 and C900, and is then applied via C901 and R902 to pin 5 of the AM/SSB selector U1C.

(5) AM demodulation circuits. Figure 2-28 shows the simplified diagram of the AM demodulation circuits. The IF voltage appearing across the emitter resistor of Q301 is coupled through C400 to a buffer stage built around Q400.

The output voltage of Q400 is coupled through transformer T400 to the envelope detector comprising L400, CR400, C406 and R407, via resistor R406 and capacitor C405. The secondary winding of T400 is tuned to 5.25MHz by CV400.

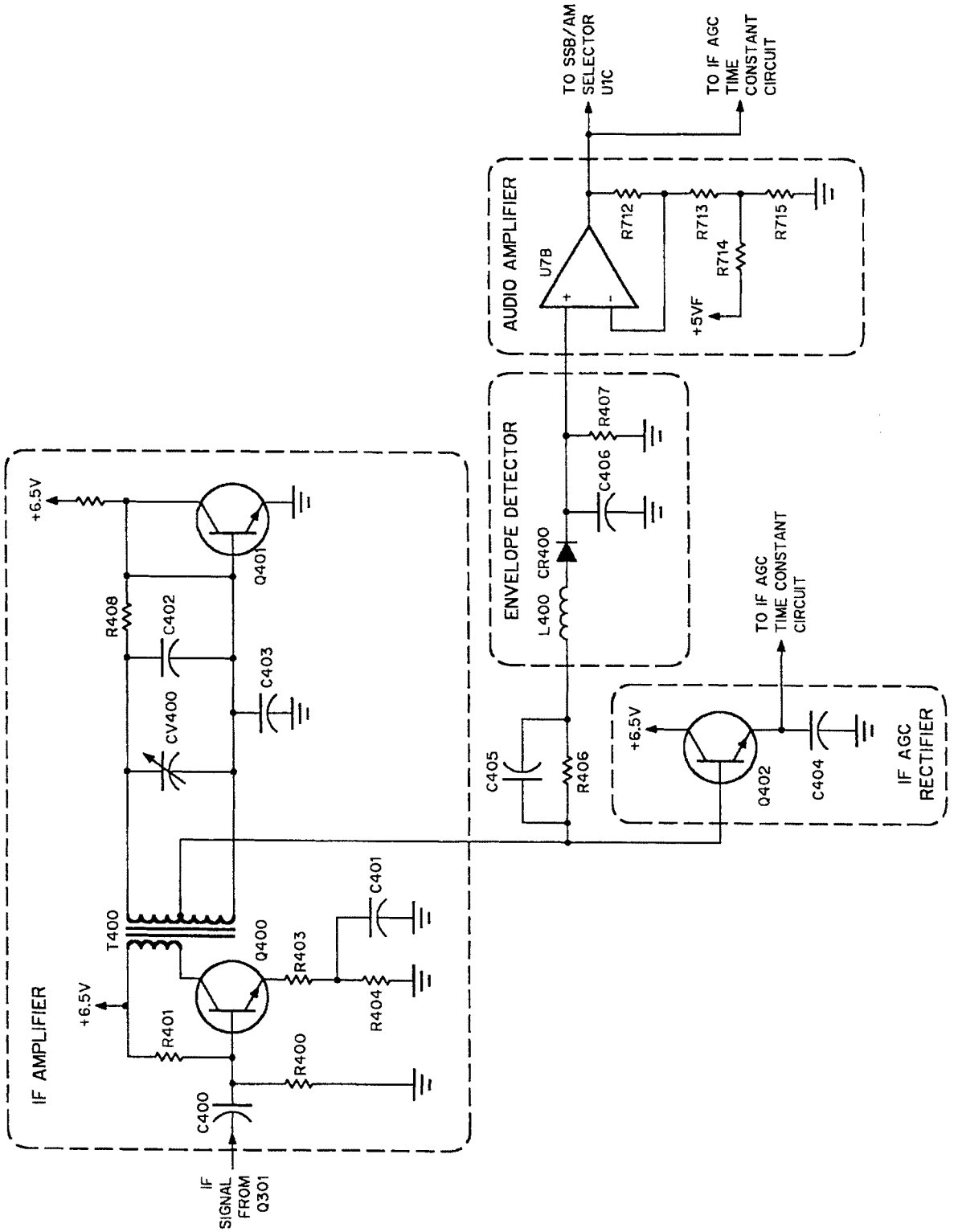


Figure 2-19. AM Demodulation Circuits, Simplified Diagram

To improve detection linearity, the envelope detector receives a small forward bias, developed from the voltage drop across the emitter base junction of Q401.

The output signal of the envelope detector is amplified by the audio amplifier built around U7B and applied to pin 3 of the AM/SSB selector U1C, via C902 and R903.

(6) AM/SSB selector. The AM/SSB selector U1C is controlled by the AM/SSB* line. A high level on this line selects the AM signal, connected to pin 3 of U1C, and a low level selects the SSB signal connected to pin 5. The output signal of U1C (pin 4) is amplified by U10A and sent to module AUDIO, via the DEMODULATION SIGNAL line.
The level of the AM signal is determined by the ratio of R904 and selected resistor R903, and the level of the SSB signal by the ratio of R904 to R902.

In the downgraded version of the module, U1 is disconnected.

(7) IF AGC and S-METER voltage generation (fig. 2-18 and 2-20 thru 2-22). Figure 2-20 shows the simplified diagram of the IF AGC time constant circuits and the S-METER amplifier.

(a) The output signal of the IF amplifier (para. (3) above) is rectified by transistor Q402. The peak-rectified signal appearing at the emitter of Q402 is applied to the time constant network, consisting of capacitors C700 and C701 and resistors R700 thru R705. The AGC time constant is determined by means of switches according to the operating mode (see para. (c) thru (g) below). The DC voltage appearing at the output of the time constant circuit is amplified by the non-inverting amplifier U10C. The gain of U10C is determined by the ratio of R706 to R707 and RV700. The output voltage of U10C passes through R300 to the gain control input of U11 and through CR300 and R301 to the gain control input of U12 (see (3) above).

(b) S-METER amplifier (fig. 2-29). The S-METER amplifier, built around U10B, combines the IF AGC and RF AGC signals and generates a DC voltage proportional to the received signal level. The IF AGC signal is taken at the input of U11. The RF AGC voltage provided by the RF AGC circuit is applied to the non-inverting input of U10B, via voltage divider R910, R911. U10B combines the AGC signals and amplifies them according to the ratio of R907 to R908. VR900, CR904 and R906 are used to decrease amplifier gain when low-level RF signals are received. The output signal of U10B is filtered by R913 and C904 and sent to the MCU module. CR902 and CR903 are protection diodes.

(c) Attack time constant, normal operation (fig. 2-29 and 2-30). During normal operation, switches U2C, U2D, U3C and U3D are open and switch U2B is closed (the HOLD AGC* line is at a high level). The equivalent time constant circuit for this case is shown in figure 2-30.

When the received signal strength increases, capacitors C701 and C700 charge. The voltage developing across C700 and C701 is amplified by U10C, and sent to the IF amplifiers U11 and U12 to reduce their gain.

(d) Release time constant for slow changes in the received signal. The equivalent time constant circuit for this case is shown in fig. 2-31.

When the received signal decreases slowly, capacitors C701 and C700 discharge slowly via resistor R700 and the AGC voltage sent to the IF amplifiers U11 and U12 increases their gain.

(e) Release time constant for fast changes in the received signal. When the received signal changes abruptly, such as during short pauses occurring between words, it is necessary to increase the release time constant (to approximately 1 sec

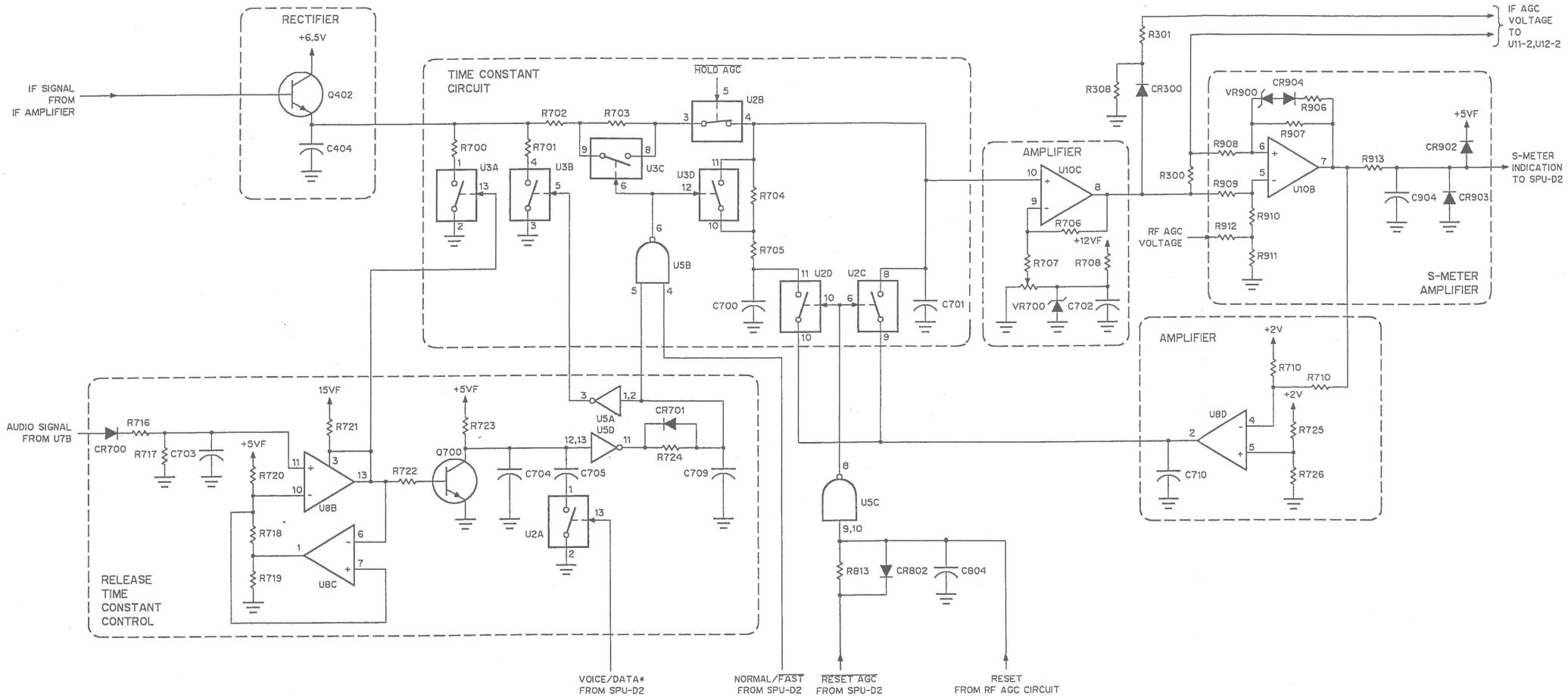


Figure 2-20. IF AGC Time Constant Circuits, Simplified Diagram

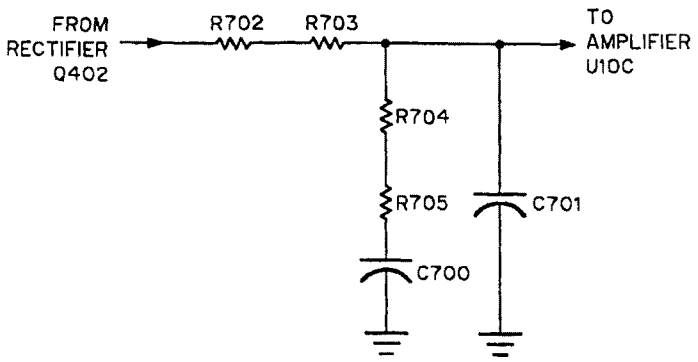


Figure 2-21. Time Constant Circuit During Attack Time, Equivalent Circuit

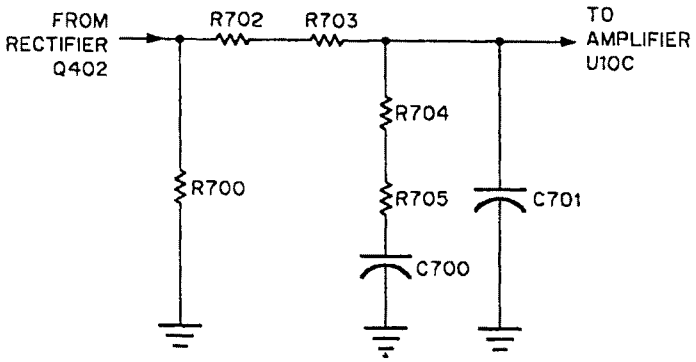


Figure 2-22. Equivalent Time Constant Circuit for Slow Decrease in Received Signal

for voice modulation, and 0.1 sec for data modulation) in order to maintain a constant gain.

The control circuit comprising CR700, U8B, U8C, Q700 and U2A performs envelope detection of the audio signal and controls the release time constant.

The audio signal provided by the audio amplifier U7B is rectified by CR700, R716, R717 and C703 and applied to the non-inverting input (pin 11) of the comparator U8B.

The inverting input (pin 10) of U8B receives a reference voltage, determined by the ratio of R720 to R718 and R719. The amplifier U8C provides hysteresis. During normal reception, the rectified voltage exceeds the threshold and U8B output is high.

When the received signal decreases abruptly the DC voltage applied to pin 11 of U8B falls below the reference voltage at pin 10, therefore a low level appears at the output of U8B. This low level is applied to the control input (pin 13) of switch U3A. The switch is opened and C700, C701 discharging via R700 stops immediately.

Simultaneously, the low level is applied to the base of Q700. Q700 cuts off and capacitor C704 starts charging via resistor R723. When voice modulation is used , the VOICE/DATA* line is at a high level, and capacitor C705 is connected in parallel to C704, by means of switch U2A, to increase the hold time to 1 sec. If the output of U8B does not return to a high level, C704, C705 eventually charge and the voltage across C704, C705 exceeds the threshold of U5D. U5D then generates a low level. Capacitor C709 discharges rapidly via diode CR701 and a low level is applied to gates U5A and U5B. As a result, switches U3B, U3C and U3D close, and capacitors C701 and C700 discharge via R701. When after the hold time, a signal is received again, the output of the comparator U8B rises to a high level, resistor R700 is connected and R701 disconnected.

(f) When using frequency hopping, the AGC voltage is reset before starting reception on the new frequency, to obtain maximum sensitivity. The reset action is controlled by the RESET AGC* pulses, applied while the actual frequency changes (hops) take place. The pulses are applied to the control inputs of switches U2C and U2D (pins 6 and 12, respectively).

The switches close and the output of U8D is now connected to capacitors C701 and C700. As a result, the output of the S-METER amplifier U10B is connected to the input of amplifier U10C, via amplifier U8D, and a loop is formed. Capacitors C701 and C700 then discharge to the output voltage of U8D. At the end of this rapid discharge process, the output voltage of the S-METER amplifier falls to a value of 0 volt, which is equivalent to the sensitivity threshold of a received RF signal (-110dBm).

To make the attack time shorter during hopping, the NORMAL/FAST* line falls to a low level, which closes switches U3C and U3D. Resistors R703 and R704 are short-circuited and the attack time is made shorter.

(g) When the received signal is very strong (above -50dBm), a reset command is provided from the RF AGC circuit, and the IF AGC circuit is reset as described in (f) above.

(8) RF AGC generation (fig. 2-23). Figure 2-23 shows the simplified diagram of the RF AGC time constant circuits.

(a) The IF signal from module RF is amplified by a two-stage transistor amplifier, consisting of Q500 and Q501 and it is then applied to the detector CR500, C505 and R506. The detector provides significant signal only under strong signal conditions. The peak detected signal is amplified by U7D and applied to the time constant circuit consisting of diode CR800, resistors R800 thru R803 and capacitors C800 and C801. The time constant of the RF AGC circuit is determined by means of switches, according to the operation mode (see para. (b) thru (d) below). The DC voltage appearing across capacitor C801 is amplified by the non-inverting amplifier U10D. The inverting input (pin 13) of U10D receives a reference voltage of approximately 2 Volt from the buffer U7C, via resistor R805. The output signal of U10D is driven by Q800, via the RF choke L800 to the AGC attenuator in the RF module and to the S-METER amplifier (see para. (7)(b) above).

(b) Time constant during normal operation. During normal operation, (NORMAL/FAST* line at high level), the switches U4A, U4C and U4D are controlled by the S-METER signal, applied to the comparator U8A (pin 8). As long as the S-METER voltage applied to pin 8 of comparator U8A is above the reference voltage at its non-inverting input (pin 9), switches U4A, U4C and U4D are open-circuited. Switch U4B is closed, because the HOLD AGC* line is at a fixed high level. When the received signal increases, beyond the level at which the RF AGC starts operating, capacitor C801 charges via R800 and R801, and capacitor C800 charges via R800 thru R803. As a result, the RF AGC voltage sent to the AGC attenuator in the RF module increases and the attenuation of the received RF signal increases. When the reception of a message is finished, the S-METER voltage falls and comparator U8A generates a high level. As a result, switch U4D closes and C801 and C800 discharge rapidly to the output voltage of U7C (approximately 2 volt).

(c) During frequency hopping, while actual frequency changes take place, RESET AGC* pulses (low level) are applied to pin 9 of gate U6D. As a result, switch U4D closes and capacitors C800 and C801 discharge rapidly to the output voltage of U7C, to obtain maximum sensitivity.
To make the attack time shorter during hopping, the NORMAL/FAST* line assumes a low level. Therefore, gate U6A generates a high level, and switches U4A and U4C close. R802 and R801 are short-circuited and the attack time is shorter.

(d) The RF AGC and IF AGC circuits are also reset when a very strong RF signal (above -40dBm), usually caused by pulsed interference, is received. The output signal of amplifier U7D is applied via the differentiator C805, R815, R816 to the base of transistor Q801. When the FAST mode is used (low level on the NORMAL/FAST* line), transistor Q801 is biased.

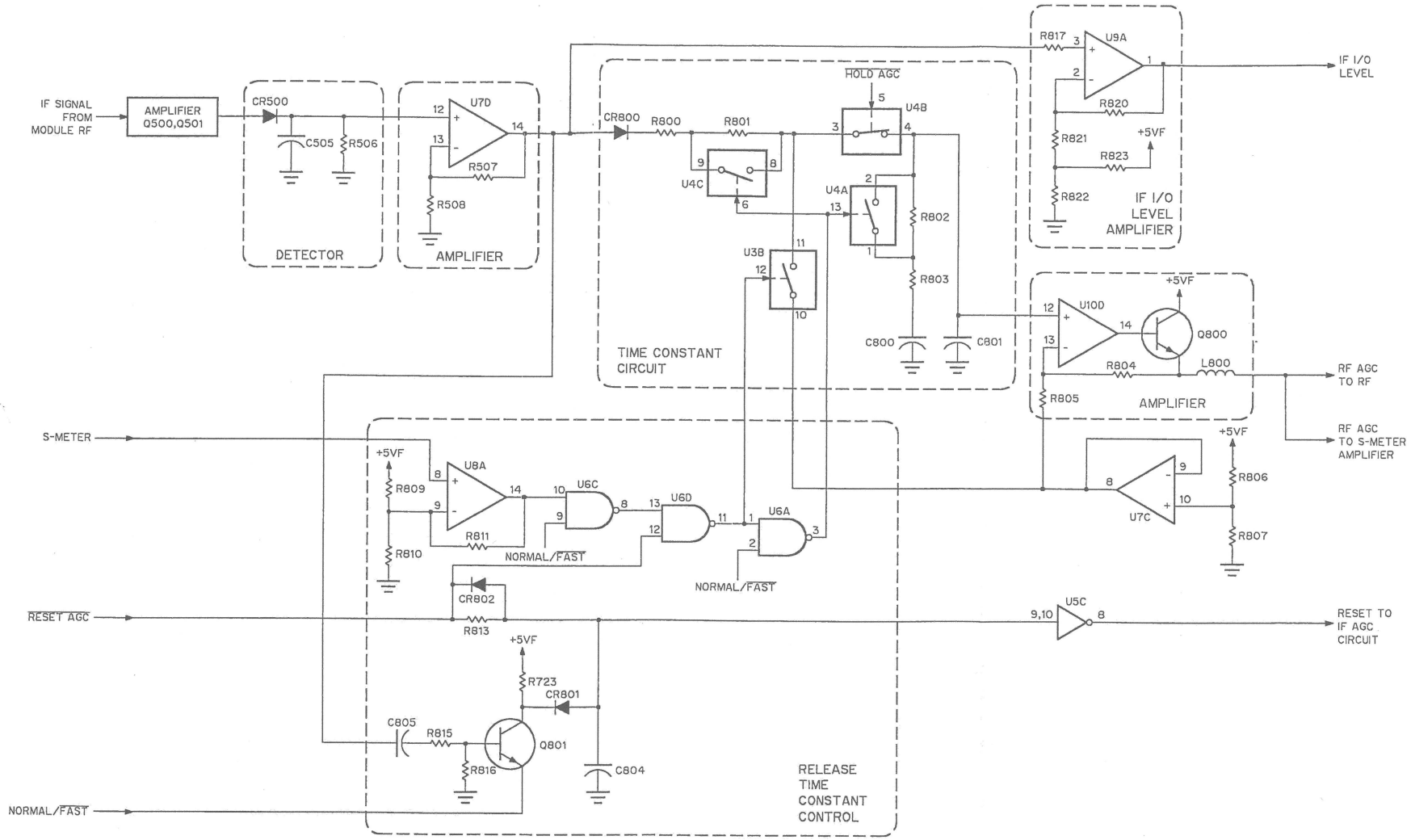


Figure 2-23. RF AGC, Time Constant Circuits, Simplified Diagram

When the voltage applied to the base of Q801 rises suddenly, Q801 saturates, pin 12 of U6D receives a low level and its output rises to a high level. As a result, switch U4D closes, and the AGC circuit is reset.

(e) IF I/O level indication. The output signal of the RF AGC detector, appearing at pin 14 of U7D, is amplified by the IF I/O LEVEL amplifier U9A and sent to the microprocessor in the MCU module. This indication uses for monitoring the IF transmit level, or the received RF signal.

d. IF SENSOR Indication. The resistor network composed of R22, R21, R20, R23, R24, averages the supply voltages of -5V, +5V, +7V and +12V, respectively, across resistor R24. When all the voltages appear at the module inputs, a voltage of approximately +2.2V appears across resistor R24. This voltage is sent to the microprocessor in the MCU module. This indication is used for monitoring the supply voltages to the module.

2-10. Module RF

(fig. 2-24 thru 2-26)

a. Block Diagram Analysis (fig. 2-24). Figure 2-24 shows the block diagram of the RF module.

(1) Transmit path.

(a) Activation of transmit path. The transmit path is activated by turning on its supply voltage switches, under control of the PTT* line. Concomitantly, the supply voltages of the receive path are disconnected by the receive patn supply switch, thereby disabling the receive path.

(b) Signal path. The transmit path receives the modulated 5.25MHz signal generated by the IF module via the connector J3. The input signal passes through the TX IF amplifier.

The output signal of the TX IF amplifier is applied to the first transmit mixer. In the mixer, the transmit signal is mixed with the F2 signal to 109.35MHz (para. c.(1) below). The frequency of the F2 signal is 104.1MHz for LSB operation, and 114.6MHz for USB and AM operation.

The 109.35MHz output signal of the mixer passes through the TX/RX switch No.1 to the 109.35MHz crystal filter. The filtered signal appearing at the filter output passes through TX/RX switch No.2 to the second transmit mixer. In this mixer, the 109.35MHz signal is mixed with the F1 signal (110.85 to 139.3499 MHz), to convert it to the final RF frequency.

The output signal of the second transmit mixer is filtered by a low-pass filter, which allows only the difference frequency - in the 1.5 to 29.9999MHz range - to pass. The filtered signal is amplified and applied to the PRC/VRC selector.

The PRC/VRC selector is controlled by the TX/RX control circuit:

1. In the PRC-2200, the selector routes the signal to the AM module via the AM DRIVE line (connector J5).

2. When the RT-2001 is part of a vehicular radio set, the selector routes the signal to a 100mW amplifier. The amplified RF transmit signal is then connected by the 100mW TX switch to a 1.5 to 30MHz band-pass filter. The filtered signal is then sent to module AM (para. 2-12) via connector J4.

(c) Blanking the RF transmit path. Each mixer in the transmit path is an active mixer, which receives DC power from the 11.5V and +5V-TX line. The DC supply can be turned off by the TX supply switch, under control of the RFS* line.

This allows interrupting the RF output signal during frequency changes, component switching in the matching network, etc.

(2) Receive path.

(a) Activation of receive path. The receive path is activated by turning on its supply voltage switches, under control of the PTT* line. At the same time, the supply voltages of the transmit path are disconnected by the transmit path supply switch, thereby disabling the transmit path.

(b) Signal path. The received RF signal arrives from the AM module, and is applied to a 1.5 to 30MHz band-pass filter. An input protection circuit limits the maximum amplitude of the input signal, to protect the components at the input of the receive path.

The output signal of the 1.5 to 30MHz band-pass filter is applied to another band-pass filter. There are seven sub-octave band-pass filters, and the filter corresponding to the operating frequency is inserted in the signal path by means of PIN diode switches. The PIN diode switches are controlled by a filter control circuit. The filter control circuit receives the FIL SEL commands from the microprocessor in module MCU and converts them to drive signals for the PIN diode switches.

The filtered signal is then applied to the RF AGC attenuator, which is controlled by the RF AGC voltage provided by module IF. The RF AGC attenuator starts attenuating the input signal level only when the received signal strength is too high and could overload the IF amplifiers. The output signal of the RF AGC attenuator is applied to the first receive mixer. In the first receive mixer, the received signal is up-converted to a frequency of 109.35MHz by mixing with the F1 signal. The mixer output signal passes through the TX/RX switch No.2 to the 109.35MHz crystal filter.

The filtered signal passes through the TX/RX switch No.1 to the second receive mixer, where it is mixed with the F2 signal. The resulting 5.25MHz upper-sideband IF signal is amplified by the RX IF amplifier. The amplified signal is sent to the IF module via connector J3.

(3) Paths of F1 and F2 signals.

(a) The F2 signal is received from module SYNT and amplified by the F2 amplifier located in the RF module. The amplified F2 signal is routed to the first transmit mixer or to the second receive mixer, according to the operating mode, by means of a PIN diode switch.

(b) The F1 signal is received from module SYNT and amplified by the F1 amplifier located in the RF module. The amplified F1 signal is routed to the second transmit mixer or to the first receive mixer, according to the operating mode, by means of a PIN diode switch.

(c) The gain of the F1 and F2 amplifiers is determined according to the operating mode: during transmission, the gain is higher than in reception.

(4) Test sub-system. The test signal generator is activated during self-test. The test signal generator receives a 700kHz reference signal from the SYNT module, and generates a comb signal having a known amplitude. The test signal is applied to the input of the receive path. The microprocessor in the MCU module measures the received signal strength, to check that the receive path circuits are operational.

b. Transmit Path Circuit Analysis (fig. 2-25 and 2-26).

(1) TX and RX path supply switches. The TX path supply switch, built around transistor Q12 and gate U4F, is controlled by means of the PTT* and RFS* lines. The RX path supply switch, built round transistor Q11 and gate U4E, is controlled only by the PTT* line.

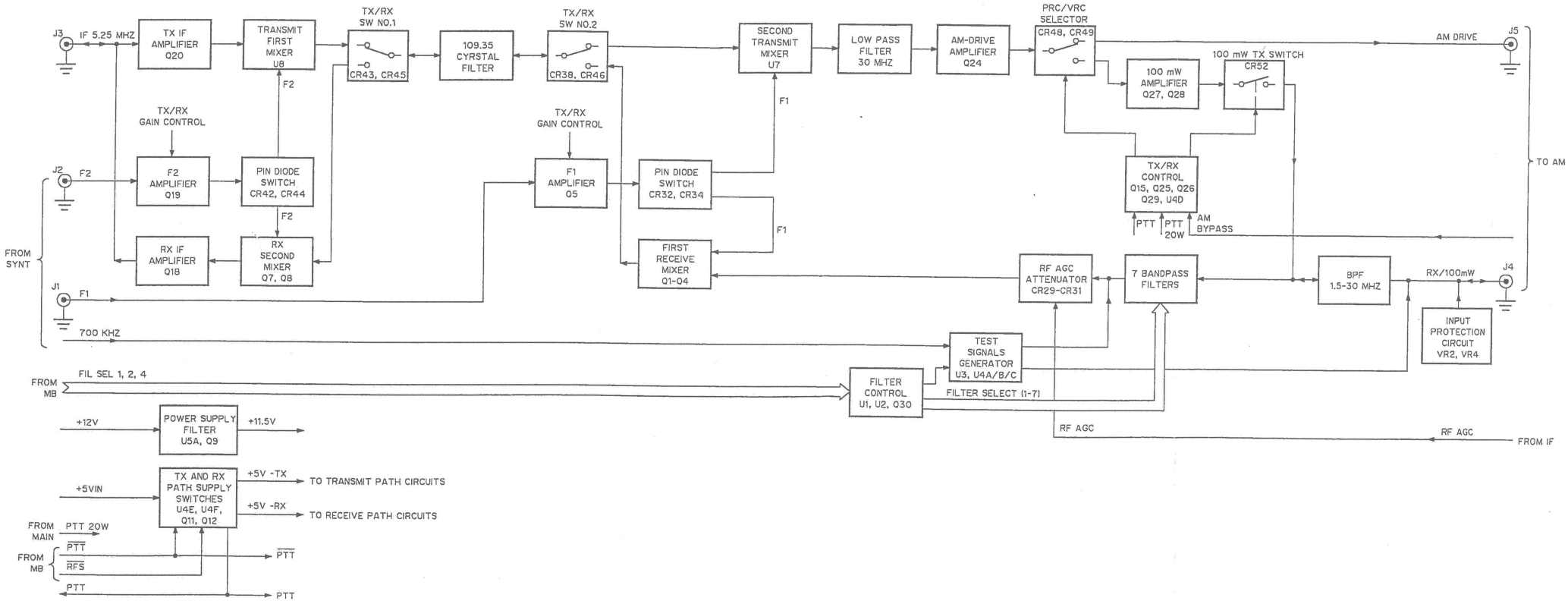
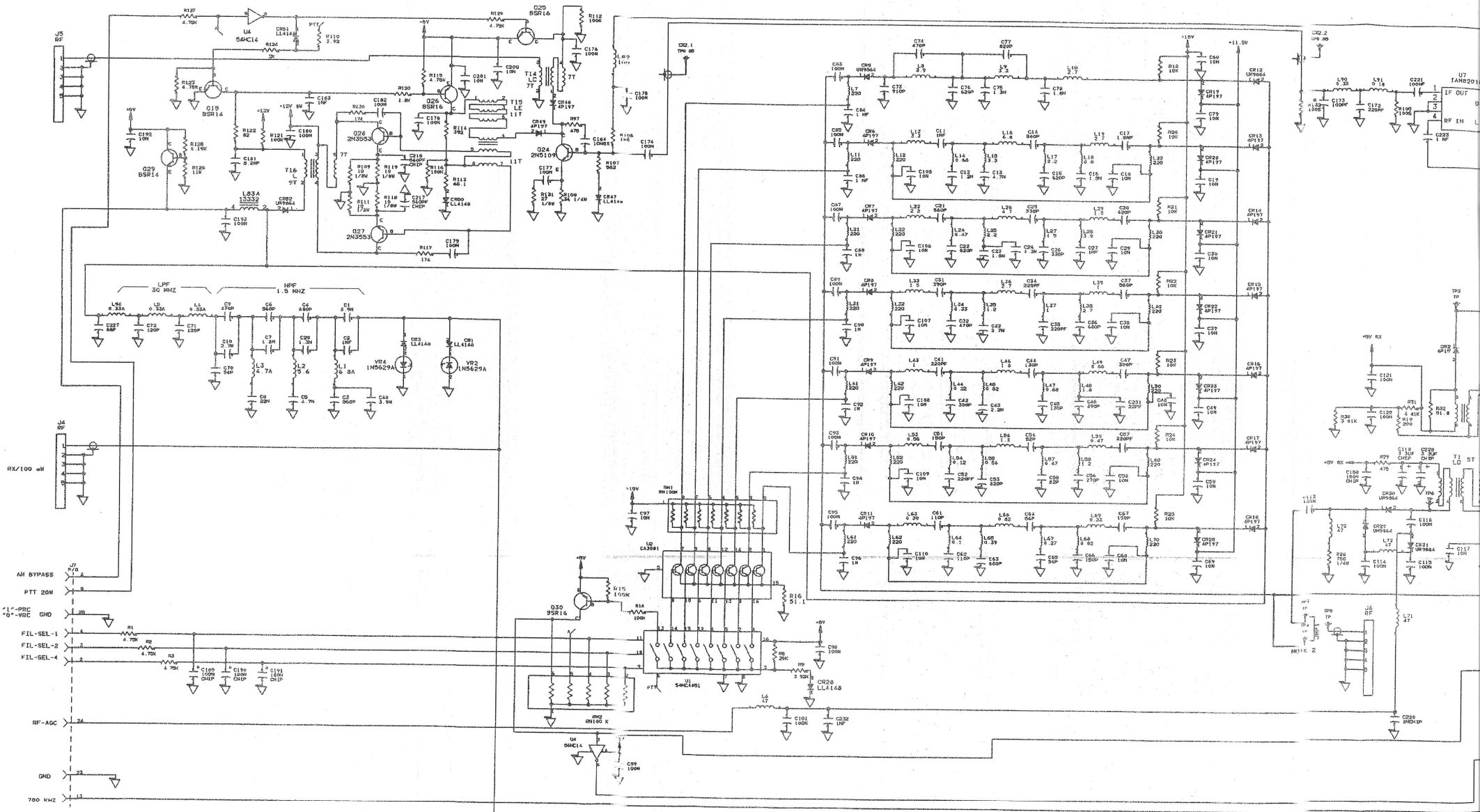


Figure 2-24. Module RF, Block Diagram


J5 RF
J4 RF
J6 RF
LPF 30 MHZ
HPF 1.5 MHZ
RX/100 mW
AM BYPASS
PTT 20W
"1"-PRC
"0"-VRC
GND
FIL-SEL-1
FIL-SEL-2
FIL-SEL-4
RF-AGC
GND
700 KHZ
+5V
+8V
+10V
+12V
+15V
+11.5V
PTT
U4 54HC14
U5 54HC14
U1 54HC4051
Q18 BSR14
Q29 BSR14
Q26 2N3553
Q27 2N3553
Q25 BSR16
Q30 BSR16
Q24 2N5109
T14 LC 7T
T15 LE 11T
T16 L 9T 2
L83A 13332
CR82 LM9044
VR4 1N5629A
VR2 1N5629A
CR3 LL4148
CR1 LL4148
CR47 LL4148
CR48 4P197
CR49 4P197
CR28 LL4148
RN1 RN100K
RN2 RN100 K
U8 LA3081
U7 TAN8201
IF OUT
RF IN
ANT 2
ANT 1
ASV RX
+8V RX
Y1 LO 57

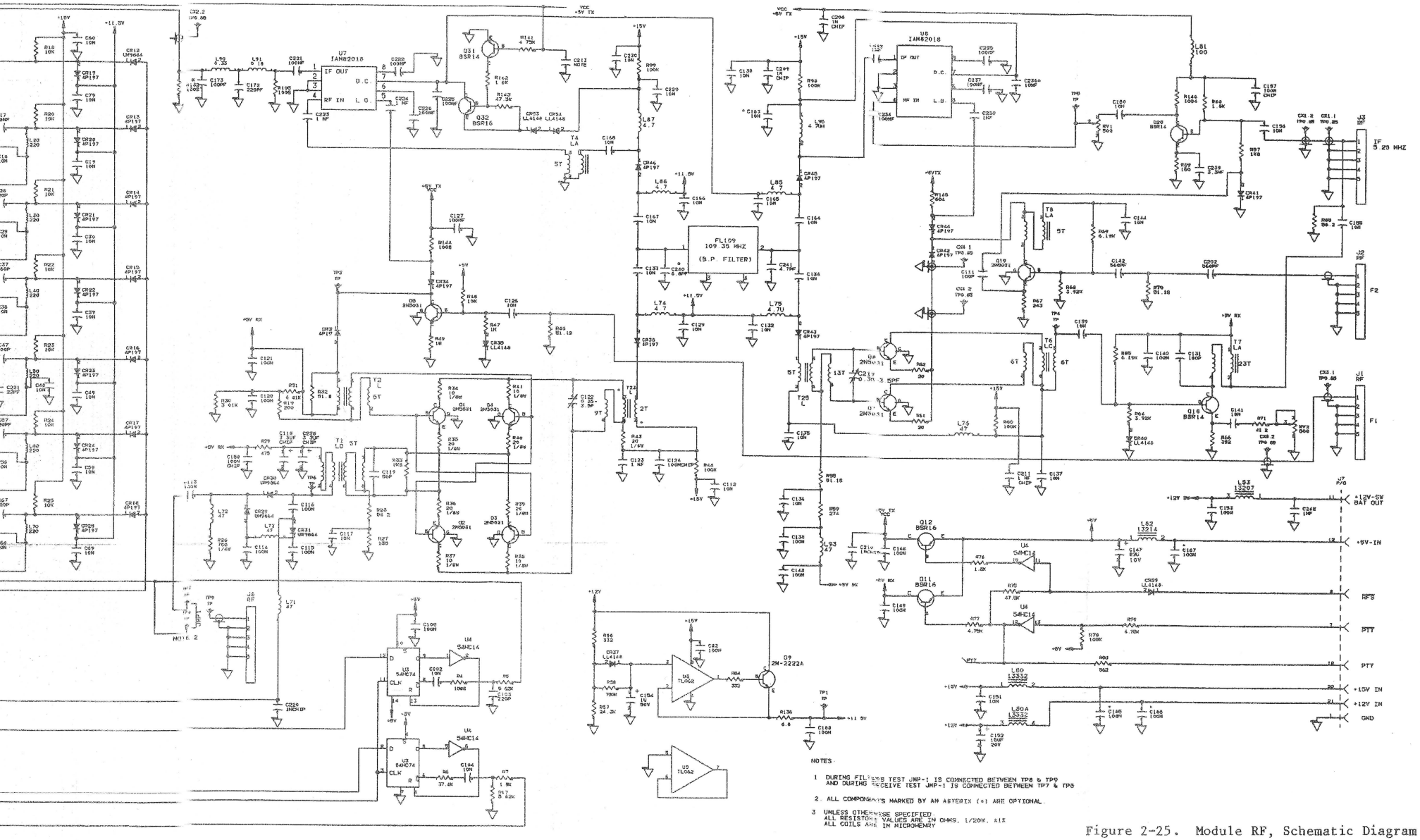


Figure 2-25. Module RF, Schematic Diagram

(a) During transmission, when the PTT is activated, the PTT* line falls to a low level. As a result U4F receives a high level, via U4E and R75, and its output falls to a low level. This low level activates transistor Q12. Therefore, the +5V-IN supply voltage passes through the filtering network L82, C147, C187 and through Q12 to the +5V-TX line, connected to the circuits of the transmit path, and the transmit path is activated. Concomitantly, when the PTT* line falls to a low level, transistor Q11 is reverse-biased and the supply voltage +5V-RX of the receive path circuits is disconnected, thereby disabling the receive path.

(b) When the PTT is not activated, the PTT* line rises to a high level and causes an opposite response - the +5V-IN supply voltage passes via Q11 to the receive path supply line +5V-RX, powering receive circuits, and the transmit path supply voltage is disconnected.

(c) The RFS* command is used to blank the RF transmit path whenever necessary (during frequency changes, component switching in matching network, etc.).
To blank the transmit path, the RFS* line falls to a low level. As a result, U4F generates a high level and Q12 is cut-off, thereby disabling the transmit path.

(2) TX IF amplifier. The TX IF amplifier is built around Q20. The 5.25MHz signal, arriving from module IF (para. 2-9) to the coaxial connector J3, is coupled through C156 to the base of Q20. The amplified signal passes through the coupling capacitor C150 to the first transmit mixer.

(3) First transmit mixer. The amplified IF signal is attenuated by potentiometer VR1 and is then applied to pin 4 of balanced mixer U8. Pin 5 (LO input) of U8 receives the F2 signal (104.1MHz for LSB operation, 114.6MHz for USB and AM operation) from the F2 amplifier (para. d.(1) below), via the forward-biased PIN diode CR44.

Diode CR42 is used to apply the F2 signal to the receive path mixer. The 109.35 MHz signal is amplified by an internal amplifier in U8.

(4) Crystal filter. The 109.35MHz output signal of the first transmit mixer passes through the forward-biased PIN diode CR45 to the 109.35MHz band-pass filter.

The filtered signal passes through PIN diode CR46 (also forward-biased during transmission) to the input of the second transmit mixer. PIN diode CR38 and CR43, used to insert the filter to receive path, are reverse-biased during transmission.

(5) Second transmit mixer, U7. This mixer is identical to the first transmit mixer, U8. The input signal is applied to pin 4 of U7 through a winding of transformer T4, that is used for impedance matching at a frequency of 109.35MHz.

The F1 variable synthesizer frequency (110.85 to 139.3499MHz), received from the collector of Q5, is applied via PIN diode CR34 (forward-biased by the +5V-TX voltage during transmission) and via C224 to pin 4 (LO input) of U7.

The mixer output signal is passed through a low pass filter comprising R105, L91, C172, L90 and C173. The filter passes the difference signal, which is at the required operating frequency in the 1.5 to 29.9999MHz band.
The DC operating voltage of U7 is controlled by Q31 and Q32. In the receive mode the operating voltage of U7 is blocked by Q32. In the transmit mode, the base voltage of Q31 is obtained from the +5V-TX supply voltage via resistor R141. Transistor Q31 saturates and turns on transistor Q32. As a result, the +9V voltage is connected by Q32 to pin 7 of U7.

(6) TX/RX CONTROL. The simplified diagram of the TX/RX control circuits (including the AM drive amplifier and the 100mW amplifier) is shown in fig. 2-26.

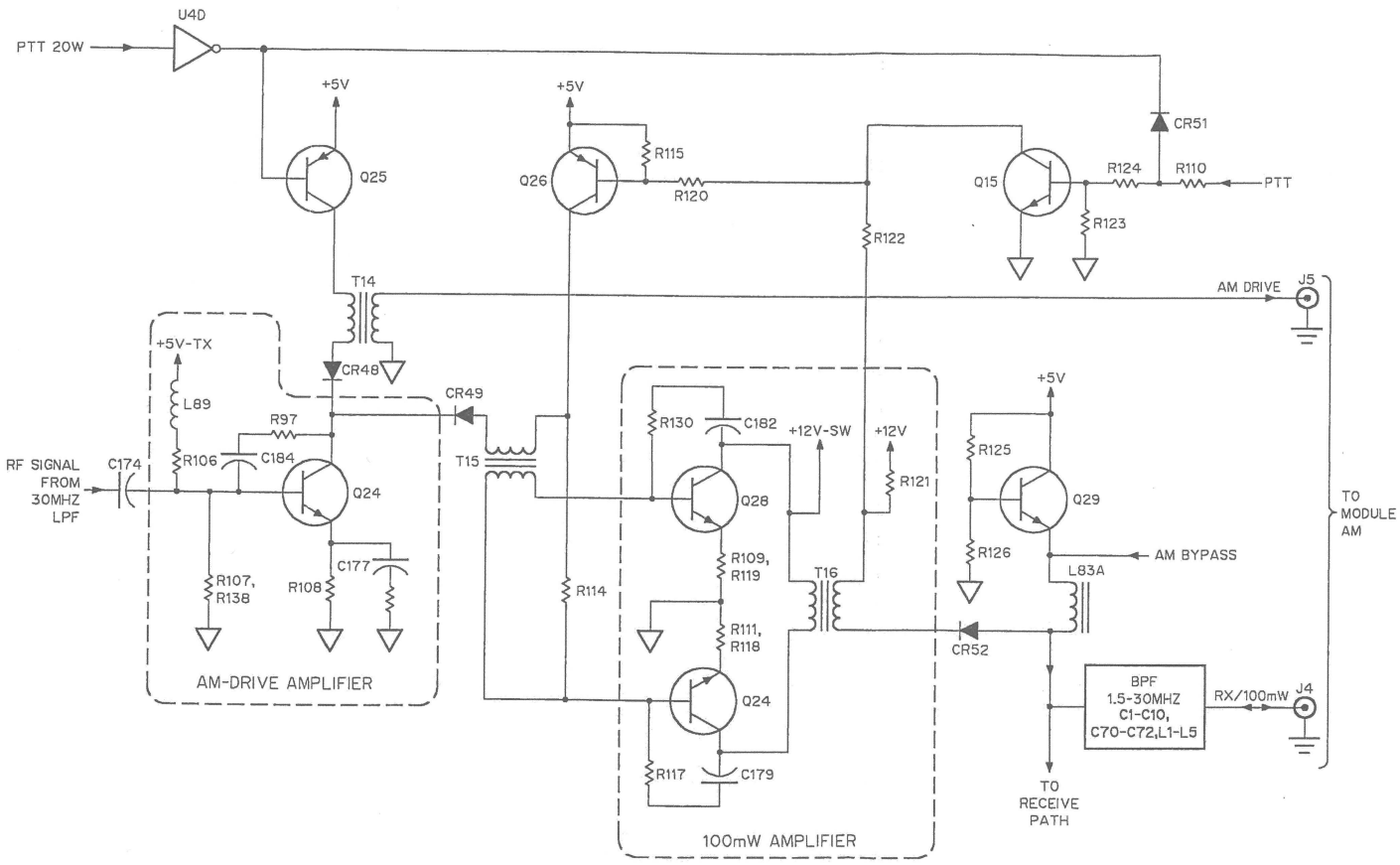


Figure 2-26. TX/RX Control, Simplified Diagram

The filtered output signal of the second transmit mixer, at the RF band of 1.5 to 29.9999MHz, is applied to the AM drive amplifier built around Q24.

The RF signal is coupled via capacitor C174 to the base of Q24. The amplified signal developing at the collector of Q24 is routed to the 100mW amplifier or directly to the AM module, according to the PRC/VRC command received via the PTT 20W line:

(a) When the RT-2001 is used in the PRC-2200, the PTT 20W line is at a high level. The high level is inverted by U4D to a low level, which causes transistor Q25 to conduct. As a result, diode CR48 is forward-biased and the RF signal appearing at the collector of Q24 is coupled by T14 and routed to module AM, via connector J5.

(b) When the RT-2001 is part of a vehicular radio set, the PTT 20W line is at a low level. U4D inverts this low level and causes diode CR51 to be reverse-biased. During transmission, the PTT line, from the TX and RX path supply switches (pin 12 of U4E), assumes a high level. This high level is applied to the base of transistor Q15, via resistors R110 and R124. Transistor Q15 is activated and activates transistor Q26. DC current flows through the primary of transformer T15 and through diode CR49 to transistor Q24. As a result, diode CR49 is forward-biased and the RF signal from the collector of Q24 passes via CR49 and is coupled through transformer T15 to the 100mW push-pull amplifier, built around Q27 and Q28. Simultaneously, when transistor Q15 is activated during transmission of the vehicular radio set, a DC loop is closed via diode CR52, the secondary of transformer T16 and transistor Q15. The DC voltage is supplied from the AM BYPASS line or from transistor Q29:

1. When the RT-2001 is used in the PRC-2200, the DC voltage is received from module AM, via the AM BYPASS line.

2. When the RT-2001 is a part of a vehicular radio set that does not contain the AM module, the DC voltage is supplied by means of transistor Q29.
The 100mW RF signal generated by the push-pull amplifier is coupled via T16 and forward-biased diode CR52 to the 1.5 to 30MHz band-pass filter. The filtered signal is then sent to module AM via connector J4.
During reception, when the PTT line is not active, diode CR52 does not conduct, thereby the output of then 100mW amplifier is disconnected.

c. Receive Path Circuit Analysis (fig. 2-25).

(1) Input protection circuit. The received RF signal arriving at the J4 coaxial connector from module AM is applied to the 1.5 to 30MHz band-pass filter. The band-pass filter and other components at the input of the receive path are protected by an input protection circuit. The input protection circuit comprises diodes CR1 and CR3 and Zener diodes VR2 and VR4, which conduct and limit the input signal whenever it exceeds their conduction threshold.

(2) Bandpass filters and associated control circuit. The output signal of the 1.5 to 30MHz band-pass, comprising capacitors C1 thru C10, C70, C71 and inductors L1 thru L5, is applied to the 7 sub-octave band-pass filters. The filter corresponding to the operating frequency is inserted into the signal path by means of PIN diodes connected to the input and output of each filter. The PIN diode switches are controlled by the filter control circuit built around demultiplexer U1 and the transistor network U2. The control circuit receives the binary FIL SEL commands from the microprocessor in module MCU and converts them to drive signals for the PIN diodes. For example, when operating in the band of 1.5 to 2.2MHz, the binary code 001 is applied to the control inputs of U1 (pins 9, 10, 11 respectively). Switch U1-14 is closed (the other seven switches of U1 are open) and the appropriate transistor (U2-7,8) is activated.

As a result, PIN diodes CR12 and CR5 are forward-biased and connect the 1.5 to 2.2MHz band-pass filter into the receive path.

Diodes CR19 thru CR25 are used to prevent leakage when the band-pass filter is disconnected. Therefore, when the 1.5 to 2.2MHz band-pass filter is inserted to the receive path, diode CR19 cuts-off and the other six diodes conduct.

Table 2-8 lists the selected band-pass filter according to the FIL SEL commands.

Table 2-8. 7 Bandpass Filters Control

FIL SEL Commands (U1 Inputs)			Closed Switch	Activated Transistor	Forward-biased PIN diodes	Selected Bandpass Filter
Pin 9	Pin 10	Pin 11				
0	0	0	U1-13	Q30	--	Used for test signal generation (see para. e. below)
0	0	1	U1-14	U2-7,8	CR5, CR12	1.5 to 2.2MHz
0	1	0	U1-15	U2-9,10	CR6, CR13	2.2 to 3.4MHz
0	1	1	U1-12	U2-4,6	CR7, CR14	3.4 to 5.2MHz
1	0	0	U1-1	U2-12,11	CR8, CR15	5.2 to 8MHz
1	0	1	U1-5	U2-14,13	CR9, CR16	8 to 12.3MHz
1	1	0	U1-2	U2-2,3	CR10, CR17	12.3 to 19MHz
1	1	1	U1-4	U2-1,16	CR11, CR18	19 to 30MHz

(3) RF AGC attenuator. The filtered RF signal is applied to the RF AGC attenuator comprising PIN diodes CR29, CR30 and CR31. These diodes receive the RF-AGC voltage supplied by the IF module. When the received signal strength is normal, CR31 and CR29 are cut-off, CR30 conducts, and the RF signal is not attenuated. When the received

signal strength exceeds a certain threshold, the RF AGC voltage starts increasing, so that diodes CR31 and CR29 are now forward-biased. The dynamic resistance of diode CR30 is determined by the current flowing through it as a result of the RF AGC voltage: when the RF AGC voltage increases, the resistance of CR30 decreases and the attenuation of the RF signal increases.

(4) First receive mixer. The RF signal at the AGC attenuator output is applied, through transformer T1 to the emitters of the four transistors Q1 to Q4. The transistors form an active, wide-dynamic range mixer with improved linearity and noise figure. The local oscillator signal is the F1 variable frequency, from the F1 amplifier, Q5. The F1 signal is connected to the bases of the four transistors, via transformer T2 and diode CR32 (forward-biased during reception). The collectors of the transistors are connected to the tuned transformer T23, whose primary is adjusted by C122 to resonate at the 109.35MHz frequency appearing at the output of this mixer.

(5) Crystal filter. The output of the first receive mixer is connected, via PIN diode CR38, to the 109.35MHz band-pass filter, which selects the difference frequency generated in the mixer. The filtered signal pass through PIN diode CR43 to the input of the second mixer.

(6) Second receive mixer. The second receive filter is built around transistor Q7 and Q8. The filtered 109.35MHz signal is applied to the bases of Q7 and Q8. The emitters of the two transistors receive the F2 signal from the F2 amplifier (Q19) via PIN diode CR42 (forward-biased during reception). The resulting 5.25MHz IF signal is applied to the RX IF amplifier.

(7) RX IF amplifier. The RX IF amplifier is built around transistor Q18. The gain of the amplifier can be adjusted by means of resistor R71. The amplified 5.25MHz IF signal developing at the collector of Q18 is coupled by transformer T7 and capacitor C155 and sent to the IF module via connector J3.

d. F1 and F2 amplifiers.

(1) F1 amplifier. This amplifier is built around Q5. The F1 signal (110.85 to 139.3499MHz), arriving from module SYNT to the coaxial connector J1, is coupled through C126 to the base of Q5. The amplified signal developing at the collector of Q5 is taken to the operative mixer (via CR34 during transmission or via CR32 during reception).

(2) F2 amplifier. This amplifier is built around Q19. The F2 signal arriving from module SYNT (104.1MHz for LSB and 114.6MHz for USB operation) to connector J2 is coupled through the high pass filter consisting of C202, R70 and C142 to the base of Q19. The gain of Q19 is determined by the emitter resistance. During transmission diode CR41 is forward-biased, capacitor C111 is connected in parallel to resistor R67 and therefore the gain is increased. The amplified signal is connected to the operative mixer through switching diode CR42 or CR44.

e. Test Sub-system. The test signal generator is built around the D flip-flops U3A and U3B.

(1) Flip-flop U3A is enabled when the binary code 000 is applied via the FIL SEL lines to the control inputs of U1. This activates transistor Q30 and a high level is applied to the D input of U3A (pin 12). U3A is clocked by the 700kHz clock receives from the SYNT module. The Q output is connected to the reset input of the flip-flop via U4A, so that the flip-flop is reset immediately and therefore generates a comb signal. The comb signal appearing at the Q* output of U3A is filtered by the network comprising C102, R4, C103 and R5, and applied directly to the RF AGC attenuator (the 7 band-pass filters are bypassed).

(2) The operation of flip-flop U3B is the same as that of U3A, except that the comb signal generated by U3B passes through all the receive path, including the 7 band-pass filters. Therefore, U3B is activated when the FIL SEL lines apply the binary codes 001 thru 111 (each code connects one of the seven band pass filter, see para. c.(2) above).

f. Power Supply Filter. The power supply filter is built around amplifier U5A. The 12V supply voltage is filtered by the network comprising R56, CR37, R58, R57 and C154. The filtered 11.5 volt signal is buffered by U5A and driven by Q9.

2-11. Module AM

(figure 2-27 thru 2-29)

a. Block Diagram Analysis (Figure 2-27). Figure 2-27 shows the block diagram of module AM.

(1) Routing of RF signals. The routing of the RF signals in the AM module is controlled by two signals: FRONT/REAR and PTT 20W.

(a) The FRONT/REAR signal selects the RF connector: the front panel RF OUT connector, or the rear panel connector.

(b) The PTT 20W signal selects between the receive and transmit paths, and controls the operation of the power amplifier in module AM:

1. In the receive mode, the PTT 20W signal turns off the 20W power amplifier and routes the received RF signal passed by the FRONT/REAR switch to the RF module, via the bypass switch.

2. The bypass mode is similar to the receive mode, except that the bypass switch connects the 100mW RF transmit signal from the RF module to the FRONT/REAR switch. In addition, during transmission at the 100mW level, a +5V DC voltage is supplied to the RF module, via the AM BYPASS line.

3. In the transmit mode, the PTT 20W signal turns on the 20W power amplifier in module AM and disconnect the RF path through the bypass switch. The low-level AM DRIVE signal received from module RF is amplified by the 20W power amplifier and exits via the FRONT/REAR switch.

(2) Operation of 20W power amplifier. The 20W RF power amplifier is a high-efficiency power amplifier which uses switching techniques to maximize efficiency.

(a) Principles of operation. The 20W power amplifier uses the fact that a modulated RF signal can be described as the product of two signals: a constant-amplitude signal, having the instantaneous frequency and phase of the modulated RF signal, and a signal describing the instantaneous amplitude ("envelope") of the modulated signal. Using this principle, the 20W power amplifier separates the two components and applies each one to a high-efficiency amplification path: one for the envelope signal, and the other for the RF signal. The amplified signals are then multiplied to regenerate the high-power modulated signal.

(b) Functional analysis.

1. Separation of RF signal components. The low-level modulated RF signal, AM DRIVE, received from module RF, is applied to two signal processors:

- A limiter, which extracts the constant amplitude RF component.

- An envelope detector, which extracts the low-frequency modulating envelope.

2. Constant amplitude path. The output signal of the limiter is amplified to the required level by a driver amplifier.

3. Envelope processing. The output signal of the envelope detector is applied to a variable amplifier, whose gain is controlled by the PWR CONT bus. The variable amplifier is the control element of the automatic level control (ALC). The gain of the variable amplifier is varied by the microprocessor in module MCU such as to obtain the required output power.
The output signal of the variable amplifier is amplified by a high-efficiency switching power amplifier, to obtain the control signal for the mixer.

4. Regeneration of high-power RF signal. The output signals of the driver and of the power amplifier are applied to the mixer. The mixer operates as multiplier. The PA OUT signal appearing at the mixer output is an amplified replica of the AM DRIVE signal.

(3) Output filters. The PA OUT signal is filtered by a low-pass filter. There are seven sub-octave filters, and the filter corresponding to the operating frequency is inserted in the signal path by means of PIN diode switches. The PIN diode switches are controlled by a filter control circuit. The filter control circuit receives the FIL SEL commands from the microprocessor in module MCU and converts them to drive signals for the PIN diode switches.
The filtered signal is routed by the FRONT/REAR relay to the rear connector, for driving the antenna connected to the CP-2003 or to the front connector.

(4) Monitoring of power amplifier operation, module presence and module operating voltages. The microprocessor in module MCU can monitor the operation of the 20W power amplifier and the condition of the operating voltages supplied to the module by means of several sensors. Sensor outputs are connected to the AM MUX line by means of a multiplexer, controlled by the MUX SEL lines.

The available sensors are:

(a) Power amplifier current sensor. This sensor provides a DC voltage, designated CURRENT, proportional to the current drawn by the 20W power amplifier, used for BIT purposes.

(b) AM DRIVE envelope detector. The output signal of the envelope detector can be monitored by the microprocessor.

(c) Power detector. The output power of the 20W power amplifier is monitored by a power detector, which provides two signals: a fast attack/fast release signal designated ALC LVL, which follows PA OUT envelope, and a TX LVL signal, which indicates the peak level of the PA OUT signal.

(d) Indication of module AM presence (AM EXIST). A DC voltage of about +2V applied to the MUX indicates that the AM module is properly installed in its place. This indication can be monitored by the microprocessor for BIT purposes.

(e) Indication of module operating voltages. A DC voltage of about +2V applied to the MUX indicates that the +12V voltage is appearing at pins 1 and 16 of J1. This indication can be monitored by the microprocessor for BIT purposes. A DC voltage of 0V applied to the MUX indicates that the +5V and -5V voltages are appearing at pins 7 and 5 respectively of J1. This indication can be monitored by the microprocessor for BIT purposes.

(5) Control of 20W power amplifier.

(a) Power amplifier activation. The power amplifier is activated by connecting the battery voltage, arriving on the FUSED-12V line, to the power amplifier circuit. The connection is made by means of the supply switch, controlled by the PTT 20W* control circuit.

(b) Output power control. The output power is controlled by an ALC system, which includes the microprocessor as the ALC controller. In addition, the output power is also effected by a current sensor located in the PS module. The PS current sensor monitors the total current drawn by the PRC-2200 from the battery and immediately reduces the peak output power when the current is too high.

(c) RF power control algorithm.

1. Initial setting. When starting transmission or changing frequency, a 1kHz matching tone is generated. This tone has a known level, and the microprocessor can read the ALC LVL output while the matching tone is present and make a rapid adjustment of the RF output power, using the PWR CONT bus.

2. Routine control. After the initial setting, the microprocessor uses the TX LVL signal to stabilize the RF output power at the desired average level.

3. Current consumption considerations. The microprocessor monitors the current drawn from the battery, and checks that it does not exceed the maximum allowable value. This keeps the current drawn from the battery within the allowable limits.

4. Local current limiting. To obtain maximum protection, the current sensor can also control directly the variable amplifier. When the current exceeds the maximum available, the DC voltage proportional to the power amplifier current reduces the gain of the variable amplifier, even without the intervention of the external ALC loop.

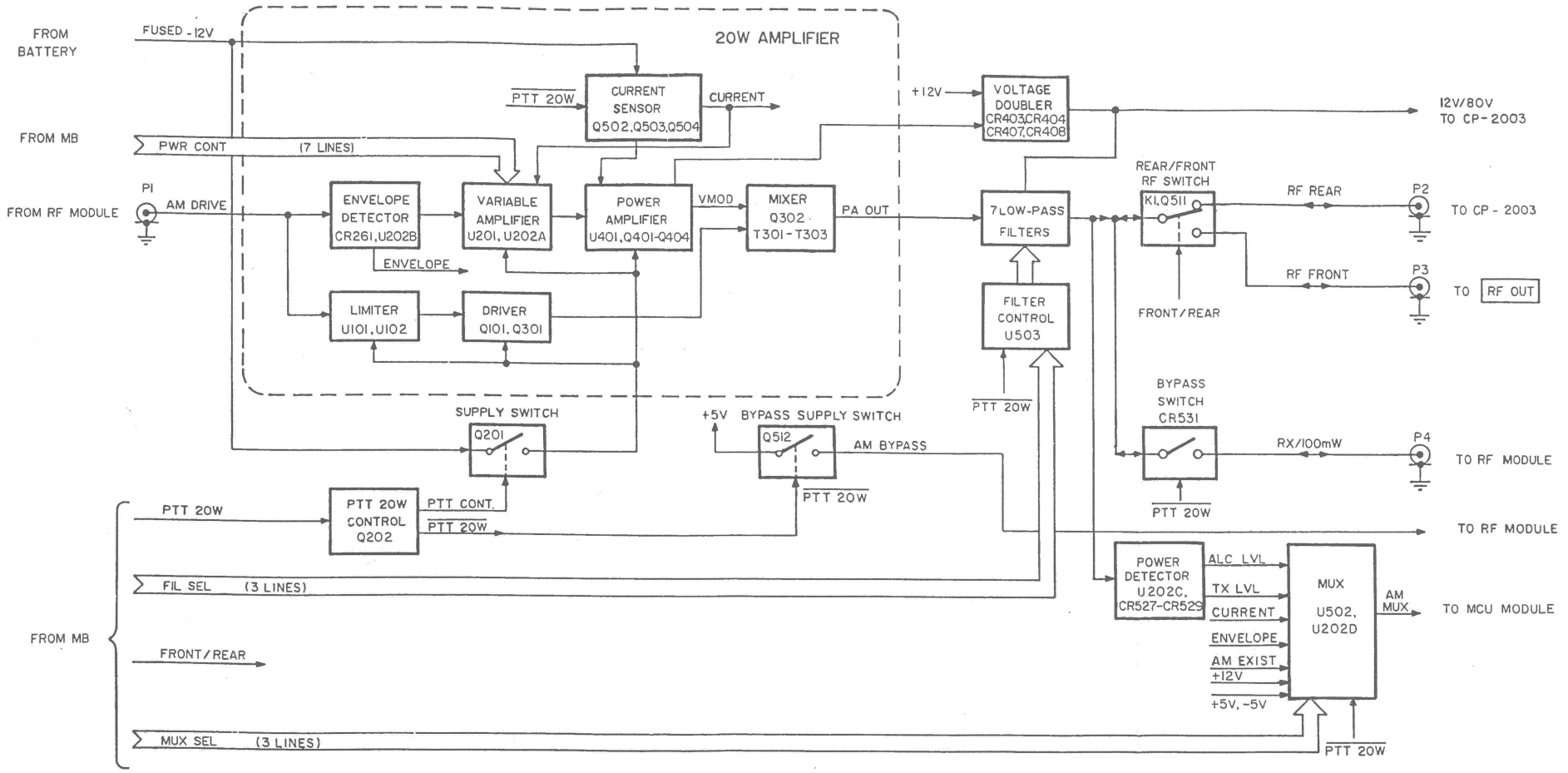


Figure 2-27. Module AM, Block Diagram

(6) Voltage doubler. During transmission, it is necessary to generate a high voltage of about 80V. This voltage is used to reverse-bias PIN diode CR531, disconnecting the bypass switch and to disconnect six of seven low pass filters. In addition, the voltage doubler output is transferred to the CP module via the 12V/80V line (12V during reception, 80V during transmission).

b. Circuit Analysis (fig. 2-28, 2-29)

(1) 20W power amplifier.

(a) Power amplifier activation. In the transmit mode, the PTT 20W line rises to a high level. Transistor Q202 saturates and turns on transistor Q201. As a result, the 12V battery voltage, filtered by L201 and C201, is connected by Q201 to the various circuits of the power amplifier.

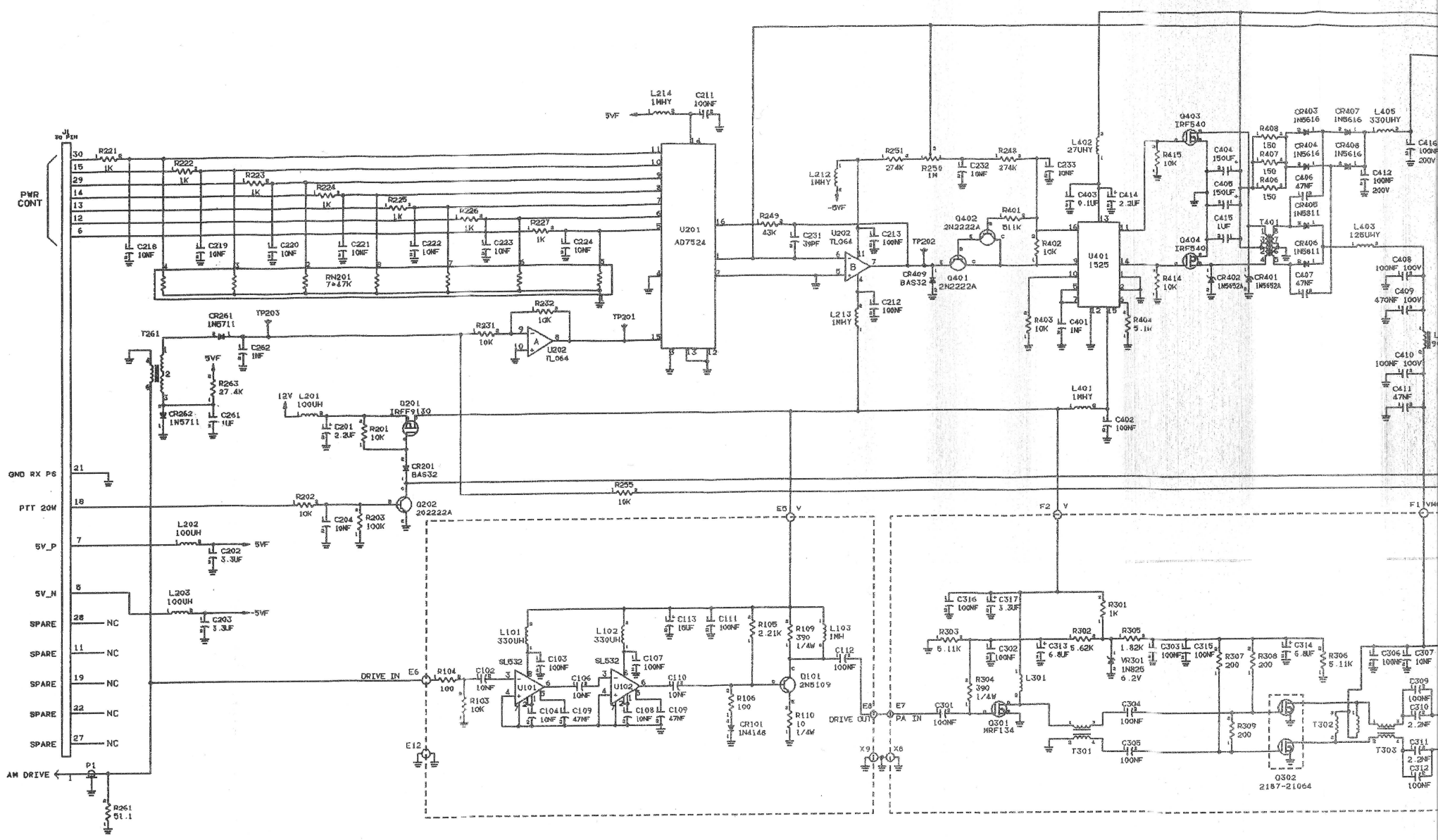
(b) Limiter and driver. The low level modulated signal, AM DRIVE, received from module RF, is applied via coupling capacitor C102, to the limiter comprising U101 and U102. U101 and U102 are wide-band amplifiers, which are connected in series via coupling capacitor C106. The constant-amplitude RF component appearing at the output (pin 6) of U102 is applied to the driver built around transistor Q101. Q101 receives bias from the 12V battery voltage, via Q201, R105, R106 and CR101. CR101 is a temperature-compensation diode. The output signal appearing at the collector of Q101 is applied via C112 and C301 to another driver, built around FET Q301. R301, R303, R304 and VR301 are used to supply a gate bias voltage to Q301. The amplified signal appearing at the drain of Q301 is applied to the mixer comprising T301, Q302 and T303 (para. (3) below).

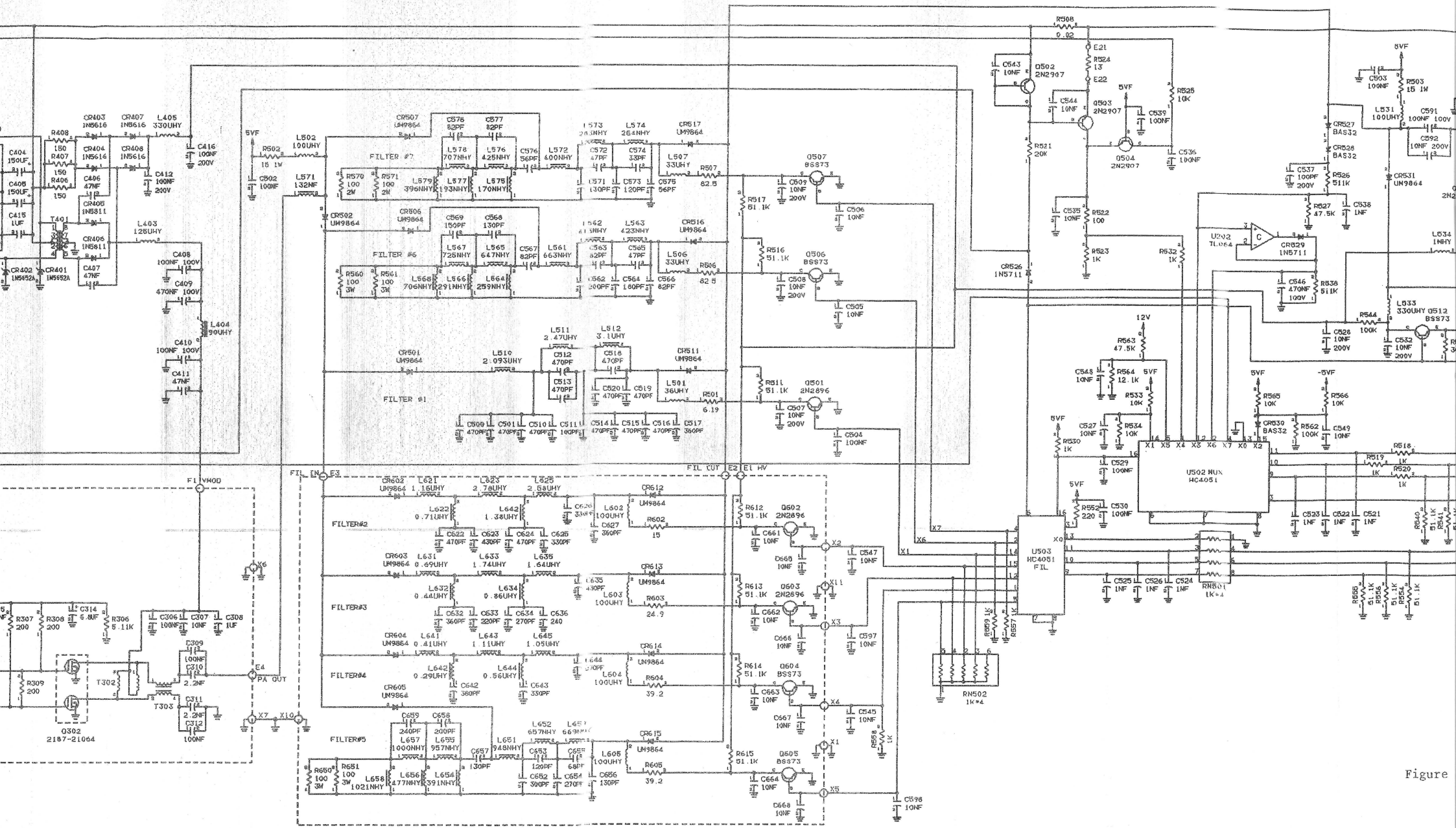
(c) Envelope detector. The AM DRIVE signal, arriving from the RF module, is coupled by T261 to the envelope detector comprising CR261 and C262. The peak-detected signal is applied via the inverting buffer U202B to input VREF of D/A converter U201.

(d) Variable amplifier. The variable amplifier is built around the D/A converter U201 and the amplifier U202A. The gain of the variable amplifier is controlled by the microprocessor in module MCU. The control lines, designated PWR CONT, are applied to pins 5 thru 11 of U201. These lines determine the equivalent resistance between the VREF input (pin 15) and the OUT1 output (pin 1), connected to the inverting input of U202A. The RFB output (pin 16) is connected to the OUT1 output, via an internal resistor having a fixed value. The inverting input (pin 6) of U202B also receives the output voltage of the current sensor (para. (7)(a) below). When the current drawn from the battery is too high, the output voltage of the current sensor increases. The envelope signal applied to the inverting input of U202B is always negative, therefore when the current sensor output increases the peak output signal of U202A is reduced.

(e) Power amplifier. The power amplifier is a high-efficiency switching amplifier built around the pulse-width modulator (PWM) U401. The simplified diagram of the power amplifier is shown in fig. 2-38.

1. U401 contains an oscillator that provides a sawtooth signal. This signal is compared with the voltage applied to the COMP input (pin 9) of U401. The COMP input receives two signals: a constant reference voltage via R402, and a voltage inversely-proportional to the envelope signal provided by the amplifier U202B, via Q401 and Q402. When the output voltage of U202B increases, the voltage across R401 decreases. Therefore, the base current of Q402 decreases and the collector-emitter voltage of Q402 and Q401 increases. The result is that the voltage applied to the COMP input decreases. Diode CR409 protects against negative voltages.


PWR CONT
GND RX PS
PTT 20W
5V_P
5V_N
SPARE
SPARE
SPARE
SPARE
SPARE
AM DRIVE
DRIVE IN
DRIVE OUT
PA IN
U201 AD7524
U202 TL064
U401 1525
Q101 2N5109
Q201 IRF9130
Q202 2N2222A
Q301 MRF134
Q302 2187-21064
Q401 2N2222A
Q402 2N2222A
Q403 IRF540
Q404 IRF540
U101 SL632
U102 SL632
T301
T302
T303
T401


FILTER #7
FILTER #6
FILTER #1
FILTER#2
FILTER#3
FILTER#4
FILTER#5
FIL IN
FIL OUT
FIL HV
FIL VMOD
PA OUT
U502 MUX HC4051
U503 HC4051 FIL
RN501 1K*4
RN502 1K*4
Q502 2N2907
Q503 2N2907
Q504 2N2907
Q507 BSS73
Q506 BSS73
Q501 2N2896
Q502 2N2896
Q503 2N2896
Q604 BSS73
Q505 BSS73
Q302 2187-21064
T302
T303
T401
CR529 1N5711
CR526 1N5711
CR527 BAS32
CR528 BAS32
CR530 BAS32
CR531 UM9864
U202 TL064

Figure

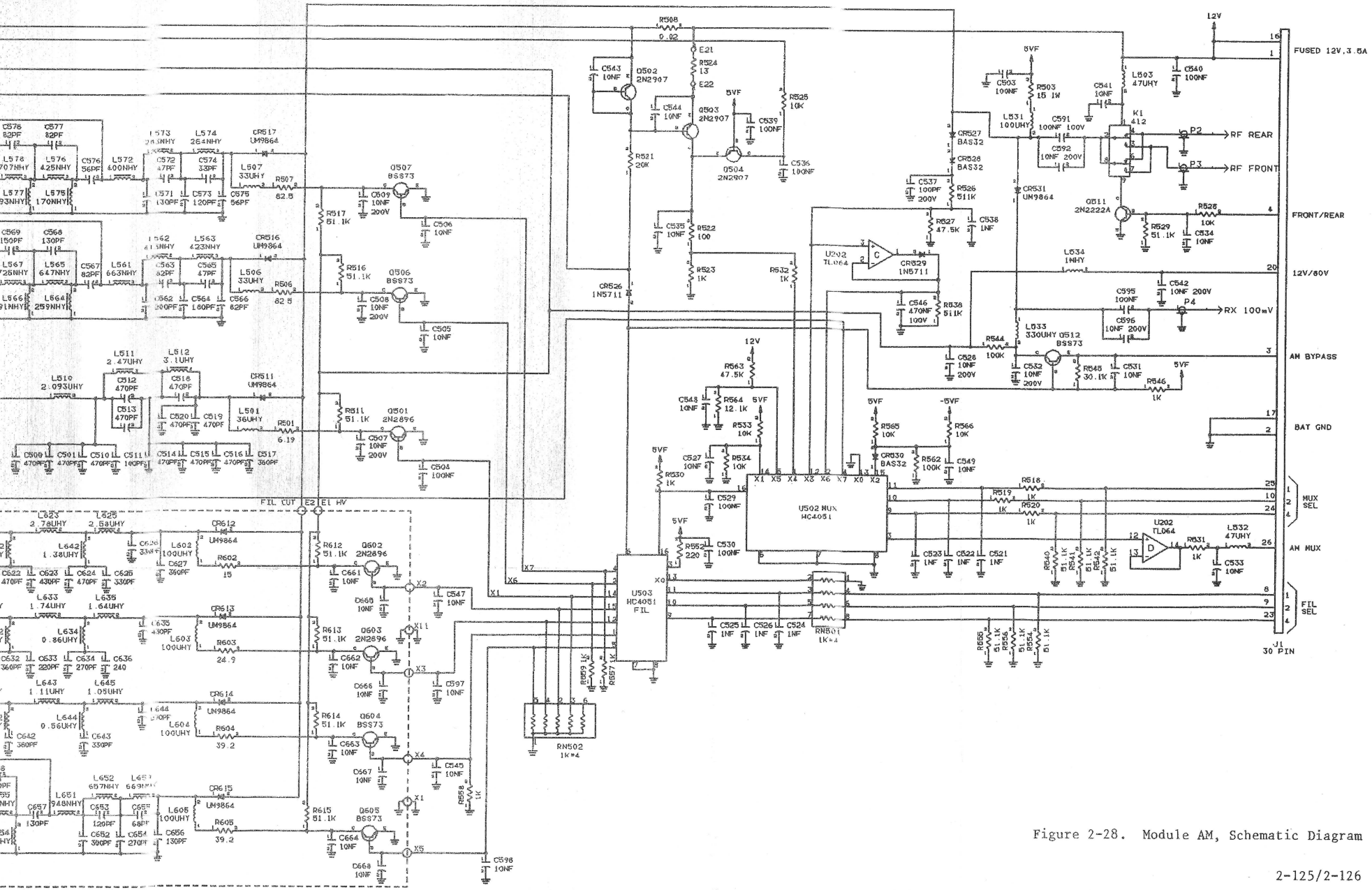


Figure 2-28. Module AM, Schematic Diagram

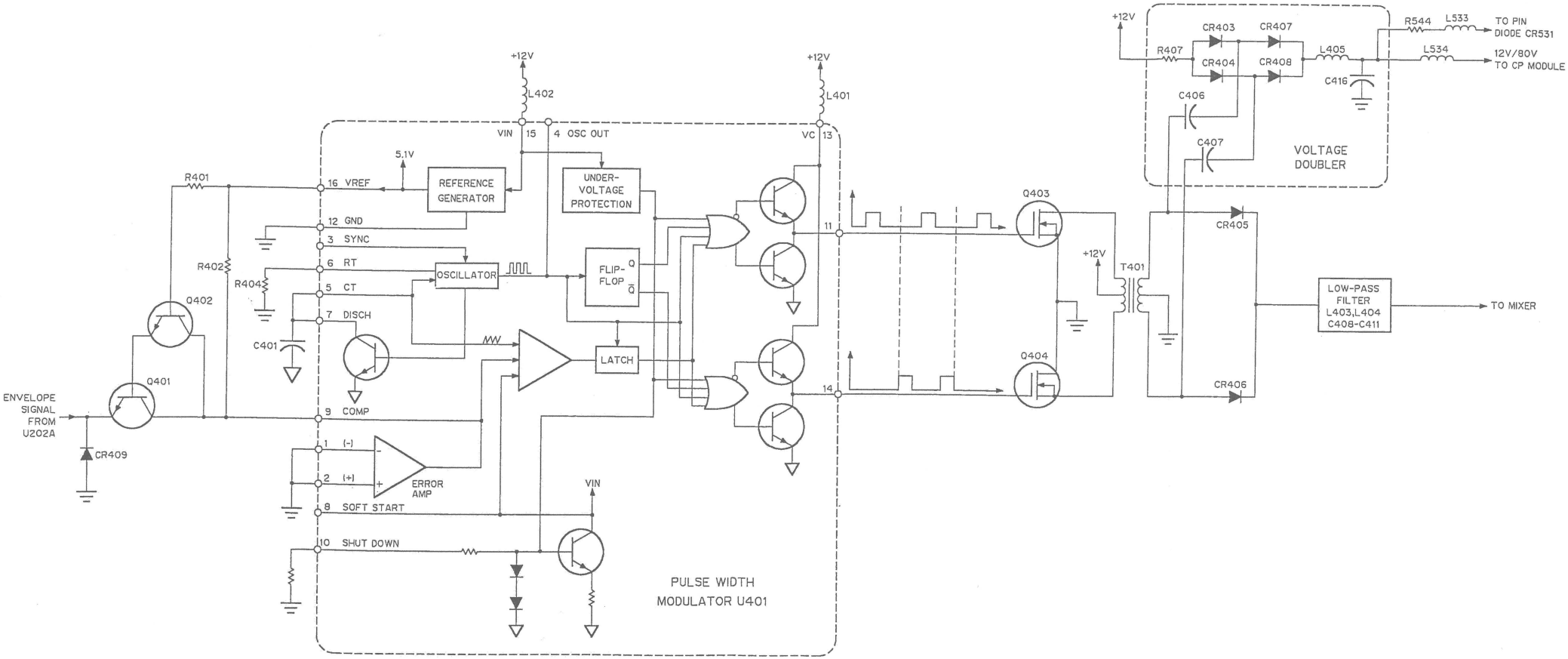


Figure 2-29. Power Amplifier, Simplified Diagram

2. The comparator included in U401 provides a signal whose duty cycle is inversely-proportional to the voltage applied to the COMP input: when the voltage at the COMP input decreases, the duty cycle increases, and vice-versa.

3. The output signal of the comparator is processed by the output circuit of U401 and then applied to the gates of the FETs Q403 and Q404.

4. Q403 and Q404 are the switching transistors, that control the current pulses flowing through the primary of transformer T401. The voltages appearing at the secondary of T401 are rectified by CR405 and CR406 and filtered by a low-pass filter, which attenuates the switching frequency of U401. The resulting signal is sent to the mixer (para. (3) below).

(2) Voltage doubler (fig. 2-28, 2-29). The voltage doubler generates a voltage of 12V in the receive mode, and a voltage of approximately 80V in the transmit mode. The voltage doubler is built around capacitors C406 and C407 and diodes CR403, CR404, CR407 and CR408.

(a) In the receive mode, the power amplifier is disconnected, therefore no pulses appear across the secondary of the transformer T401. The +12V supply voltage passes through CR403, CR407, CR404 and CR408 to the CP module and to the cathode of PIN diode CR531.

(b) During transmission, the power amplifier is activated and pulses appear across the primary windings of step-up transformer T401. The turns ratio of the transformer is approximately 3.3. These pulses charge capacitors C406 and C407. The voltage developed across them is twice the voltage of the pulses at the secondary of T401. The pulses are rectified by CR407 and CR408 and filtered by L405 and C416. The resulting

DC voltage, of about 80V, is applied to the CP module and to the cathode of PIN diode, CR531, which is now reverse-biased and applied to disable six of the seven filters.

(3) Mixer. The mixer comprises T301, Q302 and T302, operates as a multiplier. The output signal of the driver Q301 is applied to the balun transformer T301. T301 splits the signal into two equal signals having a phase difference of 180°. The two signals are coupled via C304 and C305 to the gates of the two FETs contained in Q302. The drains of the two FETs receive the output signal of the power amplifier through the transformer T302. The mixed signals are combined by balun transformer T303 and coupled via C309 through C312 to the seven low-pass filters.

(4) Low-pass filters and associated control circuit. The output signal of the mixer is applied via L571 to the 7 sub-octave low-pass filters. Two types of filters are used: One type includes low-pass filters 2, 3 and 4. The other type includes low-pass filters 1, 5, 6 and 7, which are diplexers that present a constant input impedance of 50 ohm even at frequencies in their stop-band.
The filter corresponding to the operating frequency is inserted into the signal path by means of PIN diodes connected to the input and output of each filter. The PIN diode switches are controlled by the filter control circuit built around demultiplexer U503 and the transistor Q501, Q506, Q507 and Q602 through Q605. The control circuit receives the binary FIL SEL commands from the microprocessor in module MCU and converts them to drive signals for the PIN diodes.

For example, when operating in the band of 1.5 to 2.2MHz, the binary code 001 is applied to the control inputs of U503 (pins 9, 10, 11 respectively). The X1 output (pin 14) of U503 rises to a high level and the other six outputs of U503 fall to a low level, and transistor Q501 is activated. As a result, PIN diodes CR511 and CR501 are forward-biased and connect the 1.5 to 2.2MHz low-pass filter (filter No. 1) into the transmit path. U503 is controlled by the PTT 20W* line, applied to its chip-select input (pin 6) from the collector of

Q202, via CR526. In the receive mode, a high level is applied to pin 6, U503 is disabled, and all the seven filters are disconnected.

Table 2-9 lists the selected filter according to the FIL SEL commands.

Table 2-9. 7 Low-pass Filters Control, Module AM

FIL SEL Commands (U503 Inputs)			Active Output of U503	Activated Transistor	Forward-Biased PIN Diodes	Operating Frequency
Pin 9	Pin 10	Pin 11				
0	0	1	X1 (pin 14)	Q501	CR501, CR511	1.5 to 2.2MHz
0	1	0	X2 (pin 15)	Q602	CR602, CR612	2.2 to 3.4MHz
0	1	1	X3 (pin 12)	Q603	CR603, CR613	3.4 to 5.2MHz
1	0	0	X4 (pin 1)	Q604	CR604, CR614	5.2 to 8MHz
1	0	1	X5 (pin 5)	Q605	CR605, CR615	8 to 12.3MHz
1	1	0	X6 (pin 2)	Q506	CR506, CR516	12.3 to 19MHz
1	1	1	X7 (pin 4)	Q507	CR507, CR517	19 to 30MHz

(5) Rear/front RF switch. This switch selects between the front panel RF OUT connector and the rear panel connector.

(a) In the PRC-2200, usually the FRONT/REAR line applied to the base of Q511 is at a low level. Q511 is cut-off, and the relay K1 transfers the RF output signal of the selected low-pass filter to the rear panel connector.

(b) In vehicular configurations, the FRONT/REAR line is at a high level, Q511 saturates and K1 is energized. As a result, the RF signal is transferred to the front panel connector.

(6) Bypass mode. The 20W amplifier is bypassed in the receive mode, and also when transmitting at the 100mW level.

(a) In the receive mode, the PTT 20W line is at a low level, therefore the base of Q512 receives +5V via resistor R546.

As a result, PIN diode CR531 is forward-biased. Current flows through it via R503, L531, L533 and Q512 to the AM BYPASS line. The AM BYPASS line is connected to the 7 band-pass filters in the RF module (para. 2-11), and the DC path closes via the PIN diodes of the selected band-pass filter. When CR531 is forward-biased, the received RF signal passes via K1, C591, C592, C595 and C596 to the RX 100mW line, connected to the RF module.

(b) When transmitting at a level of 100mW, the PTT 20W line is at a low level. The DC path is closed as module, described in para. (a) above, except that in the RF the DC path is closed via the TX/RX control circuit (CR52, T16, T112 and Q15).

(7) Monitoring circuits.

(a) Current sensor. The current sensor, comprising transistors Q502, Q503 and Q504, generates a DC voltage proportional to the current drawn by the 20W power amplifier. This voltage is applied to the multiplexer U502, for monitoring. In addition, the current sensor reduces immediately the peak output power when the current drawn from the battery is too high.

1. The current flowing via the FUSED 12V line from module PS is sampled by the current sense resistor R508. The voltage developing across this resistor is applied to the emitter-base junction of Q503, via resistor R524 and transistor Q502. Q502 operates as a diode (forward-biased by the DC current flowing from the FUSED 12V line via R508, Q502, R521 and Q202 to ground). Q503 collector is connected to the voltage divider R522, R523. The voltage appearing across R523 is proportional to the current flowing via R508. This voltage is applied via R532 to pin 1 of the multiplexer U502.

2. The voltage appearing at the collector of Q503 is applied to the emitter of Q504, which functions as a comparator. The base of Q504 receives a reference voltage of +5V. When the voltage at the emitter of Q504 increases above approximately +5.5V, Q504 starts conducting and drives a DC current, via R525, into the inverting input of the amplifier U202B (para. (1) (d) above). This current reduces the peak output power.

(b) Power detector. The output voltage of the 20W power amplifier is applied through one of the seven low-pass filters to the envelope detector, comprising CR527, CR528, R526, R527 and C538. This detector has a fast attack/fast release characteristic. This signal is applied to pin 12 of U502. In addition, the output signal of the envelope detector is applied to pin 3 of the amplifier U202C. U202C together with CR529 operate as a peak detector, and generate a voltage proportional to the peak level of the power amplifier output signal. This voltage is applied to pin 2 of U502.

(c) Multiplexer U502. U502 passes one of the seven signals applied to its inputs (pins 14, 1, 12, 2, 4, 5 and 15), according to the MUX SEL commands applied to its control inputs (pins 9, 10 and 11). Table 2-10 lists the signals selected by U502.

The output signal of the multiplexer U502 (pin 3) is buffered by U202D, filtered by R531, C533 and L532, and then sent to the MCU module via AM MUX line.

Table 2-10. U502 Operation

MUX SEL Commands (U502 Inputs)			Selected Input	Selected Signal
Pin 9	Pin 10	Pin 11		
0	0	1	X1 (pin 14)	Existence of the AM module
0	1	0	X2 (pin 15)	Average of +5V and -5V voltages. Shall be 0 volt when both voltages are present
0	1	1	X3 (pin 12)	ALC LVL - envelope of the transmitted signal
1	0	0	X4 (pin 1)	CURRENT - DC voltage proportional to the current drawn from the battery
1	0	1	X5 (pin 5)	+12V SAMPLE - +2V DC voltage, when +12V DC is appearing at J1(1, 16)
1	1	0	X6 (pin 2)	TX LVL - Power amplifier output level
1	1	1	X7 (pin 4)	ENVELOPE- The output signal of the envelope detector CR261, C262

2-12. Module SYNT

(fig. 2-30 thru 2-34)

a. Block Diagram Analysis (fig. 2-30). Figure 2-30 shows the block diagram of module SYNT.

(1) Output signals. The synthesizer module provides the following output signals:

(a) F1 signal. The frequency of this signal may be varied in 100Hz increments over the frequency range of 110.85 to 139.3499MHz. Its frequency is exactly 109.35MHz above the operating frequency.

(b) F2 signal. Its frequency is 104.1MHz for LSB operation and 114.6MHz for USB.

(c) 5.25MHz carrier. This frequency is used by module IF. The generation of the 5.25MHz signal is interrupted in the AM receive mode.

(d) 10kHz signal for the MCU and AUDIO modules.

(e) 3.5MHz reference for the AUDIO module.

(f) 700kHz signal for the RF module, used during test.

(2) Synthesizer frequency control. The main output frequency of the synthesizer is controlled by the frequency bus. The frequency bus carries serial data which indicates the required operating frequency. In frequency operation, the frequency bus is controlled by the microprocessor in module MCU. The frequency data, designated DATA, is accompanied by a clock signal, and loaded into the variable divider control circuit. The variable divider control circuit also receives a HOP signal, which indicates the end of received data control word. The variable divider control circuit processes the frequency data and generates two internal control words, one for each variable divider.

(3) Generation of fixed frequencies.

(a) Synthesizer frequency standard. The frequency standard is a 3.5MHz temperature controlled crystal oscillator (TCXO). The 3.5MHz reference frequency is also sent to the MCU and AUDIO modules.

(b) Generation of internal reference frequencies.

1. The 100kHz reference frequency for the F1 phase-lock loop (PLL) is obtained by dividing the 3.5MHz frequency by 35.

2. The 10kHz signal for the MCU and AUDIO modules is obtained by dividing the 100kHz F1 reference by 10.

3. The reference frequency for the FLOCAL PLL, 60kHz, is obtained by multiplying the 3.5MHz frequency by three, to obtain 10.5MHz, then dividing this frequency by 175.

4. The 5.25MHz frequency for the IF module is obtained by dividing by 2 the 10.5MHz frequency. The divider is disabled in the AM receive mode, under control of the PTT and AM/SSB lines.

5. The 700kHz test signal for module RF is obtained by dividing the 3.5MHz reference by 5. The divider by 5 is enabled during self-test, by means of the L.TEST line.

6. The F2 signal, used by module RF, is obtained from a separate crystal oscillator. Its frequency is controlled by the USB/LSB line and changes as listed in para. (1)(b) above. The output signal of the F2 oscillator is sent via a buffer to the RF module.

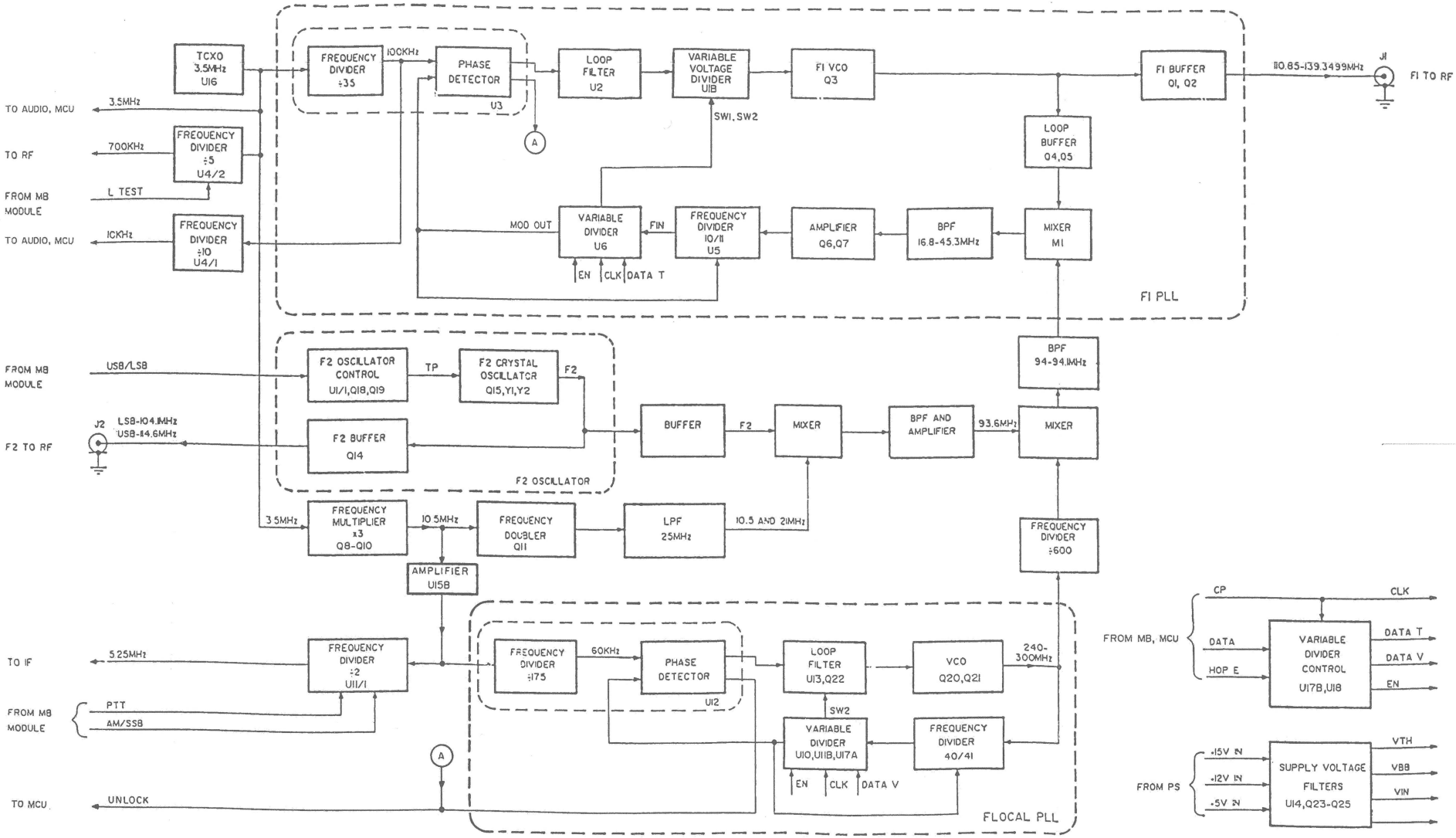


Figure 2-30. Module SYNT, Block Diagram

7. The internal 93.6MHz frequency is obtained by mixing the output signal of the F2 oscillator with the 10.5MHz signal, or with its second harmonic, 21MHz. The 21MHz signal is obtained by doubling the frequency of the 10.5MHz signal, and attenuating the higher harmonics by a 25MHz low-pass filter.

- When operating in the SSB/LSB mode, F2 frequency is 104.1MHz and the 93.6MHz signal is obtained by taking the difference frequency between F2 and 10.5MHz.

- When operating in the SSB/USB mode, F2 frequency is 114.6MHz and the 93.6MHz signal is obtained by taking the difference between F2 and 21MHz.

The 93.6MHz signal is filtered by a bandpass filter and amplified, before application to the mixer M3.

(4) Generation of 100Hz steps. The 100Hz steps are obtained from the output signal of the FLOCAL PLL.

(a) The FLOCAL PLL generates frequencies in the range of 240 to 299.4MHz, in 60kHz steps (step size is determined by the 60kHz reference frequency). The PLL uses a dual-modulus (40/41) prescaler, and a variable divider. The division ratio of the divider is programmed by the DATA V control word, serially received from the variable divider control circuit. A new control word is loaded into the variable divider by means of a CLK (clock) signal, whenever the 10kHz, 1kHz and 100Hz digits of the operating frequency are changed. The load command is provided on the EN line.

Following the change in the division ratio, the phase-lock loop action changes the VCO frequency such as to obtain lock at the programmed frequency.

The UNLOCK line sent to module MCU indicates the state of the FLOCAL loop.

(b) The output frequency of the FLOCAL PLL is divided by 600, to obtain a frequency which changes in 100Hz step within the range of 400 to 499.9kHz. This frequency is mixed by mixer M3 with the 93.6MHz signal (para c.(2)(g) above), to obtain frequencies in the 94.0 to 94.0999MHz range. The output signal of the mixer M3 is filtered by a narrow-bandpass filter. The filtered signal is applied to the mixer M1, in the F1 PLL.

(5) Generation of F1 signal. The F1 signal covers the 110.85 to 139.3499MHz range in 100Hz steps. The F1 PLL uses two techniques to obtain the required frequency resolution:

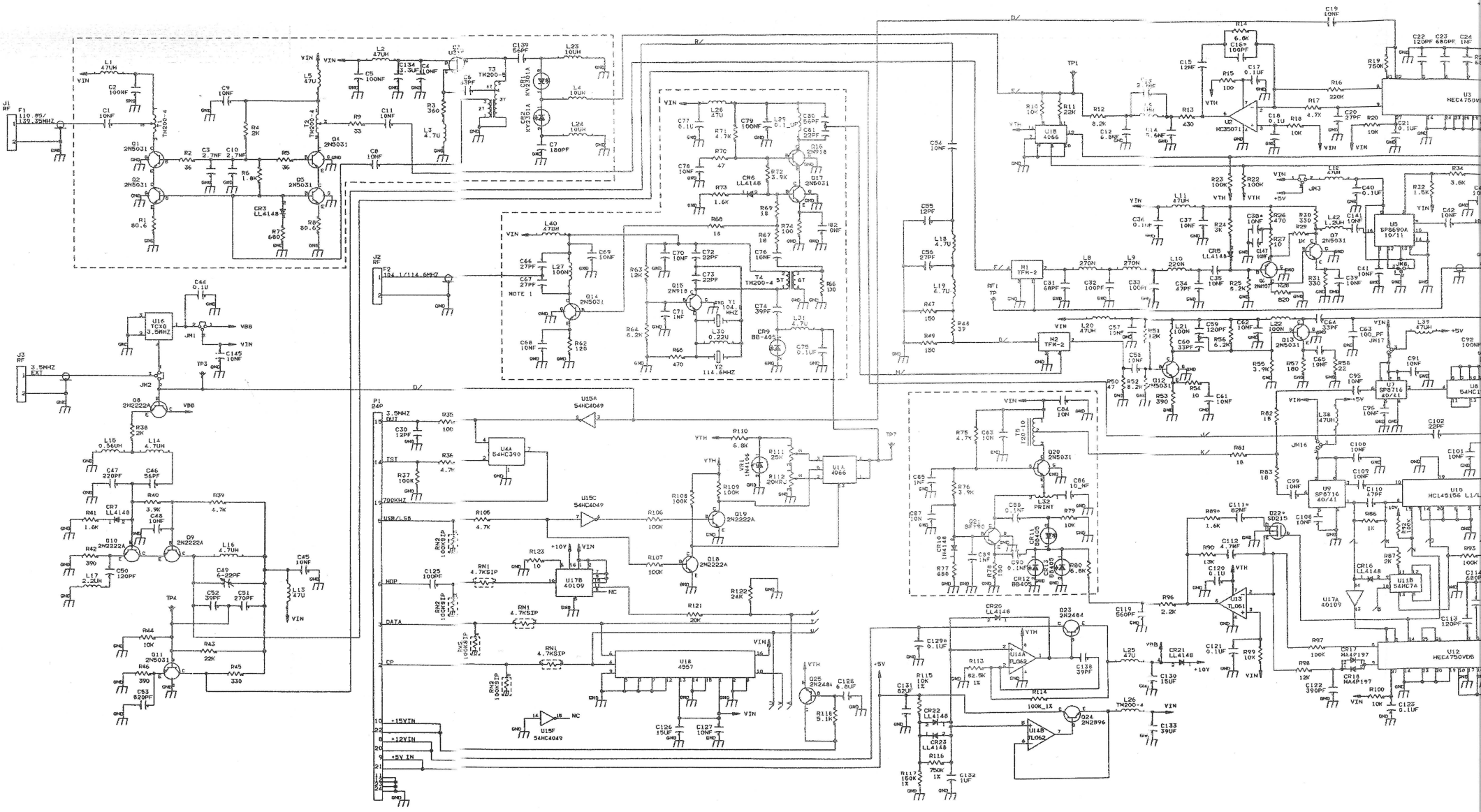
(a) 100kHz steps are introduced by changing the division ratio of the dual-modulus variable divider included in the F1 PLL. The division ratio is controlled by the DATA T control word, sent by the variable divider control circuit.

(b) The smaller steps are introduced by changing the frequency of the FLOCAL PLL. This introduces an "error" in the loop, by shifting the frequency of the signal appearing at the output of mixer M1, and applied to the input of the dual-modulus (10/11) prescaler.
The PLL reacts by changing the control voltage applied to the VCO, such that its output frequency shifts in the direction required to cancel the "error" caused by the change in the FLOCAL signal.

b. Circuit Analysis (fig. 2-31 thru 2-34).

(1) Generation of 100Hz steps.

(a) The 3.5MHz reference frequency generated by the temperature controlled crystal oscillator (TCXO) U16 is applied to a frequency multiplier by 3, via contacts 1 and 2 of the jumper JM2 (when using an external 3.5MHz frequency, contacts 2 and



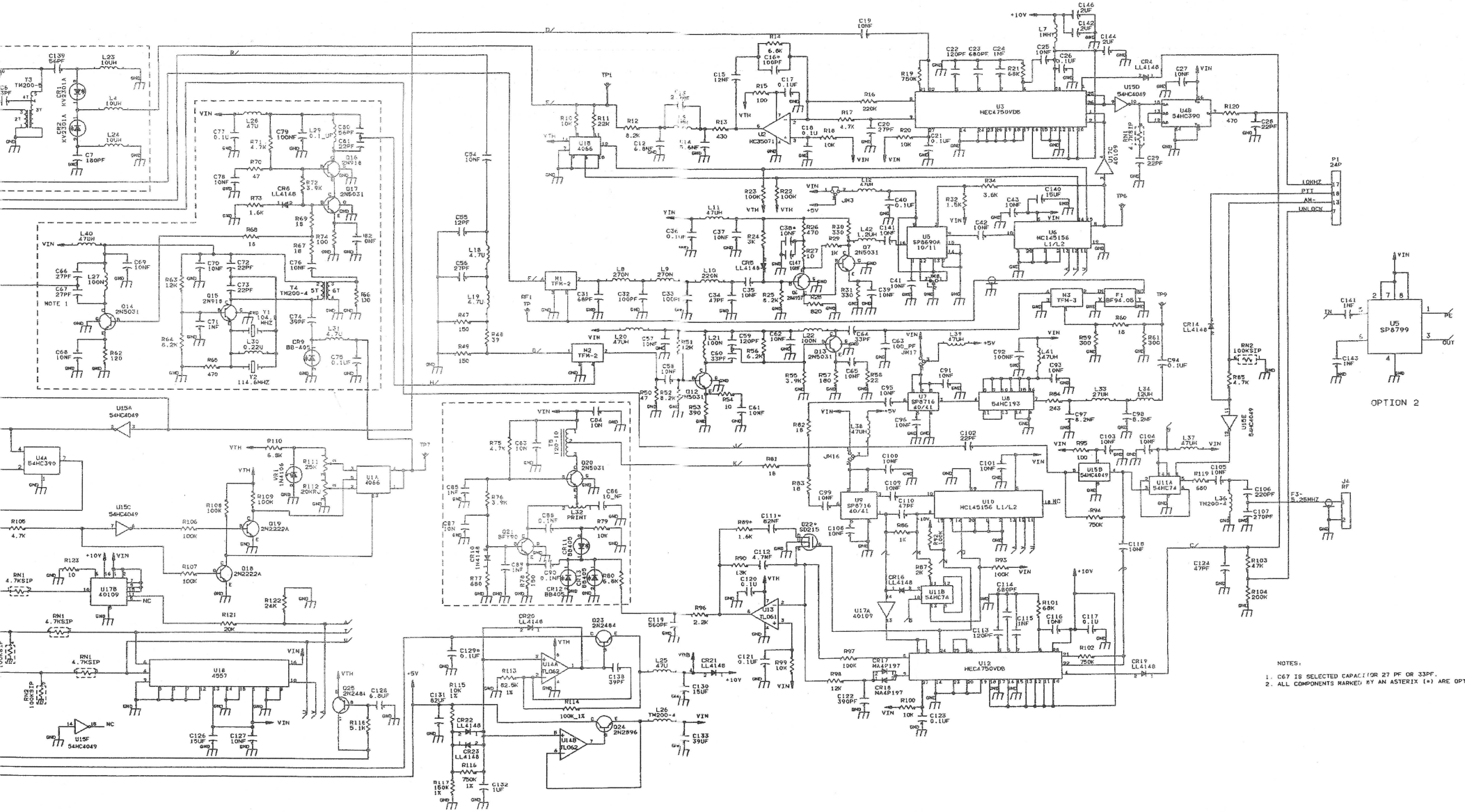


Figure 2-31. Module SYNT, Schematic Diagram

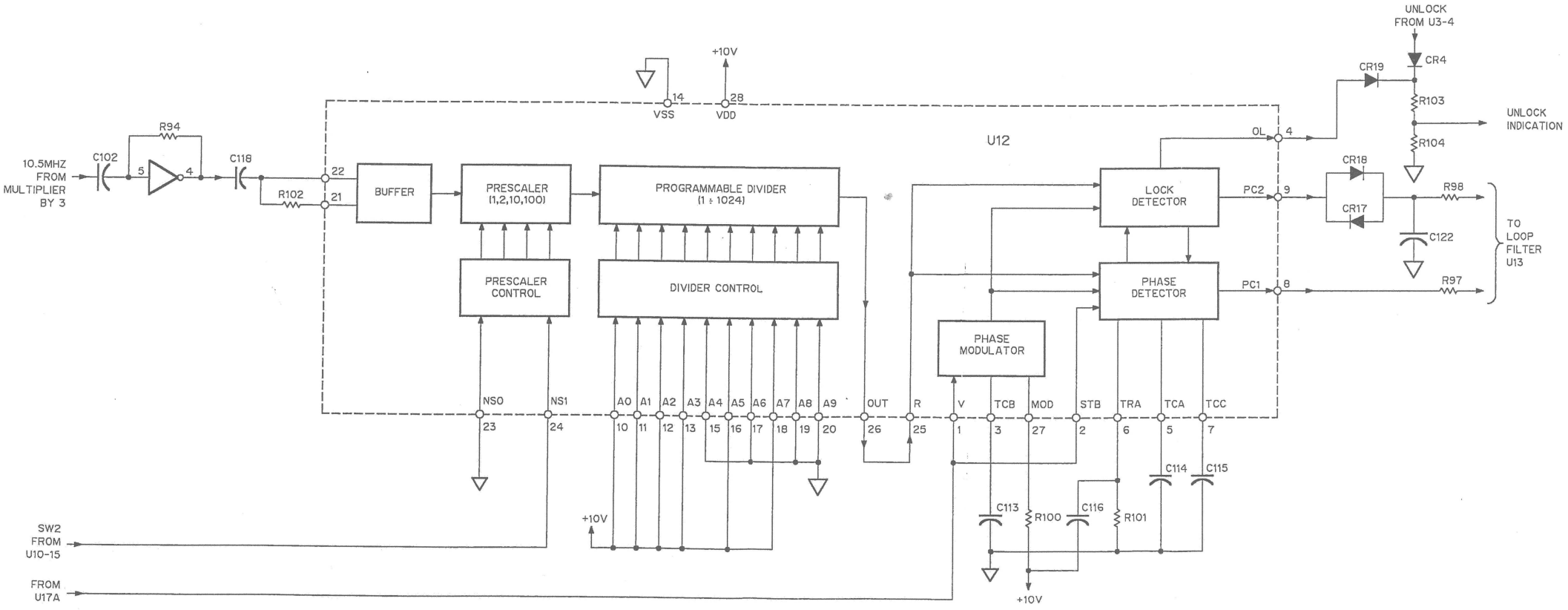


Figure 2-32. Integrated Circuit U12, Equivalent Block Diagram

3 of JM2 are connected). The multiplier by 3 is built around Q8, Q9 and Q10. Transistor Q8 oscillates between cut-off and saturation, thereby generating harmonics of 3.5MHz. The third harmonic, at a frequency of 10.5MHz, develops across the resonant circuit comprising L14, L15, C46 and C47, and is then applied to the amplifier built around Q9 and Q10. These transistors receive DC bias via R39, R40, CR72 and R41. CR7 is a temperature compensation diode. The tuned collector circuit of Q9, comprising L16, C49, C51 and C52, resonates at 10.5MHz. The output signal is applied via coupling capacitor C102, the amplifier comprising inverter U15B and resistor R94 and via the coupling capacitor C118 to pins 21 and 22 of U12.

(b) Frequency division by 175 and phase detection. These functions are performed by the circuit built around the integrated circuit U12. The block diagram of U12 is shown in figure 2-41.

1. Divider by 175. This circuit divides the frequency of the reference signal provided by the multiplier by 3, to obtain the 60kHz internal reference frequency of the FLOCAL PLL. The circuit comprises a buffer, a prescaler and a programmable divider. The 10.5MHz signal is applied to pin 22, and the divider output appears at pin 26. In U12, the signal is applied via a buffer to the prescaler. The prescaler division ratio is determined by inputs NS0 and NS1, according to Table 2-11.

Table 2-11. Reference Prescaler Control

NS1	NS0	Division Ratio
0	0	1
0	1	2
1	0	10
1	1	100

In U12, NS0 is connected to ground and NS1 usually receives a low level from the SW2 output of the two-bit shift register contained in U10 (para. (f) below). Therefore, the prescaler division ratio is usually set to 1.

There is an option to operate the unit with 10Hz steps. In this case, the NS1 input receives a high level and the prescaler division ratio is set to 10.

2. The division ratio of the programmable divider division ratio can be changed in the range of 1 to 1024, under control of the input lines A0 thru A9. The division ratio is the decimal value of the binary number applied to the control lines A0 thru A9. In U12, the division ratio is set to 175.

3. Phase detector. The input signals of the phase detector contained in U12 are the 60kHz reference signal, and the output signal of the variable divider, comprising U10, U11B, U17A and U9. The phase detector generates a voltage proportional to the phase difference between the two signals. Typical waveforms are shown in figure 2-33. The 60kHz reference frequency is applied to the R input of the phase detector (pin 25 of U12). The divided VCO signal from U17A is applied to the STB input of the phase detector (pin 2 of U12), and to the V input of the phase modulator (pin 1 of U12). The moment the V signal falls to a low level, the phase modulator generates a signal, V'. V' is a negative pulse that discharges the external capacitor C114 connected to pin 5 of U12. When pulse V' ends, C114 starts charging. Charging continues as long as a high level is present at the R input of the phase detector. When a low level appears at the R input, capacitor charging stops, and its voltage is proportional to the phase difference between signals V' and R.

U12 internal circuits transfer C114 voltage to C115. The voltage across C115 is connected through a buffer to the detector output (pin 8 of U12). Phase detector output signal is connected to the loop filter U13 via resistor R97.

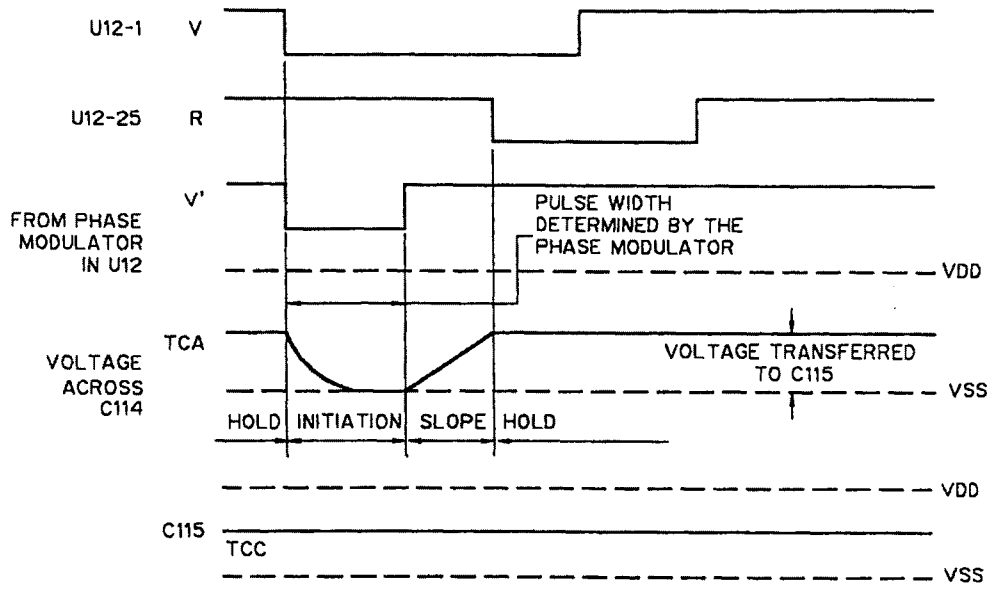


Figure 2-33. Typical Phase Detector Waveforms

4. Lock detector. This circuit contains a lock detector which monitors loop state, and a phase detector which operates when loss of lock is detected.

a. The lock circuit indicates loop state. When the loop is locked, a low level appears at the O/L output (pin 4 of U12). A high level, indicating that the loop is not locked, appears in the following cases:

- The R signal precedes the V signal.
- No pulses appear at the R input.
- No pulses appear at the V input.

The O/L signal from pin 4 of U12 is send through CR19 and the voltage divider R103 and R104, to the MCU module, via the UNLOCK line.

b. The phase detector has a wide dynamic range, up to 360°. This reduces the time required to regain lock. The input signals of the detector are the 60kHz reference signal and the V signal from the phase modulator. The phase detector generates a voltage proportional to the phase difference between the two signals.
The phase detector output (pin 9 of U12) is connected to the loop filter U13 via the filtering network CR17, CR18, C122 and resistor R98.

(c) Loop filter. The loop filter of the FLOCAL PLL is built around amplifier U13. The loop filter receives the output signals of the phase detectors contained in U12. Usually when operating with 100Hz channel spacing, transistor Q22 is cut-off and the transfer function is determined by R97, R98, C112 and R90.

When the option of 10Hz spacing is used, the gate of Q22 receives a high level from from U10-15. As a result, Q22 conducts, so R89 and C111 are now connected in parallel to R90 and C112.

(d) Voltage-controlled oscillator (VCO). The VCO of the FLOCAL PLL is built around Q21 and Q20. Oscillation frequency is determined by the resonant circuit comprising the variable capacitance diodes CR11, CR12 and CR13 and the inductor L32. Diodes capacitance is controlled by the DC output voltage of the loop filter U13-6. Q20 and Q21 receive bias via R75, R76, CR10 and R77. CR10 is a temperature compensation diode. C88 and C90 are coupling capacitors. C86 blocks DC current. The output signal of the oscillator taken from a tap on L32, is buffered by Q20. The output signal of Q20 is coupled by T5 distributed via by R81, R82 and R83 to the frequency divider by 600, comprising U7 and U8, and to the 40/41 prescaler, U9.

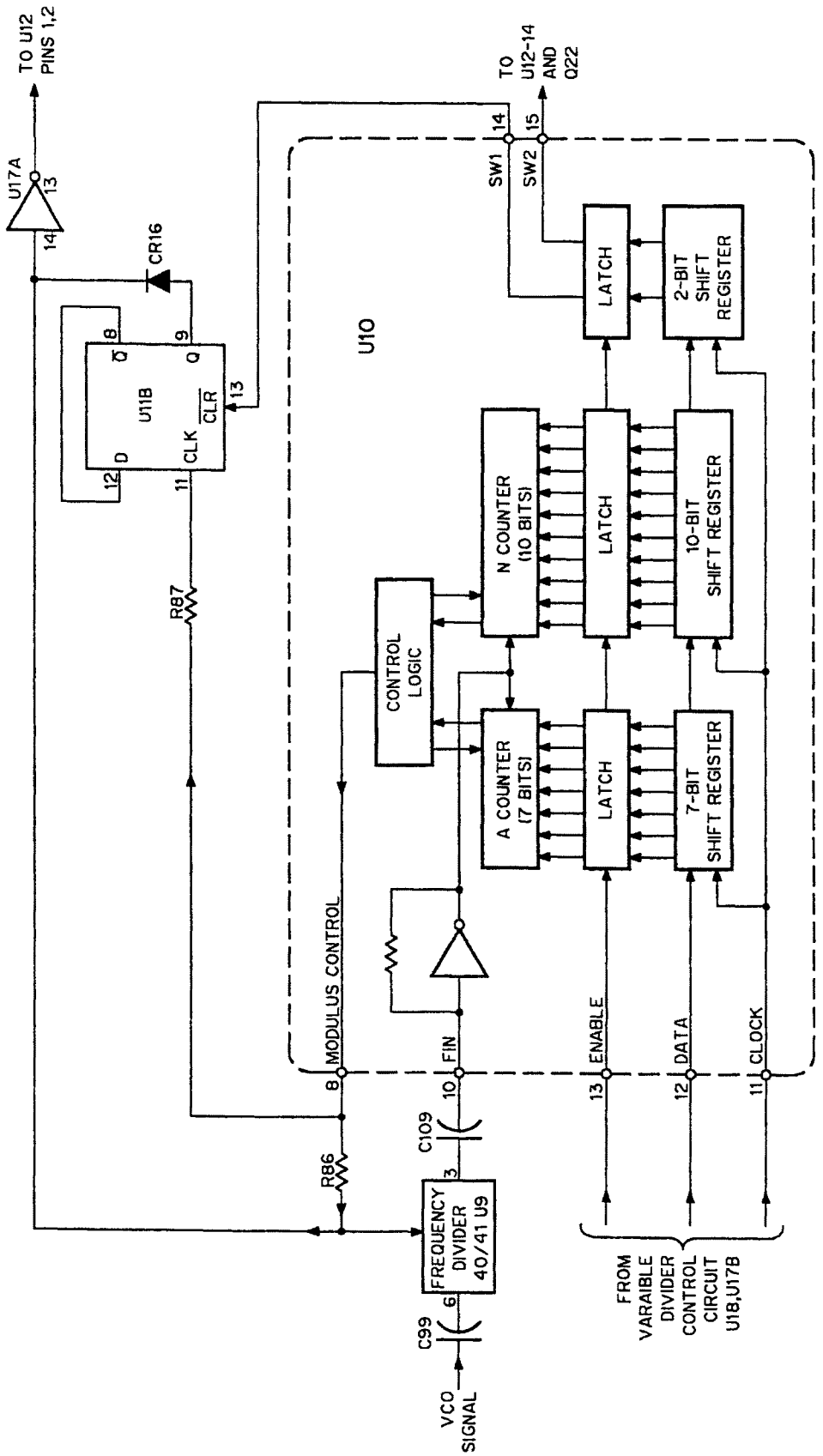


Figure 2-34. Variable Divider U10 and Prescaler 40/41 U9, Simplified Circuit Diagram

(e) 40/41 prescaler (fig. 2-34). The VCO output signal is applied via R81, R83 and C99 to the clock input of divider U9 (pin 6). U9 is a dual-modulus divider, which can divide by 40 and 41.

The output signal of U9 (pin 3) is applied through C109 to the clock input of U10 (pin 10).

The division ratio of U9 is determined by the control signal arriving from pin 8 of U10, via resistor R86.

1. When pin 8 of U10 is at a low level, a low level appears at pin 1 of U9 and the division ratio is 41.

2. When pin 8 of U10 is at a high level, the division ratio is 40.

(f) Variable divider (figure 2-34). U10 receives serial division control data from the variable divider control circuit (U17B, U18) and divides accordingly, the output signal of the 40/41 prescaler to achieve a frequency equal to that of the reference frequency (60kHz). U10 block diagram is shown in figure 2-43.

1. Loading data into the shift registers. Each low-to-high transition on the CLOCK line (pin 11) loads one bit of the 19-bit serial data, presents on the DATA line (pin 12) at the time of the positive clock transition.

The serial data, arriving from the variable divider control circuits (para. (6), below, provides programming information for the A counter (7 bits), for the N counter (10 bits) and for the two switch control signals, SW1 and SW2.

2. Enabling the latches. After the 19-bit word has been loaded into the shift registers, the ENABLE line (pin 13) rises to a high level. As a result, the contents of the shift registers are transferred to the latches, the programmable counters, and the switches SW1 and SW2.

When data transfer is completed, the ENABLE line falls to a low level, and thus allows changes to be made in the shift register data without affecting counter programming and switch outputs.

3. Programmable counters A and N. The positive-edge triggered A and N counters are clocked by the output signal of the 40/41 prescaler, applied via C109 to the Fin input of U10 (pin 10).

The division ratios of the programmable counters are determined by the data stored in the latches. At the beginning of a division cycle, the counters are loaded with the latch data, and start counting down according to the clock rate appearing at the output of the 40/41 prescaler.

4. Modulus control system. At the beginning of the division cycle, the division modulus control line is at a low level, hence, prescaler division ratio is set to 41. This line stays at a low level until divider A ends its division cycle. Then, the line rises to a high level, and the division ratio of the prescaler is set to 40. The control line remains at a high level until the division cycle of divider N ends. When divider N cycle ends, the control line falls to a low level, and dividers A and N are reloaded with data from the latches.

5. SW1 and SW2 outputs. SW1 and SW2 (pins 14 and 15, respectively) provide latched outputs corresponding to the first two data bits of the 19-bit word. These two bits are used to select the 10Hz spacing option. When this option is being used, SW1 and SW2 rises to a high level.

6. D flip-flop U11B. U11B is activated only when using the 10Hz steps option. When using the 100Hz steps, SW1 output (pin 14) is at a low level, therefore the Q output (pin 9) of U11B is forced to a low level, and diode CR16 is reverse-biased. As a result, the MODULUS CONTROL signal (pin 8 of U10) is applied via R86 and U17A to the phase modulator and phase comparator contained in U12. When the 10Hz steps option is used, SW1 rises to a high level and enables the D flip-flop U11B. As a result, the MODULUS CONTROL signal, applied to the CLK input (pin 11) of U11B is divided by two, and then sent through CR16 and U17A to U12.

(g) Divider by 600. The output frequency of the FLOCAL PLL is divided by 600, to obtain a frequency which changes in 100Hz steps within the range of 400 to 499.9kHz. The divider by 600 is built around the dividers U7 and U8. U7 is a dual-modulus 40/41 prescaler. The modulus control input of U7 (pin 1) receives a high level, therefore U7 is divided by 40. U8 is a divider by 15. The output signal of the VCO (Q21, Q20) is applied via R81, R82 and C95 to the clock input (pin 6) of U7. U7 divides signal frequency by 40 and applies it to the clock input (pin 4) of the divider by 15, via U8. The output signal of U8 (pin 7) is filtered by R84, C97, L33, C98 and L34, attenuated by R61, R60 and R59 and then applied to the mixer M3 (see para. (3) below).

(2) Generation of F2 and 93.6MHz frequencies.

(a) F2 oscillator and associated control circuit. The F2 signal, used by module RF, is obtained from a separate oscillator built around transistor Q15 and crystals Y1 (resonance frequency of 104.1MHz) and Y2 (resonance frequency of 114.6MHz).

The oscillation frequency is determined by the resonant circuit comprising the variable capacitance diode CR9, capacitors C74, C73, C72 and transformer T4.

CR9 capacitance is controlled by the DC voltage applied by the control circuit built around U1A, Q18 and Q19. The control circuit is controlled by the USB/LSB command as follows:

1. During LSB operation, the USB/LSB line falls to a low level. As a result, transistor Q18 cuts-off and transistor Q19 saturates. As a result, pins 2 and 1 of switch U1A are connected and pins 3 and 4 are disconnected. The DC voltage developing across R112 is sampled, and applied via pin 2, 1 of U1A and via L31 to the cathode of CR9, to determine a resonant frequency of 104.1MHz.

2. During USB operation, the USB/LSB line rises to a high level. Now, Q19 cuts off and Q18 saturates, therefore pins 3 and 4 of U1A are connected and pins 2 and 1 are disconnected. As a result, the DC voltage developing across R111 is sampled and applied to the cathode of CR9, so the crystal oscillator oscillates now at a frequency of 114.6MHz.

The output signal of the oscillator is coupled by T4, split by R67, R68 and R69 and applied to two buffers:

- The buffer built around Q14 buffers the F2 signal to the RF module, via the F2 104.1/114.6MHz line.

- The buffer built around Q16 and Q17 buffers the F2 signal to pin 4 of the mixer M2.

(b) Mixer M2. The mixer M2 is used to generate the 93.6MHz internal frequency. This frequency is obtained by mixing the output signal of the F2 oscillator (pin 4 of M2) with the 10.5MHz signal, or with its second harmonic, 21MHz (pin 1 of M2). The 21MHz signal is obtained by means of transistor Q11. Q11 generates harmonics of the 10.5MHz signal. The higher harmonics are attenuated by the 25MHz low-pass filter, comprising C55, L18, C56, L19, R47, R48, R49, while passing the second harmonic.

(c) Bandpass filter and amplifier. The 93.6MHz signal appearing at the output of the mixer M2 (pin 2) is amplified by the two-stage bandpass filter and amplifier built around transistors Q12 and Q13. The resonant network of the first stage comprises L21, C59 and C60. The resonant network of the second stage comprises L22, C64 and C63.
The 93.6MHz signal appearing at the output of the bandpass filter is applied to pin 4 of the mixer M3.

(3) Mixer M3. The output frequency of the divider by 600 (para. (1)(g) above), which changes in 100Hz steps within the range of 400 to 499.9kHz (pin 1 of M3) is mixed with the 93.6MHz signal (pin 4 of M3), to obtain frequencies in the 94.0 to 94.0999MHz range.

(4) Bandpass filter F1. The output signal of the mixer M3 (pin 2) is filtered by the narrow bandpass filter F1. The filtered signal is applied to the mixer M1 in the F1 PLL (para. (5) (e) below).

(5) Generation of F1 signal.

(a) The 3.5MHz reference frequency generated by the temperature controlled crystal oscillator (TCXO) U16 is applied via coupling capacitor C19 to pin 22 of the integrated circuit U3.

U3 contains a reference frequency divider, phase detector and lock detector, that are identical to the circuits contained in U12 (para. (1)(b) above). The block diagram of U12 is shown in figure 2-41. The block diagram of U3 is similar to the block diagram of U12, but the pin connections are different (see fig. 2-31).

1. Pin 23 and 24 of U3 (NS0 and NS1) are connected to ground, therefore the division ratio of the U3 prescaler is always 1.

2. The binary number applied to the control line A0 thru A9 sets the division ratio of the programmable divider included in U3 is 35.

3. Loop filter. The phase detector output signals (pins 8 and 9) are applied to the loop filter of the F1 PLL. This loop filter is built around the amplifier U2. The transfer function of U2 is determined by R16, R17, R14 and C15.

   The output signal of U2 (pin 6) is filtered by a 100kHz low-pass filter comprising C14, L6, C13 and C12.

(c) Variable voltage divider. The variable voltage divider comprises resistor R10, R11 and R12 and the switch U1B. The switch is controlled by the SW1 and SW2 bits from U6 (pins 14 and 15), in accordance with the operating frequency, as listed in Table 2-12.

Table 2-12. Variable Voltage Divider Control

Operating Frequency	Control Bits (U1B Inputs)		Resistor Connection
	SW1 (pin 6)	SW2 (pin 12)	
1.5 - 7.9999MHz	1	1	R10 and R11 are connected to ground
8 - 14.9999MHz	1	0	R10 - connected to ground R11 - disconnected
15 - 21.9999MHz	0	1	R11 - connected to ground R10 - disconnected
22 - 29.9999MHz	0	0	R10 and R11 are disconnected

(d) F1 VCO. The voltage-controlled oscillator of the F1 PLL is built around transistor Q3. The oscillation frequency is determined by the resonant circuit comprising the variable capacitance diodes CR1 and CR2, transformer T3 and capacitor C139. The diodes capacitance is controlled by the DC voltage applied from the loop filter U2 thru the 100kHz low-pass filter and the variable voltage divider.

The output signal of the oscillator is coupled by T3 and C8 and then split and applied to two buffers:

1. The F1 buffer, built around Q1 and Q2, applies the F1 signal (in the frequency range of 110.85 to 139.34999MHz) to the RF module.

2. The loop buffer, built around Q4 and Q5, applies the F1 signal to pin 4 of the mixer M1, via resistor R9 and coupling capacitor C11.

(e) Mixer M1. The output signal of the loop buffer Q4, Q5 at the frequency range of 110.85 to 139.3499MHz (pin 4 of M1) is mixed with the output signal of the bandpass filter, covering the range of 94.0 to 94.0999MHz (pin 1 of M1) in steps of 100Hz. The output signal of the mixer (pin 2) is filtered by a bandpass filter, having a passband of 16.8 to 45.3MHz. The filter comprises C31, L8, C32, L9, C33, L10 and C34. The filtered signal is amplified by a two-stage amplifier comprising transistors Q6 and Q7. The amplified signal appearing at the collector of Q7 is coupled by C141 to the 10/11 prescaler U5.

(f) 10/11 prescaler. U5 divides signal frequency by 10 or 11, according to the control line from the variable divider U6 (pin 8, via resistor R34):

1. When pin 8 of U6 is at a low level, the division ratio of U5 is set to 11.

2. When pin 8 of U6 rises to a high level, the division ratio is set to 10.

The output signal of U5 is applied via C42 to pin 10 of the variable divider U6.

(g) Variable divider U6. U6 is an integrated circuit which receives serial division control data from the variable divider control circuit (U17B, U18) and divides accordingly, the output signal of the 10/11 prescaler, to obtain a frequency equal to that of the reference frequency (100kHz). U6 operation is similar to the operation of the variable divider U10, described in para. (1)(f) above (U10 block diagram is shown in figure 2-43).

(6) Variable divider control circuit. The variable dividers of the FLOCAL PLL and F1 PLL are controlled by serial data, which indicates

the required operating frequency. The data is processed by the control circuit comprising U18 and U17B. U18 is a 19-bit shift register and U17B is a level shifter.
The 38-bit data word arriving from the microprocessor in the MCU module via the DATA line, is connected to the variable divider U6 via line T and to the input (pin 6) of the shift register U18. The last 19 bits form the control word of the variable divider U6 (F1 PLL), and the first 19 bits form the control word of the variable divider U10 (FLOCAL PLL). Therefore, the control bits of U10 are delayed by the 19-bit shift register U18 before being applied to U10 (via the V line).

The data bits are accompanied by a CLOCK signal, which is applied to both variable dividers via line U, and is used to load the data into the shift registers included in the variable dividers (see para. (1)(f) above) and into the shift register U18.

The HOP signal is used as a strobe for the serial data. After the 38-bit word has been sent, a positive pulse appears on the HOP line and the data is latched into the variable divider. The level of the HOP pulse is shifted by U17B from +5/0V to +10/0V, before applied to the variable dividers, to improve pulse shape.

(7) Generation of fixed output frequencies. The synthesizer module provides the following output signals:

(a) 10kHz signal for the MCU and AUDIO modules. This signal is obtained by dividing the 100kHz F1 reference by 10. The divider by 10 is built around the counter U4/1 (pin 9 thru 15). The 100kHz reference signal is applied from pin 26 of U3 to the CLOCK input (pin 15) of U4/1, via the inverter U15D. The QA output (pin 13) is connected to the B input (pin 12) to obtain BCD count. The resulting 10kHz signal appearing at pin 9 of U4/1 is filtered by R120 and C28 and sent to the AUDIO and MCU modules.

(b) 5.25MHz frequency for the IF module. This signal is obtained by dividing by 2 the 10.5MHz frequency. The divider is built around the D flip-flop gate U11A. The 10.5MHz square-wave signal at the output of U15B (pin 4) is applied to the CLK input (pin 3). The Q* output (pin 6) of U11A is connected to the D input (pin 2) to obtain division by 2. The resulting 5.25MHz signal appearing at pin 5 of U11A is filtered by R119, C105, L36, C106 and C107 and then sent to the IF module.

In the AM receive mode, the inverter U15E applies a low level to the CLR* input (pin 1) of the flip-flop and the Q output of U11A is forced to a low level, thereby stopping the generation of the 5.25MHz signal.

(c) 700kHz test signal for the RF module. This signal is obtained by dividing the 3.5MHz reference by 5. The divider by 5 is built around the counter U4/2 (pins 1 thru 7). The 3.5MHz reference from the TCXO U16 is inverted by U15A and applied to clock input (pin 4) of U4/2. Pin 7 of U4/2 is connected to pin 1, to obtain division by 5. The resulting 700kHz signal appearing at pin 7 of U4/2 is applied to the RF module.

The counter is controlled by the test line, connected via resistor R36 to the clear input (pin 2) of U4/2. During self-test, the clear input receives a low level and the counter operation is enabled.

(8) Supply voltage filters. The DC supply voltages are filtered by the following active filters.

(a) The +15VIN supply voltage is filtered by an active filter comprising transistor Q25.

(b) The +12VIN line is filtered by the active filter built around U14A and Q23. The +5VIN line is filtered by a similar filter, built around U14B and Q24.

2-13. Module MCU

(fig. 2-35 thru 2-43)

a. Block Diagram Analysis (fig. 2-35). Module MCU contains a special-purpose microcomputer system, which performs digital signal processing, encryption and decryption, and controls the operating frequency, as well as frequency hopping and AUTOCALL operation. The MCU module also controls data transfer on the address and data buses, by generating the required clock and control signals.

The block diagram of the MCU module is shown in figure 2-35. The module MCU has five main functional blocks (CPU, I/O, TIMING, PGA, ADC) which connect to two connectors: connector P1 to the motherboard, and connector P2 - to the panel.

(1) Microprocessor. Module MCU uses a 80C188 microprocessor running at a clock frequency of 19.6608 MHz.

This microprocessor is an eight-bit central processing unit (CPU), with a 16-bit internal data bus.

(2) EPROM. The EPROM contains 256kB of program code.

(3) RAM. The RAM contains 32kB of memory, used for temporary storage of variable, tables and data generated during program execution. In addition, the RAM stores operational parameters. To preserve the stored data when the RT-2001 is turned off or does not receive power, the RAM is connected to a backup battery, located on the AUDIO module.

(4) Address latch. The address latch stores the lower-order address byte, received from the microprocessor on the DB0 thru DB7 lines at the beginning of a memory or I/O access. Latching is controlled by the ALE signal. The address byte appearing at the outputs of the address latch is combined with the higher-order lines, appearing at the A8-A17 microprocessor outputs, to form the complete 18-bit address.

(5) Power-up reset and watchdog circuit. This circuit contains a power up/down detector, which monitors the VDD (+5V) and the battery voltage and generates the following control signals when power is applied or removed:

(a) Reset to the microprocessor, generated when power is applied or removed.

(b) Inhibit command to the RAM, which disables RAM accessing while battery voltage is removed. RAM contents are then preserved by the Lithium backup battery, located on the AUDIO module.

This circuit also contains a watchdog system. The watchdog monitors program execution and issues a reset command to the microprocessor if program execution is disrupted.

(6) TIMING LSI. This is a large-scale integrated (LSI) circuit that provides the following functions:

(a) Generation of timing signals for the internal circuits (T signals), according to information stored in an EPROM (U9).

(b) Generation of clock signals, phase-locked to the reference clock from the SYNT module, or, when power is off, from the local oscillator used by the real-time clock.

(c) Maintains the current TOD, even when the RT-2001 is not powered. When the RT-2001 is not powered, the TOD circuit receives a backup voltage from the Lithium battery located on the AUDIO module.

(d) Parallel-to-serial conversion of frequency data and generation of clock and strobe signals for the frequency bus. The frequency bus exits the MCU module via the PGA unit.

(7) CODEC. The codec is an analog/digital (A/D) and digital/analog (D/A) converter, especially designed for optimal processing of speech.

(8) PGA. This circuit is a programmable gate array. Its functions are determined by software, loaded from the program EPROM upon power-up.

(9) Multiplexer and A/D converter. Module MCU includes an analog/digital (A/D) converter, which is used to measure various analog signals. The signal to be measured is selected by means of a multiplexer, controlled by the microprocessor.

To measure a specific signal, the microprocessor applies the appropriate selection code, via the data bus, to the multiplexer, then starts the A/D conversion by applying a chip-select signal to the A/D converter. When the conversion ends, the A/D converter sends an EOC signal to an input port located in the PGA, and in response the microprocessor reads the A/D conversion data through the data bus.

(10) Transceiver. The transceiver is a bi-directional data bus buffer. The buffer is used to send and receive data to/from the module selected by the microprocessor: the PANEL module, or other RT-2001 modules, via the motherboard (MB).
The panel data bus lines are designated DBP0 thru DBP7. The motherboard data bus lines are designated DBM0 thru DBM7.

(11) Communication interface. The communication interface of the microprocessor uses two serial data lines, RXD and TXD. The data lines are available in the rear connector (lines RX-SER-R and TX-SER-R, respectively), for communication with the microprocessor in the CP-2003, and in the front-panel RMT/DATA connector (lines RX-SER-F and TX-SER-F, respectively). The data lines connected to the front-panel RMT/DATA connector pass through an RS-232 interface, which translates the internal logic levels to RS-232 levels and vice-versa. When the microprocessor in the CP-2003 or a device connected to the front-panel RMT/DATA connector wants to send data, it first issues a communication request on the COM-REQ-R or COM-REQ-F lines.

(12) Chip-select generator. This circuit decodes the addresses provided by the microprocessor (A0 thru A2, A4 thru A6) MB-CS* and PNL-CS* and generates timed chip select signals for the ports located on module AUDIO, ports on the motherboard and to various internal circuits (TIM-CS for the TIMING component, ADC-CS for the A/D converter and the output port). It also generates chip-select signals for components on the panel (for the keyboard, the selectors, the dot matrix and seven-segment displays and for the LEDs).

(13) Output port. This port latches the lines ADC-MUX 1 thru 4 applied from the microprocessor via the data bus. It selects the analog multiplexer input which will be measured by the A/D converter.

(14) Input port. This port latches the indication signals applied from the module AUDIO (SQ OUT), from the panel (DAKB), from the PGA (DONE, BUSY*), and PTT inputs. This information is transferred to the microprocessor via the data bus lines DB0 thru DB7.

(15) Transfer of frequency information. The frequency information is generated by the TIMING LSI, located in the MCU module. The frequency information is applied on the frequency bus, together with a clock signal and a stroke signal, HOP BLANK.

The HOP BLANK signal instructs the other modules using the frequency data to read the new data just applied on the frequency bus.
As an option, the PGA can also read frequency data from the frequency bus.

(16) Interrupt sources. The microprocessor can receive interrupts from several sources:

(a) Interrupts generated when a communication request is received from a device connected to the RMT/DATA connector (from the PANEL module via the COM-REQ-F line). This interrupt (INT URT) is generated by the PGA and is applied to INT2 in the microprocessor.

(b) Interrupt generated when the microprocessor in the CP-2003 CONTROLLER module makes a request to communicate with the MCU microprocessor (from the rear connector via the COM-REQ-R line): this request causes the generation of the INT URT, applied to input INT2.

(c) Interrupt generated when the synthesizer loses lock (indication received from the SYNT module, which causes the generation of the NMI signal from the PGA).

(d) The INT BIT interrupt from the TIMING LSI (through the PGA), applied to the INT0 input of the microprocessor, provides software timing.

(e) The INT MC signal interrupt generated by the TIMING LSI, and applied to the INT3 of the microprocessor, provides software timing.

(f) The INT SW interrupt, generated by the TIMING LSI and applied to the INT1 input of the microprocessor, provides software timing.

(g) The interrupts INT SW, INT MC, INT BIT, INT URT, NMI generated on the PGA and TIMING units are handled by the programmable interrupt controller in the microprocessor according to their priorities. When any of these interrupts is received, the microprocessor executes the interrupt handling routine pointed to by the corresponding interrupt.

(h) A high-priority interrupt is provided when a new frequency word is received from the frequency bus. This interrupt appears after each frequency change, and upon reception of every frequency byte from the frequency bus.

This interrupt is generated by the PGA and sent on the NMI line input of the microprocessor.

(17) Signal path through the MCU module.

(a) Transmit operation. In the voice mode with selective squelch, the audio signal received from the AUDIO module on the CODEC IN line is applied to the codec. The digitized transmit signal generated by the A/D section of the codec is then applied to the PGA.

In the internal modem mode, the transmit data signal arriving on the TXBB-IN line is applied directly to the PGA.

The data from the PGA is collected by the microprocessor, processed, and then returned to the PGA as processed data.

This data appears at the output of the PGA and is applied to the D/A section of the codec, which converts it to the analog transmit signal, sent via the CODEC OUT line to the AUDIO module.

The MCU module also prepares the frequency data and applies it on the frequency bus.

(b) Receive operation. In the voice mode with selective squelch, the receive signal arriving from the AUDIO module is applied to the codec. The digitized signal generated by the A/D section of the codec is applied to the PGA.

The data from the PGA is collected by the microprocessor, processed, and then returned to the PGA. This data appears at the output of the PGA. In the voice mode, the PGA output data is applied to the codec, which converts it to the analog receive signal. In the internal modem mode, the PGA output data is connected directly to the DATA/RMT connector via lines RXBBD, RXBB-F and the AUDIO module.

b. Circuit Analysis (fig. 2-36 thru 2-43k). Figure 2-36 shows the functional interconnections between the internal circuits of module MCU.

Figure 2-37 shows the schematic diagram of the module. Figure 2-37 includes six sheets:

- The CPU circuit is shown in fig. 2-37A.
- The TIMING circuit is shown in fig. 2-37B.
- The PGA circuit is shown in fig. 2-37C.
- The I/O circuit is shown in fig. 2-37D.
- The ADC circuit is shown in fig. 2-37E.
- The PF circuit is shown in fig. 2-37F.

(1) Microprocessor operation (fig. 2-37A, 2-38). The functions performed by the microprocessor U4 are determined by a set of program instructions stored in the EPROM U5.

The RAM U6 is used to store temporary variables and tables required for program execution and programming commands.

U4 includes all the circuits necessary for fetching, interpreting and executing instructions stored in the memory. The microprocessor addresses the memory or the other input/output circuits via a 20-bit address bus.

Data and instructions are transferred to and from the microprocessor via an eight-bit bi-directional data bus.

(a) The microprocessor input and output lines used in the MCU module are described below:

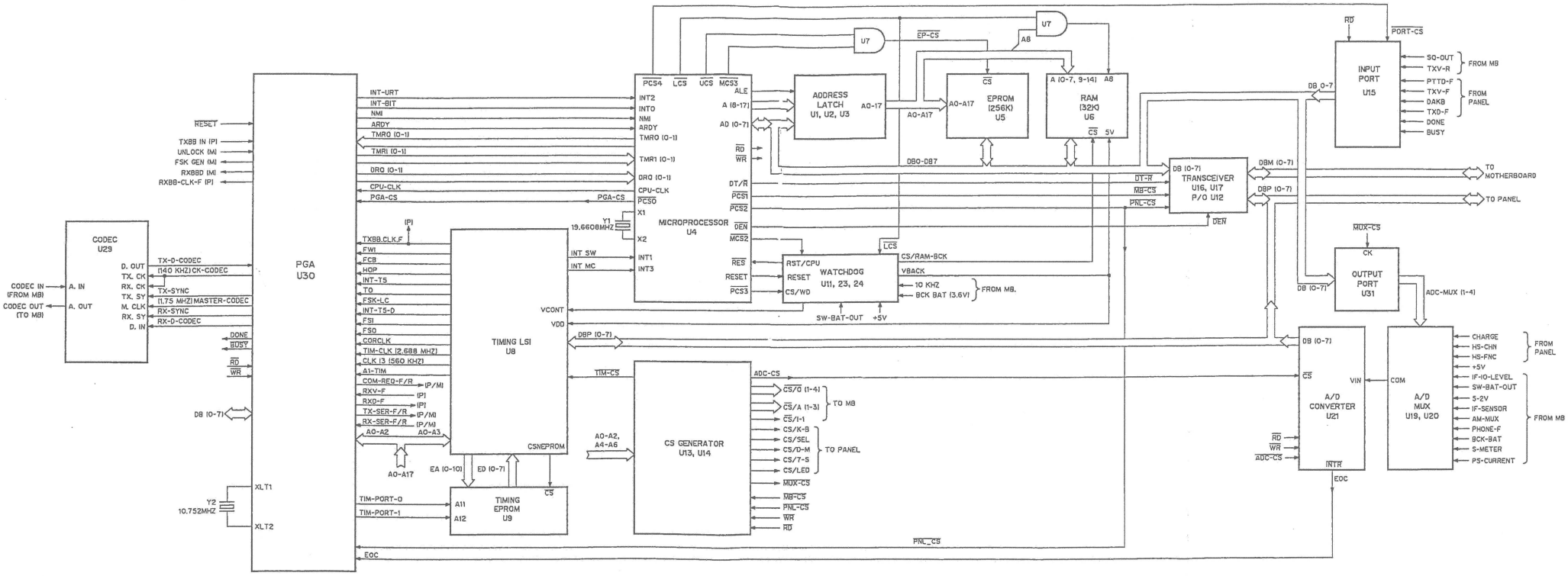
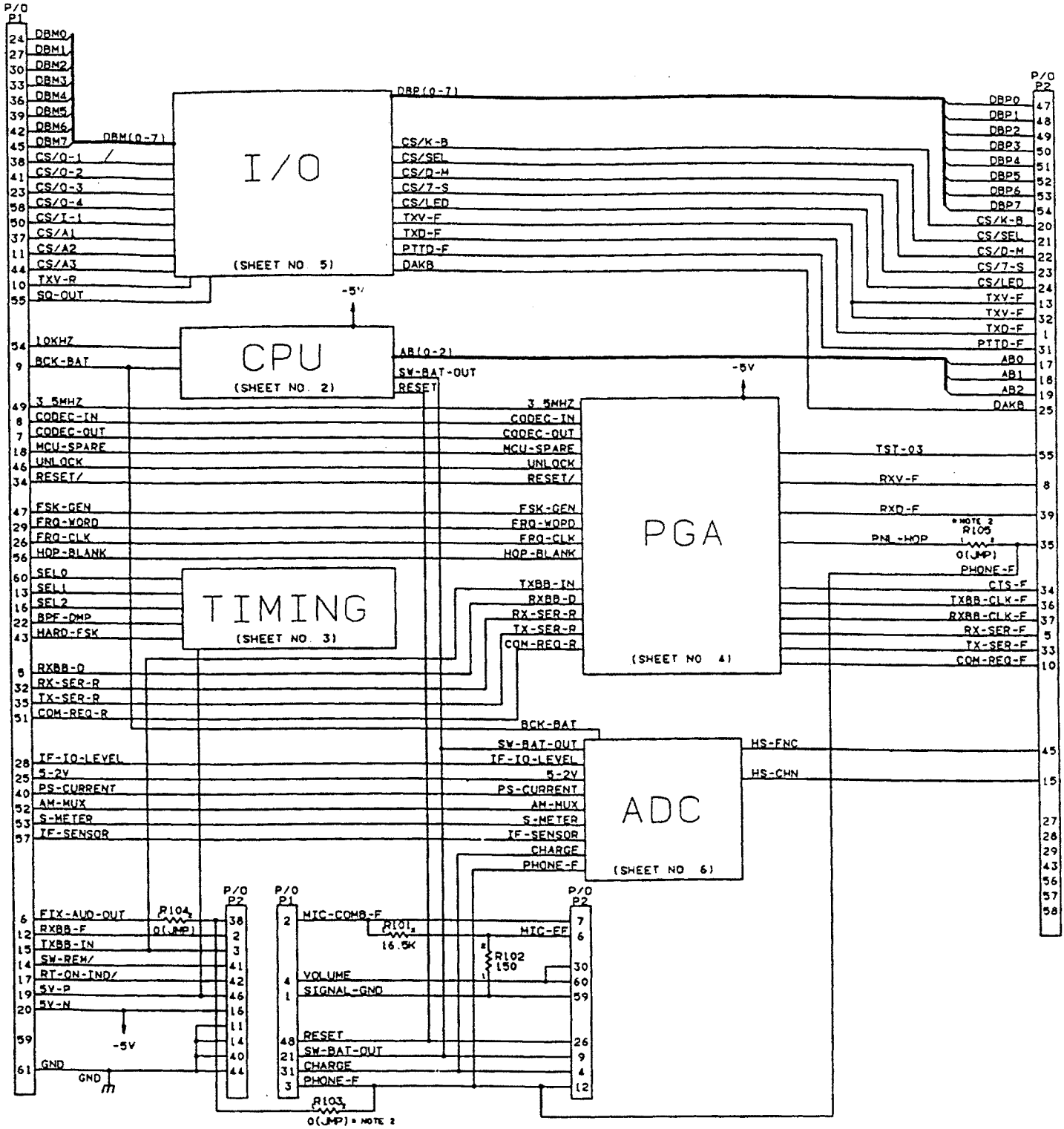


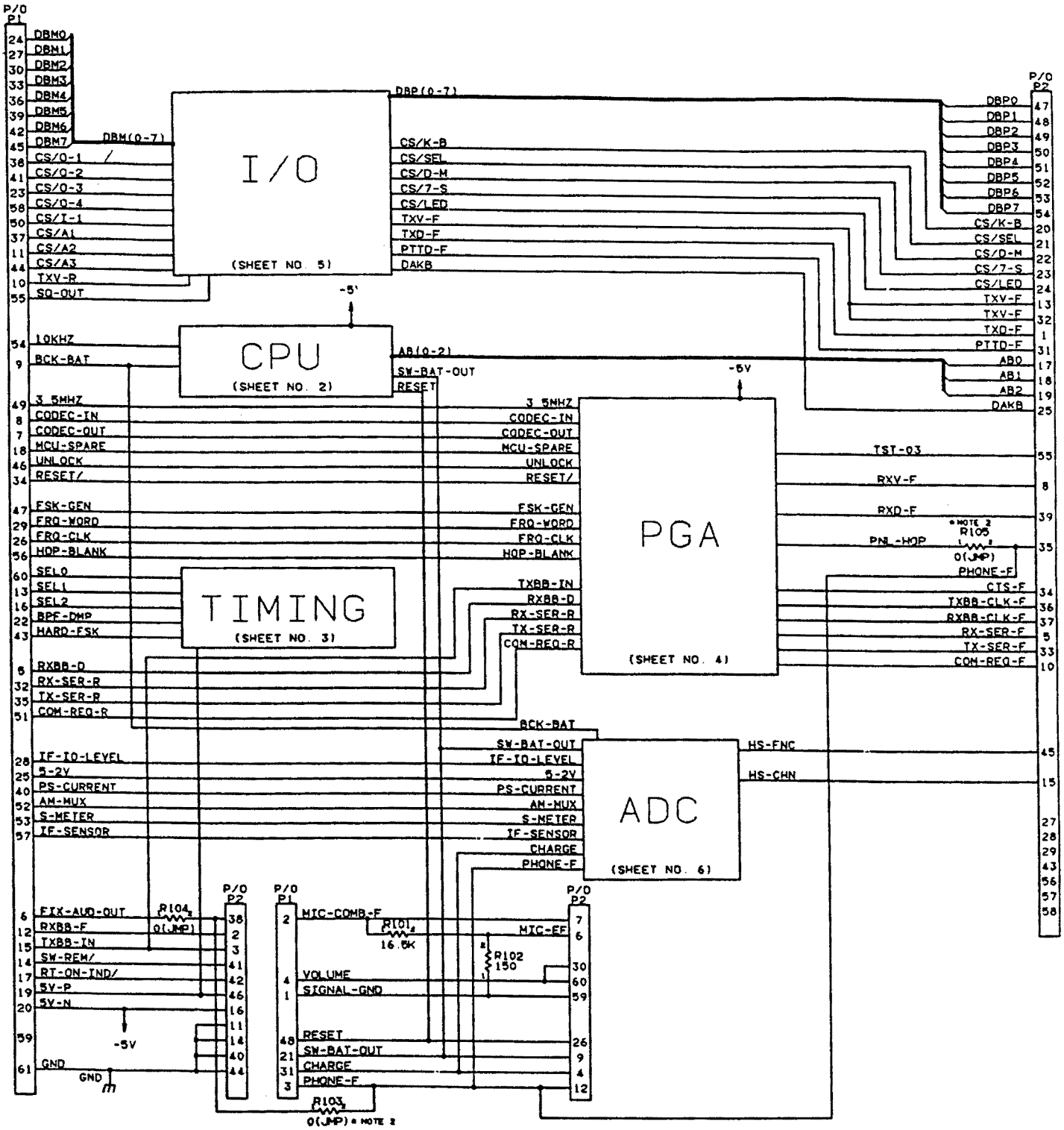
Figure 2-35. Module MCU, Block Diagram



NOTES:

1. INTERCONECTIONS BETWEEN BLOCKS ARE NOT SHOWN.
* 2. R103,R105 NOT CONNECTED.

Figure 2-36. Module MCU, Functional Interconnection and Connector Wiring Diagram



NOTES:

1. INTERCONNECTIONS BETWEEN BLOCKS ARE NOT SHOWN.
* 2. R103,R105 NOT CONNECTED

Figure 2-36. Module MCU, Functional Interconnection and Connector Wiring Diagram

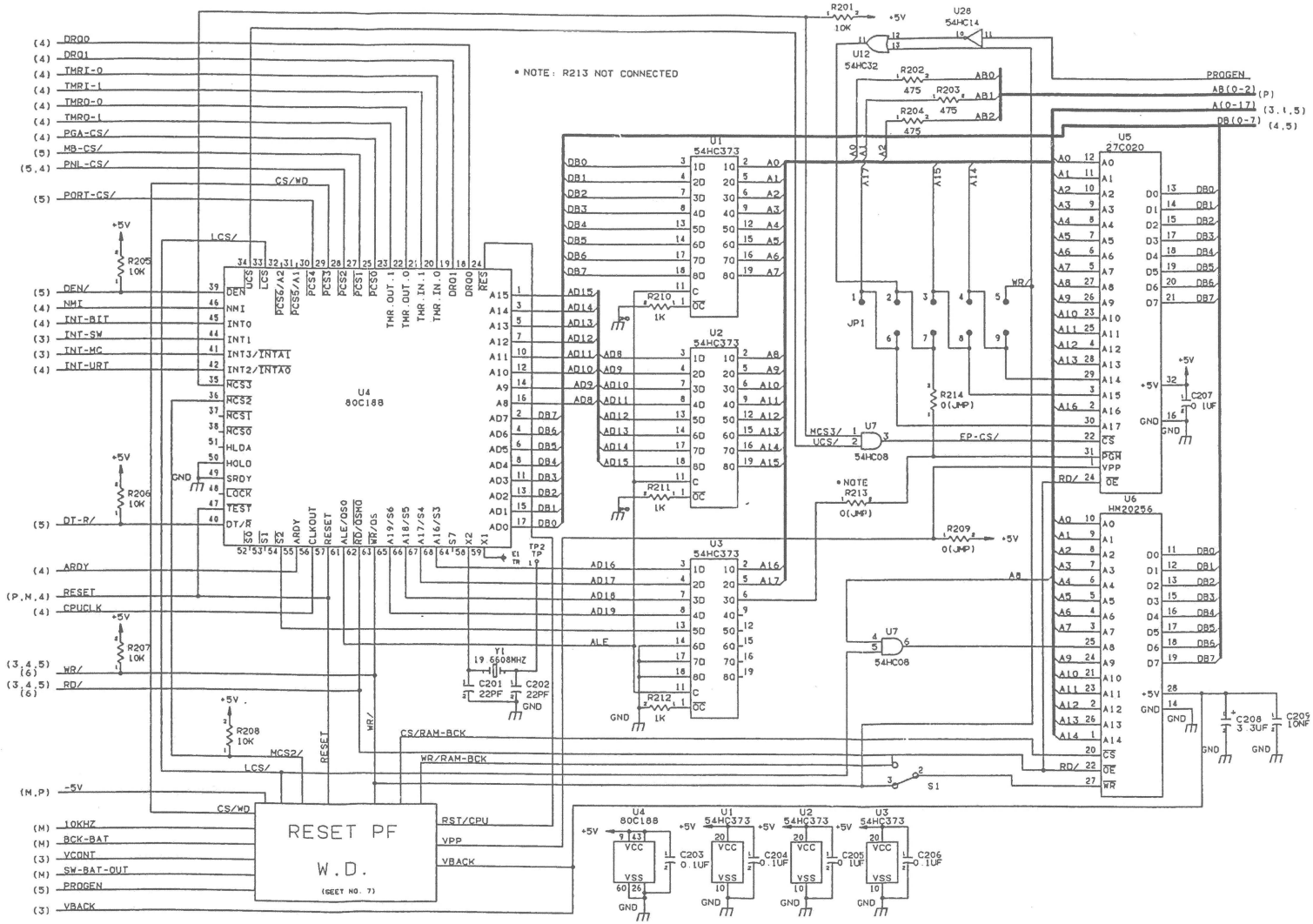


Figure 2-37A. Module MCU, CPU Circuit Schematic Diagram (Sheet 1 of 6)

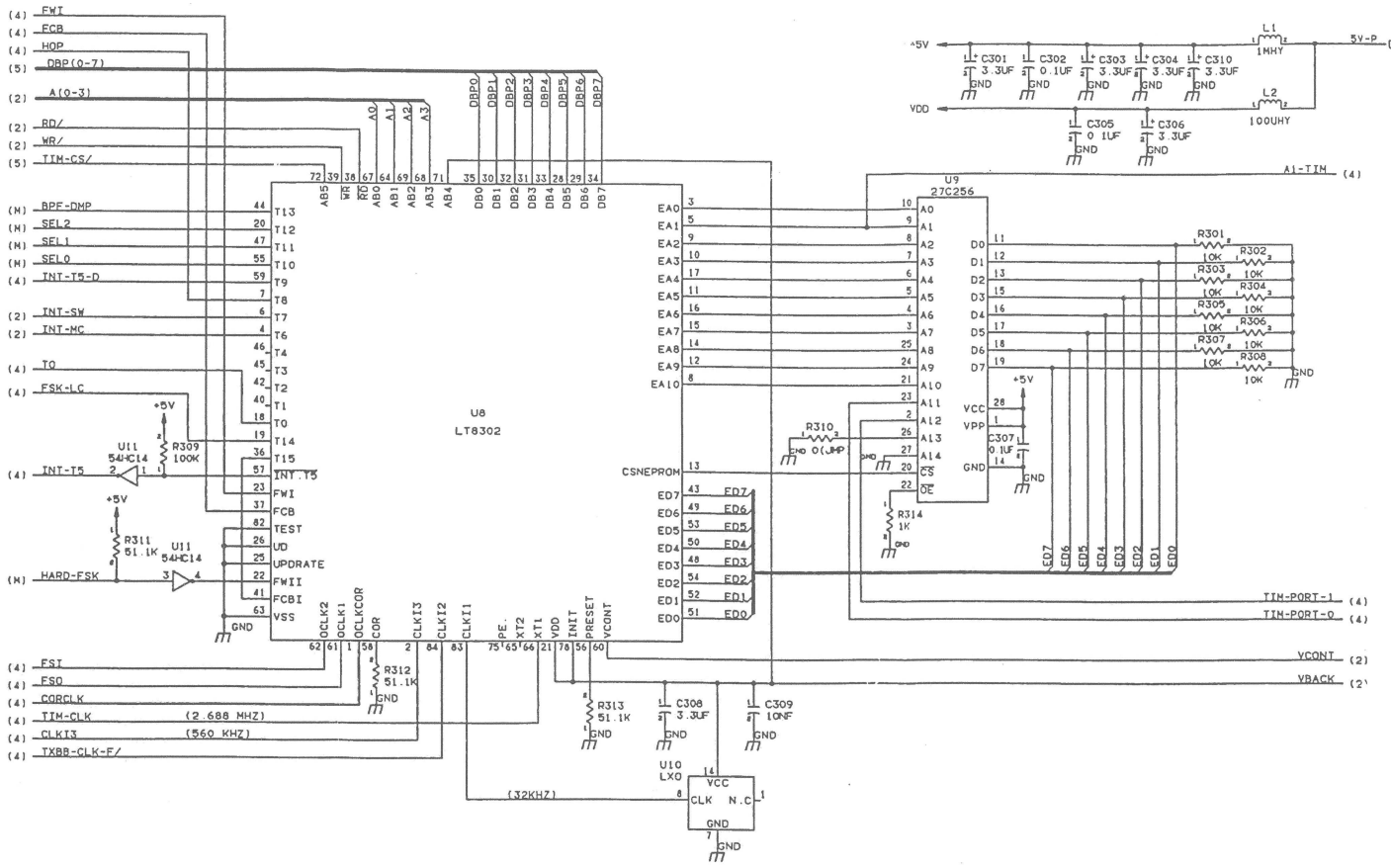


Figure 2-37B. Module MCU, TIMING Circuit, Schematic Diagram (Sheet 2 of 6)

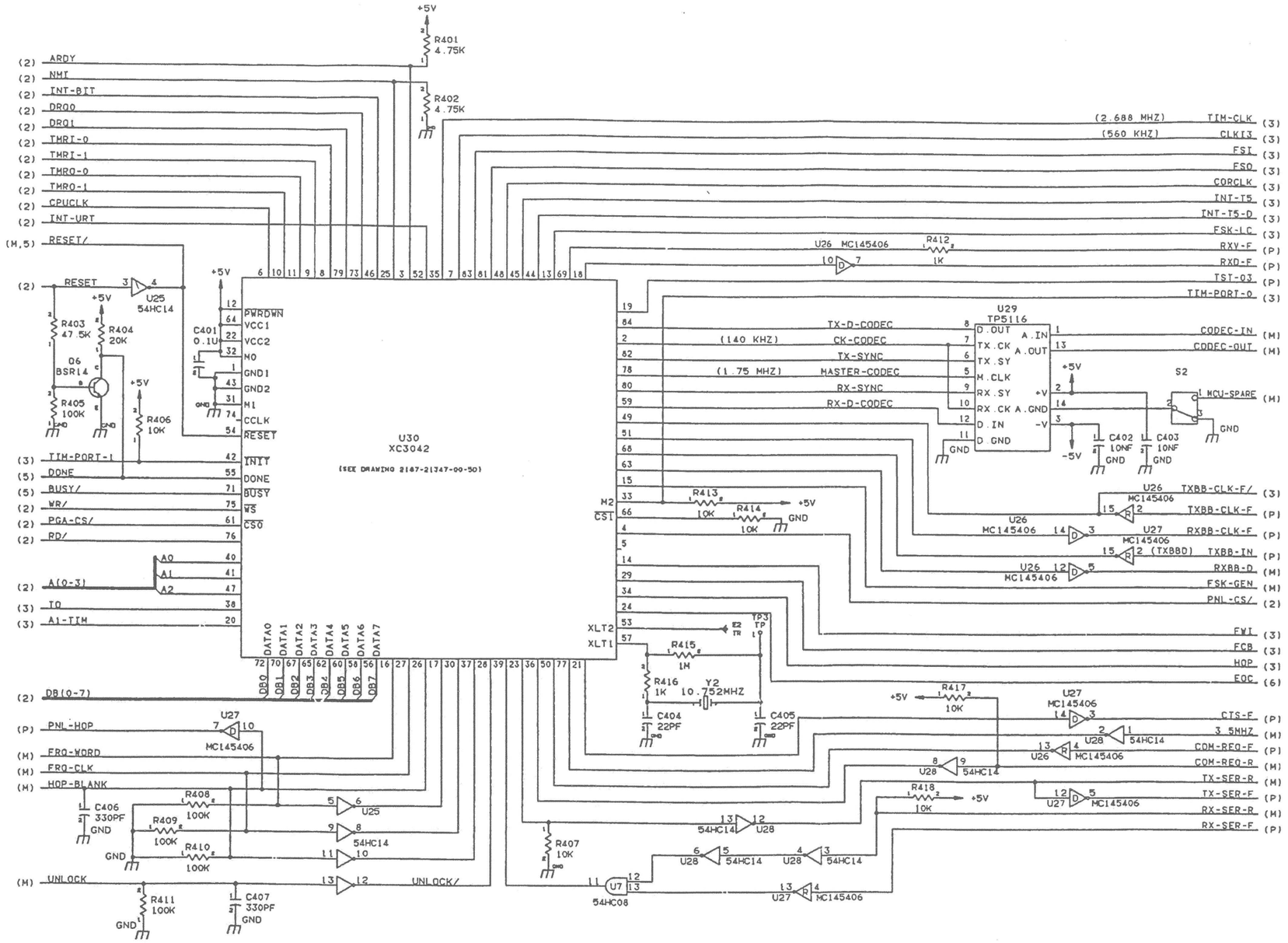


Figure 2-37C. Module MCU, PGA Circuit, Schematic Diagram (Sheet 3 of 6)

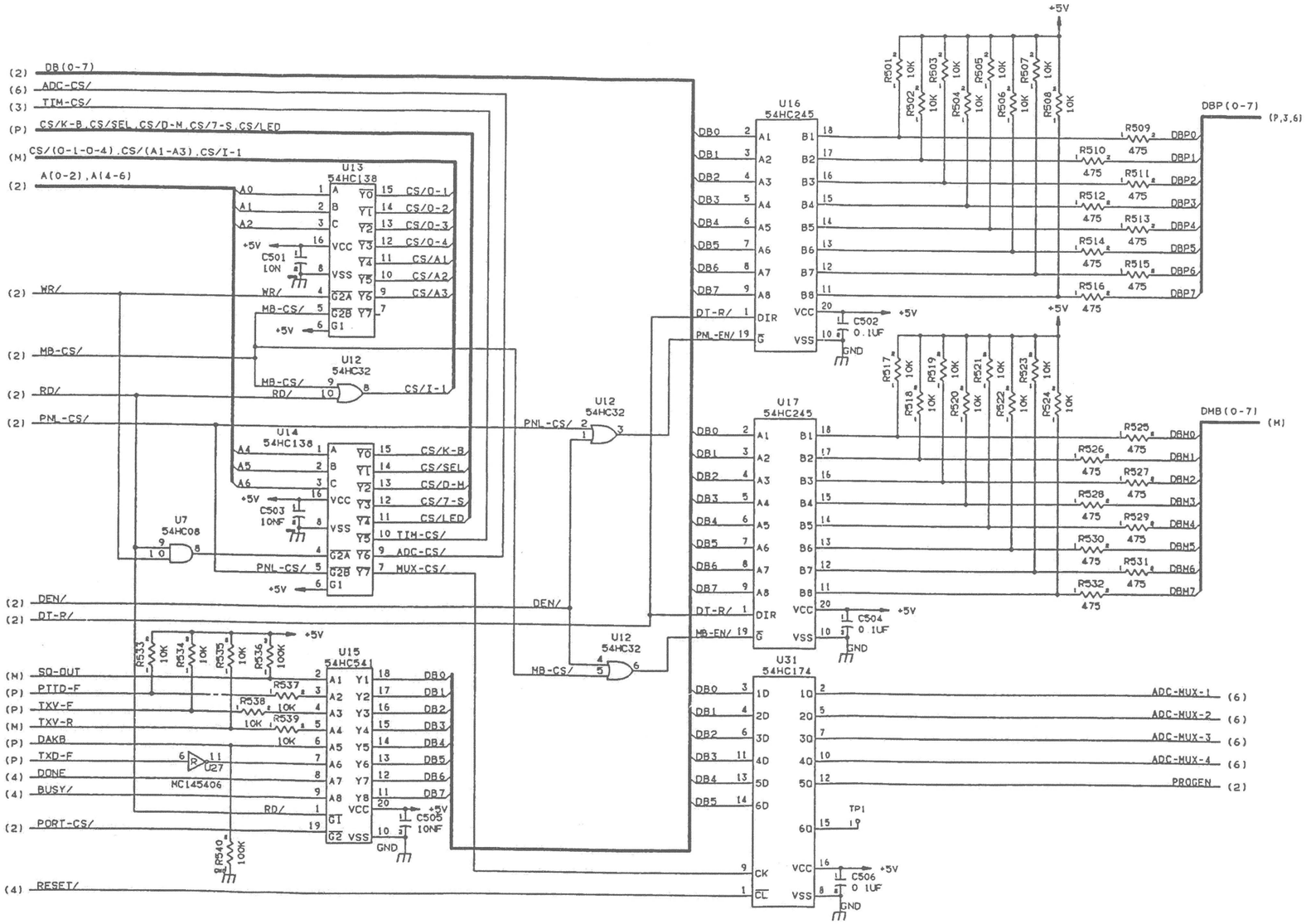


Figure 2-37D. Module MCU, I/O Circuit, Schematic Diagram (Sheet 4 of 6)

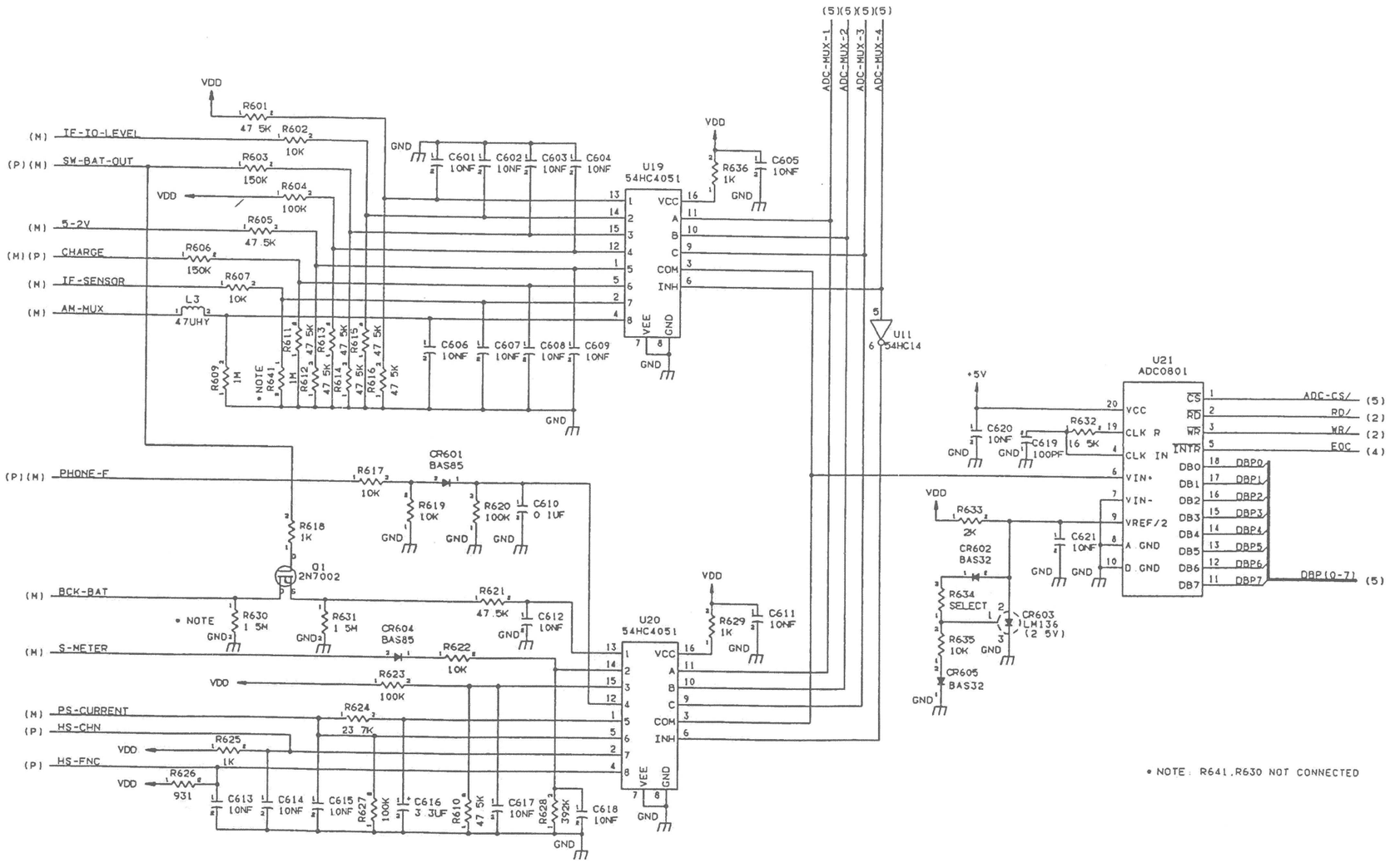


Figure 2-37E. Module MCU, ADC Circuit, Schematic Diagram (Sheet 5 of 6)

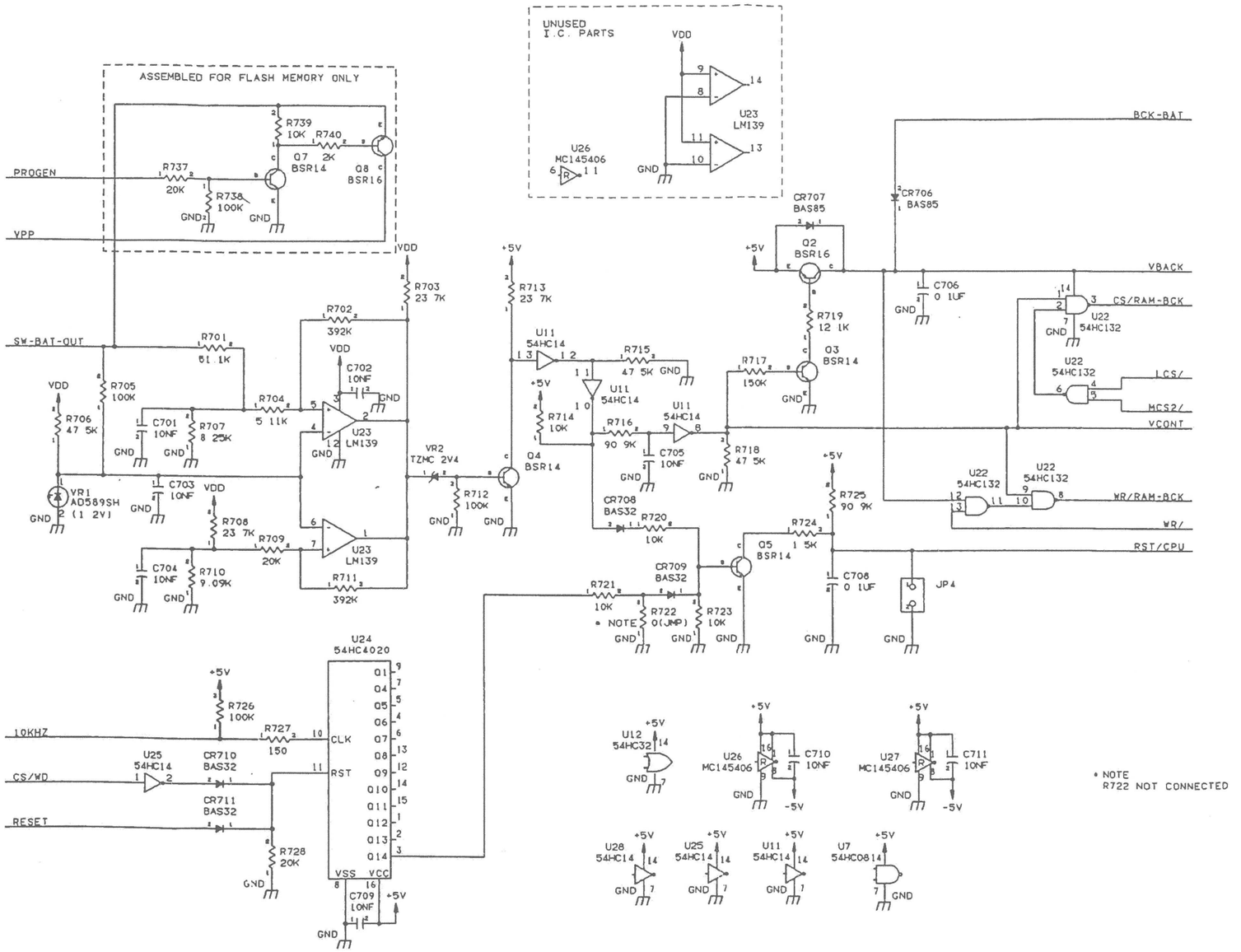


Figure 2-37F. Module MCU, PF Circuit, Schematic Diagram (Sheet 6 of 6)

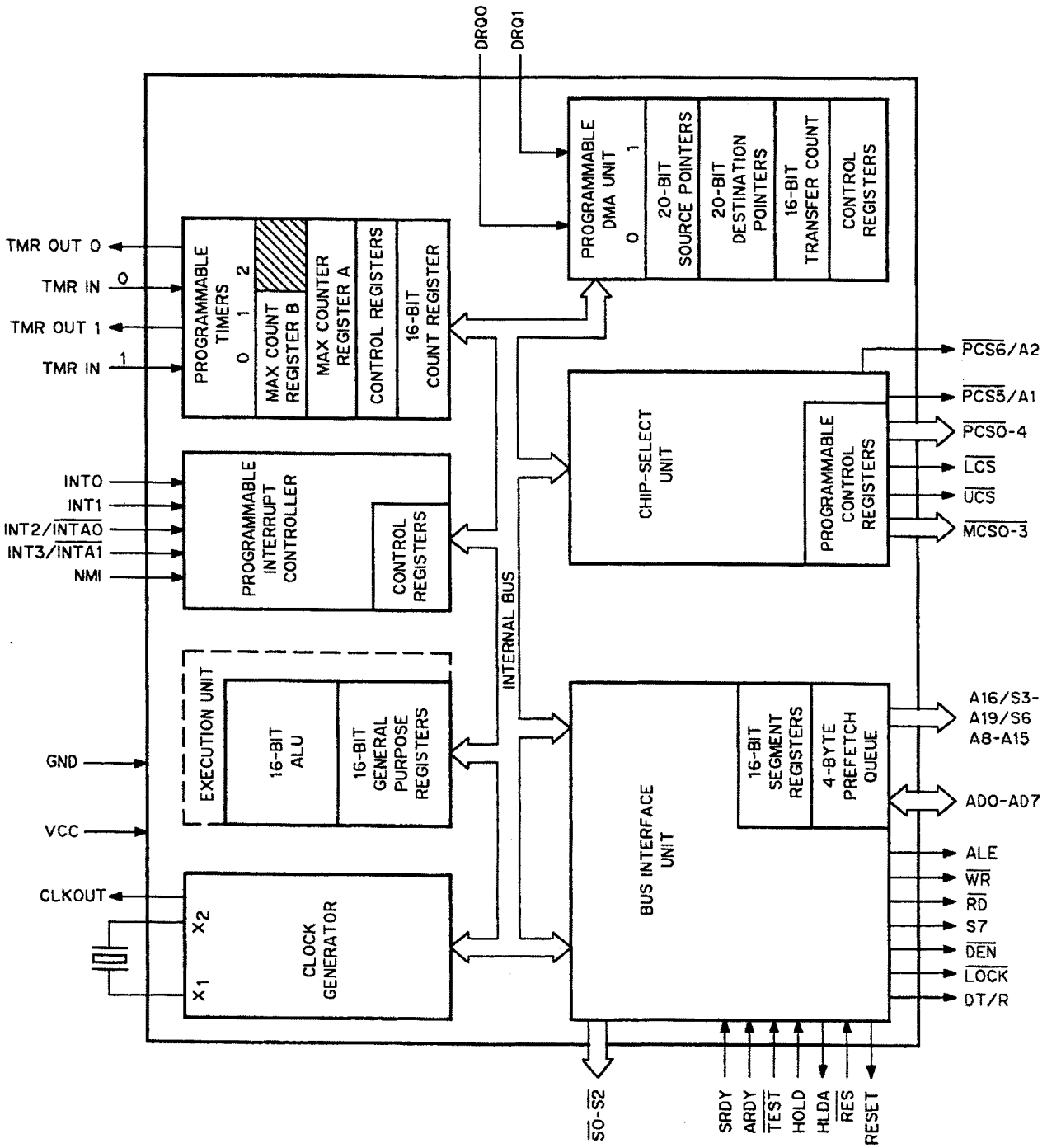


Figure 2-38. Microprocessor U4, Block Diagram

1. AD0 through AD7 - multiplexed address and data lines. The lower-order address byte (A0 through A7) appears on the bus during the first clock period of the machine cycle and are strobed into latch U1 on the rising edge of signal ALE generated by the microprocessor.

   During the following clock periods, lines AD0 through AD7 become a bi-directional data bus.

2. A8 through A15 - address lines. These lines provide the middle address byte, which is present throughout the instruction cycle.

3. A16/S3 through A19/S6 - multiplexed address/status lines.

   During the first clock period of the machine cycle, these lines provide the four higher-order address bits for memory operations cycle.

   During memory and I/O operations, status information is available on these lines during the following clock periods. In module MCU, the status lines are not used.

4. RD* - read pulse. This low level pulse appears during a microprocessor read cycle, after the address signals have stabilized.

5. RESET - reset output, indicates that the CPU is being reset. Can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the RES* signal. This line is applied to the watchdog circuit, to periodically reset its counter.

6. X1, X2 - crystal inputs. Connections for the 19.6608MHz crystal oscillator.

7. ALE - address latch enable pulse. This high-level pulse appears during the first clock period of each machine cycle. Signal ALE is used to latch the low-order address bits, into the latches U1, U2, U3.

8. WR* - write pulse. This low level pulse appears during a microprocessor write cycle, after the output data has stabilized.

9. DEN* - data enable output. The DEN* line, connected to the I/O circuit (U12), indicates that data is present on the data bus, and enables the U16, U17 transceiver.

10. DT/R* - data transmit/receive output. This signal selects the direction of data transfer through the transceivers U16, U17.

11. CLKOUT - Clock output, provides a 50% duty cycle waveform. All device pin timings are specified relative to CLKOUT. This clock output provides the CPUCLK signal.

12. RES* - System reset, causes the 80C188 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the 80C188 clock. The 80C188 begins fetching instructions approximately 7 clock cycles after RES* is returned HIGH. RES* is required to be LOW for more than 4 clock cycles and is internally synchronized. For proper initialization, the LOW-to-HIGH transition of RES* must occur no sooner than 50 microseconds after power up. When RES* occurs, the 80C188 drives the status lines to an inactive level for one clock period, and then switch them to the high-impedance state. This input receives the RST CPU signal from the power fail detector.

13. ARDY - Asynchronous ready, informs the 80C188 that the addressed memory space or I/O device will complete a data transfer. The ARDY input pin accepts an asynchronous input, and is active HIGH.

14. UCS* - Upper memory chip select is an active LOW output that appears whenever a memory reference is made to the defined upper portion (1K - 256K block) of memory. This line is not floated during bus HOLD. The address range activating UCS* is software programmable. This line provides the EP-CS* signal for U5.

15. LCS* - Lower memory chip select, is active LOW whenever a memory reference is made to the defined lower portion (1K - 256K block) of memory. This line is not floated during bus HOLD. The address range activating LCS* is software programmable. This line provides the CS/RAM-BCK signal for U6.

16. MCS0-3* - Mid-range memory chip select signals, are active LOW when a memory reference is made to the defined mid-range portion of memory (8K - 512K). These lines are not floated during bus HOLD. The address ranges activating MCS0-3* are software programmable. The MCS2* line provides an override CS for U6 (RAM), and the MCS3* line provides the EPROM chip select signal.

17. PCS0-4* - Peripheral chip select signals 0-4, are active LOW when a reference is made to the defined peripheral area (64K byte I/O space). These lines are not floated during bus HOLD. The address range activating PCS0*-4 are software programmable.

The functions of these signals are as follows:

- The PCS0* signal provides the PGA-CS*.

- The PCS1* signal provides the MB-CS* chip select signal, for the transceiver U17, which connects the internal bus to the to motherboard bus and the ports located on it, and to the AUDIO module.

- The PCS2* signal provides the PNL-CS* chip select signal, for the transceiver U16, which connects the internal bus to the panel bus and the ports located on it.

- The PCS3* signal is connected to the CS/WD line, used to periodically reset the watchdog circuit.

- The PCS4* signal provides the PORT-CS* input for U15.

18. TMRIN 0-1 - Timer Inputs, are used as time gate signals. These inputs are active HIGH and internally synchronized.

19. TMROUT0, TMROUT1 - Timer outputs, are used to provide single pulse or continuous waveform generation, depending upon the timer mode selected.

    The two timers are used to generate FSK tones.

20. DRQ0 or DRQ1 - DMA Request is driven HIGH by an external device when it requests a DMA channel (channel 0 or 1) to perform a data transfer. These signals are active HIGH, level-triggered, and internally synchronized.

    The two channels are used for transferring data between the codec and the RAM.

21. NMI - Non-Maskable Interrupt, an edge-triggered input which causes a type 2 interrupt. NMI is not maskable internally. A transition from LOW to HIGH initiates the

interrupt at the next instruction boundary. NMI is latch internally. An NMI duration of one clock or more will guarantee service. This input is internally synchronized.
This line is used by the PGA.

22. INT0 thru INT3 - Maskable Interrupt Requests, can be requested by strobing one of these pins. When configured as inputs, these pins are active HIGH. Interrupt requests are synchronized internally. INT2 and INT3 may be configured via software to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured via software to be either edge - or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged.

These four lines are used for the INT BIT, INT. SW, INT MC and INT URT interrupts.

(b) Timing of instruction execution (figure 2-39). The time required for the microprocessor to execute an instruction depends on the type of instruction and on the internal clock frequency of the microprocessor. An instruction cycle consists of three to five bus cycles.

A bus cycle is required each time the microprocessor accesses memory or an I/O circuit. Every machine cycle consists of at least four clock periods, i.e. requires at least 0.8us. The four clock periods are referred to as T1, T2, T3 and T4 (see figure 2-39).
The actual number of clock periods depends upon the instruction being executed and on the particular bus cycle. The address appears during T1, and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of data transfer on the bus during read operations.

Idle periods can occur between bus cycles. These are referred to as idle states (Ti) or inactive clock cycles. The processor uses these cycles for internal housekeeping.

The ALE signal is generated during the T1 period of any bus cycle. On the trailing edge of this pulse, a valid address and certain status information for the cycle can be latched. Figure 2-39 shows the basic system timing.

1. Read cycles. When reading, the ALE line assumes a low level and enables address latches outputs (U1, U2, U3). As a result, the data stored at the location indicated by the address applied to U1, U2, U3 appears on the data bus.

2. Reading from RAM/EPROM and other components addressed by the microprocessor. Reading from these components is controlled by the RD* signal. This signal assumes a low level during reading, and a high level at any other time. When reading, the low level on the RD* line enables the output of the selected component. As a result, the data stored at the selected component indicated by the address lines appears on the data bus.

3. Write cycles. Writing data to RAM and other outputs is controlled by the WR* signal. This signal assumes a low level during writing and a high level at any other time. The low level on the WR* line enables writing the bits appearing on the data bus line to the memory location indicated by the address lines (appearing at the outputs of the address latches U1, U2, U3).

(c) Address latches (U1, U2, U3). The microprocessor addresses the EPROM and RAM memories via 18 or 15 address lines, respectively, controlled by pins 1 thru 8 and 10 thru 17.

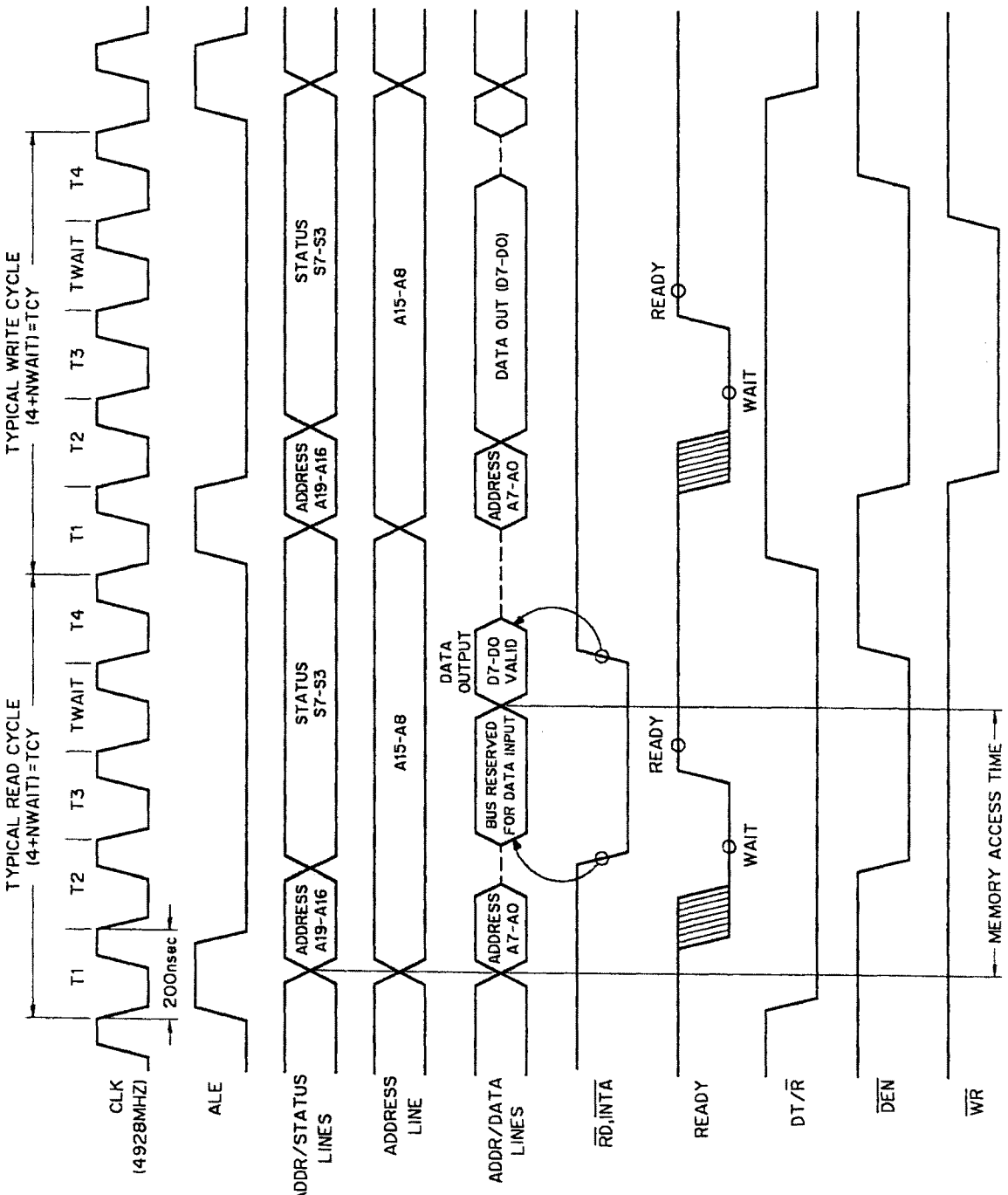


Figure 2-39. Microprocessor U4, Basic System Timing

1. The lower byte of the address appearing on the eight internal bus lines DB0 thru DB7, is latched into U1 when the ALE line (pin 61 of U4), connected to the C inputs (pin 11) of U1, U2 and U3, rises to a high level.

   The higher order address lines A8 thru A17 are also latched into U2 and U3 when the ALE line rises to a high level.

2. After the lower address byte is latched into U1, the internal data bus (lines D0 thru D7) is used for data transfer, while the full 18 bit address is now available on the latched address lines (A0 thru A17).

(d) Memories.

1. EPROM (U5). To read data stored in a specific EPROM location, the 18-bit address of that location is applied, via the address bus, to the address inputs (A0 through A17) of the EPROM. Since the address bus is connected to all the memory devices, the chip select signal by means of the gate (EP-CS*) generated by combining the UCS* and MCS3* signals U7 (pins 1, 2, 3) is applied to pin 22 of the EPROM, to enable the EPROM.

   When the chip-select signal applied to the EPROM falls to a low level, the data stored in the location pointed to by the 18-bit address appearing on the address bus, is made available at the EPROM outputs. When the RD* signal, applied to input pin 24 of the EPROM, falls to a low level, the microprocessor reads the data via the data bus.

   When the chip-select signal is high, the EPROM outputs assume a high-impedance state, thus allowing other data to flow on the data bus.

The timing diagram for a EPROM read cycle is shown in figure 2-39.

2. RAM (U6). Data can be written into, and read from the RAM U6. To write data into the RAM, the 15-bit address identifying a specific memory location is applied to the RAM address inputs A0 through A14.

A chip-select signal (CS/RAM-BCK) generated by the LCS* and MCS2* lines through the watchdog circuit is applied to the chip enable input CS* (pin 20). When a low level is applied to the CS* input, the RAM is enabled.

When the WR* signal, applied to input pin 27 of the RAM, falls to a low level, the address signals are latched into the RAM and the data appearing on the data bus is written into the RAM location pointed to by the latched address. Data is applied to the RAM via the bi-directional data bus DB0 thru DB7.

To read data from a RAM, the 15-bit address of the data storage location is applied to the address lines of the RAM. When the RD* signal applied to pin 22 of the RAM falls to a low level, the RAM outputs are enabled, and the stored data is applied on the data bus.

To preserve the stored data when the RT-2001 is turned off or does not receive power, the RAM is connected to a backup lithium battery, located on the AUDIO module (VBACK line).

(e) Initialization. The microprocessor starts program execution after receiving the +5V supply voltage on the VCC line (pin 9), and after reception of the power-up reset pulse RST/CPU from the power-up circuit to pin 24-RES*.

(2) Power up/down detector and watchdog circuit (figures 2-37F and 2-37A).

(a) Power up/down detector. The power up/down detector comprises the comparators U23-2 and U23-1, the reference diode VR1, the transistor Q4 and the inverter U11-12.

1. The circuit monitors the battery voltage provided by module PS on the SW BAT OUT line and the VDD line (+5V). The battery voltage is applied to the non-inverting input (pin 5) of the comparator U23-2, via the voltage dividers R701, R707, and the +5V voltage is applied to the non-inverting input (pin 7) of U23-1 via the voltage divider R708, R710.

The inverting inputs of the two comparators receive 1.2V from the reference diode VR1. The current through the diode is provided by resistor R705 (for rapid setup of the reference voltage upon turn-on) and by R706 (from the +5V power supply).

Upon turn-on, before the applied voltages exceed threshold voltage, comparator outputs are at a low level, therefore transistor Q4 is cut-off.

As a result, the CS/RAM BCK line is at a high level, the output of inverter U11-12 and VCONT line are both at low levels and therefore RST/CPU line is also low. This generates a reset command to the microprocessor U4.

2. After the battery voltage (SW BAT OUT line) and the regulated +5V supply voltage stabilize at their nominal values, the two comparators generate a high level which causes Q4 to saturate.

Diode VR2 prevents Q4 from saturating when the output voltage of the comparators is less than about +3V. When Q4 saturates, the following occurs:

a. Capacitor C705 discharges via resistor R716. After approximately 1 millisecond, the output of inverter U11-8 rises to a high level.

   This high level is applied to the gate U22-3: when the LCS* or MCS2* lines are at a low level, U22-3 enables RAM (U6) operation by means of a low level on the CS/RAM-BCK line. The VCONT line assumes a high level, which enables the operation of U8 (TIMING LSI).

b. The output of inverter U11-10 falls to a low level, therefore transistor Q5 cuts-off. Capacitor C708 charges via R725, and the output voltage on the RST/CPU line increases. After approximately 30 milliseconds, the RST/CPU rises to a high level and the microprocessor can start normal operation.

3. As long as the supply voltages remain normal, the output of U11-12 remains at a high level.

When power is removed, the output of U11-12 falls to a low level. C705 charges via R716, therefore the VCONT line falls to a low level after approximately 1 millisecond delay.

In addition, transistor Q5 saturates and capacitor C708 discharges via R724, therefore the RST/CPU line falls to a low level after approximately 100 microseconds and the microprocessor is reset.
In addition, the CS/RAM-BCK line rises to a high level, therefore the RAM is inhibited and its contents are then preserved by the backup battery.

(b) Power-fail controller. The power-fail controller comprises the inverter U11-8, the transistors Q2 and Q3 and the diodes CR706 and CR707.

(c) Watchdog circuit. The watchdog circuit comprises the 14-stage binary counter U24 and gate U25-2, and the resistors R726, R727, R721, CR711, CR710, R728.

1. During normal operation, the counter counts the 10kHz clock pulses arriving from the SYNT module, via resistor R727.

   The microprocessor can reset the watchdog counter by applying a low level pulse on the CS/WD line. This pulse passes via the inverter U25-2 to the reset input of the counter U24.

   U24 is also reset when a high level pulse is applied on the RESET line arriving from the microprocessor.

2. During normal operation, the counter is periodically reset. Thus, the Q14 output never assume a high level. If the normal execution of microprocessor software is disrupted, the reset pulse will not appear, and the output of U24 (Q14) will rise to a high level 800 milliseconds after the last CS/WD pulse. This high level passes via Q5 to the RST/CPU input of the microprocessor. The microprocessor is reset, and it returns to normal operation.

(3) I/O circuit (figure 2-37D). The I/O circuit comprises two transceivers, U16 and U17, two ports, U15, U31, and two selectors U13, U14.

(a) Transceivers. The transferring direction of U16, U17 is determined by the DT/R line applied from the microprocessor.

U17 connects the internal data bus (DB0-7) to motherboard on the DMB0-7 lines. U17 is enabled by MB-CS* and DEN* lines applied from the microprocessor via OR gate U12-6. U16 connects the internal data bus (DB0-7) to panel on the DBP0-7 lines. U16 is enabled by PNL-CS* and DEN* lines applied from the microprocessor via OR gate U12-3.

The transceivers allow quick disconnection of the internal data bus from slow components located on panel, and disconnection of buses which are not used.

(b) Input port. U15 is an input port, enabled by the PORT-CS* and RD* signals, applied from the microprocessor. This port latches indication signals received from module AUDIO (SQ-OUT), from the panel and from the PGA (DONE, BUSY) and transfers them to the internal data bus (DB0-7) when the port is enabled.

The signal functions are as follows:

1. SQ OUT - indicates the state of the syllabic squelch circuit, located on the AUDIO module.

2. The PGA status is indicated by two signals: the DONE signal, which appears after correct initialization of the PGA, and the BUSY* signal which appears when the PGA is busy and cannot accept commands.

3. The other signals determine the communication status, in accordance with the state of the various PTT lines.

4. DAKB - indicates that a key has been pressed on the front panel.

(c) Output port. U31 is an output port enabled by the MUX-CS* signal generated by the CS generator (U13-7). U31 can be cleared by the RESET signal from the microprocessor (applied to pin 1). When the port is enabled, U31 transfers the information appearing on the internal data bus lines DB0 thru 5 to its outputs lines, Q1 thru Q5.

The information transferred by U31 includes:

* The ADC-MUX 1 thru 4 lines, which are applied to the multiplexer comprising U19 and U20. These lines control the selection of the input signal applied to the A/D converter for measurement.

* The PROGEN signal, which is applied to the EPROM U5 (figure 2-37A) as an optional program enable signal.

(d) CS generator. The CS generator circuit consists of the selectors U13 and U14. These selectors generates various chip select signals which are determined by the input select lines A, B, C.

The chip select signals control ports on the AUDIO modules for components on the motherboard and on the panel, and for components on the MCU module.

1. U13 is enabled by the WR* and MB-CS* signals, and the low address lines A0, A1, A2 used as the input select lines A, B, C.

Table 2-13. Address Decoder U13, Chip-Select Signals

Address Lines (U3 Select Inputs)			Low U3 Output	Connected to	Enabled Circuit or Function
A2 (pin 3)	A1 (pin 2)	A0 (pin 1)			
0	0	0	Pin 15 - CS/0-1	Motherboard	Controlling latch U1 on motherboard
0	0	1	Pin 14 - CS/0-2	Motherboard	Controlling latch U2 on motherboard
0	1	0	Pin 13 - CS/0-3	Motherboard	Controlling latch U3 on motherboard
0	1	1	Pin 12 - CS/0-4	Motherboard	Controlling latch U4 on motherboard
1	0	0	Pin 11 - CS/A1	Module AUDIO	Controlling latch U25 on AUDIO module
1	0	1	Pin 10 - CS/A2	Module AUDIO	Controlling latch U26 on AUDIO module
1	1	0	Pin 9 - CS/A3	Module AUDIO	Controlling latches U27, U28 on AUDIO module
1	1	1	Pin 7 - not used	-	-

2. The CS/I-1 is generated by the logic OR operation between the RD* and MB-CS* signals, performed by gate U12-8. This line selects input port U5 on motherboard.

3. U14 is enabled by the WR*, RD* (combined by AND gate U7-8) and PNL-CS* signals. Its input select lines A, B, C are connected to address lines A4, A5, A6.

Table 2-14. Address Decoder U14, Chip-Select Signals

Address Lines (U14 Select Inputs)			Low U14 Output	Connected to	Enabled Circuit or Element
A6 (pin 3)	A5 (pin 2)	A4 (pin 1)			
0	0	0	Pin 15 - CS*KB	Panel	Keyboard
0	0	1	Pin 14 - CS*SEL	Panel	Selectors
0	1	0	Pin 13 - CS*DM	Panel	Dot-matrix display
0	1	1	Pin 12 - CS*7-S	Panel	Seven-segment display
1	0	0	Pin 11 - CS*LED	Panel	LEDs
1	0	1	Pin 10 - TIM-CS*	U8-72 (module MCU)	TIMING LSI
1	1	0	Pin 9 - ADS-CS*	U21-1 (module MCU)	A/D converter
1	1	1	Pin 7 - MUX-CS*	U31-9 (module MCU)	Output port

(4) Timing circuit (fig. 2-37B and 2-40). The timing circuit comprises the TIMING LSI, U8, and the EPROM, U9.
Figure 2-40 shows the block diagram of the TIMING LSI.

(a) The TIMING LSI comprises the following functional blocks:

1. Bus interface. This circuit interfaces between the data bus lines arriving from the microprocessor to the internal circuits of the TIMING LSI.

2. PLL. The PLL circuit comprises the oscillator and the digital PLL. The oscillator uses the 2.688MHz TIM CLK signal provided by the PGA circuit to drive the digital PLL and to generate the CLK COR signal.
The digital PLL generates the F1 (1344kHz) and 128Hz clock signals, phase-locked to one of the clock signals on the CLKI1, CLKI2, CLKI3 lines (when power is on, the reference clock is CLKI2[when power is off, CLKI1 is selected).

* The CORCLK signal is applied to the PGA U30.
* The F1 and 128Hz signals are applied to the UPDATE and TOD circuits, respectively.
* The 32kHz clock signal from the LXO is connected to the CLKI1 line.
* The TXBB-CLK-F transmit clock signal from the AUDIO module is connected to the CLKI2 line.
* The 560kHz clock signal from the PGA U30 is connected to the CLKI3 line.

When power is disconnected from the MCU module, the PLL circuit receives only the 32kHz clock signal (CLKI1) and generates the 128Hz signal for the TOD circuit.

3. TOD. The TOD circuit maintains the time-of-day information by counting the 128Hz clock pulses from the PLL. The TOD information can be updated according to CPU commands, upon operator request, or upon reception of more accurate TOD information from another PRC-2200.

4. UPDATE. The UPDATE circuit receives the F1 clock signal from the PLL and generates the F2 and F2* clock signals (512kHz each), whose phases are corrected and updated according to the CPU commands. In this way, all the

clock and timing signals derived from the F2 and F2* clock signals, can be phase-shifted according to data received from the CPU.

5. TIMING 1. The first timing circuit receives the F2* clock signal from the update circuit and generates the T0 thru T15 signals. The timing of the T0-T15 signals is determined by the data stored in one of the four 2 kbyte pages of the EPROM U9. The timing circuit generates address signals EA0-EA10, applied to the EPROM A0-A10 address lines.

The data stored in the EPROM location pointed to by the address lines is applied to the ED0-ED7 inputs of the timing circuit. This data indicates the actual state (high or low) of the T0 thru T15 outputs and the number of F2* clock cycles that must elapse until the next change of state at one or more outputs.
After the required number of F2* clock cycles has elapsed, new data is read from the EPROM.

At the end of the waveform cycle, the timing circuit executes a "loop" to the first address of the cycle.

Thus, predetermined waveform patterns appear at the T0-T15 outputs, according to the data stored in the EPROM U9. Several waveform patterns (frames) may be smoothly switched on-line.

a. The T0 output is connected to PGA (U30) for generating the TIM-PORT-0, TIM-PORT-1 signals.

b. The T1 thru T4 outputs are internally connected to the TIMING 2 circuit.

c. The T5 output is connected via the inverter U11-2 and the INT T5 line to the PGA U30 input for generating the INT BIT (fig. 2-37B).

d. The T6 output, designated INT MC, is connected to the microprocessor.

e. The T7 output, designated INT SW, is connected to the microprocessor.

f. The T8 output, designated HOP, is connected to the PGA U30. This line provides the strobe signal accompanying the frequency data applied to the SYNT module.

g. The T9 output, designated INT-T5-D, is connected to the PGA U30 for generating the INT BIT.

h. The T10-T12 outputs, designated SEL0 thru SEL2, are connected to the select inputs of module AUDIO input selector.

i. The T13 output, designated BPF DMP, is connected to the AUDIO module for discharging the four FSK detectors, and to the select input of U3.

j. The T14 output, designated FSK LC, is connected to a D flip-flop in PGA (U30), which generates the control signals TMRI0 and TMRI1 for the microprocessor. These signals switch between the two timers, that generate the FSK tones.

k. The T15 output drives the FCBI clock input of the second timing circuit, TIMING 2.

6. TIMING 2. The second timing circuit receives the F2 clock signal from the update circuit and the signals T1 thru T4, and T15 from the TIMING 1 circuit. TIMING 2 generates the following signals: CLOCK 02, CLOCK 01, FCB and FWI, and receives the PWII signal.

FCB & FWI are freq bus

a. The CLOCK 02 and CLOCK 01 outputs are connected via the FSI and FSO lines to the PGA. The PGA generates the timing signals used for data transfer from the codec to the RAM and vice-versa.

b. Outputs FCB, FWI are connected to the PGA U30. These lines carry the frequency data and clock signals and are part of the frequency bus.

c. The FWII input line is connected to the HARD FSK line, arriving from the AUDIO module, through the inverter U27/4. The TIMING LSI reads via the HARD FSK line the signal appearing at the output of the FSK detector/-comparator located on the AUDIO module.

(b) The EPROM contains four 2 kbyte pages. The CPU selects a page using the TIM PORT 0 and TIM PORT 1 output lines of the PGA. These lines are connected to the address inputs A11 and A12 of the EPROM U9.

(c) When power is disconnected from the MCU module, the power-fail controller supplies an operating voltage from the lithium battery for the TOD and for part of the PLL circuits via the VBACK line.
TOD information is protected against accidental modification during the transition from normal to low-power operation.

(d) Low-power oscillator (LXO) (fig. 2-37C). The LXO provides a 32kHz clock signal for the timing circuit. Power is supplied to the LXO from the power-fail controller, via the VBACK line.

(5) Analog signal measurement circuit (fig. 2-37E). This circuit is built around the multiplexers U19 and U20, and A/D converter U21.

(a) Signal selection. The measured signal is selected by means of the multiplexers U19 and U20. U19 and U20 are controlled

by the microprocessor via the control lines ADC-MUX1-4, applied through the output port U31 (fig. 2-37D).

To measure a specific signal, the microprocessor sends first an enable command via the output port U31 to one of the two multiplexers, via the ADC-MUX-4 control line. When ADC-MUX-4 is at a low level, the INH* input of U19 receives a low level, therefore U19 is enabled. When ADC-MUX-4 is at a high level, U20 is enabled.

While the microprocessor selects the required multiplexer, it also applies the appropriate selection code via the ADC-MUX1-3 lines, to select one of the 8 analog signals connected to the selected multiplexer inputs.

(b) The output of the multiplexer (pin 3) is connected to the analog input VIN+ (pin 6) of the A/D converter U21. The A/D converter starts the conversion when the microprocessor sends a low level on the ADC-CS* line, via the CS generator U14-9 (fig. 2-37D). At the same time, the microprocessor applies a low level on the WR* line.

(c) When the conversion is started, U21 pulls the INTR* (EOC line) output to a high level, to indicate that conversion is in process. When the conversion ends, the A/D converter provides a low level at the INTR* output. This low level is sent via the EOC line to the PGA, which then transfers the signal, via the PGA to the microprocessor. This signal indicates that the microprocessor can read the data from U21.

(d) In response, the microprocessor applies a low level on the ADC-CS* and RD* lines. This low level is connected to the RD* input (pin 2) of U21. As a result, the data outputs of U21 (pins 11 thru 18) are enabled and the data word appearing at the A/D converter output is sent to the microprocessor via the data bus.

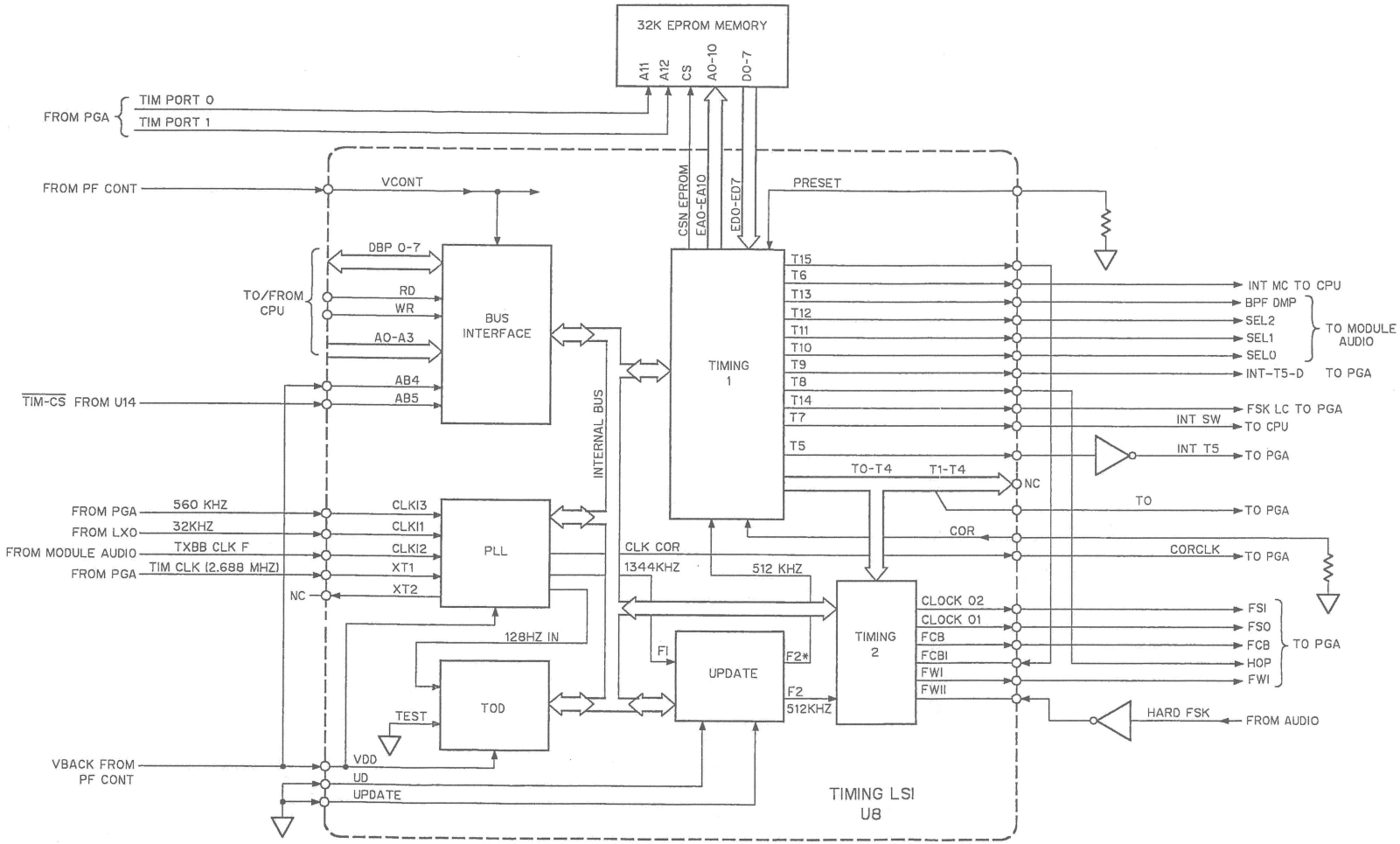


Figure 2-40. TIMING LSI U8, Block Diagram

(e) An accurate reference voltage of 2.5V is connected to pin 9 of U21. This voltage is provided by the circuit built around 2.5V reference diode CR603. CR602 and CR605 are temperature-compensation diodes. R634 is selected to obtain an accurate 2.5V voltage.

(f) The analog signals which can be measured by the microprocessor are listed below. The signals applied to U19 are connected via voltage dividers.

1. +5V MCU module supply voltage.

2. IF IO LEVEL voltage from module IF.

3. Battery voltage (SW BAT OUT) from module P.S.

4. 5 - 2V supply voltage generated by the TX power supply in module PS, through CP-2003.

5. CHARGE line from the RMT/DATA connector.

6. IF-SENSOR line from module IF.

7. AM MUX signal, selected by means of the BIT multiplexer in module AM.

8. PHONE-F line from module AUDIO. The audio signal arriving on this line is attenuated by R617, R619 and peak-rectified by CR601, R620 and C610.

9. Voltage of backup battery (BCK BAT). When the RT-2001 is turned on (+12V at the SW BAT OUT line), the FET Q1 conducts and the BCK BAT line is applied via R621 to pin 13 of U20. When the unit is turned off, Q1 cuts off and no current is drawn from the backup battery.

10. S-METER (received signal strength) line from module IF.

11. PS CURRENT from module PS.

12. HS CHN and HS FNC lines from module PANEL. When the H-739 handset is connected to the RT-2001, these two lines carry DC voltages which indicate that a control handset is connected, and the positions of the channel and function switches located on the handset. These voltages are decoded by the microprocessor and used as control information, instead of the commands received by setting the corresponding front-panel controls.

(6) Codec (fig. 2-37.C, and 2-41). The codec U29 (fig. 2-37.C) operates as an interface between the AUDIO module and the PGA, U30.

The block diagram of the codec circuit is shown in figure 2-41. The codec contains A/D and D/A circuits, designed for optimal processing of speech. The transmit path uses the A/D section of the codec to convert the analog input signal to digital data. The analog signal is applied from module AUDIO to pin 1 of the codec U29. The analog signal is sampled and converted to u-law encoded PCM data, appearing at pin 8. The codec conversion clock, used by both the transmit and the receive paths, has a frequency of 140kHz. The clock signal is applied from the PGA to pins 7 and 10 of U29, via the CK-CODEC line.

The PCM data is sent to the PGA U30 via the DATA OUT line. Data transmission is synchronized by means of the TXSYNC pulses applied to pin 6. The TXSYNC pulses are provided by the PGA U30.

The processed data, returning from the PGA via the DATA IN line, is applied to the D/A section of the codec via pin 12. The data is converted back to an analog signal. Data transfer from the PGA is synchronized by means of RXSYNC pulses applied from the PGA to pin 9.

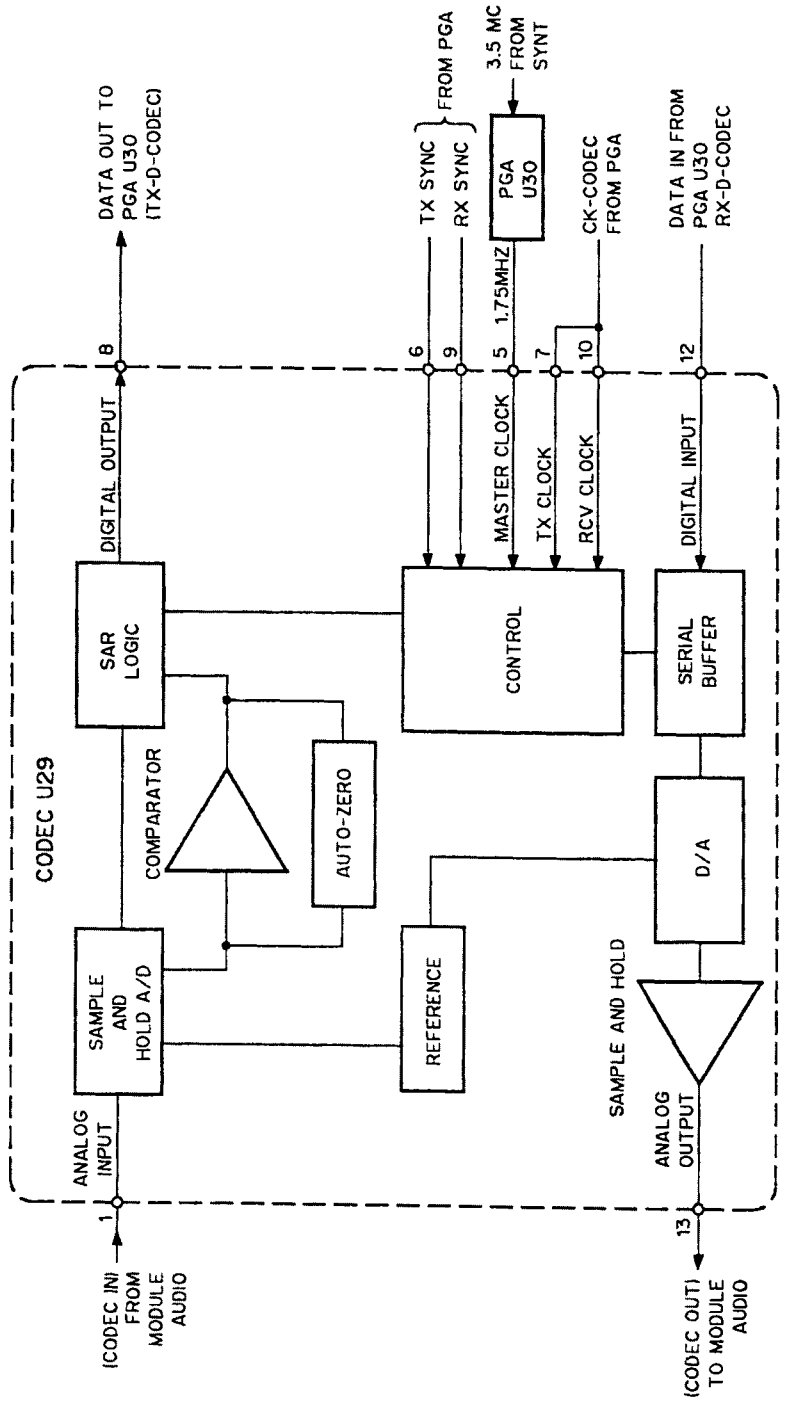


Figure 2-41. Codec U29, Simplified Block Diagram

The master clock used to operate the internal A/D and D/A sequencers is provided from the SYNT module, via the 3.5 MC line. The 3.5 MHz clock received via this line is divided by two in the PGA U30. The resulting 1.75 MHz clock signal is applied to pin 5 of U4, via the MASTER_CODEC line.

(7) Communication interface (fig. 2-37C). This circuit provides an interface for the serial communication signals arriving from the CP-2003, and for the external user connected to the front panel RMT/DATA connector.

The inverters U26 and U27 marked by an R receive RS-232 levels (±5V) and convert them to 0V and 5V levels. The inverters marked by a D make the opposite conversion.

(a) Receive path.

1. The serial data from the CP-2003 is applied via the rear connector to the RX-SER-R line. The data is applied by the two Schmitt trigger inverters U28-4 and the U28-6 to the serial input line (PIN 39) of the PGA, via the AND gate U7-11.

2. The serial data arriving from the front panel RMT/DATA (RX-SER-F) connector at RS-232 levels is converted into the internal +5/0V levels by U27-13. The converted data is driven by U7-11 to the PGA, via the serial input line (pin 39).

(b) Transmit path. The serial data from the PGA (pin 23), is buffered by U28-12 and sent to one of the following destinations:

1. To the CP-2003 via the TX-SER-R line.

2. To the input of the inverter U27-5. The inverter

converts the internal levels to RS-232 compatible levels (±5V) and applies the data to the front panel RMT/DATA connector via the TX-SER-F line.

(8) Serial communication channel operation (figure 2-37C). The serial communication channel is implemented by means of an asynchronous half-duplex receiver/transmitter (UART). This UART is used for communication between the microprocessor in RT-2001, the CP-2003 and an external user connected to RMT/DATA connector. The output data is transmitted serially via the TX-SER-R/F lines and serial input data is accepted at the RX-SER-R/F inputs. The data word frame contains 10 bits: one start bit, eight data bits and one stop bit. The processing clock is 140 kHz.

(a) Transmission. The CPU writes the data to be transmitted into the shift register serving the PGA. In the first stage, the start bit is transmitted. In the second stage, the shift register receives a shift instruction, and data loaded into the shift register is transmitted on the TX-SER-R/F lines, starting with the least significant bit (LSB). After ending data bit transmission, the stop bit is transmitted.

After transmitting the stop bit from the shift register, the PGA transmits an NMI interrupt to the CPU, and then the CPU writes a new data word.

(b) Reception. The process begins when a high-to-low transition appears at one of the RX-SER-R/F inputs. The RX-SER-R/F input is sampled three times during each receive clock cycle, to confirm the signal level. The received bit is determined by majority voting, i.e., according to the level of the input signal detected during at least 2 out of the 3 samples taken during one receiver clock cycle.

1. If during the reception of the start bit, the majority decision is that the signal is high, the receive process

is aborted and will restart after detecting the next high-to-low transition in the input signal level.

2. After the detection of a valid start bit, the bit detected during the following receive clock cycle is loaded into the receive shift register of the PGA.

3. The process of bit reception and loading into the receive shift register repeats itself until all the data bits are received.

After receiving one additional bit (the stop bit), the PGA transmits an NMI interrupt to the CPU, and the CPU reads the data stored in the receive shift register.

(9) Programmable gate array (PGA - U30) (figure 2-37C, 2-42 and figure 2-43 A thru K). Figure 2-42 describes the functional interconnection diagram and the figures 2-43A through 2-43K describe the ten functional blocks (designated 2 through 11 in figure 2-42) of the PGA.

(a) Block 2 - PGA-CS (fig. 2-43.A). This block receives from the microprocessor three address lines A0, A1, A2 (pins 40, 41, 47), the RD* and WR* signals (pins 76, 75) and the PGA-GS* signal from the CS generator (pin 61). These signals are used to generate internal chip select signals for reading from the ports R0-R7 and for writing to ports W0-W7.

(b) Block 3 - CODEC (fig. 2-43.B). This block simultaneously converts the transmit and receive data from serial to parallel and from parallel to serial format, and provides buffering of parallel data. This block performs the connection between the RAM serving the microprocessor and the codec U29, and therefore serves as the gateway through which digital signal processing is introduced in the transmit and receive signal paths. This operation is controlled by a DMA mechanism.

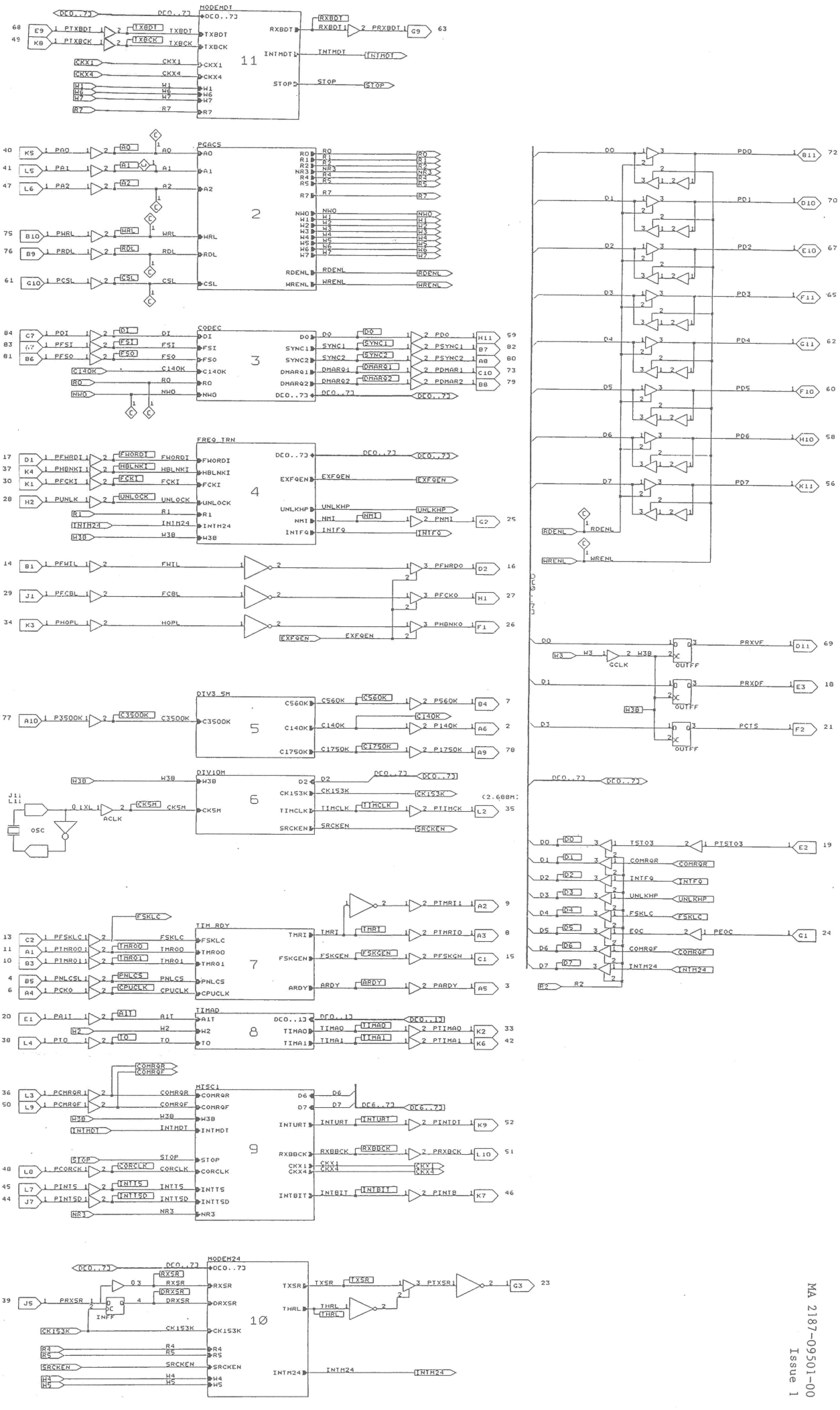


Figure 2-42. PGA, U30 - Functional Interconnection and Connector Wiring

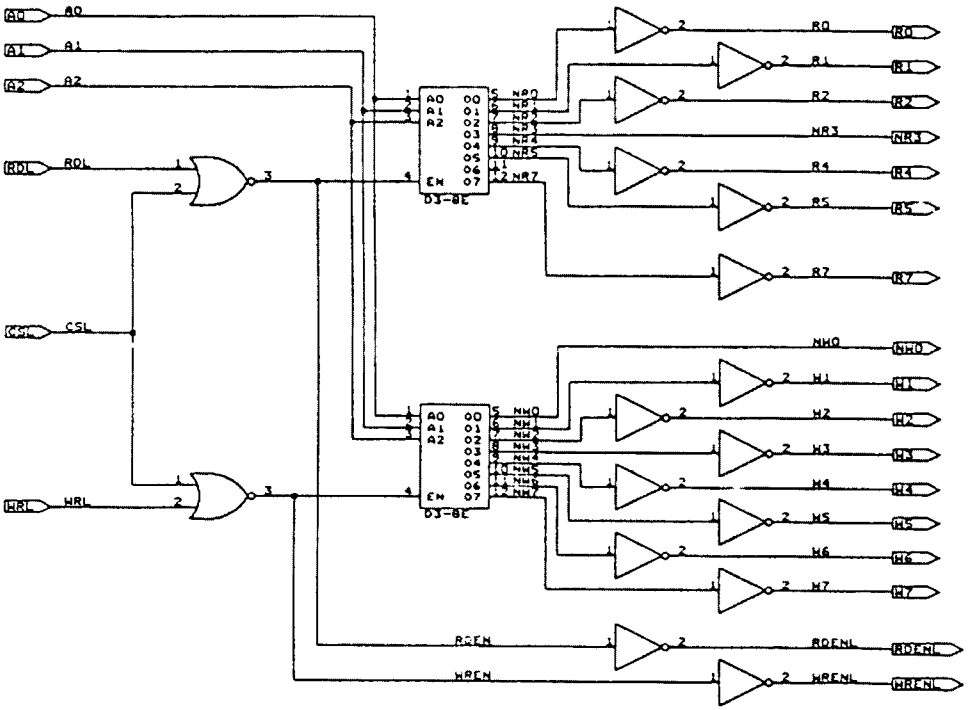


Figure 2-43A. PGA, U30 - PGA-CS Section, Schematic Diagram (Sheet 1 of 10)

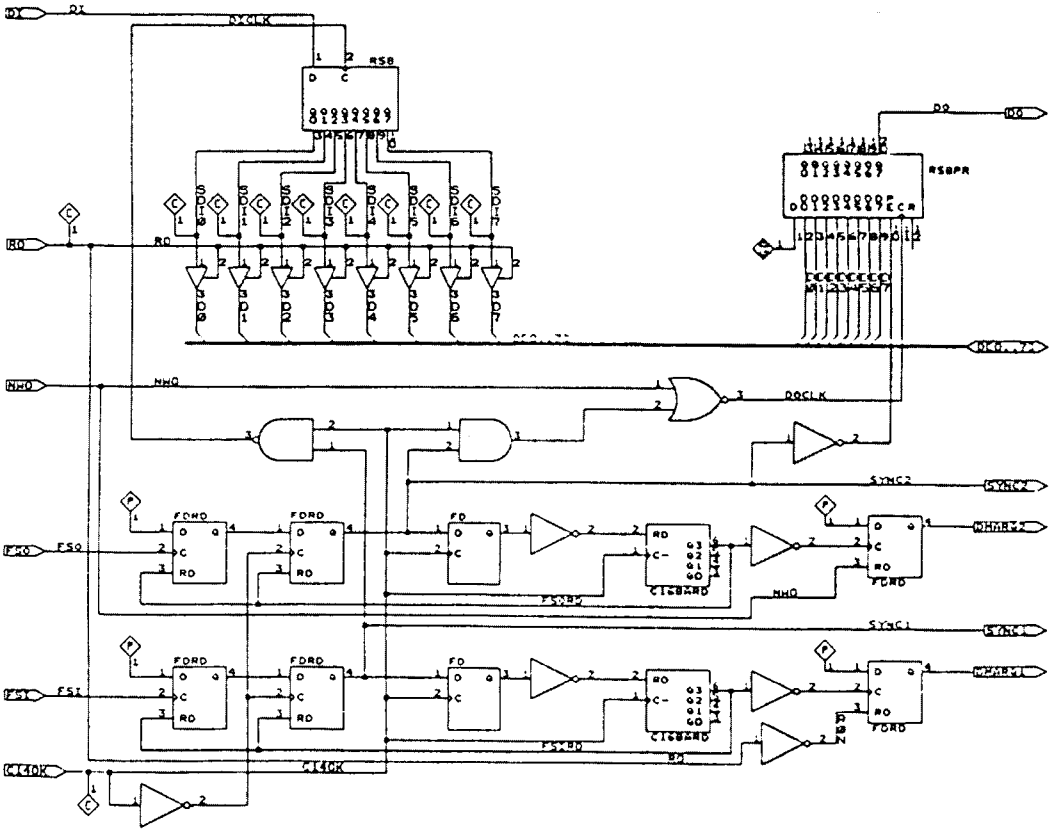


Figure 2-43B. PGA, U30 - Codec Section, Schematic Diagram (Sheet 2 of 10)

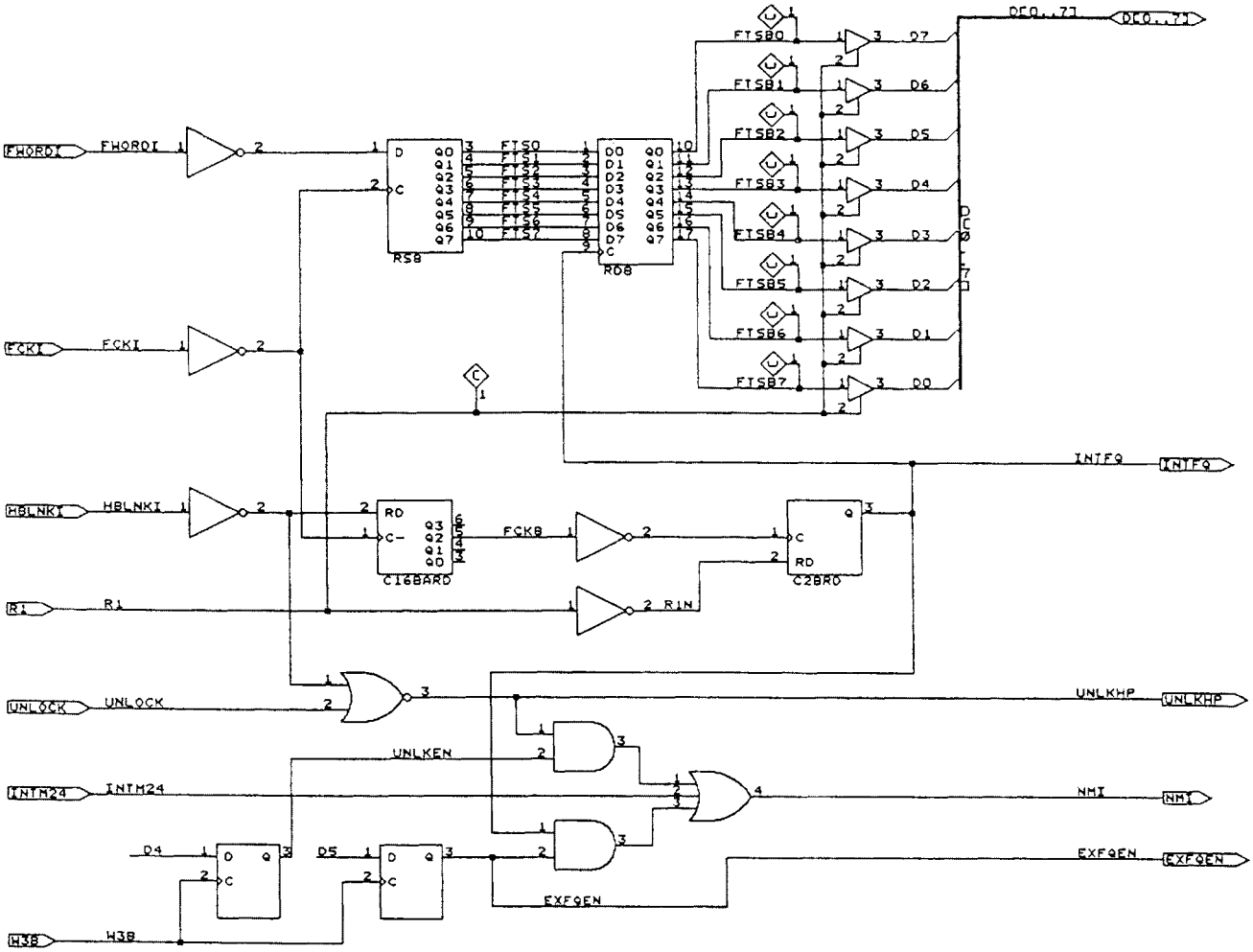


Figure 2-43C. PGA, U30 - FREQ TRN Section, Schematic Diagram (Sheet 3 of 10)

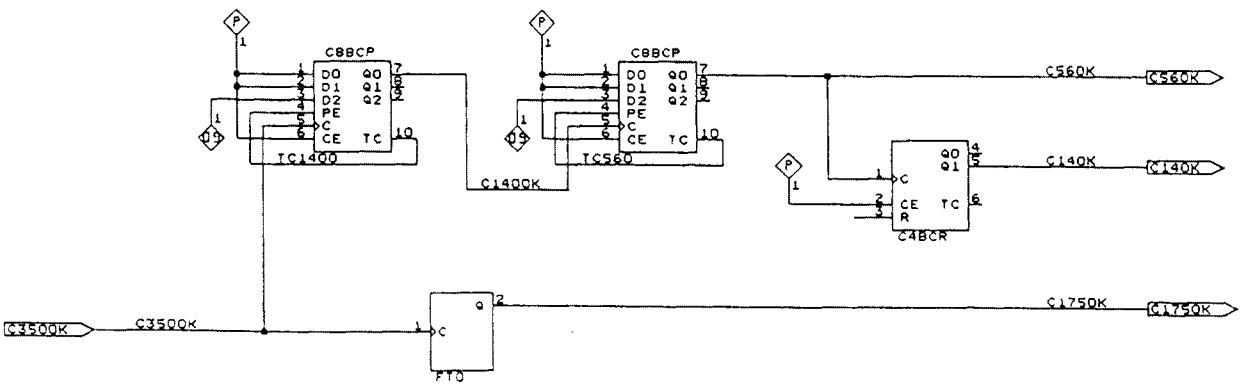


Figure 2-43D. PGA, U30 - DIV3-5M Section, Schematic Diagram (Sheet 2 of 10)

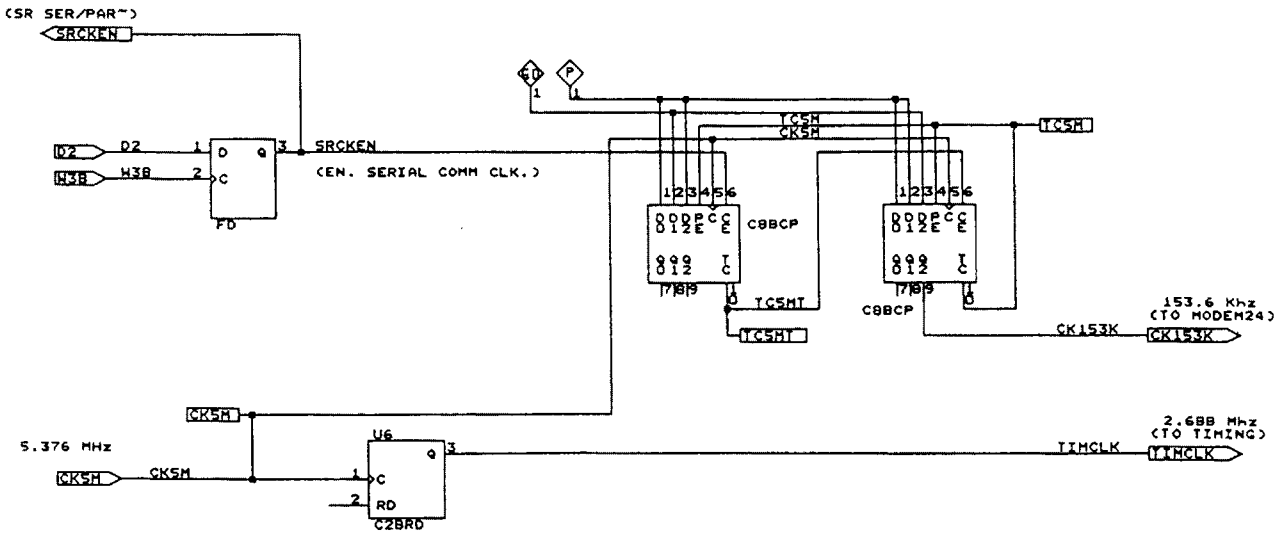


Figure 2-43E. PGA, U30 - DIV10M Section, Schematic Diagram (Sheet 5 of 10)

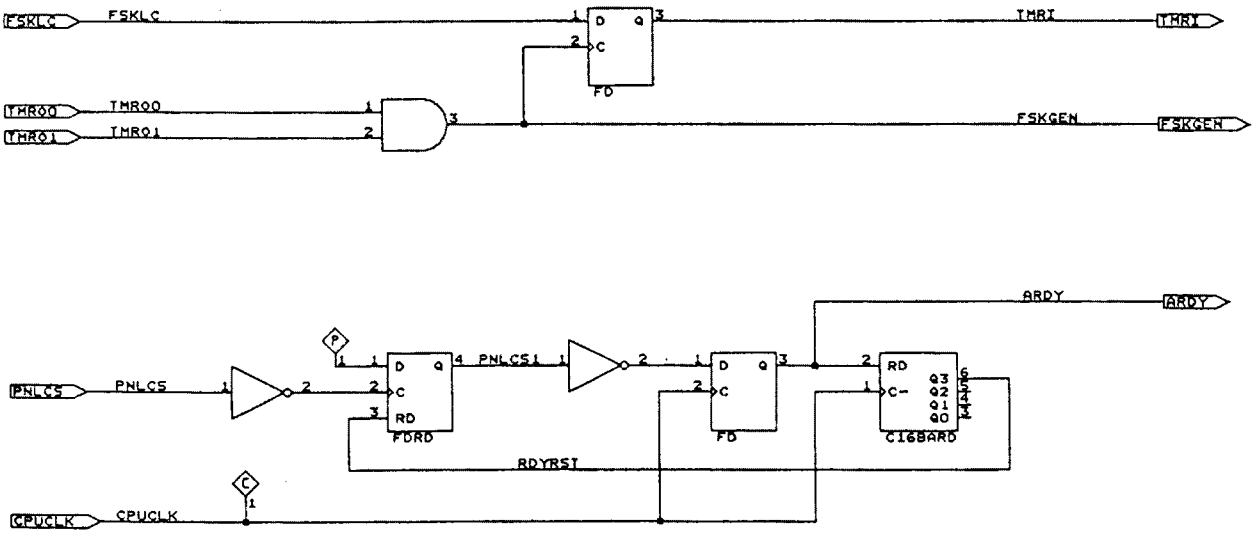


Figure 2-43F. PGA, U30 - TIM-RDY Section, Schematic Diagram (Sheet 6 of 10)

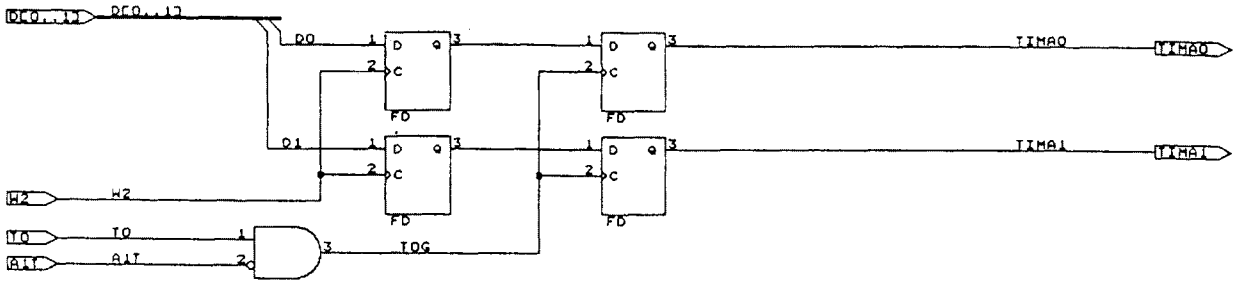


Figure 2-43G. PGA, U30 - TIMAD Section, Schematic Diagram (Sheet 7 of 10)

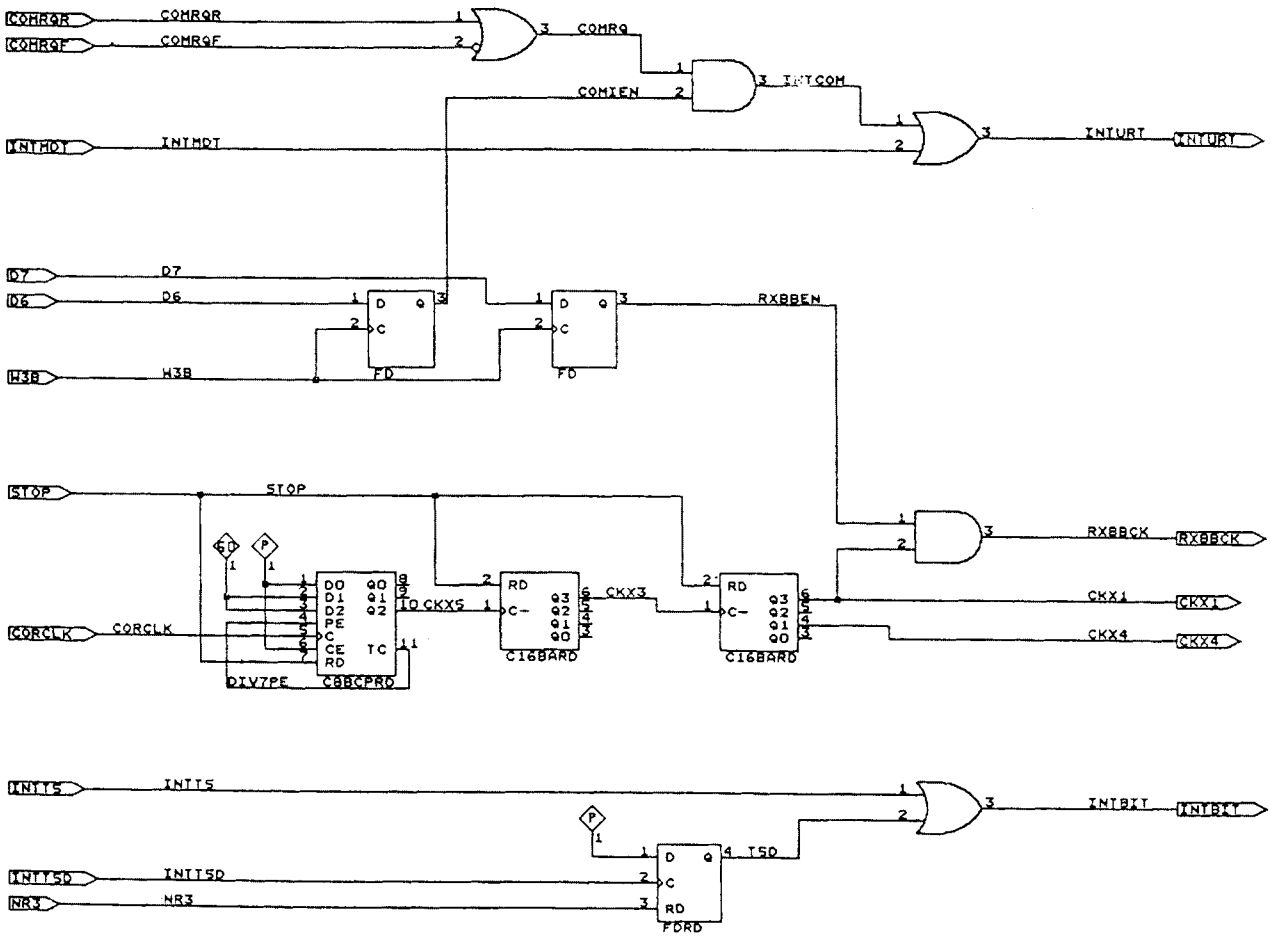


Figure 2-43H. PGA, U30 - MISC1 Section, Schematic Diagram (Sheet 8 of 10)

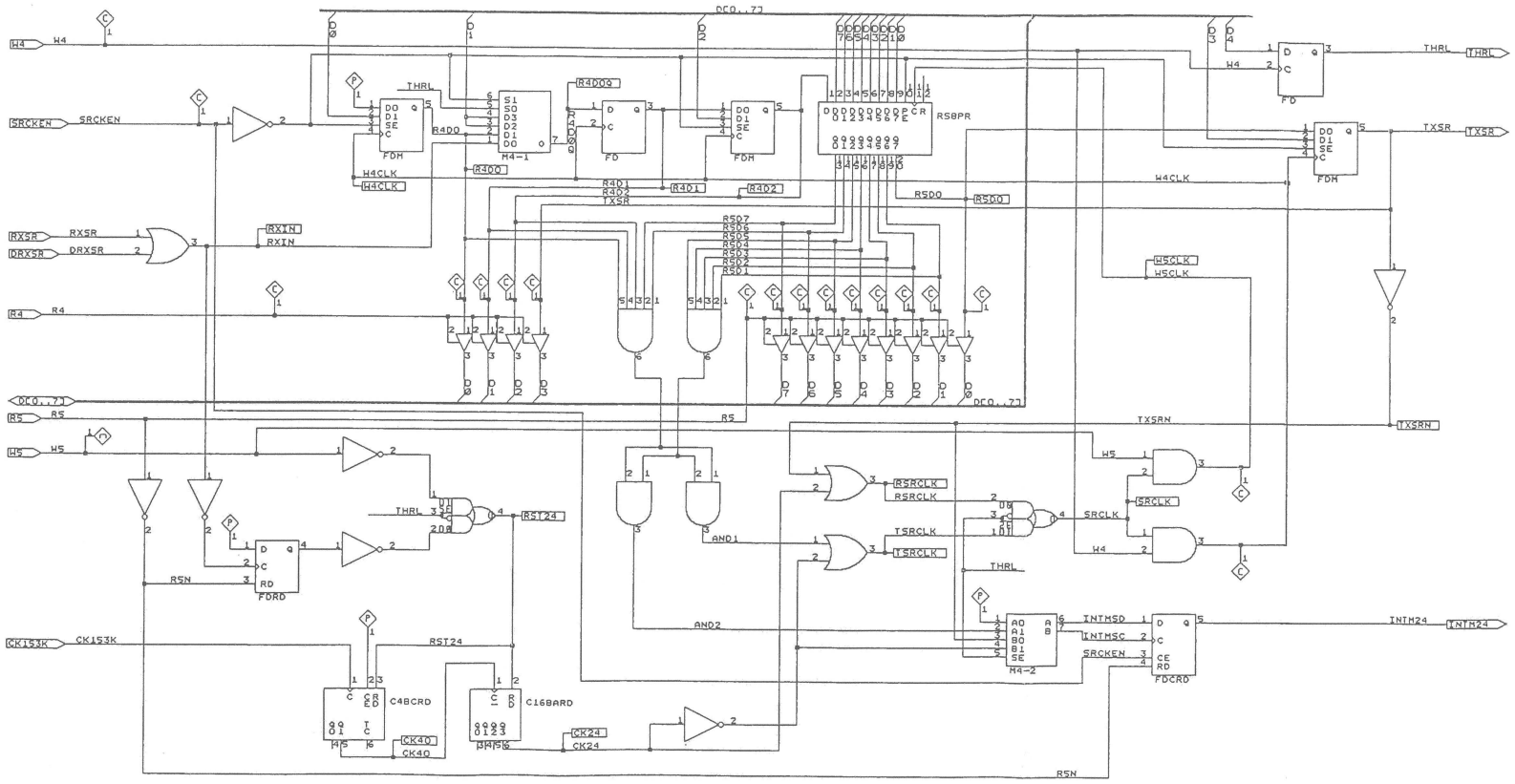


Figure 2-43J. PGA, U30 - MODEMDT Section, Schematic Diagram (Sheet 9 of 10)

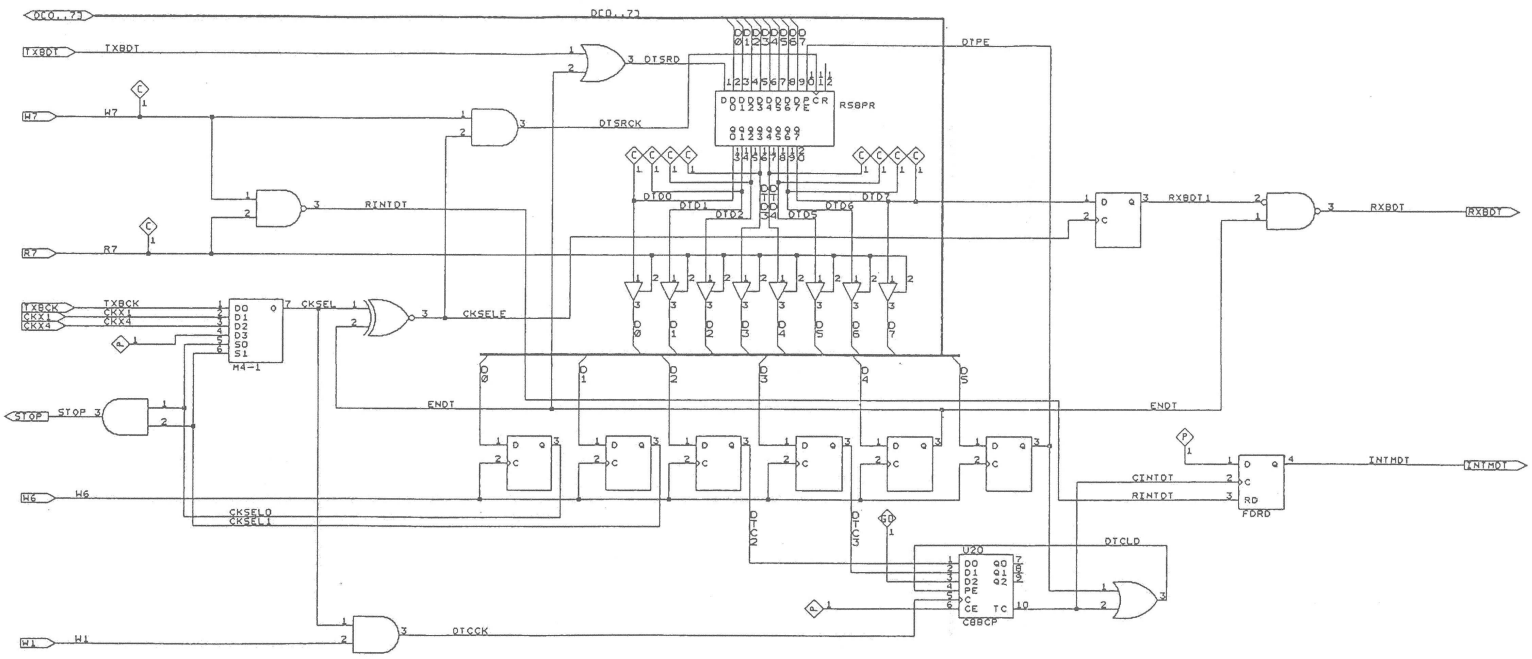


Figure 2-43K. PGA, U30 - MODEM24 Section, Schematic Diagram (Sheet 10 of 10)

1. Transferring data from the codec to the RAM. The process starts when the FSI (from U8) signal rises to a high level. The rising edge is synchronized by the 140 KHz clock. As a result, the SYNC1 signal rises to a high level (pin 82). Then the codec samples the present analog input and transfers the previous sample value via the DI line (pin 84), at a rate of 140 KHz, to the shift register. This serial information includes 8 bits and the transfer is made byte after byte.

   The byte is applied to the shift register bit after bit. When the bit counter reaches 8, the SYNC1 signal falls to a low level and the DMA-RQ1 signal (pin 73) rises to a high level. This signal is applied to the microprocessor via DRQ-0 line.

   The DRQ-0 signal indicates that a byte can be sent from the shift register to the RAM via the data bus, therefore, a DMA process starts for this purpose. When this process ends, the DMA-RQ1 signal is returned to a low level by the microprocessor. During this process, the shift register is enabled by means of RO signal (from block 2).

2. Transferring data from the RAM to the codec. When the FSO signal (from U8) rises to a high level. The rising edge is synchronized by the 140 KHz clock. As a result, the SYNC2 (pin 80) signal rises to a high level. Then a block of processed data is transferred from the shift register to the D/A section of the codec, via the DO line (pin 59), while the codec converts the previous digital information to an analog form. The byte transfer continues until the bit counter reaches 8, then the SYNC-2 signal falls to a low level. In response, the DMA-RQ2 (pin 79) rises to a high level. This signal is applied to the microprocessor via the DRQ-1 line, to indicate

that a new byte of processed data can be sent from the RAM to the shift register via the internal data bus.

During this process, the shift register is enabled by means of the NWO signal (from block 2).

(c) Block 4 - FREQ TRN (fig. 2-42, 2-43.C). This block is an option, which allows the reading of frequency information from an external source. The frequency data, clock and strobe signals arriving from the TIMING LSI, U8, to pins 14, 29 and 34, respectively, of U30 pass through internal buffers to pins 16, 27, 26, respectively (figure 2-42). The internal buffers are controlled by the internal EXFGEN line. The pins 16, 27, 26 are connected via the inverters U25 (pins 6, 8, 10) to the inputs of block 4 (pins 17, 30, 37, respectively) of PGA (U30) together with the UNLOCK line (pin 28) from the SYNT module.

Block 4 also generates the NMI interrupt in case the SYNT module signals loss of lock (UNLOCK line).

(d) Block 5 - DIV3.5M fig. (2-43.D). This block receives a 3.5 MHz clock from module SYNT, and divides its frequency. This block generates 560 KHz for the TIMING LSI, U8, to 1.75 MHz for the MASTER CODEC line, and 140 KHz for the codec clock.

(e) Block 6 - DIV-10M (fig. 2-43.E). The PGA is connected to an external crystal oscillator that provides 10.752 MHz. This block divides the frequency of the 10.752 MHz signal by 4, and applies it to the TIMING LSI U8 via the TIM-CLK line (pin 35) and generates a 153.6kHz signal for the asynchronous modem (block 10). The SRCKEN signal enables the generation of the 153.6 KHz clock. The SRCKEN (serial clock enable) signal is controlled by writing to a D flip-flop the state of data bus line D2 by means of the W3 signal generated in block 2.

(f) Block 7 - TIM RDY (fig. 2-43.F). This block performs two functions:

1. Generates an ARDY signal for the microprocessor. The ARDY signal controls the microprocessor wait states necessary for communication with all the devices which are enabled by the PNL-CS signal.

2. Control over the generation of the four FSK tones. The FSK tones are generated by counter 0 and counter 1 in the microprocessor. Each counter can generate each of the four FSK tones (frequencies of 2400, 2700, 3000 and 3300 Hz). To achieve fast switching from one FSK tone to another, one counter generates the present FSK tone and the other is loaded with the data necessary for the following FSK tone. Therefore when counter 1 is enabled, counter 0 is disabled, and vice versa. The FSK LC line, provided by the TIMING LSI U8, controls the accurate timing of the FSK tone switching.

   The selected FSK tone is sent via the FSK GEN line to module AUDIO, for transmission.

(g) Block 8 - TIMAD (fig. 2-43.G). This block generates TIM-PORT-0/1 (pin 33 and 42) signals to expand the address space of TIMING LSI (U8) to 8kbyte, by connecting TIM-PORT-0/1 to A11-A12 input lines of the EPROM U9.

(h) Block 9 - MISC1 (fig. 2-43.H). This block generates the following signals:

1. INT URT - appears after the reception of a COM-REQ-F, COM-REQ-R or INTMDT signal from the internal modem - block 11.

2. INT BIT - is a function of INT-T5 and INT-T5-D (from U8), and appears during self-test.

3. CKX1, CKX4 are obtained by dividing the frequency of the CORCLK signal (from U8) by 256 and by 128, respectively. These clock signals are applied to block 11.
Block 9 also generates the RXBB-CK signal (pin 51). Signal generation is enabled by the signals D6 and D7 (RXBBEN) signals, and is controlled by the W3 signal. The W3 signal is generated in block 2.

(j) Block 10 - MODEM 24 (figure 2-43.J). This block contains a 2.4 kbps asynchronous receiver/transmitter (UART). It has a serial input (pin 39) and a serial output (pin 23). The asynchronous serial data produces an INTM24 which is applied to block 4. This block generates the NMI interrupt for the microprocessor, and then the microprocessor reads the received word via the data bus in a parallel format. This process can also operate in the opposite way.

(k) Block 11 - MODEMDT (fig. 2-43.K). This block is used as the internal modem. This modem operates at rates of 50, 75 and 150 baud. The transmit data arriving on the TXBB-IN (pin 68) line is directly applied to the PGA. The receive data from the PGA it is directly applied to the RXBB-D line (pin 63).
This block generates an INTMDT signal which is applied to block 9. In response, this block creates the INT-URT interrupt for the microprocessor. The microprocessor then reads data from the internal modem, via the internal data bus and vice versa.

(l) The internal data bus of U30 is used for bi-directional data transfer between the modem (block 11) and the UART (block 10). Two other parts which are connected to the internal data bus are the Reading Port and the Writing Port.

These ports latch control signals for internal and external purposes.

c. MCU Module Software.

(1) The operation of RT-2001 and the protocols used by the RT-2001 to communicate with the CP-2003 and external units are controlled by the software stored in the EPROM U5.
The main functions of the software are:

(a) Initialization upon turn-on.

(b) Transmission and reception of messages to and from the external user connected to the front panel RMT/DATA connector.

(c) Transmission to and reception of messages from, the CP-2003.

(d) Writing to and reading optionally frequency data from the frequency bus.

(e) Processing of information received from the CP-2003 and the various RT-2001 modules, and generation of appropriate commands for the various modules.

(f) Monitoring of the outputs of the various signal sensors located in the other modules, and performing continuous on-line checks and off-line self-test (BIT system).

(g) Processing of the commands received from the operator and their conversion to control signals for the various modules.

(h) Display of messages on the front panel LCD display.

(j) Processing of digital data applied to, and received from, the codec.

(k) Generation of various signals that control signal routing in module AUDIO.

(2) Main software modules. The software is modular and comprises the following main modules:

(a) INITIALIZATION module. Performs microprocessor initialization and determines the initial values for the various variables. After ending its execution, it enables the interrupts and calls the main program.

(b) MCU module. Receives information from the other software modules, processes the received information and operates the service routines.

(c) INTERRUPT module.

1. Handles reading and writing of data from and to the PGA.

2. Handles reading of frequency data byte from frequency bus.

3. Handles the self-test interrupt.

4. Handles the interrupt coming from TIMING LSI (U8).

(d) Service functions. The software comprises service functions, used by the MCU module. The service functions perform all the operations and tasks listed in para. (1) above, under control of the MCU module.

2-14. Module PANEL

(fig. 2-44 thru 2-48)

a. Block Diagram Analysis (fig. 2-44). The PANEL module contains the connections between components located on the front panel and the RT-2001 motherboard. The connections to the front panel components are made by means of a special flexible printed circuit board (fig. 2-44). In addition, the front panel contains interface circuits to the keypad, to the LCD displays and to the various selectors. These circuits are located on the DISPLAY module.

(1) Interface to front-panel controls.

(a) Keypad interface. The keypad interface comprises an encoder, which scans the keypad and detects key pressings. When a key pressing is detected, the encoder sends a signal to the MCU module, via the DAKB line. When interrogated by the microprocessor in the the MCU module, the encoder sends the code of the pressed key via the data bus.

(b) Control interface. The control interface comprises a buffer. When interrogated by the microprocessor in the MCU module, the buffer transfers the data indicating the position of the front-panel channel and function selectors via the data bus.

(2) Interface to front-panel displays and indicators.

(a) LED interface. The front-panel LEDs are controlled via a dedicated control latch. The contents of the latch are updated by the microprocessor in module MCU whenever necessary, via the data bus.

(b) LCD display and keypad lighting. The front-panel LCD displays and the keypad can be backlighted, by means of electro-luminiscent (EL) elements. The EL elements are controlled via the LED control latch. When lighting is on,

the microprocessor turns on a DC/AC converter, which generates the operating voltage, 110VAC, for the EL elements.

(c) Seven-segment and dot-matrix displays. The seven-segment and dot-matrix displays use multiplexing. The display information is transferred by the microprocessor in module MCU via the data bus, together with select signals for each display unit.

On the DISPLAY module, the display information is converted to local drive signals by a dot-matrix display controller and by a seven-segment driver. To obtain optimum contrast, the dotmatrix controller and seven-segment driver receive a contrast correction voltage from temperature compensation circuits.

(3) Microphone amplifier. The microphone amplifier receives the low-level signal applied to the microphone line in the AUDIO connector and amplifies it. The microphone amplifier is built on a separate printed circuit card.

b. Microphone Amplifier Circuit Analysis (fig. 2-45). Microphone amplifier (fig. 2-45). The microphone amplifier is built around operational amplifier U1. Its schematic diagram is shown in figure 2-45.

c. DISPLAY Module, Circuit Analysis (fig. 2-46, 2-47). Figure 2-46 shows the schematic diagram of module DISPLAY.

Figure 2-47 shows the wiring diagram of the front-panel flexible PCB. The flexible PCB uses the following connectors:

- Connector P2 (60 pin), connected to module MCU.
- Connector P1, connected to module DISPLAY.
- Connector P3, connected to the RMT/DATA connector.
- Connector P4, connected to the FUNCTION selector.
- Connector P5, connected to the CHANNEL selector.
- Connector P6, connected to the volume control.

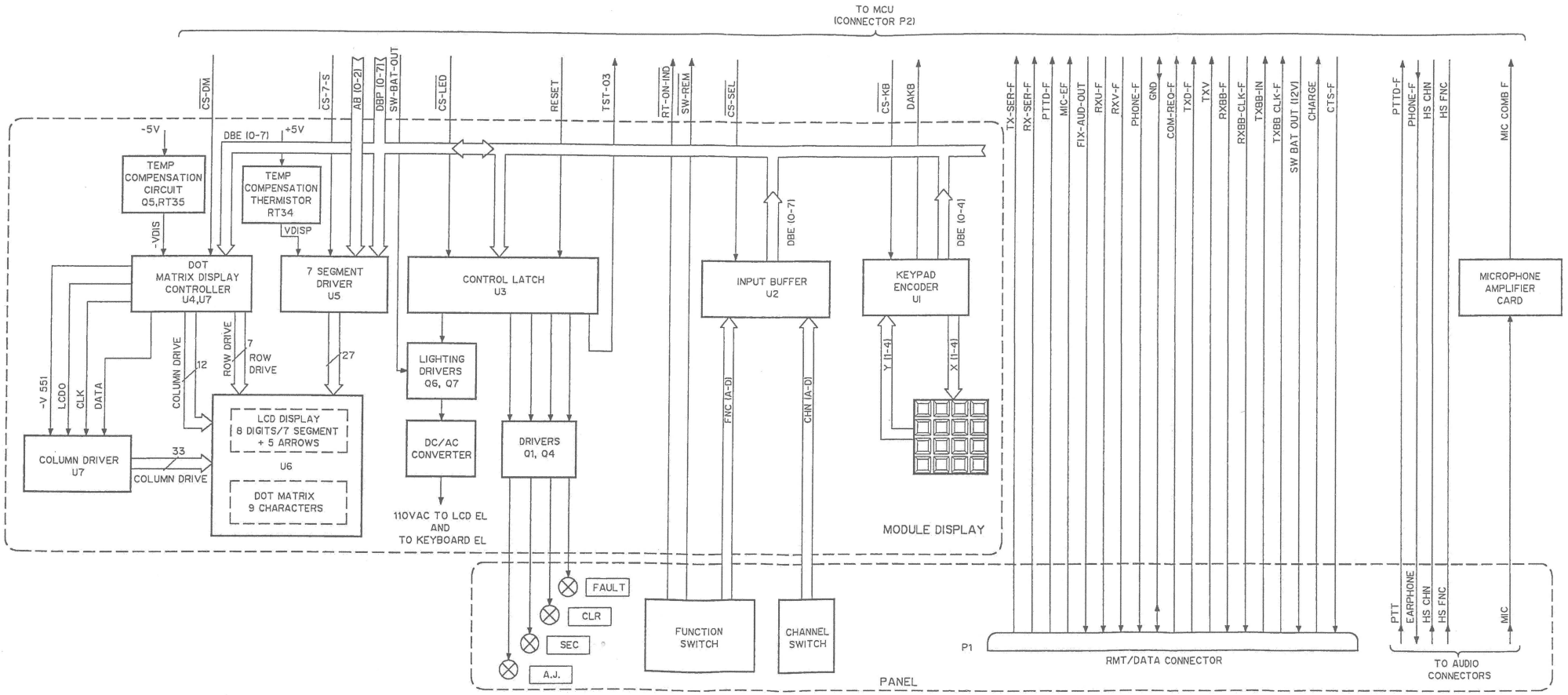


Figure 2-44. Module PANEL, Block Diagram

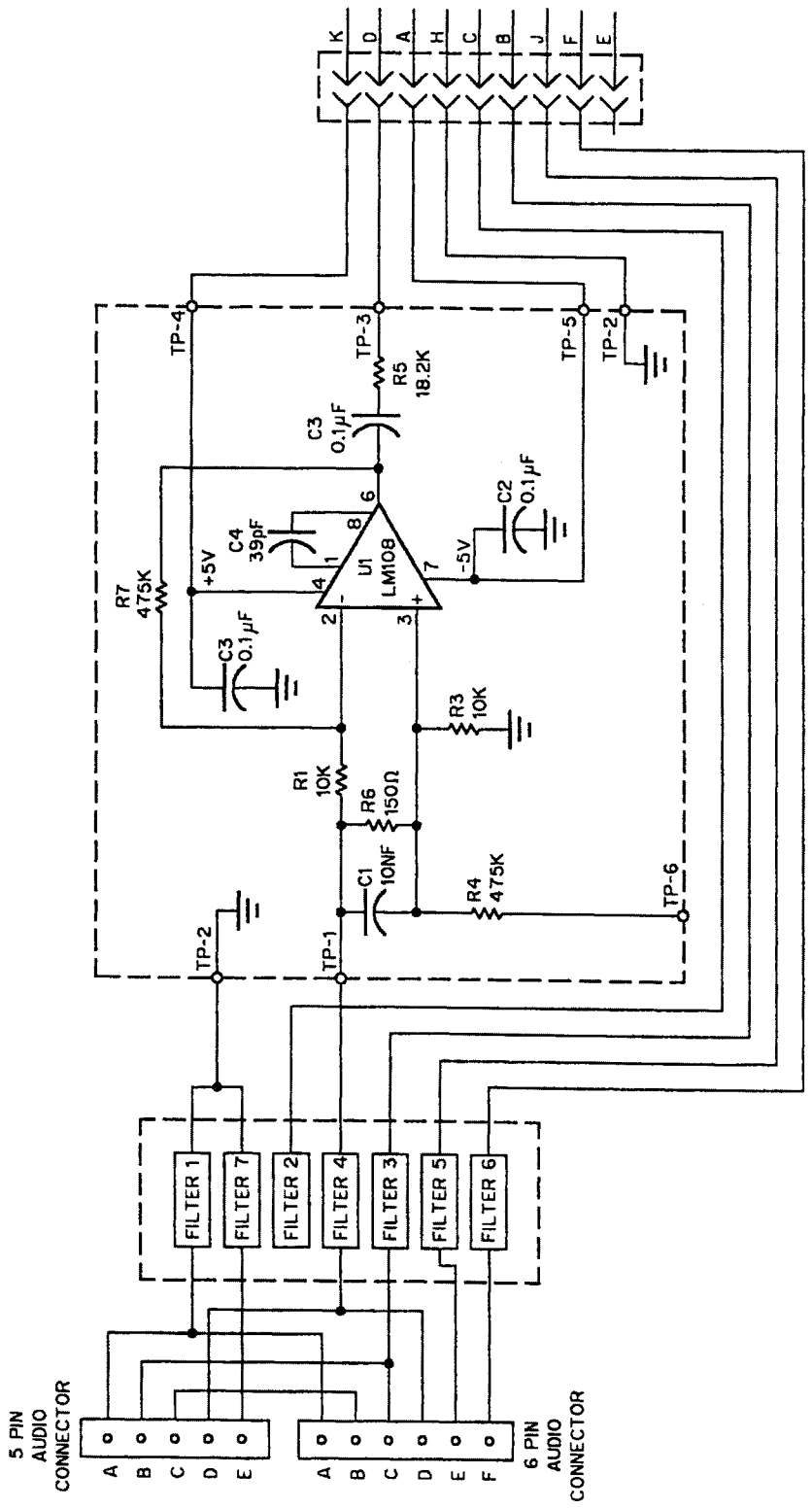


Figure 2-45. Microphone Amplifier Card, Schematic Diagram

(1) Keypad operation.

(a) The keypad consists of two groups of conducting strips, forming four rows (Y1 through Y4) and four columns (X1 through X4). A key is located at each intersection. When depressed, the key connects the corresponding strips together (i.e. key "1" connects the X1 and Y1 strips, key "0" connects the X2 and Y4 strips, etc.).

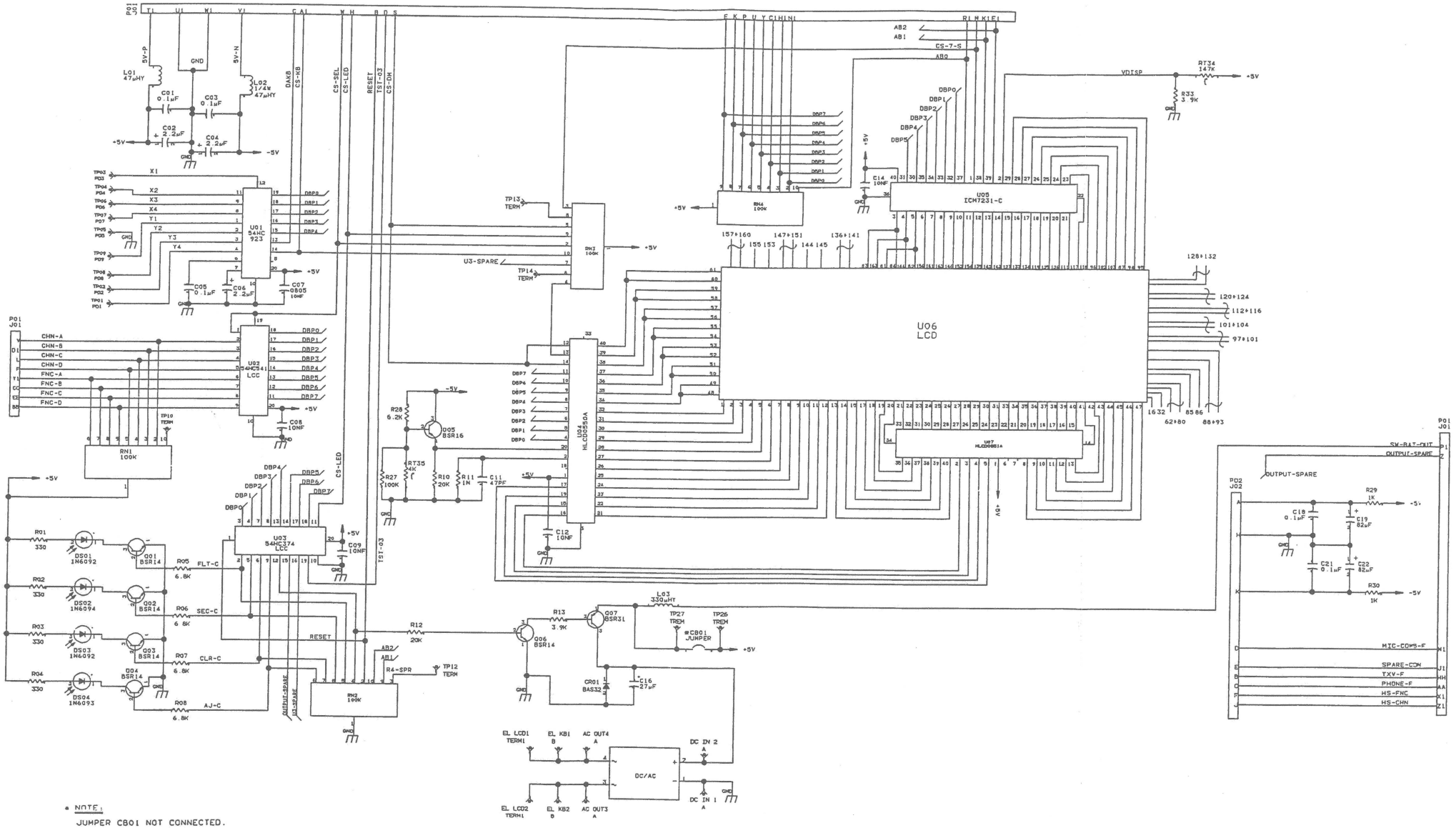
(b) Keypad encoding. The eight output lines of the keypad are connected to the input of the keypad encoder U1. The keypad encoder supplies a four-bit output word, DBP0 thru DBP3 (DBP4 is not used), which indicates the number of depressed key in binary format. Table 2-15 lists the encoded outputs.

Table 2-15. Keypad Encoder Truth Table

Key	Output Word			
	DBP3 (Pin 16)	DBP2 (Pin 17)	DBP1 (Pin 18)	DBP0 (Pin 19)
RST	H	H	L	L
0/TEST	H	H	L	H
PROG	H	H	H	L
ENT	H	H	H	H
7/TIME	H	L	L	L
8/AUTO	H	L	L	H
9/KEY	H	L	H	L
NET/DOWN	H	L	H	H
4/DATA	L	H	L	L
5/PWR	L	H	L	H
6/MODE	L	H	H	L
ADDR/UP	L	H	H	H
1/LITE	L	L	L	L
2/SQ	L	L	L	H
3/STAT	L	L	H	L
FRQ	L	L	H	H

H - High logic level

L - Low logic level



* NOTE:
JUMPER CB01 NOT CONNECTED.

Figure 2-46. Module DISPLAY, Schematic Diagram

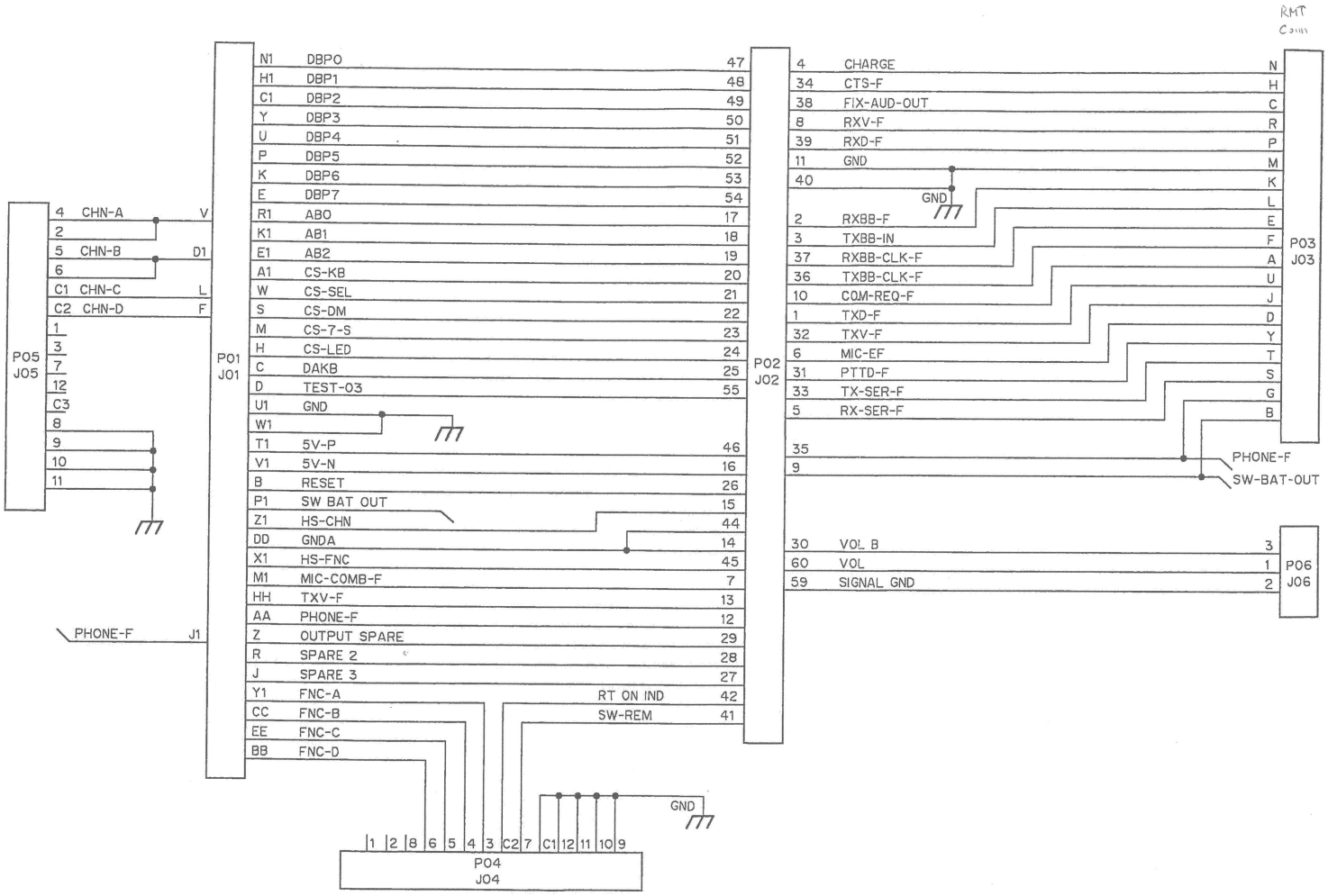


Figure 2-47. Front Panel Flexible PCB

(c) Keypad encoder operation (fig. 2-48).

1. The keypad encoder, U1, scans the input lines at a rate determined by an internal oscillator. The oscillator frequency depends on the value of C5 (connected to pin 6).

2. When a key is depressed, its identification code is stored in an internal register and a high level pulse appears at the DAKB (data available KB) output - pin 13. The pulse persists as long as the key is depressed. An internal debounce circuit and capacitor C6 connected to pin 7 prevent the appearance of multiple pulses due to key bouncing.

3. The DAKB pulse is sent to the MCU module. The MCU module responds by performing a read operation from the keypad port. During the read operation, a low level appears at the output of the address decoder in the MCU module. This low level is applied via the keypad chip-select line (CS-KB) to pin 14 of U1, enabling its three-state output.

   The four-bit code of the depressed key is then applied on data bus lines DBP0, DBP1, DBP2 and DBP3 and is read by the microprocessor in the MCU module.

(2) Input buffer. The input buffer is built around U2. The input buffer is controlled by the CS SEL line from the MCU module. A low level on this line enables the buffer. The buffer then transfers the bits indicating the status of the channel selector (CHN A thru CHN D) and the function selector (FNC A thru FNC D) to the data bus. The data is then read by the microprocessor in module MCU, via the data bus.

(a) The channel selector position is encoded in BCD code, as listed in table 2-16.

Table 2-16. Channel Selector Encoding

Position	CHN Lines (U2 inputs)			
	CHN D (Pin 5)	CHN C (Pin 4)	CHN B (Pin 3)	CHN A (Pin 2)
M(manual)	H	H	H	H
1	H	H	H	L
2	H	H	L	H
3	H	H	L	L
4	H	L	H	H
5	H	L	H	L
6	H	L	L	H
7	H	L	L	L
8	L	H	H	H
KB	L	H	H	L

H - High logic level L - Low logic level

(b) The function lines selector position is encoded as listed in table 2-17.

Table 2-17. Function Selector Encoding

Position	FNC Lines (U2 inputs)			
	FNC D (Pin 9)	FNC C (Pin 8)	FNC B (Pin 7)	FNC A (Pin 6)
OFF	H	H	H	H
CLR	H	H	H	L
SEC	H	H	L	H
AJ	H	L	H	H
RMT	H	H	H	H
ERS	L	H	H	H

H - High logic level L - Low logic level

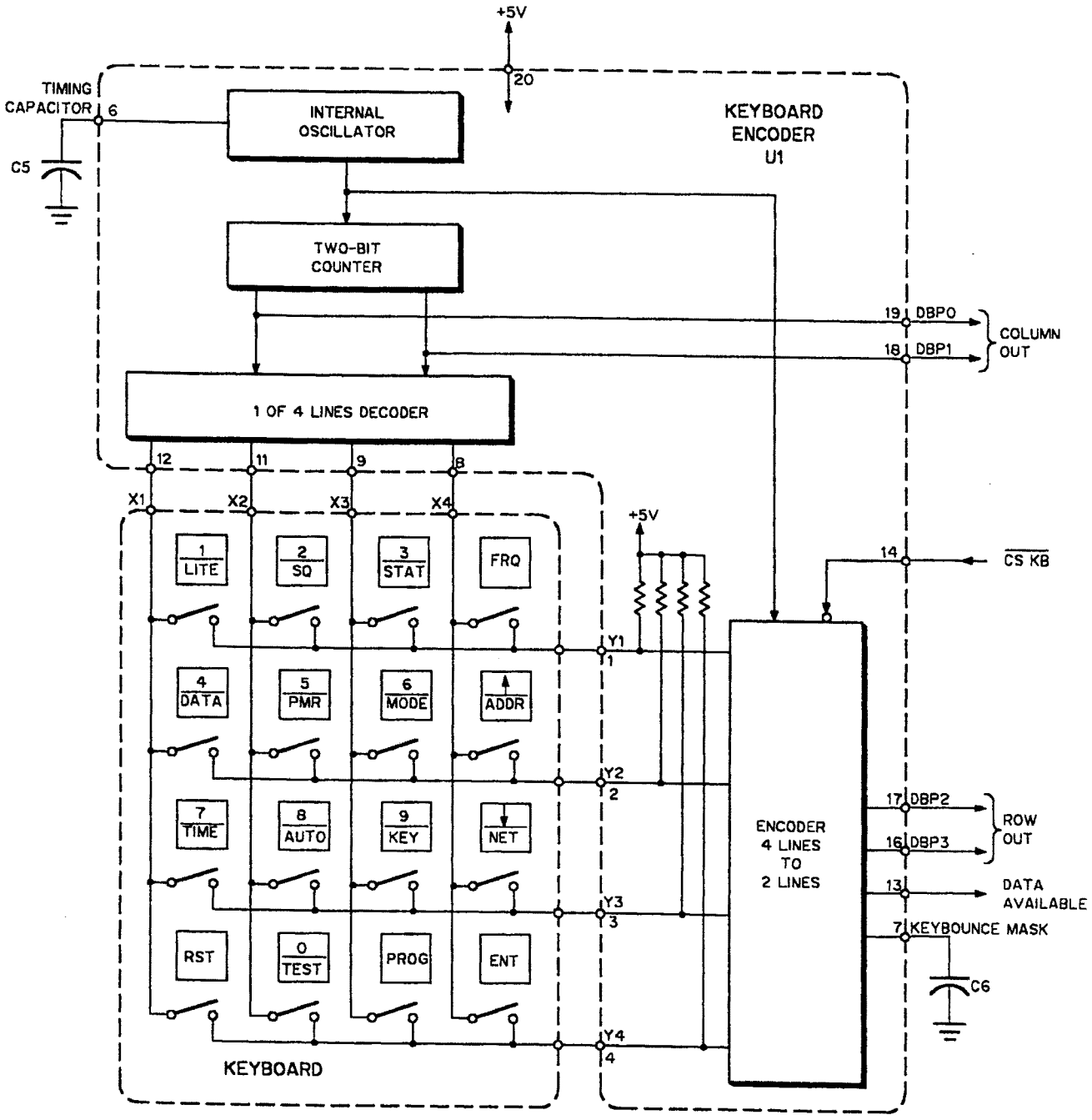


Figure 2-48. Keypad Encoder, Simplified Diagram

(4) Control latch. The control latch, U3, is used to control the operation of the front panel LEDs, LCD display and keypad backlighting. In addition, U3 provides a self-test (BIT) control line for module MCU.

(a) U3 inputs are connected to the data bus lines DBP0 thru DBP7, arriving from module MCU. U3 is enabled by the chip-select signal CS-LED* provided by the address decoder of module MCU. When the microprocessor needs to update latch contents, it sends a low level on the CS-LED* line (pin 11 of U3), and then transfers the required control information via the data bus. Upon turn-on, U3 is reset by the RESET line from module MCU.

(b) The control signals appearing at the latch outputs are listed in table 2-18.

Table 2-18. Control Latch U4

U4 Output	Line	Function
Pin 2	FLT C	Drives the FAULT LED, DS01
Pin 5	SEC C	Drives the SEC LED, DS02
Pin 6	CLR C	Drives the CLR LED, DS03
Pin 9	AJ C	Drives the A.J. LED, DS04
Pin 12	-	Drives the LCD display and keypad backlighting circuit
Pin 15	-	Output spare
Pin 16	-	Not used
Pin 19	TST 03	Self-test (BIT) control line, to module MCU

(5) LED drivers. The transistors Q1 thru Q4 drives the FAULT, SEC, CLR, and A.J. LEDs, respectively, according to the control signals applied from control latch U3. For example, when pin 2 of U3 (FLT C line) rises to a high level, Q1 saturates and the FAULT LED, DS01,

lights. When pin 2 falls to a low level, Q1 cuts off and DS1 extinguishes.

(6) LED display and keypad backlighting circuit.

(a) Backlighting element driver. The backlighting driver is built around transistors Q6 and Q7. When a lighting-enable command is received from the microprocessor, pin 12 of the control latch U3 rises to a high level. As a result transistors Q6 and Q7 conduct and the battery supply voltage is applied via the SW BAT OUT line, inductor L3 and the collector of Q7 to the DC/AC converter.

(b) DC/AC converter. This converter receives the +12V battery voltage from the backlighting driver and converts it to a 110VAC voltage, applied to the electro-luminiscent (EL) elements located on the front panel.

(8) Display operation. The LCD DISPLAY U6 is driven by a dot-matrix display controller, comprising U4 and U7, and by a seven-segment driver, U5.

(a) Dot-matrix display controller. The dot-matrix display controller is built around U4 and U7. U4 provides 7 row drive lines (pins 34 thru 40), and 12 column drive lines (pins 21 thru 32). In addition, U4 provides 4 control lines (pins 17, 19, 15 and 16) for the driver U7. U7 provides 33 column drive lines (pin 8 thru 40).

1. The data between the dot-matrix controller and the microprocessor in module MCU is transferred via the data bus lines, DBP0 to DBP7. To write display data to the dot-matrix controller, the microprocessor sends a low level on the CS-DM* line. This line is connected to the chip-select input (pin 14) and to the write-enable input (pin 12) of U4.

2. U4 includes various decoders, and a display drive circuit, which performs all the functions required to convert the display data to the appropriate drive waveforms for the LCD display. U4 internal clock frequency, provided by an oscillator contained in U4, is determined by capacitor C11 and resistor R11 connected to pin 2 of U4.

3. The negative supply voltage for U4 (pin 20) is supplied by means of a temperature-compensation circuit, built around transistor Q5 and thermistor RT35.

4. The serial data for the driver U7, appearing at the data output (pin 16) of U4, is connected to pin 2 of U7. The data is accompanied by a clock signal, provided by pin 15 of U4.

5. The negative supply voltage required by U7 is provided from pin 17 of U4.

(b) Seven-segment driver, U5. U5 drives 8 seven-segment display units and 5 arrows, by means of 27 drive lines (pins 3 to 29 of U5).

1. The microprocessor in module MCU communicates with U5 by means of three address lines AB0, AB1 and AB2 (pins 37, 38 and 39, respectively), and five data lines DBE0 thru DBE4 (data line DBP5 is not used). The information sent on the address lines selects one of the eight display units. The information sent on the data lines is decoded by U5 to drive the selected unit or arrow. The address and data bits are latched into U5 on the rising edge of the chip-select signal, CS-7-S* (pin 1). The bits are decoded by U5 and the corresponding drive signals appear at its outputs.

2. U5 is powered by a positive voltage of +5V, applied directly to it +V input (pin 40). In addition, U5 VDISP input (pin 2) receives a temperature-compensation voltage, provided by the voltage divider comprising thermistor RT34 and resistor R33.

2-15. Module PS

(fig. 2-49 thru 2-51)

a. Block Diagram Analysis (fig. 2-49). Figure 2-49 shows the block diagram of the PS module.

(1) Input circuit. The battery line is protected by a fuse located in the PS module. The battery line then passes through a current sensing resistor, exits to the CP-2003 via the RT-2001 rear connector, and returns to the PS module where is connected to the two power supplies. The battery voltage is also connected to the AM module.

(2) Current consumption sensor. The current drawn from the battery is monitored by the microprocessor in module MCU. The microprocessor uses the current information to establish the maximum allowable RF output power, as explained in para. 2-11.

(3) Main power supply. The main power supply provides regulated voltages of +5V, +7V, +12V, +15V and -5V to the various RT-2001 and CP-2003 modules. In the receive mode, the main power supply also provides +2V to the CP-2003.

(a) Power supply activation. The power supply is turned on by the ON/OFF line, which controls the main power supply switch. The main power supply switch connects the battery voltage to the regulation circuits and also to modules MCU and RF. The supply line to the MCU and RF modules is protected by a 1A fuse.

(b) Power supply operation. The power supply is a switching regulator, using pulse width modulation. The pulse width modulator provides drive signals to the switching transistor, a power MOSFET, and controls its conduction duty cycle. The conduction duty cycle is changed as required to maintain the output voltages within the specified limits. The control over duty cycle is performed by monitoring the +5V output voltage.

The switching transistor drives a transformer, whose output voltages are rectified and filtered. The filtered voltages are sent to the various modules.

(c) Power supply protection. A protection circuit monitors the current pulses flowing through the switching transistor, and compares them with a voltage derived from the +12V output. If the current is too high, because of overload or short-circuit, the protection circuit sends a shut-down command that stops the PWM output pulses. The output voltages then decrease, thereby reducing the current. This leads to a foldback action, because the +12V output voltage decreases as well.

After the fault condition disappears, the power supply returns to normal operation.

(4) TX power supply. The TX power supply provides a regulated voltage of +5V during the transmit mode. The +5V voltage replaces the +2V voltage provided in the receive mode by the main power supply.

(a) Power supply activation. The power supply is turned on by the ACTIV L.V line, which controls the TX power supply switch. The TX power supply switch then connects the battery voltage to the power supply regulation circuits.

(b) Power supply operation. The power supply is a switching regulator, similar to the main power supply.

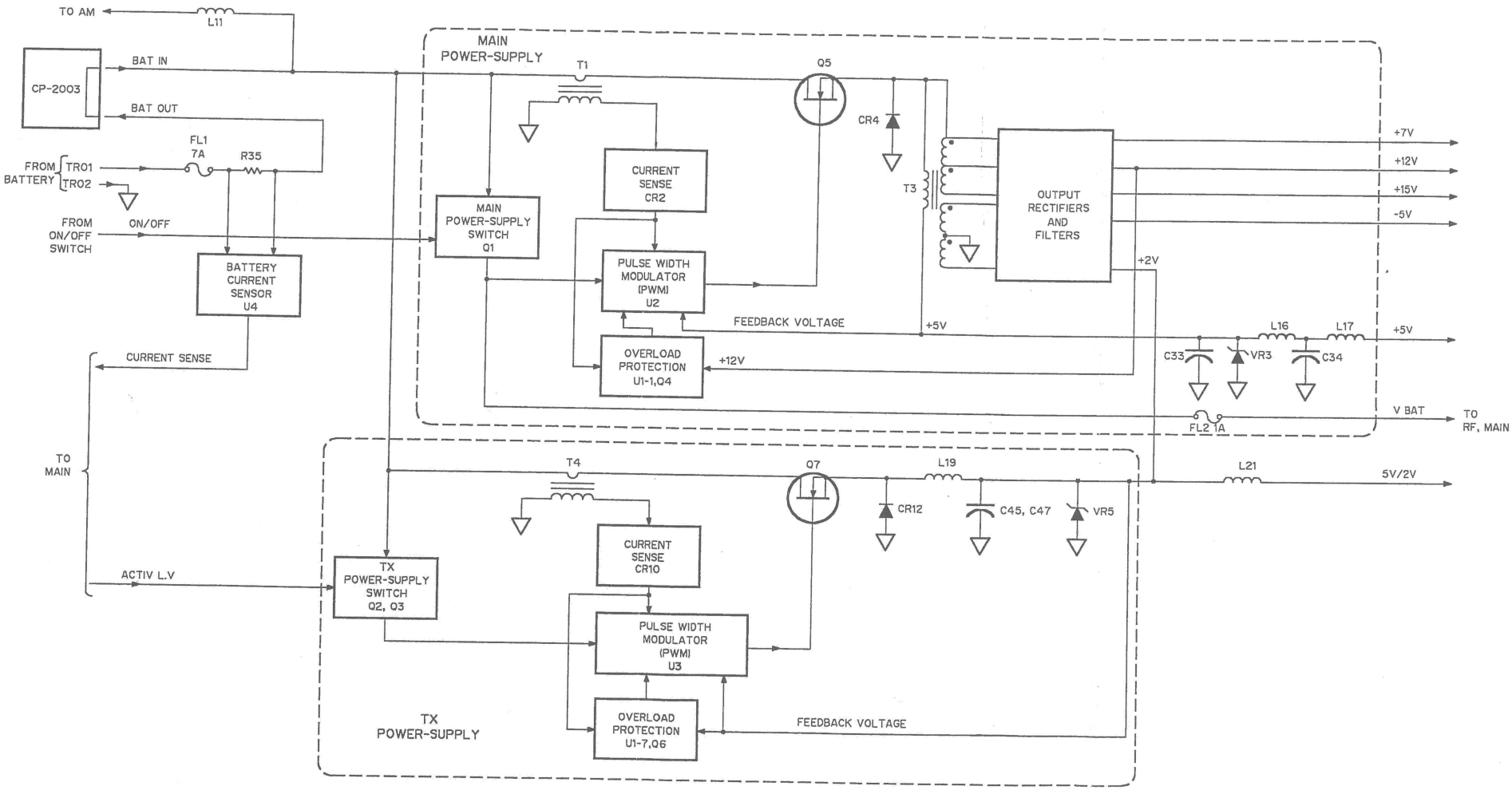


Figure 2-49. Module PS, Block Diagram

b. Circuit Analysis (fig. 2-50 and 2-51).

(1) Battery current sensor. The battery line passes via contact TR01 and the fuse FL1. The current drawn from the battery is sampled by the current sensing resistor R35. The voltage developing across R35 is applied to the amplifier U4. U4 gain of the amplifier is determined by the ratio of R39 to R38. The output voltage of U4 (pin 1) is directly-proportional to the current drawn from the battery. This indication is monitored by the microprocessor in module MCU. The microprocessor uses it to establish the maximum allowable RF output power.

(2) Main power supply (fig. 2-50, 2-51).

(a) Main power switch. The main power switch is built around the FET Q1. Q1 is controlled by the ON/OFF line connected to the ON/OFF front panel switch.

1. When the PRC-2200 is turned on, the ON/OFF line is connected to ground therefore Q1 conducts. As a result, the battery voltage is applied via the BAT IN line, inductor L1 and the drain of Q1 to the regulation circuits (pin 7 of U2 and pin 8 of U1). The battery voltage is also applied to modules MCU and RF, via the fuse FL2, the filtering network L7, C19, C18 and L6 and on the V BAT line.

2. When the PRC-2200 is turned off, the ON/OFF line is disconnected, therefore CR13 and Q1 are cut-off. As a result, the supply voltage is disconnected from the pulse width modulator U2 and the power supply is turned off.

(b) Main power supply operation (fig. 2-51). The main power supply is built around the pulse width modulator U2, FET Q5, transformers T1, T2 and T3, comparator U1-1 and transistor Q4.

1. Oscillator. The switching frequency of the pulse width modulator is determined by a sawtooth oscillator, contained in U2, whose timing components are R12 and C12. The sawtooth signal, developing across C12, is applied via the resistor R13 to the non-inverting input of the comparator contained in U2.

2. Current sensing. Current sensing is performed by the transformer T1. Current pulses flowing through the primary winding of T1 are converted to voltage pulses across the secondary winding. These voltage pulses are rectified by diode CR2.

3. Comparator. The current sense pulses are combined with the sawtooth signal, provided by the oscillator, by means of the resistors R13 and R7. The resulting signal is applied to the non-inverting input of the comparator contained in U2 (pin 3). The comparator compares this signal with the error signal. The error signal is the difference between the +2.5V reference voltage, provided by the internal reference regulator, and a sample of the +5V output voltage. The sample of the +5V voltage is applied to U2 (pin 2) via the voltage divider R20, R19.

4. The comparator output signal is a pulse whose width is controlled by the error signal: when the output voltage increases, the pulse width decreases and vice versa. Comparator output signal is applied to the output control circuit. The output control circuit controls the operation of the output push-pull stage of U2, which drives the switching FET Q5.

5. The comparator contained in U2 can receive a shut-down command from the protection circuit built around the comparator U1 and transistor Q4.

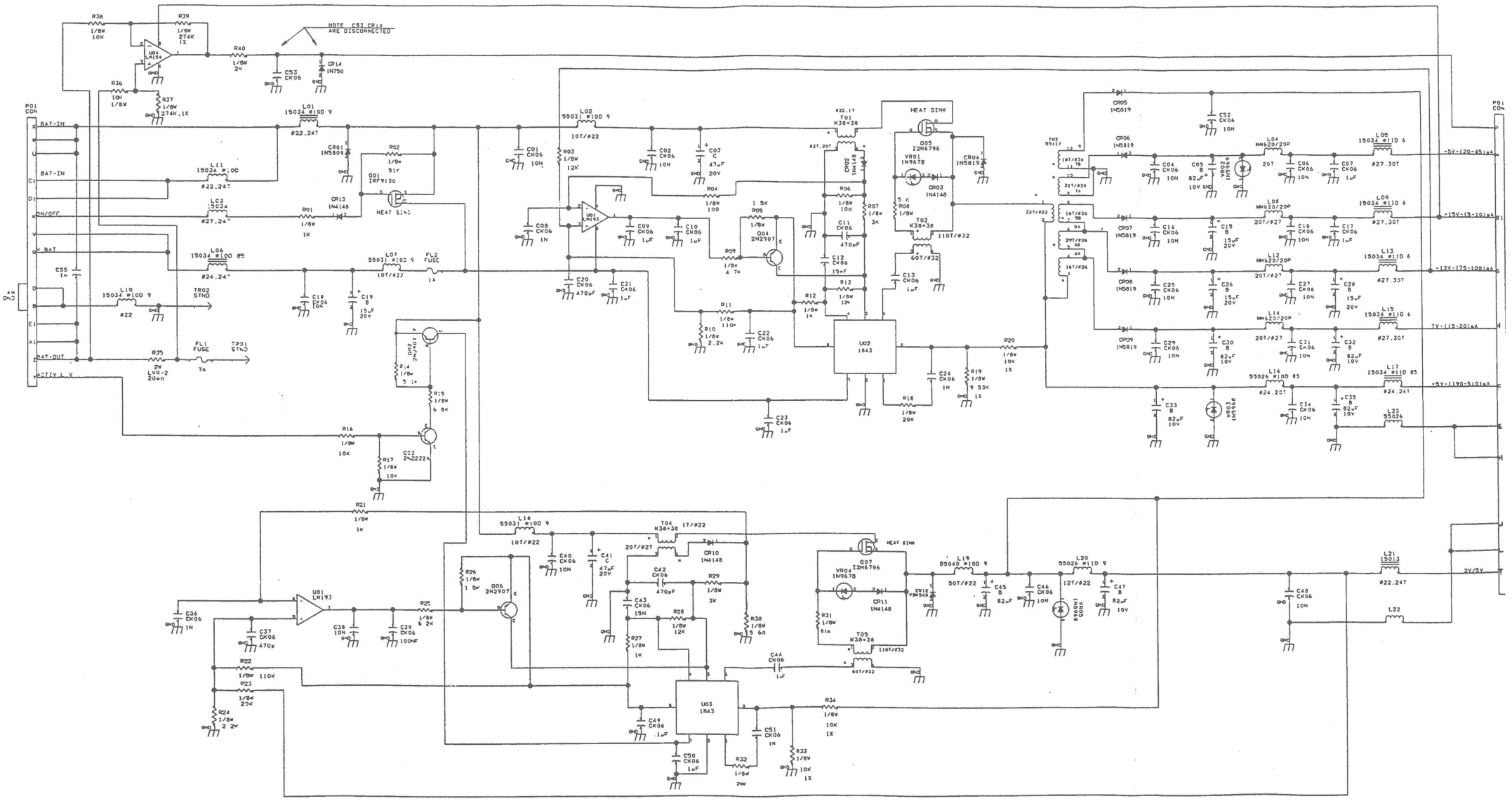


Figure 2-50. Module PS, Schematic Diagra

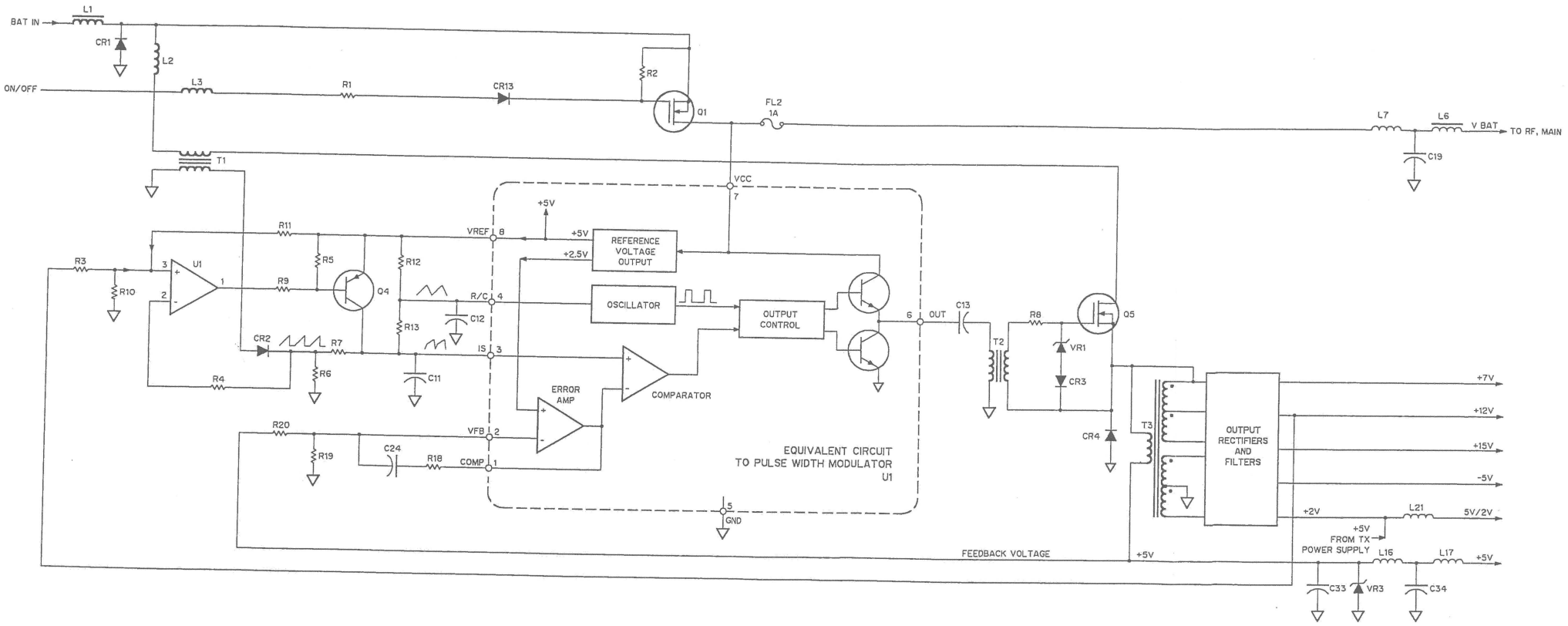


Figure 2-51. Main Power Supply, Simplified Diagram

The current pulses sampled by T1 and rectified by CR2 are applied via R4 to the inverting input of U1 (pin 2). U1 compares this signal with a sample of the +12V output voltage, connected via R3 to the non-inverting input of U1 (pin 3). Pin 3 of U1 also receives the +5V VREF voltage, connected via R11. The +5V REF voltage provides a starting voltage that prevents activation of current limiting upon turn-on, or when the +12V output voltage is missing. If the current is too high, because of overload or short-circuit, U1 output (pin 1) falls to a low level. As a result, Q4 conducts and pin 3 of U2 receives a voltage of about 1V. This voltage causes the output of U2 to remain low until the next clock cycle after the shut-down condition at pin 3 is removed.

6. Switching FET Q5. The amplified pulses appearing at pin 6 of U2 are applied to Q5, via transformer T2. These pulses drive the switching FET Q5 between saturation and cut-off. Q5 drives the primary winding of the transformer T3. The conduction of Q5 results in a square wave drive across the primary windings of T3.

7. Filtering and rectification circuits. The voltages appearing at the various secondary windings of T3 are rectified and filtered. The output voltages are all proportional to the transformer windings ratio.
Therefore, it is sufficient to monitor only one output voltage, in order to ensure that the others are within the allowable limits. The monitored voltage is the +5V output[when this voltage increases, the conduction time of Q5 is reduced, and vice versa.

8. To demonstrate the operation of the power supply, suppose that its output voltages tend to increase. In this case, the power supply output current also increases.

Therefore, the level of the current pulses flowing through the primary winding of T3 increases, and consequently the width of the pulses applied to the non-inverting input of the comparator (U2, pin 3) also increases. At the same time, the level of the error signal at the error amplifier output decreases.
As a result of these two actions, the pulse width at the comparator output decreases. The conduction time of Q5 is reduced, and thereby the power supply output voltages are decreased towards their nominal values.

(3) TX power supply.

(a) TX power supply switch. The TX power supply switch is built around transistors Q2 and Q3. The switch is controlled by the ACTIV L.V line.

1. During transmission, the ACTIV L.V line rises to a high level. As a result, Q3 and Q2 conduct. The pulse width modulator U3 (pin 7) receives the battery voltage via BAT IN, line inductor L1 and the collector of Q2. The TX power supply is therefore turned on.

2. In the receive mode, the ACTIV L.V line falls to a low level, Q3 and Q2 are cut-off, U3 is disconnected from the battery voltage, and the TX power supply is turned off.

(b) TX power supply operation. The TX power supply is built around pulse width module U3, FET Q7, transformers T4 and T5, comparator U1-7 and transistor Q6. The TX power supply operates similarly to the main power supply, described in para (2).(b) above.
In the transmit mode, the +5V voltage generated by the TX power supply reverse-biases diode CR5 (+2V output rectifier). Therefore, the +5V supply voltage replaces the +2V voltage and appears at contacts J, L and T of rear panel connector P1.

2-16. Motherboard, Module MB

a. Block Diagram Analysis (fig. 2-52). The MB module contains the interconnections among all the RT-2001 modules and the connections to the rear panel. The connections to the rear panel are made by means of a special flexible printed circuit board (PCB). One side of the flexible PCB plugs into one of the motherboard connectors, and the other side plugs into the rear panel connector and into the connector of the power supply module. In addition, module MB contains latches and buffers which distribute the control information generated by the microprocessor in module MCU to the various modules installed on the motherboard, and gather information from these modules.

Figure 2-52 shows the block diagram of the active circuits located on the MB module.

(1) The control latches transfer the information appearing on the data bus lines, DBM0 thru DBM7, to the corresponding control line of the module selected by the microprocessor.

(2) The input buffer transfers information from the RF and AUDIO modules to the data bus lines. In addition, during self-test, the buffer is also used to test the control latches, by looping back to the microprocessor one output signal from each control latch.

(3) The frequency bus control latch transfers the serial frequency data generated by the MCU module to the frequency data lines connected to the other modules. Data is latched and appears at the outputs when a complete new word is available, as indicated by the HOP BLANK signal.

b. Circuit Analysis (fig. 2-53). Figure 2-53 shows the schematic diagram of the active circuits located on the MB module.
Figure 2-54 shows the diagram of the rear flexible printed board.
Figures 2-55A thru 2-55L show the interconnections among all the RT-2001 modules.

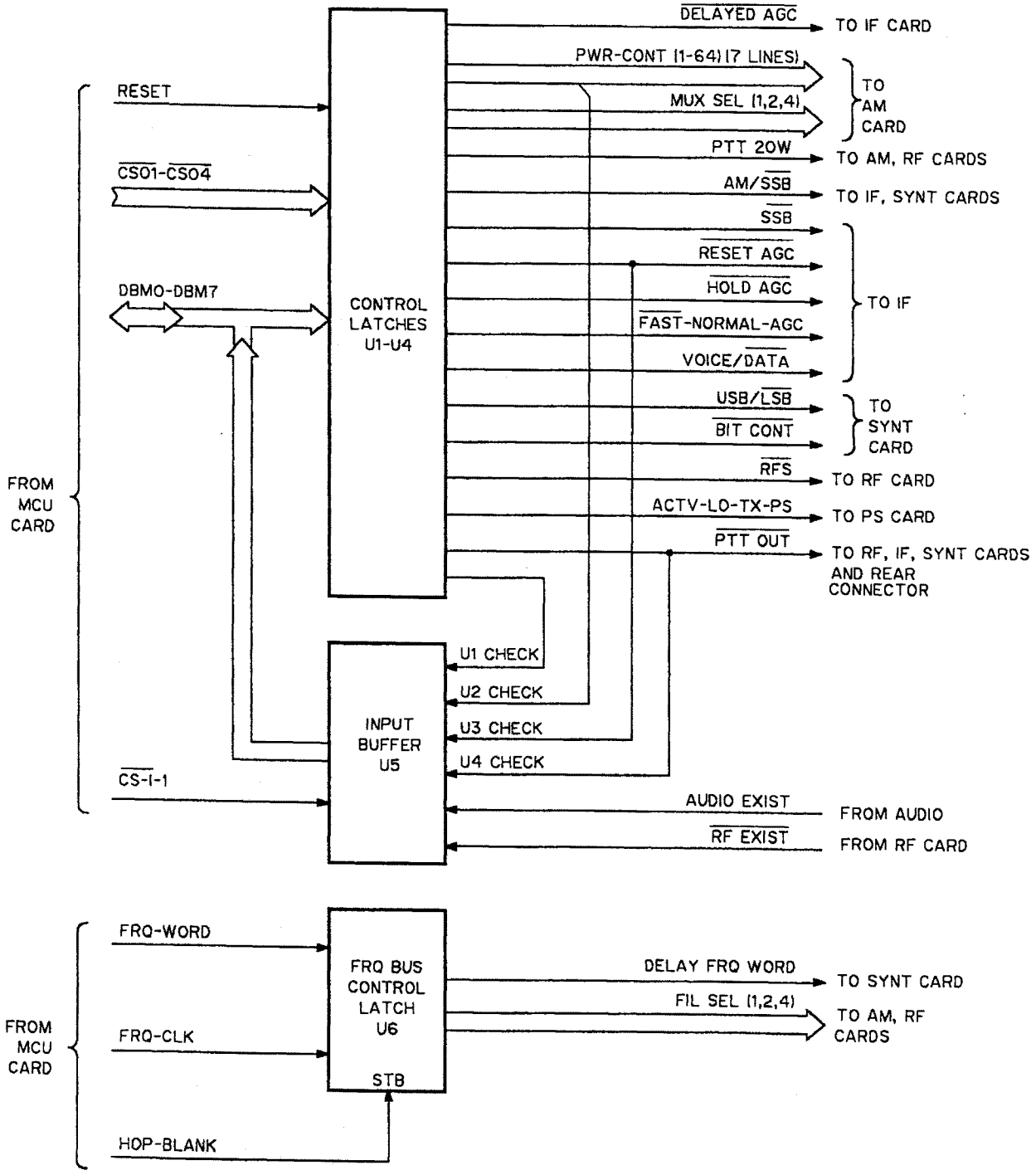


Figure 2-52. Module MB, Block Diagram

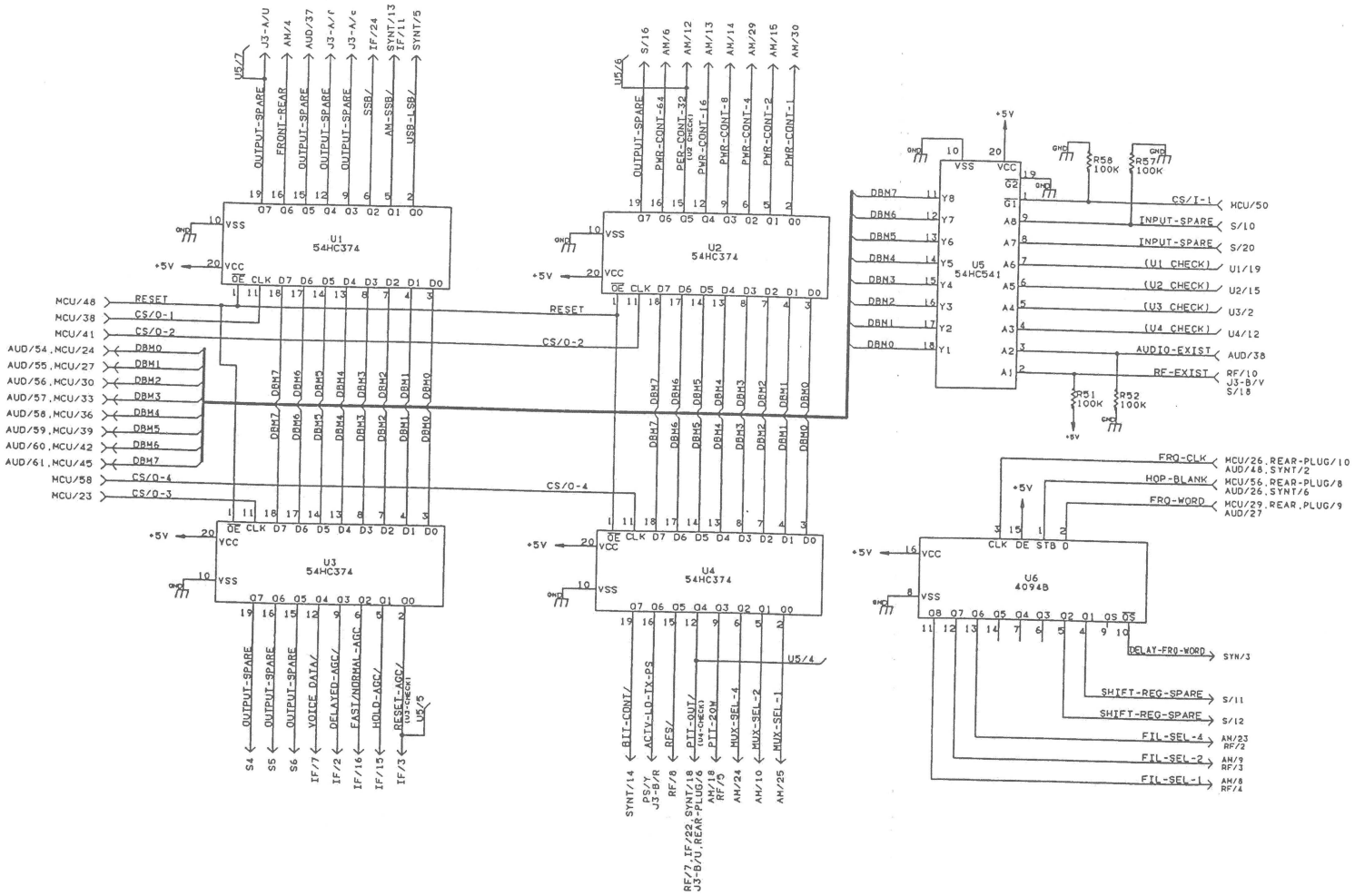


Figure 2-53. Module MB, Schematic Diagram

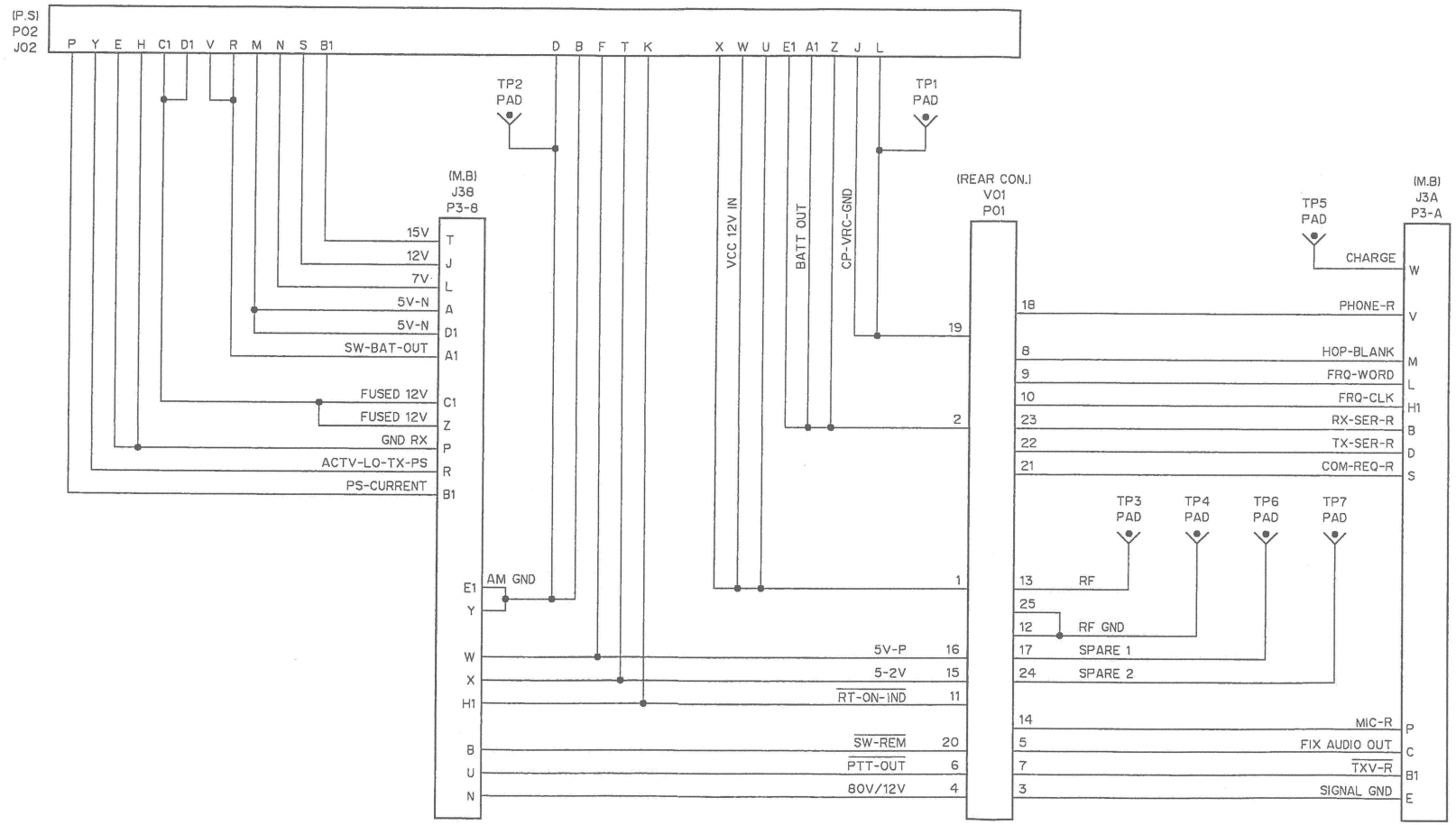


Figure 2-54. Rear Flexible Printed Board, Wiring Diagram

(1) Control latches. The latches U1, U2, U3 and U4 are used to transfer the information appearing on the data bus lines, DBM0 thru DBM7, to the control line of the module selected by the microprocessor in MCU module.

(a) Writing to latches. The microprocessor writes to the latches via the bidirectional bus lines DBM0 to DBM7. Since the data bus is connected to all the latches, a chip-select signal is used to select the desired latch (CS01* selects U1, CS02* selects U2, CS03* selects U3 and CS04* selects U4). The microprocessor sets each bit of the data byte according to the desired function. On the rising edge of the chip-select signal, the data byte is latched into the selected latch.

All four latches are controlled by the RESET line. A low level on that line enables the four latches and high level disables them.

(b) Table 2-19 lists the output lines of the control latches U1, U2, U3 and U4.

Table 2-19. Output Lines of Control Latches in Module MB

Control Latch Output	Output Line	Connected to	Function
U1 - Q0	USB/LSB*	Module SYNT	USB/LSB mode indication: "0" - LSB mode "1" - USB mode
U1 - Q1	AM/SSB*	Modules SYNT, IF	AM/SSB mode indication: "0" - SSB mode "1" - AM mode
U1 - Q2	SSB*	Module IF	SSB mode indication (active low)
U1 - Q3 to Q7	-	-	Spare

Table 2-19. Output Lines of Control Latches in Module MB (Cont'd)

Control Latch Output	Output Line	Connected to	Function
U1 - Q7	-	Input buffer U5-7	Latch U1 test
U2 - Q0 to Q6	PWR CONT lines (7 lines)	Module AM	Control lines for the 20W variable amplifier
U2 - Q5	-	Input buffer U5-6	Latch U2 test
U2 - Q7	-	-	Spare
U3 - Q0	RESET AGC*	Module IF	Reset pulse for the AGC circuits (active low)
	-	Input buffer U5-5	Latch U3 test
U3 - Q1	HOLD AGC*	Module IF	Not used (always at a high level)
U3 - Q2	$\overline{\text{FAST}}$ NORMAL AGC	Module IF	FAST/NORMAL mode indication: "0" - FAST mode "1" - NORMAL mode
U3 - Q3	DELAYED AGC*	Module IF	Always at a high level
U3 - Q4	VOICE/DATA*	Module IF	VOICE/DATA mode indication: "0" - DATA mode "1" - VOICE mode
U3 - Q5 to Q7	-	-	Spare
U4 - Q0 to Q2	MUX SEL lines (3 lines)	Module AM	Select lines for the multiplexer U502

Table 2-19. Output Lines of Control Latches in Module MB (Cont'd)

Control Latch Output	Output Line	Connected to	Function
U4 - Q3	PTT 20W	Modules AM, RF	Transmission request at a level of 20W (active high)
U4 - Q4	PTT OUT*	Modules RF, IF, SYNT and rear connector	Transmission request at a level of 100W and 20W (active low)
	-	Input buffer U5-4	Latch U4 test
U4 - Q5	RFS*	Module RF	Blank command for the RF transmit path: "0" - transmit path disabled "1" - transmit path enabled
U4 - Q6	ACTV LO TX PS	Module PS	Activation command for TX power supply (active high)
U4 - Q7	BIT CONT*	Module SYNT	Control signal for 700kHz generator (active low)

(2) Input buffer. The input buffer U5 is used for the following functions:

(a) To transfer the presence indication of modules RF and AUDIO (pins 2 and 3 of U5, respectively).

(b) To test the control latches during self-test. One output line of each of the latches U1, U2, U3 and U4 are connected to pin 7 thru 4 of U5, respectively. When testing the motherboard, the microprocessor writes known data to those latch outputs, and then reads the status of their outputs via the buffer U5 and compares it with the original data.

(c) The lines connected to pins 9 and 8 of U5 are not used.

The operation of U5 is controlled by the chip-select signal CS-I-1*, generated by the address decoder in module MCU. When this signal is at low level, the buffer U5 is enabled, and the microprocessor can read the status of the control lines connected to the inputs of U5.

(3) Frequency bus control latch. The shift register U6 transfers the serial frequency data generated by the MCU module to the frequency data lines connected to module SYNT (DELAY FRQ WORD line), and to modules AM and RF (FIL SEL lines).

The frequency data, arriving on the FRQ WORD line from module MCU is applied to the D input of U6 (pin 2). The data is accompanied by the FRQ CLK signal applied to the clock input of U5 (pin 3). The data is latched and appears at the outputs of U6 when a complete new word is available, as indicated by the HOP BLANK signal connected to the strobe input of U6 (pin 1).

The frequency data sent to module SYNT via the DELAY FRQ WORD line is 8 bits delayed from the frequency data arriving on the FREQ WORD line from module MCU.

Figures 2-55A to 2-55L.

MB INTERCONNECTION

AUDIO SIGNALS & CONTROL LINES

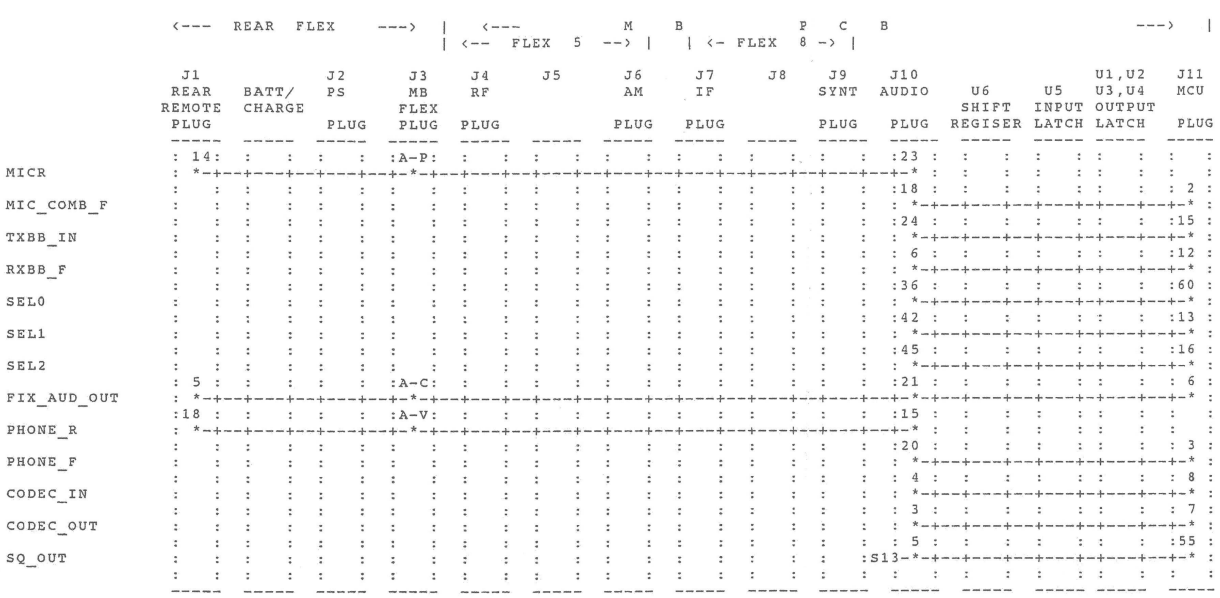


Figure 2-55A. Audio Signals and Control Lines (sheet 1 of 2)

MB INTERCONNECTION

AUDIO SIGNALS & CONTROL LINES

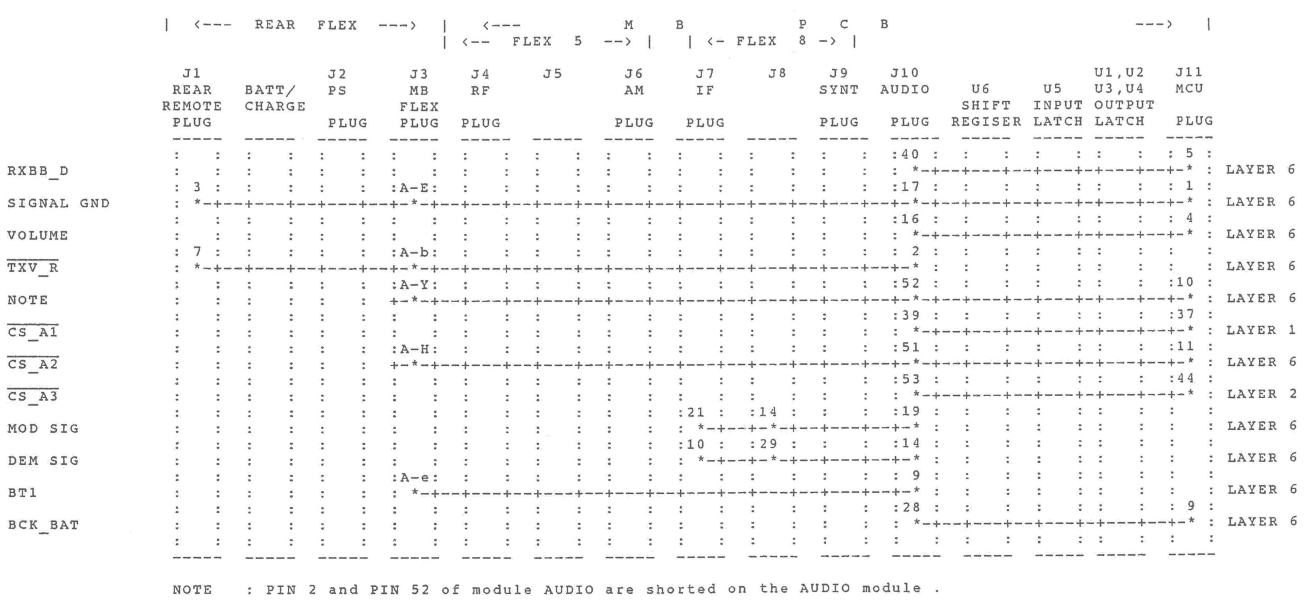


Figure 2-55A. Audio Signals and Control Lines (sheet 2 of 2)

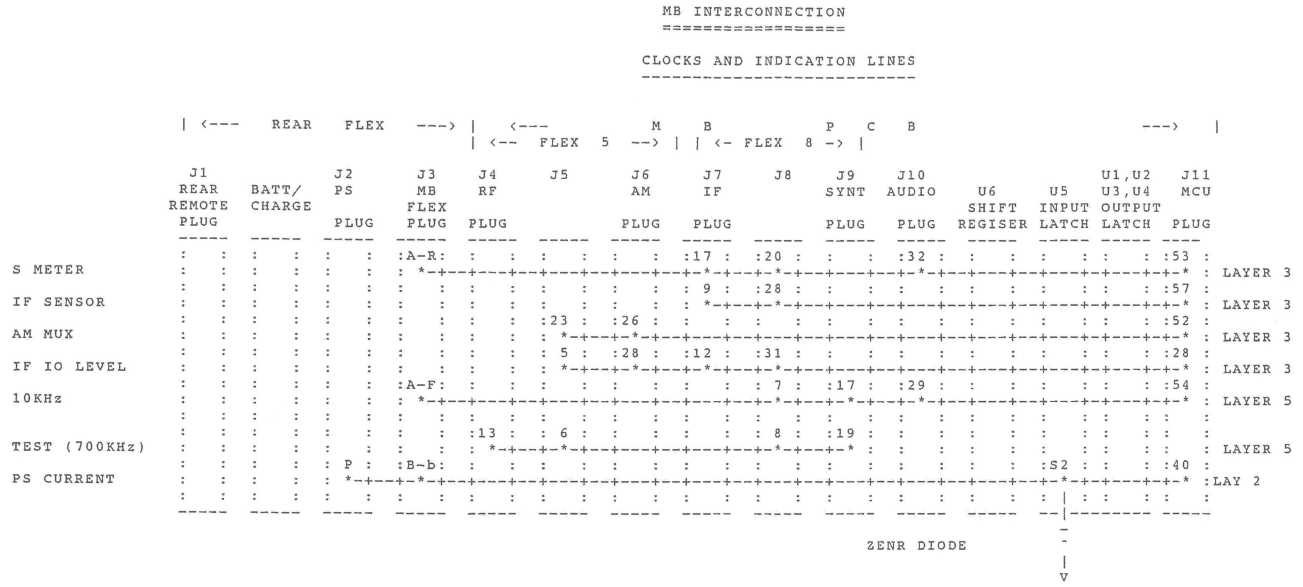


Figure 2-55B. Clock Signals and Indication Lines

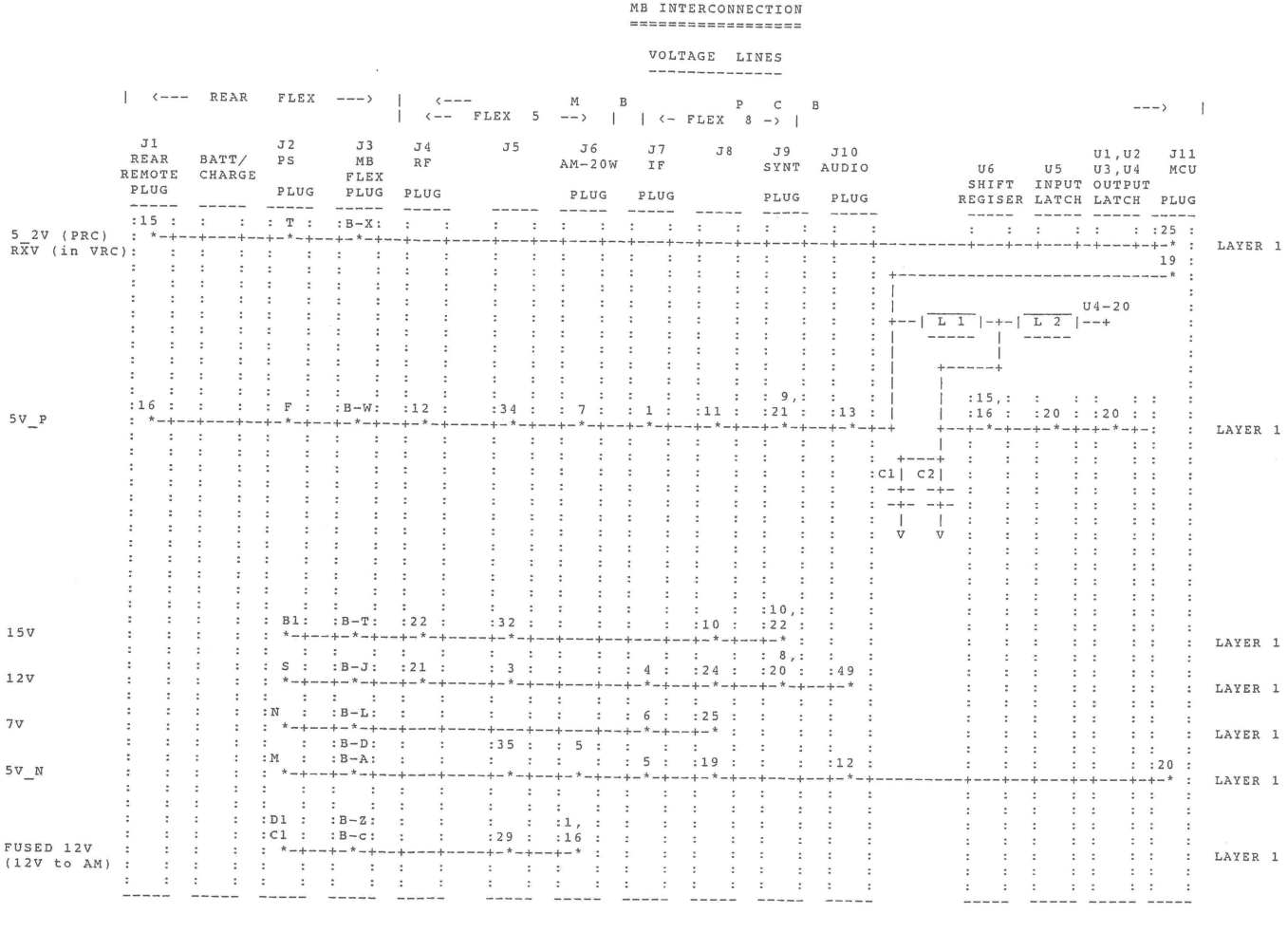


Figure 2-55C. Voltage Lines (Sheet 1 of 3)

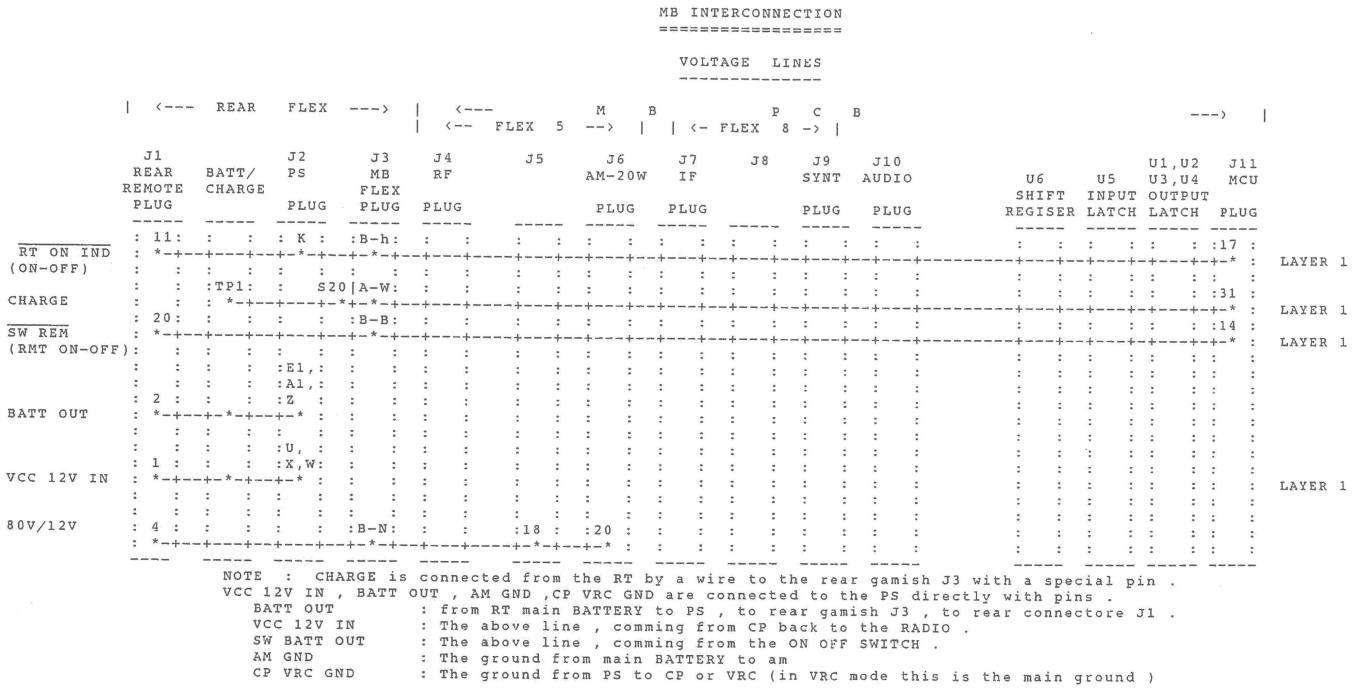


Figure 2-55C. Voltage Lines (Sheet 2 of 3)

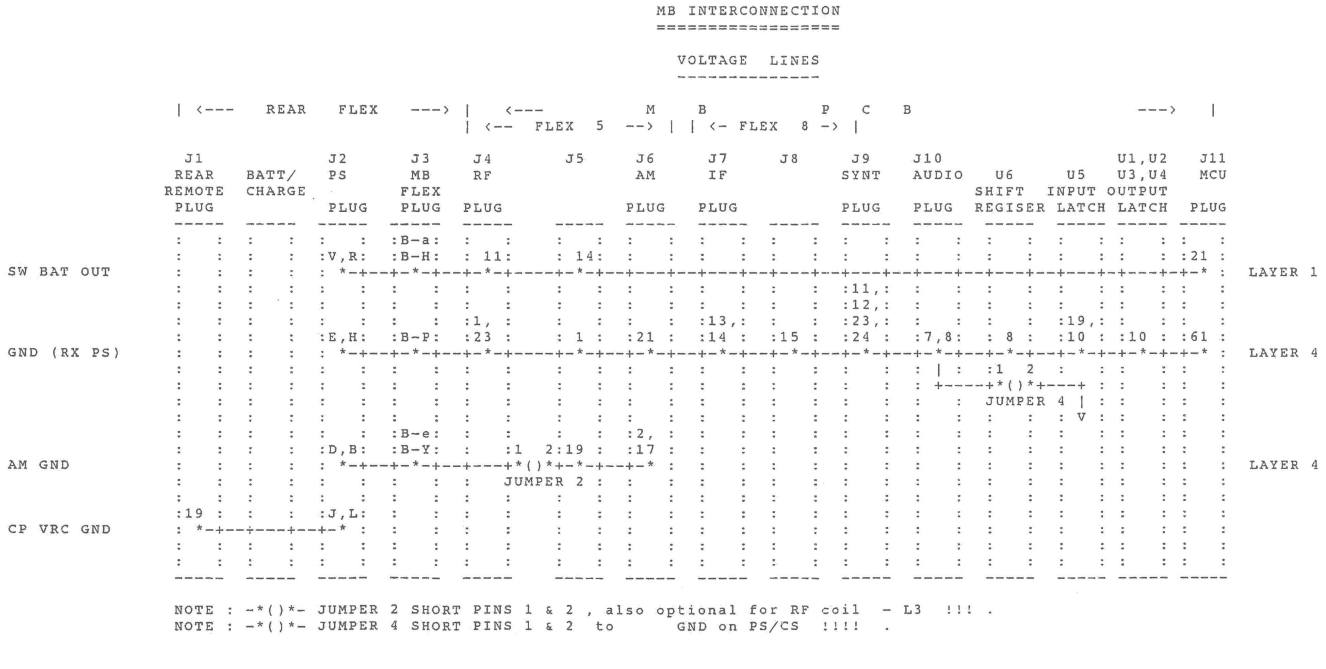


Figure 2-55C. Voltage Lines (Sheet 3 of 3)

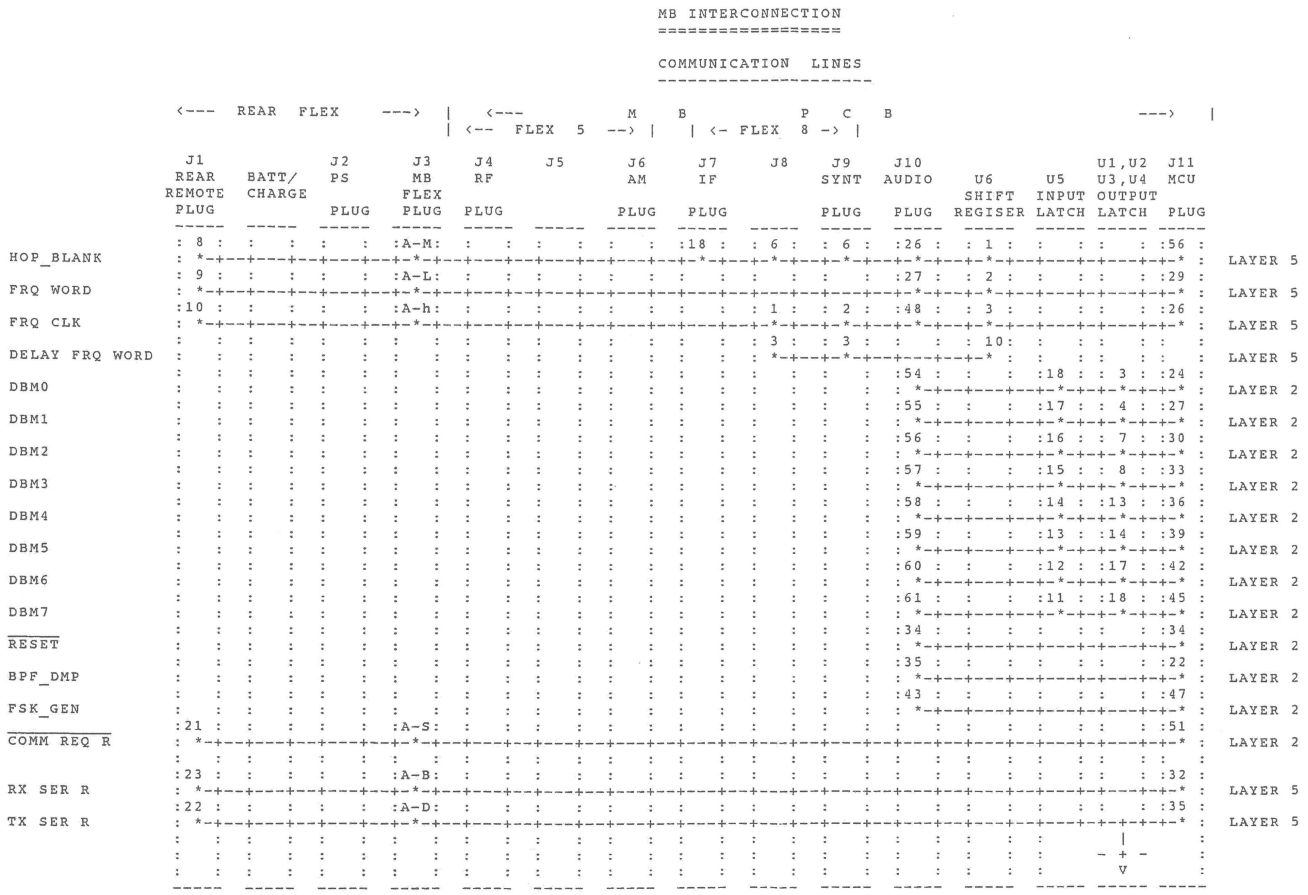


Figure 2-55D. Communication Lines

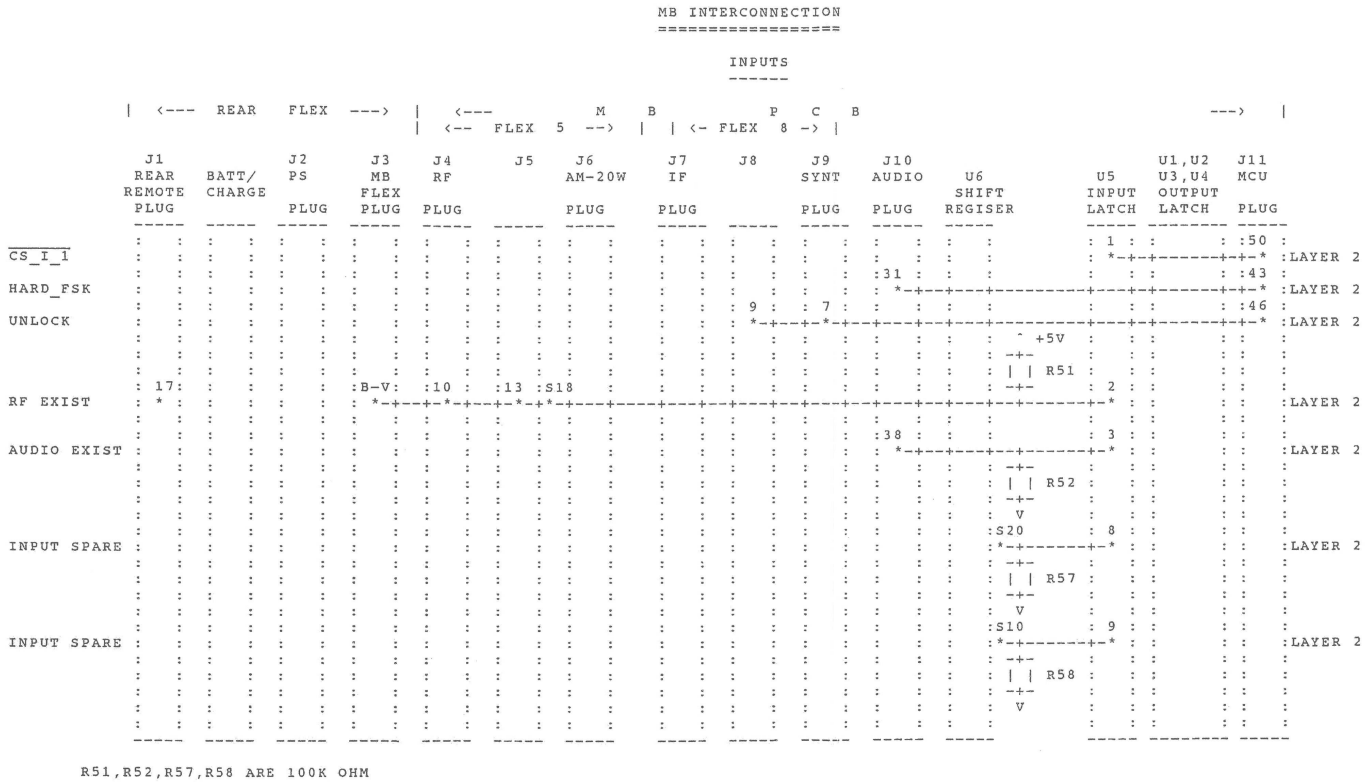


Figure 2-55E. Input Signals

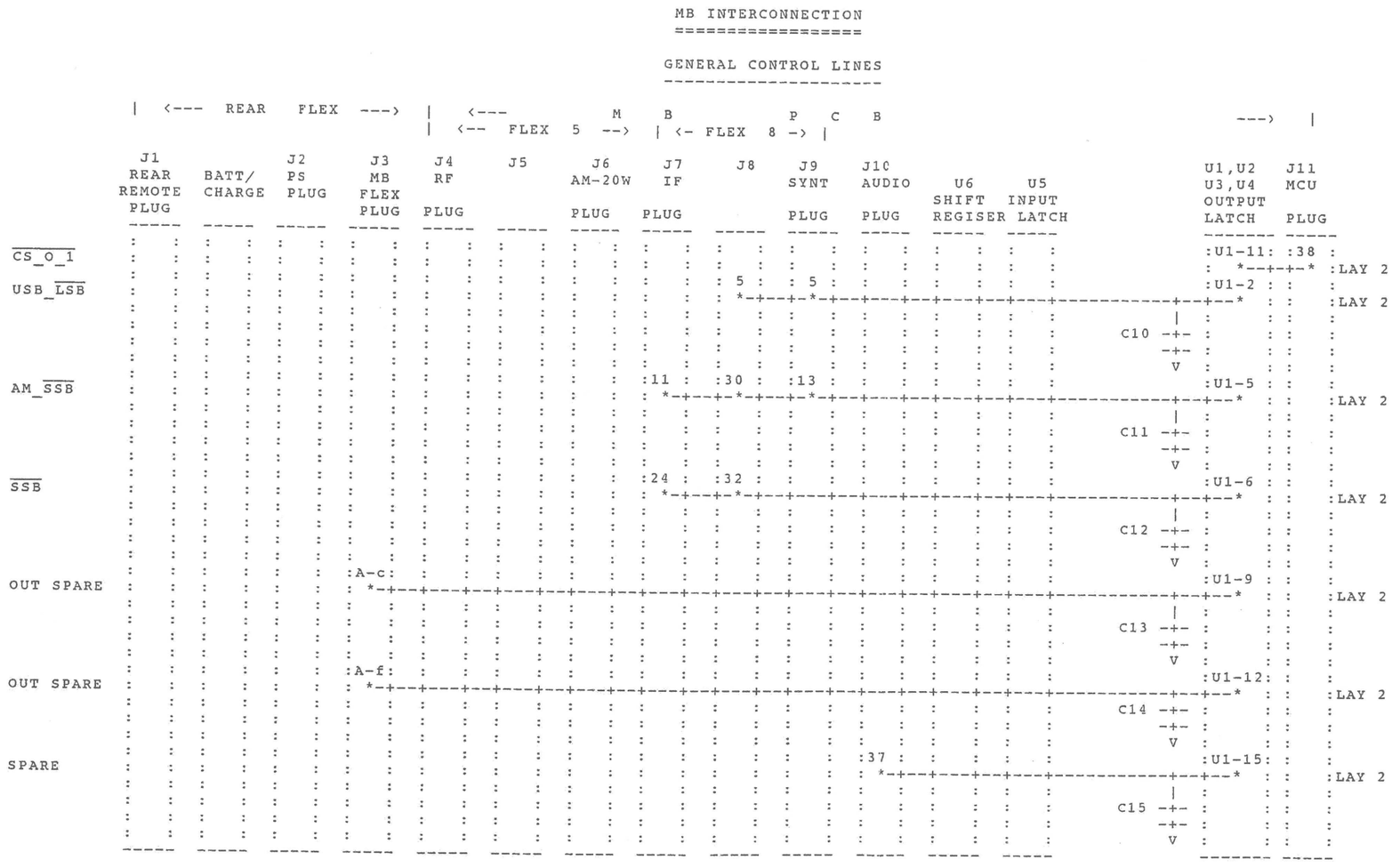


Figure 2-55F. General Control Lines (Sheet 1 of 2)

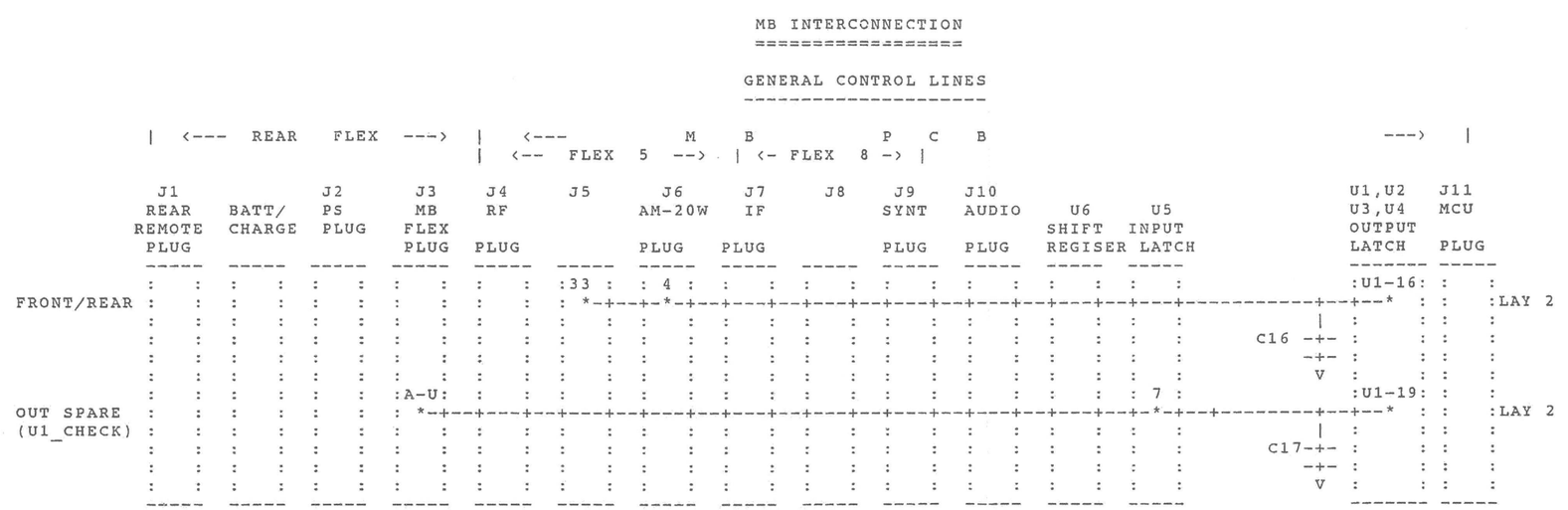


Figure 2-55F. General Control Lines (Sheet 2 of 2)

MB INTERCONNECTION

POWER CONTROL LINES

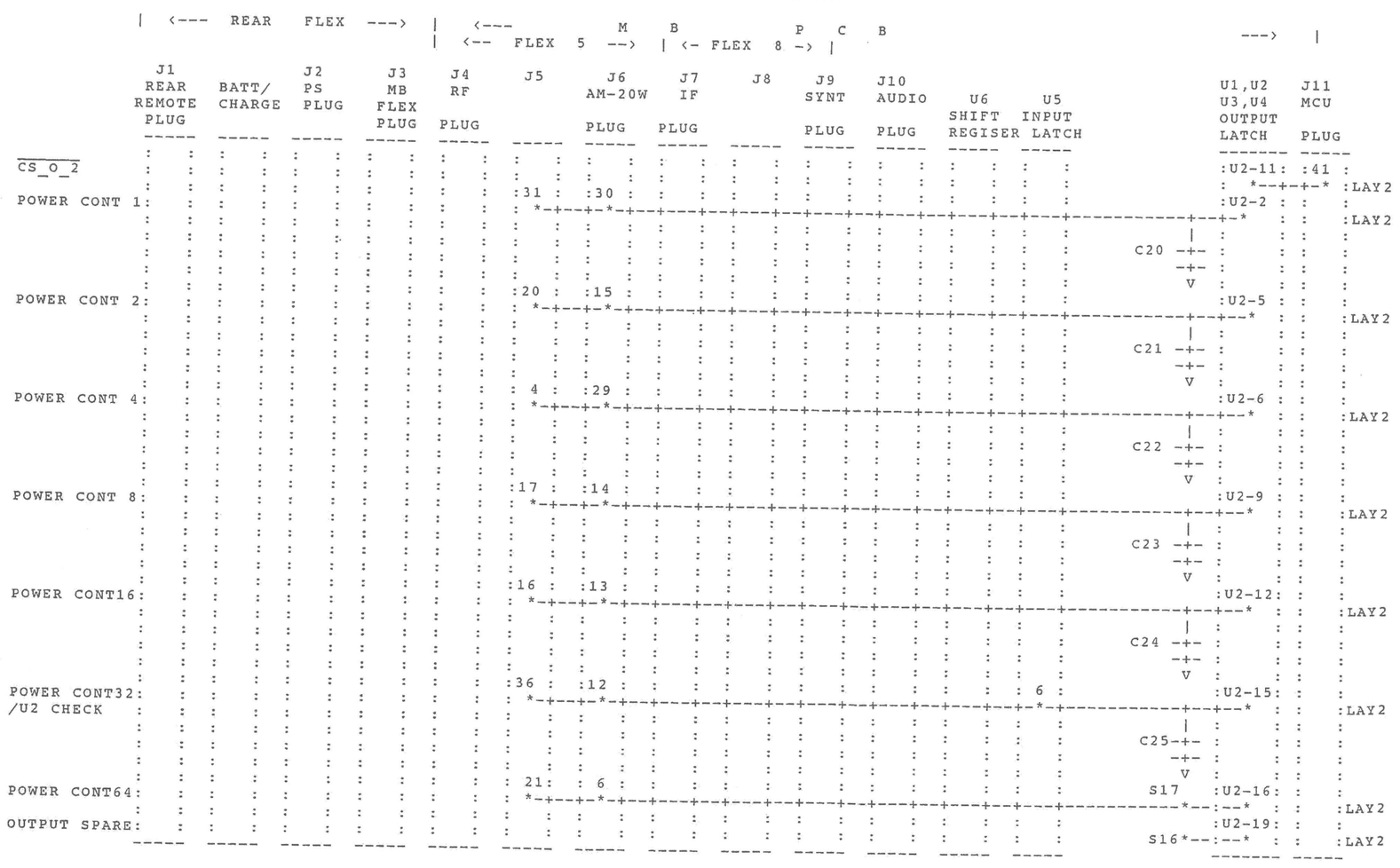


Figure 2-55G. Power Control Lines

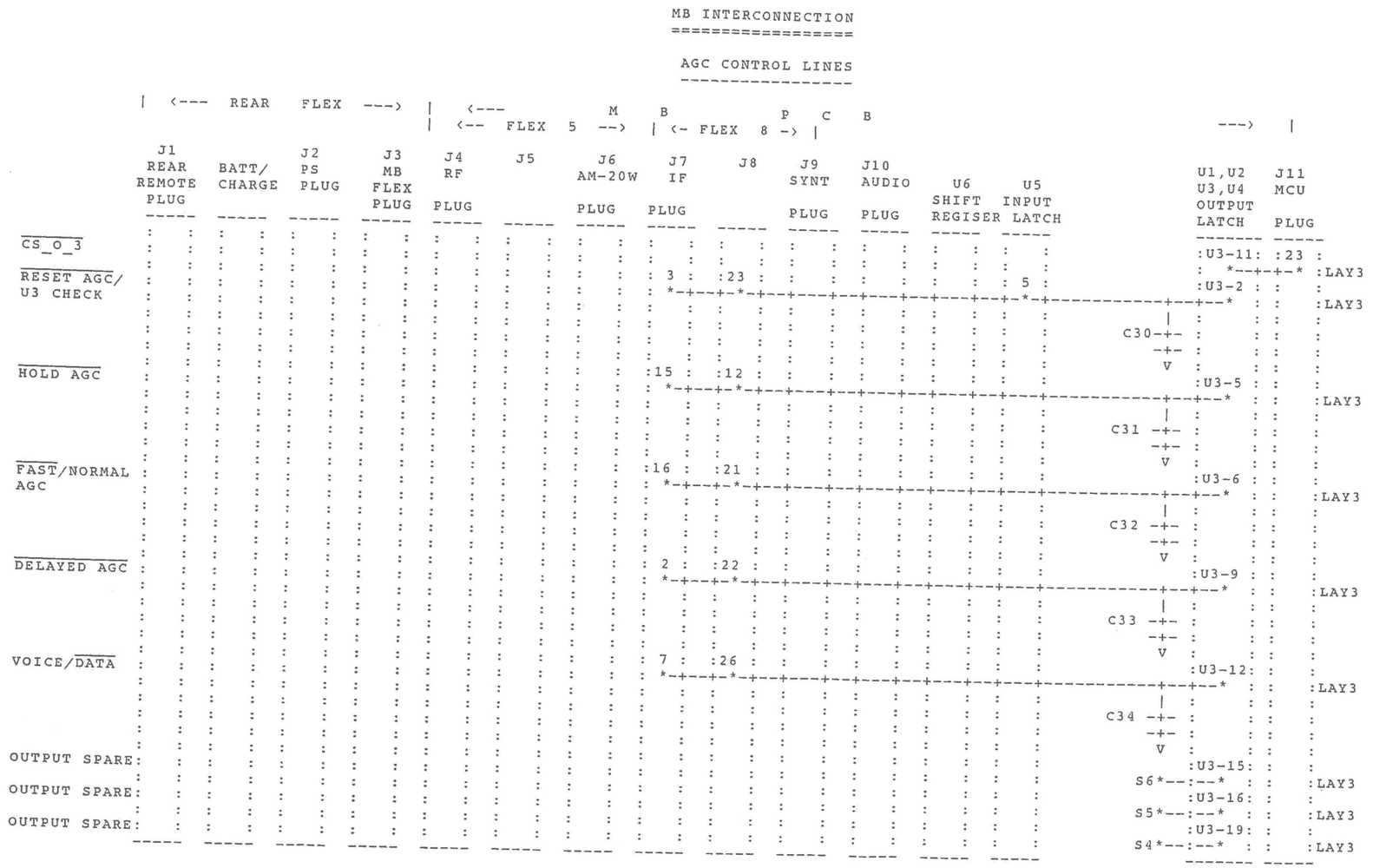


Figure 2-55H. AGC Control Lines

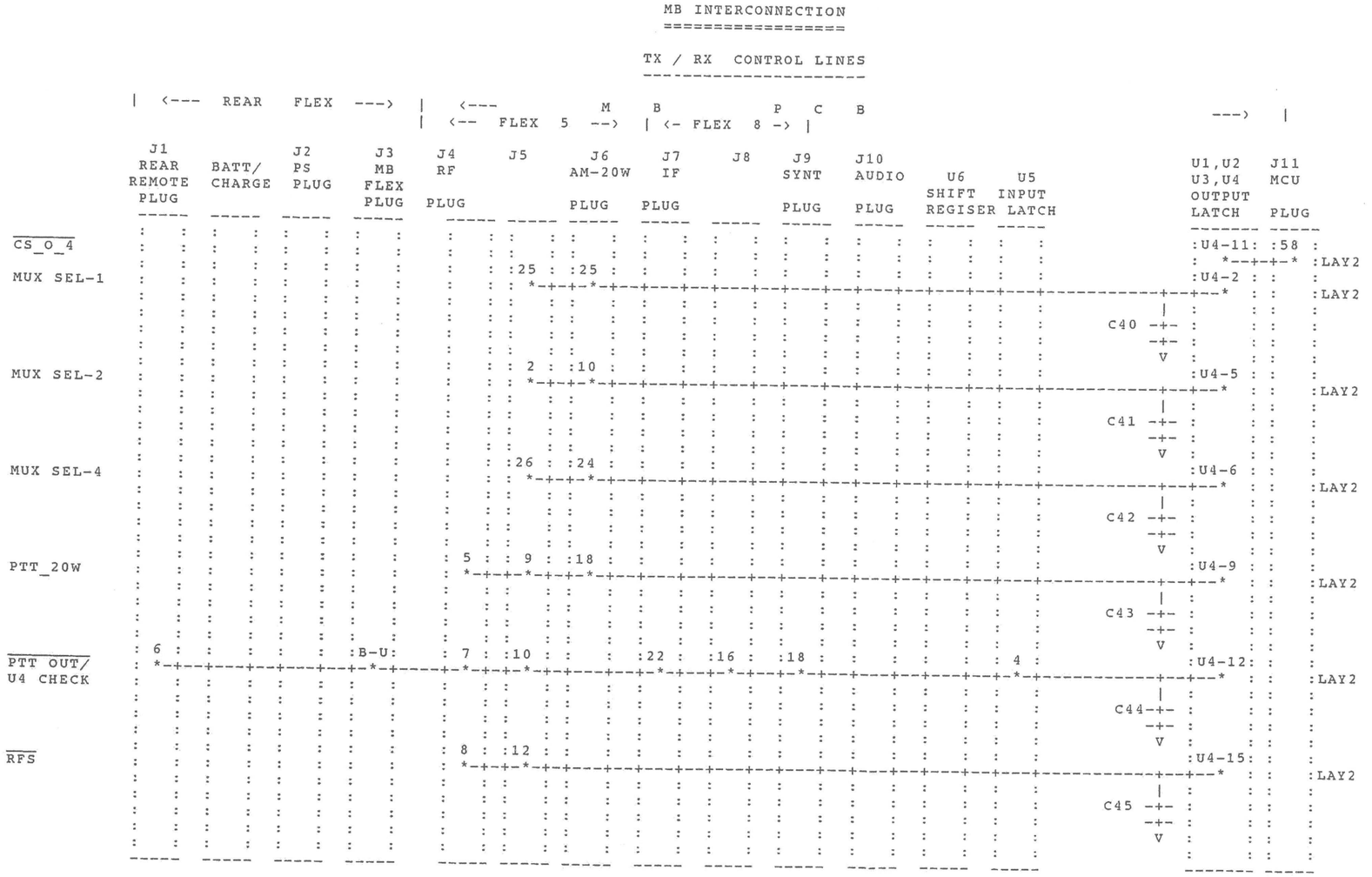


Figure 2-55I. TX/RX Control Lines

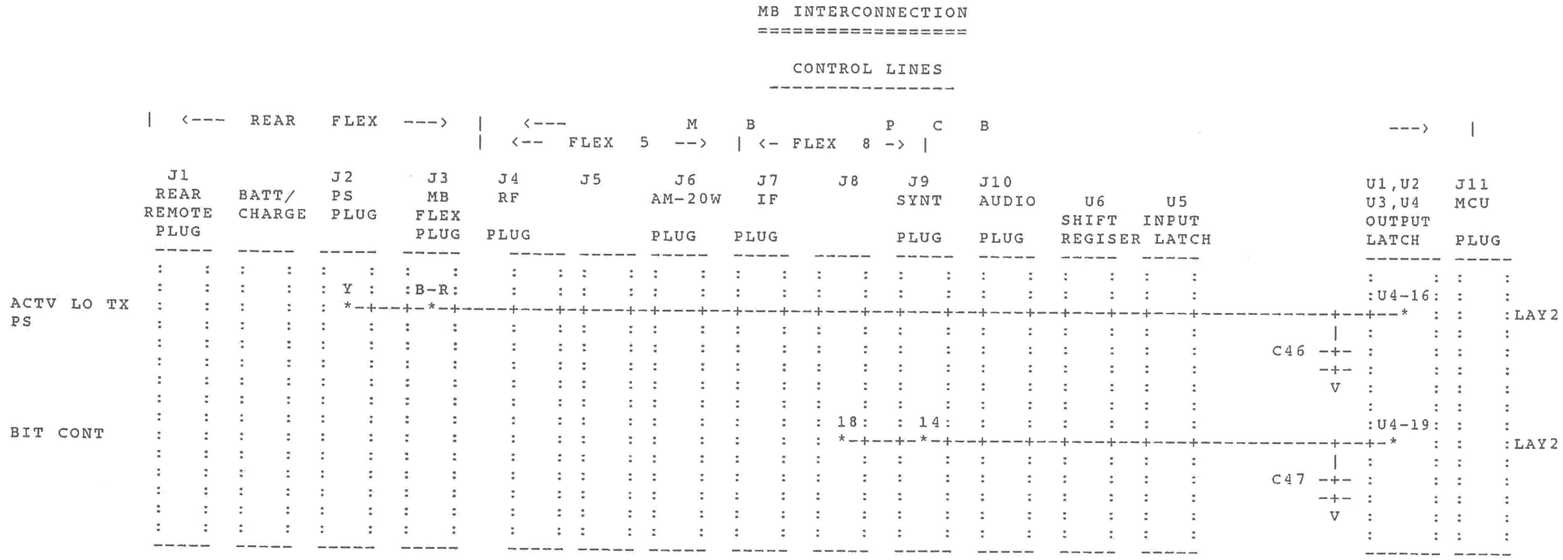


Figure 2-55J. General Control Lines (Sheet 1 of 2)

MB INTERCONNECTION

GENERAL CONTROL LINES

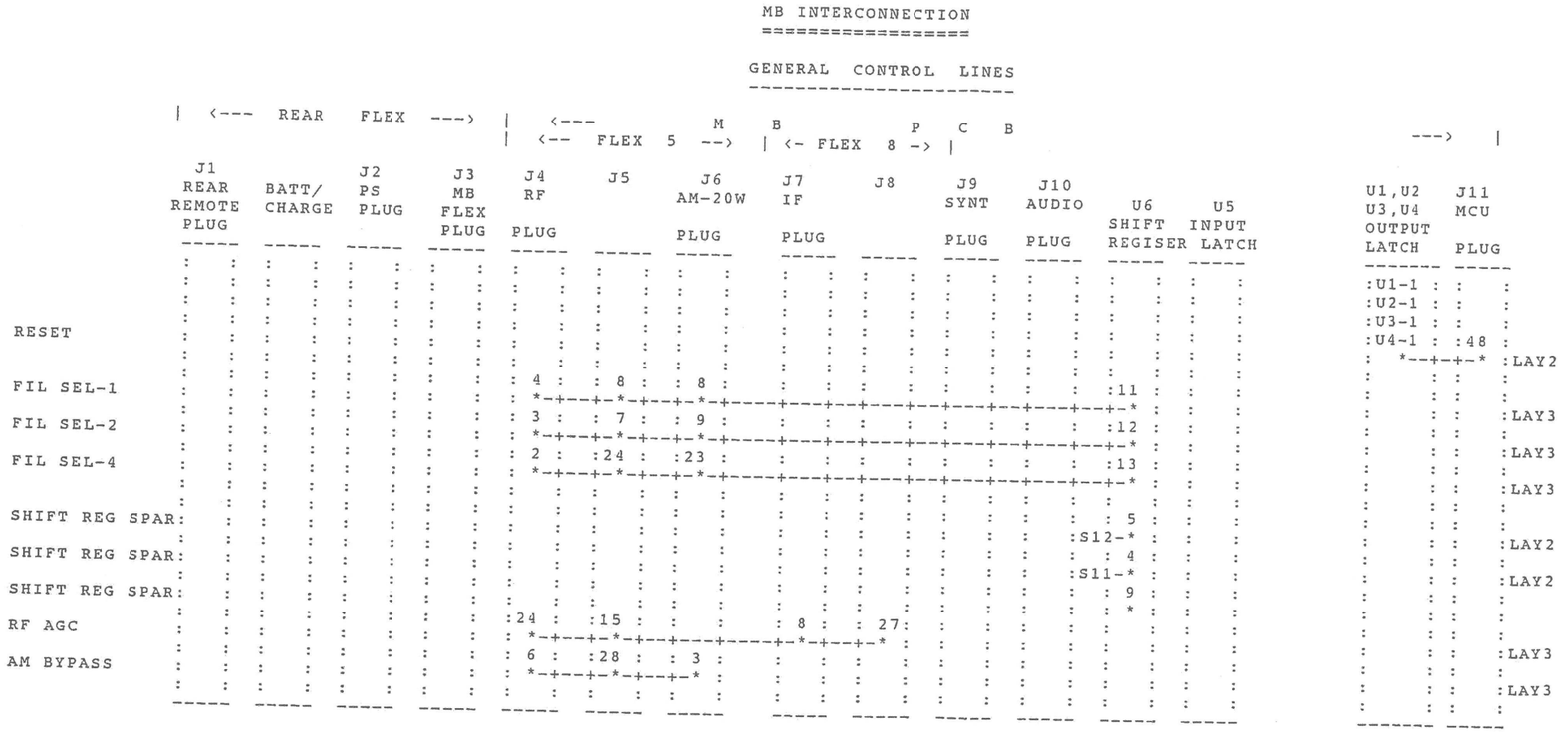


Figure 2-55J. General Control Lines (Sheet 2 of 2)

MB INTERCONNECTION

MODULE SPARE LINES

	<--- REAR FLEX --->	<--- FLEX 5 -->	M B <- FLEX 8 -> P C B	--->
	J1 REAR REMOTE PLUG	BATT/ CHARGE	J2 PS PLUG	J3 MB FLEX PLUG	J4 RF PLUG	J5	J6 AM-20W PLUG	J7 IF PLUG	J8	J9 SYNT PLUG	J10 AUDIO PLUG	U6 SHIFT REGISER	U5 INPUT LATCH	U1,U2 U3,U4 OUTPUT LATCH	J11 MCU PLUG	
MCU SPARE								18							18	
MCU SPARE															59	
IF SPARE 3								19	13					S3	S15	LAY 2
IF SPARE 2								20								LAY 2
IF SPARE 1								23								
RF SPARE					14											
RF SPARE					15											
RF SPARE					16											
RF SPARE					17											
RF SPARE					18											
RF SPARE					9											
RF SPARE					19	11		S19								LAY 2

Figure 2-55K. Spare Lines (Sheet 1 of 3)

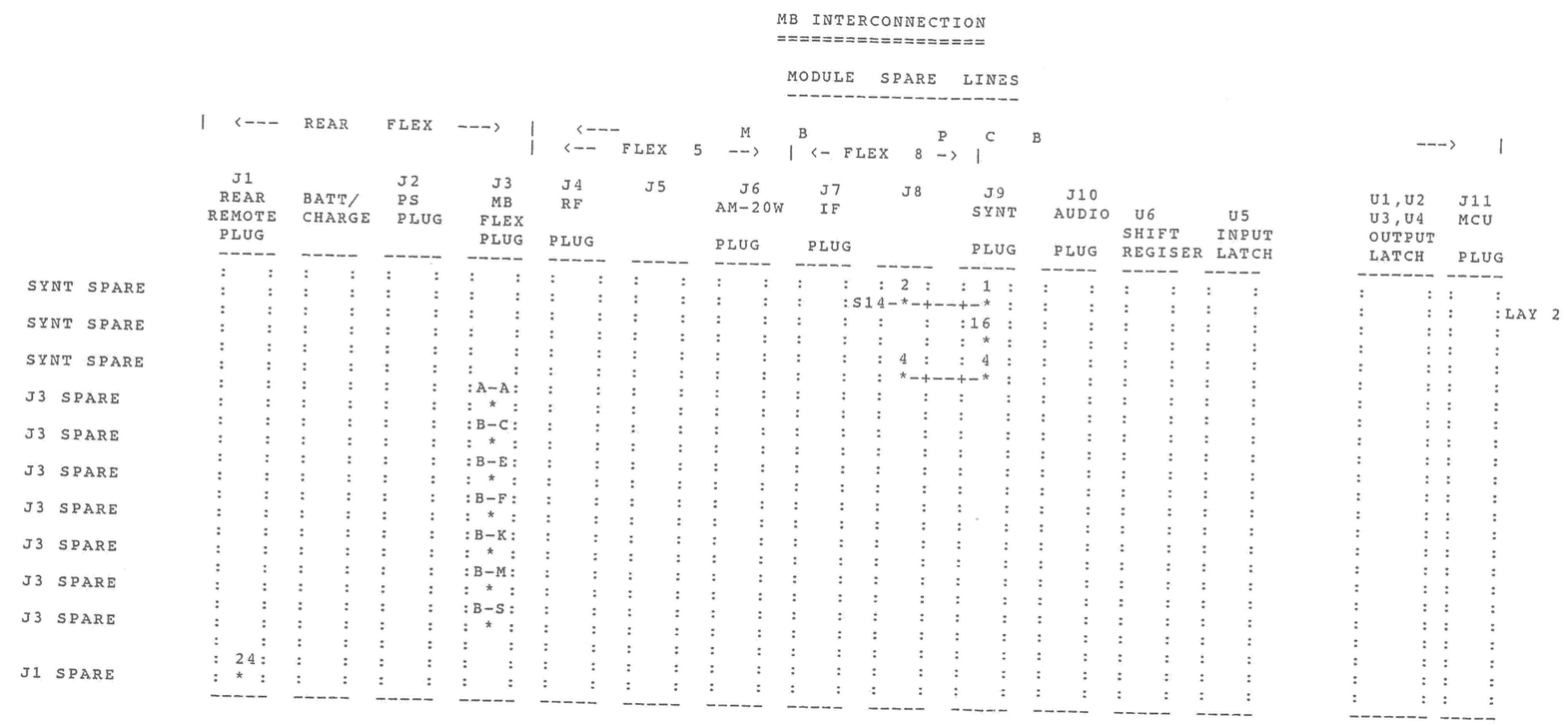


Figure 2-55K. Spare Lines (Sheet 2 of 3)

MB INTERCONNECTION

MODULE SPARE LINES

	J1 REAR REMOTE PLUG	BATT/ CHARGE	J2 PS PLUG	J3 MB FLEX PLUG	J4 RF PLUG	J5	J6 AM-20W PLUG	J7 IF PLUG	J8	J9 SYNT PLUG	J10 AUDIO PLUG	U6 SHIFT REGISER	U5 INPUT LATCH	U1,U2 U3,U4 OUTPUT LATCH	J11 MCU PLUG	
	<--- REAR FLEX --->				<-- FLEX 5 -->		<- FLEX 8 ->									--->
AM SPARE							11									
AM SPARE						30	19									
AM SPARE						27	22									
AM SPARE						22	27									
AUDIO SPARE				A-J							25					
AUDIO SPARE				A-Z							41					LAY 6
AUDIO SPARE				A-X							44					LAY 6
AUDIO SPARE				A-T							50					LAY 6
AUDIO SPARE				A-N							1					LAY 6
AUDIO SPARE				A-a							46					LAY 6
AUDIO SPARE				A-K							47					LAY 6
AUDIO SPARE				A-d							11					LAY2
AUDIO SPARE											10					LAY 1

Figure 2-55K. Spare Lines (Sheet 3 of 3)

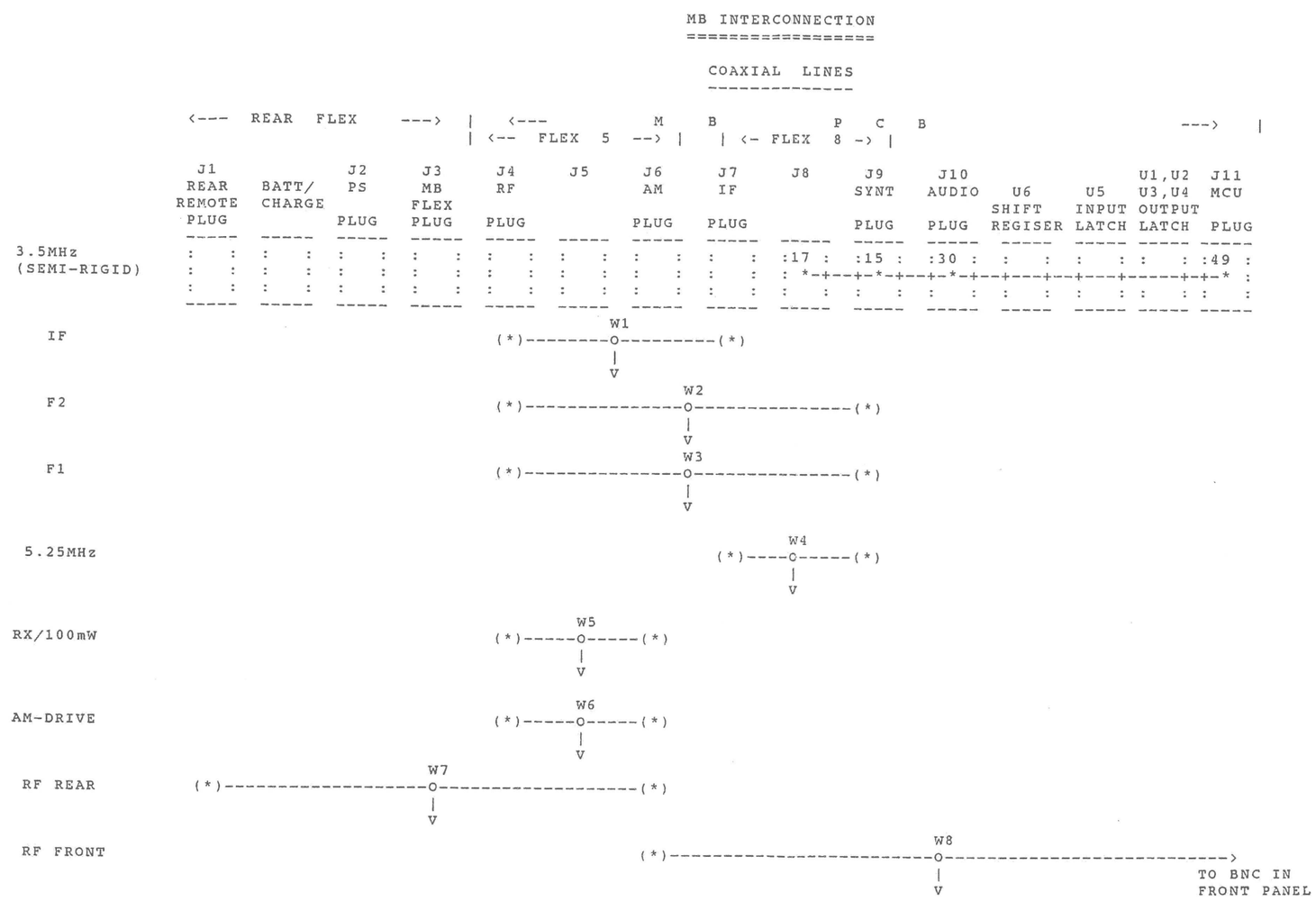


Figure 2-55L. Coaxial Lines