CHAPTER 4

FREQUENCY PROCESSING UNIT

Contents

Tables

Illustrations

INTRODUCTION

1. The Frequency Processing Unit essentially comprises two printed circuit board assemblies as follows:

(a) Synthesiser PCB

This p.c.b., which incorporates frequency synthesis circuits, is a standard assembly which, in addition to being fitted into the FPU, is also used in the non-hopping Synthesiser.

The function of this p.c.b. is as follows:

(i) To generate any one of 28 400 stable frequencies, having increments of 1kHz within the frequency band 37MHz to 65,399MHz, for use as the first mixing frequency in the Transceiver. The frequency generated, determined by the setting of the Front Panel FREQUENCY switches which select the operating frequency, is equal to the operating frequency plus 35,400MHz.
An INTERPOLATE facility is provided. This may be switched in to enable the selected frequency to be varied over ± 500Hz.

(ii) To generate a fixed 35,400 MHz for use as the second mixing frequency and the SSB suppressed carrier reinsertion frequency.

The stability of these two frequencies is the same as that of the TCXO fitted, ie. 2p.p.m. Provision is made to correct frequency shift resulting from ageing.

(b) Generator PCB

The Generator p.c.b. incorporates a microprocessor based system which is capable of controlling the Synthesiser so that the operating frequency 'hops' in a pseudo random manner. The bandwidth over which hopping occurs and the rate of hopping is controlled by the microprocessor. The pseudo random sequence is programmed by the operator from a front panel 6-digit CODE switch.

CONSTRUCTION

2. The FPU which includes a front panel and chassis, fits into the Reciter assembly through a front panel aperture.

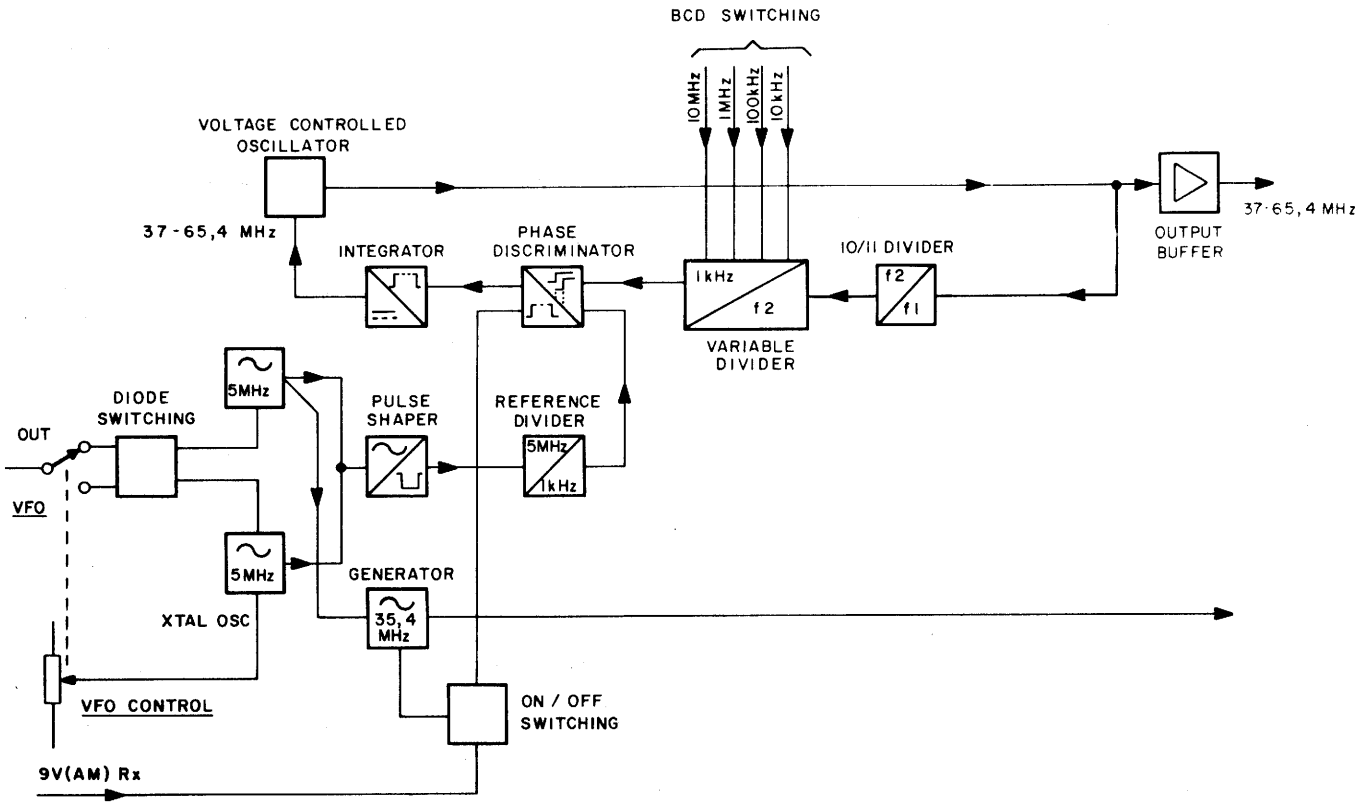
3. The procedure to install the FPU is as follows:

(i) Remove the sub-panel at the rear of the Transceiver by releasing the two Dzus fasteners.
(ii) Slide the FPU into the aperture in the Reciter front panel.
(iii) Secure the FPU by tightening the captive screws in the Reciter frame at rear of the Transceiver.
(iv) Connect the following loom sockets to the corresponding plugs in the rear panel of the FPU.
  (a) coaxial socket SK21 to plug PL21
  (b) coaxial socket SK22 to plug PL22
  (c) 25 way socket SK5 to plug PL5
  (d) 9 way socket SK19 to plug PL19
(v) Replace sub-panel at rear of the Transceiver.

4. The removal procedure is the reverse of the above.

SYNTHESISER PCB

GENERAL DESCRIPTION



5. The Synthesiser essentially comprises a voltage controlled oscillator (VCO), whose frequency is compared with that of a 1 kHz standard, derived from a temperature compensated crystal oscillator (TCXO). When the VCO output is at the same frequency as set at the Front Panel FREQUENCY selectors plus 35,400 MHz, a comparison circuit feeds a steady d.c. control voltage to the VCO frequency determining circuits, to maintain that condition. If the VCO output is not at the selected frequency, this is detected and an admustment is made to the level of the control voltage in order to correct the frequency of the VCO output.

6. Frequency comparison can only be made if the standard and Synthesiser frequencies are of the same order. The Synthesiser frequency can be any one of the 28 399 frequencies within the range 37,000 MHz to 65,399 MHz and some means is required of reducing each of these to the 1 kHz standard. This is achieved by sampling the Synthesiser output frequency and feeding the resulting pulses into digital circuits, which give an output after a predetermined number of input pulses have been counted. The resulting train of output pulses is at exactly the same frequency as the standard frequency when the Synthesiser output frequency is correct.

7. Brief descriptions of the principal stages of the Synthesiser are given in the following paragraphs.

Voltage Controlled Oscillator (VCO)

8. The VCO is basically an oscillator whose frequency is controlled by a d.c. voltage applied to varicap diodes in a tuned circuit. The oscillator output signal is compared with the standard frequency signal derived from the TCXO. Any difference in phase between these two signal results in an adjustment to the d.c. control voltage fed to the VCO varicaps. The output signal is a sine wave having a frequency 35,400 MHz above the frequency selected at the front panel FREQUENCY switches. The signal is fed through a buffer amplifier to the transceiver mixing circuits.

Divider Chain

9. A sample of the VCO output is taken through a separate buffer amplifier to a shaper circuit. This provides a square wave output, at the VCO frequency, which is fed to a divider chain comprising a 10/11 divider and a variable divider. The 10/11 divider gives the division ration required to convert f2 in the variable divider (programmed from the FREQUENCY switches) into an output of exactly 1 kHz if the VCO output is at the frequency set on the front panel switches plus 35,400 MHz. If the VCO frequency is high the pulse train frequency is greater than 1 kHz and if low, less than 1 kHz.

Phase Discriminator and Integrator

10. The divider chain output is fed to the phase discriminator, together with the pulse train at the standard frequency generated by the TCXO. In this circuit, the two inputs control two interconnected switching circuits whose outputs depend on the phase difference between individual pulses in the two trains. Each output controls one of two switching transistors. Depending on the phase relationship between the pulses in the two pulse trains (which, in turn, depends on whether the VCO frequency is higher or lower than the required frequency), an output is fed to one or the other transistor. If the VCO frequency is low the switched transistor allows a capacitor in the integrator to charge. The charging period depends on the phase difference: generally, the greater the difference the longer the charging period. If the VCO frequency is high the other transistor is brought into conduction and allows the capacitor charge to leak away. The discharge period again depends on the phase difference. The level of the control voltage fed from the integrator to the VCO varicaps is directly related to the resultant charge on the capacitor. A high charge (VCO frequency low) results in an increase in the voltage across the varicaps and hence an increase in VCO frequency. A low charge (VCO) frequency high) decreases the varicap voltage and so decreases the VCO frequency.

5 MHz Oscillator (TCXO)

11. The standard frequency with which the output from the variable divider is compared, is derived from a 5 MHz TCXO. This frequency is passed through a pulse shaper. The resulting square waves are fed to a set of series-connected integrated circuits, which divide the 5 MHz by 5000 to give a 1 kHz output. The TCXO used has a tolerance of ±2ppm so that the standard frequency from the divider is 1 kHz ±0,002 Hz.

35,4 MHz Generator

12. The 35,4 MHz generator comprises a crystal controlled oscillator and amplifier. Adjustments to the oscillator frequency are made by means of a varicap diode. The d.c. control voltage is produced by comparing the oscillator output with a reference signal derived from the TCXO 5 MHz output.

5 MHz Oscillator (Interpolate)

13. Provision is made for the operating frequency to be offset by up to ± 500 Hz. When this function is required the VFO control is set away from OUT. The input to the reference divider chain is then switched from the TCXO to the 5 MHz interpolate oscillator, the frequency of which can be adjusted over an approximate range of 5 MHz ± 100 Hz. Selection of the TCXO or the crystal oscillator is by diode switching controlled, by a single pole switch ganged to the VFO control.

CIRCUIT DESCRIPTION

14. Refer to Figure 3, Sht 1.

Voltage Controlled Oscillator (VCO)

15. The oscillator circuit comprises a depletion type, field effect transistor, TR8, with drain to gate feedback through a frequency determining pi-network formed by a coil and two varicap diodes. These diodes act as capacitors, the capacitance depending on the voltage across the diode; the higher the voltage the lower the capacitance. In this circuit a voltage range of between approximately 3V and 16V provides variation in capacitance to cover the complete band of VCO frequencies. The 180° phase shift between drain and gate necessary to maintain oscillation is provided by the pi-network and the parallel circuit C21, R23. The phase shift across this latter circuit varies slightly with frequency and compensates for inherent phase change in the pi-network. The gain of the oscillator transistor is fixed by the bias applied to the second gate from potential divider R28, R29. The oscillator operates continuously to provide a sine wave output in the range 37,000MHz to 65,399MHz. This is fed via the output buffer stage, which consists of two transistors connected in a cascade configuration to give high gain with good isolation, to the output stage.

16. The oscillator output is also sampled and applied via TR15 to the 10/11 dividers IC18. TR15 ensures that the correct signal levels are applied to IC18 (ECL).

Dividers

17. The Synthesiser front panel FREQUENCY selectors determine the Transceiver operating frequency. The first i.f. in the Transceiver is 35,400MHz, thus the mixing frequency generated by the VCO must be the operating frequency (1,600MHz to 29,999MHz) plus 35,400MHz (37,000MHz to 65,399MHz).

18. The purpose of the divider chain, comprising 10/11 divider IC18, connected in series with variable divider IC16 to IC12, is to produce a 1kHz output pulse train when the VCO output, applied to IC18 via TR15, equals the selected operating frequency plus 35,400MHz. Each divider accepts the output of the preceding divider and initially gives one output pulse for the same number of input pulses as the digit set at the associated FREQUENCY selector, after which it gives one output for every ten input pulses. Only the QA and QD outputs of the four variable divider elements IC12 to IC15 are used. These are applied to the eight-input NAND gate IC11, the output of which is a 0-going pulse immediately IC12 to IC15 outputs are simultaneously in the 1001 state. This output is gated in IC10 which provides two further outputs:

(a) A 0-going clock pulse to the phase discriminator JK flip-flop IC4b.1.
(b) A 0-going reset pulse to the LOAD inputs of dividers IC12 to IC16.1.

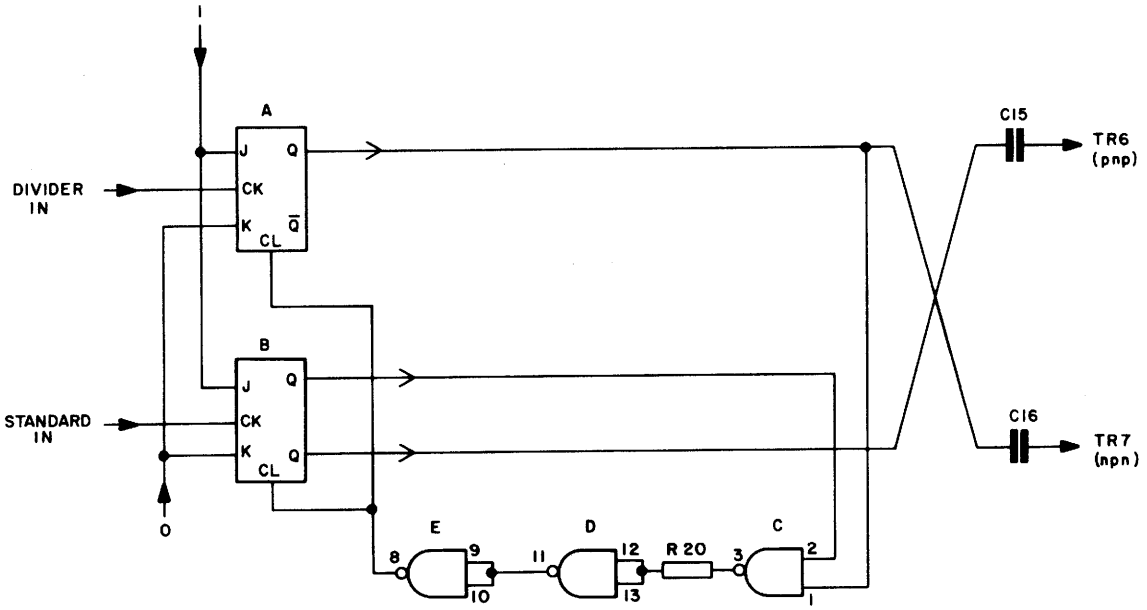
19. The 10/11 divider, the variable divider and the divider gating circuits are described in the following paragraphs.

20. **10/11 divider.** The 10/11 divider is used to count the VCO output pulses. The counting method is not the same as that for the other variable dividers,in that IC16, programmed by the 1kHz FREQUENCY selector, is used to program IC18 via the control input PE1. This type of programming makes IC18 initially divide the VCO input by 11 for each digit of the 1kHz selector and then divide by 10 for the remainder of the count, when IC16 is reset by the logic '0' pulse generated by IC10a.

21. **Variable divider.** Four dividers form this chain (IC12 to IC15). The input to each divider (except IC15) is the QD output from the previous divider. Each divider initially gives one 0-going output after counting the number of clock inputs preset on its associated front panel switch and then (except for IC12) one output for every ten clock inputs. The QA and QD outputs from IC12 to IC15 are also connected to 8 input NAND gate, IC11. When all inputs to the gate are simultaneously '1', the NAND gate is 'satisfied' and its output (pin 8) goes to '0'. It is this output (through the gating circuits of IC10) which forms the train of pulses at 1kHz and resets the variable divider chain.

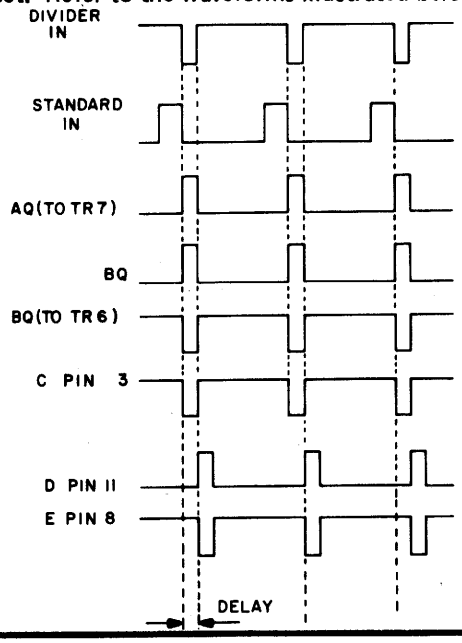
22. **Divider gating circuit.** If the reset pulse was taken to the dividers directly from IC11, general circuit tolerances would almost certainly cause one divider to be reset before the other. This divider would immediately feed a '0' to IC11 and return the reset output to '1' before the remaining dividers have been reset. To ensure sufficient time for all dividers to reset, IC11 output is taken through the gating circuits of IC10

Phase Discriminator



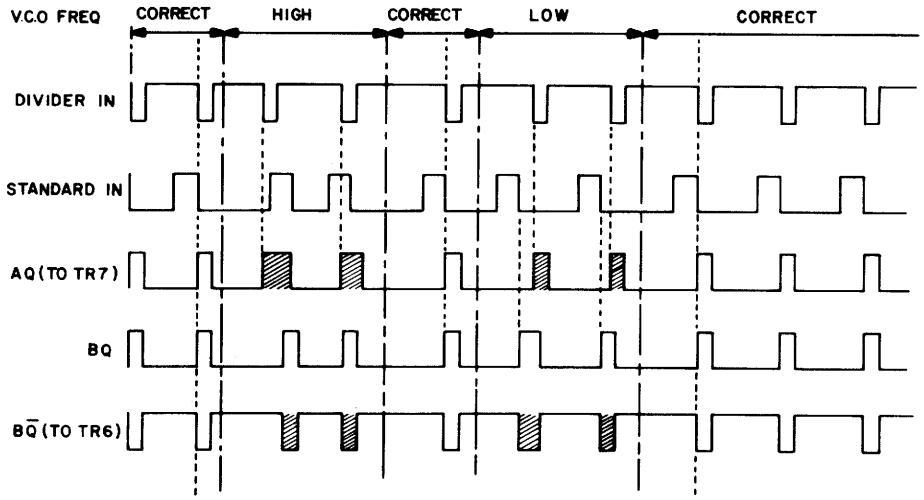
23. A simplified circuit is given above. The phase discriminator comprises the two JK flip-flops of IC4, the NAND gates of IC5 and switching transistors TR6, TR7. The phases of the divider and the standard frequencies are compared in the flip-flops. Should a phase difference occur, due to high or low VCO frequency, one of the switching transistors is brought into conduction. When TR6 conducts (VCO frequency low) capacitor 1C1 in the Integrator charges through 1D2 to increase the positive potential at the non-inverting input of 1C1. The output voltage of this op-Amp to the VCO varicaps goes more positive to increase the VCO frequency. IF TR7 conducts (VCO frequency high) 1C1 discharges through 1D1 to decrease the positive potential at the non-inverting input of IC1, which in turn decreases the VCO frequency. Under normal operation (VCO frequency correct) both transistors are held in a cut-off state, although for an extremely short time every millisecond they both conduct simultaneously. It should be noted that the J input points of both flip-flops are held permanently at '1' while both K inputs are held at '0'. All that can now happen to the flip-flops when a clock pulse is fed to the CK inputs is that Q output can change to '1'. If the Q is already at '1' the clock pulse can have no effect. Consider the operation of the circuit for correct and incorrect VCO frequencies.

24. **VCO frequency correct.** Refer to the waveforms illustrated below.



Under correct frequency conditions the negative-going edges of the divider and the standard generator output pulses coincide. Initially the Q outputs of both flip-flops are at '0' so that when these pulses are applied to the CK inputs of the flip-flops the Q outputs of both flip-flops are switched to '1' simultaneously. These two '1' outputs are fed to NAND gate a, the resulting '0' going output pulse being fed through resistor R20 to the series connected NOT gates formed by NAND gates d and e. The pulse is inverted through both NOT gates and appears as a '0' going reset pulse to the CL pins of both flip-flops, whose Q outputs immediately return to '0'. The delay due to the gates and the delay circuit is of the order of 50ns (0,05μs). The Q outputs, therefore, are narrow '1' going pulses generated once per millisecond. The positive going Q output from flip-flop B is also fed through C16 to the base of npn transistor TR7 while $\overline{Q}$ output from flip-flop A (a 0-going pulse) is fed through C15 to the base of pnp transistor TR6. Since these pulses appear simultaneously, both transistors conduct at the same time and the charge and discharge times for C13 are equal. The net change in the charge on the capacitor is zero and so there is no change in the VCO frequency.

25. **VCO frequency high/low.** The waveforms for incorrect VCO frequency conditions are shown below. It should be noted that the division ration through the variable dividers is such that even in the worst case there is never a recognisable frequency difference between the variable divider and standard outputs.



The difference can be regarded as one of phase. As soon as the front panel controls are switched to a lower frequency the division ratio through the variable divider is changed. The VCO is still running at the original frequency and this frequency is higher than required. The first pulse to flip-flop A CK input appears before the negative-going edge of the standard input to flip-flop B CK. Flip-flop A Q immediately goes to '1'. TR7 conducts and 1C1 commences to discharge. Consequently the VCO frequency decreases. Since BQ is still at '0' at this stage, NAND gate C is not satisfied and there is no resetting output from NOT gate E. The circuit remains in this state until the '0' going edge of the next standard frequency pulse takes BQ to '1'. NAND gate C inputs are then both at '1' and a resetting pulse is fed to both flip-flops so that their Q outputs return to '0'. TR6 conducts when BQ goes to '0' for the 50ns period BQ was at '1'. However TR7 will have been conducting for a much longer period so that the charge on capacitor 1C1 is lower than it was at the beginning of the cycle and the VCO frequency has been decreased. The times during which the two transistors conduct are proportional to the cross hatched parts of the waveforms. A similar action occurs for subsequent pulses to the two flip-flops. In the worst case the VCO frequency is correct after no more than ten inputs pulses from the variable divider. After this the negative-going edges of the two pulses coincide and the VCO frequency is held at the required value. If the VCO frequency is low, say after switching to a higher frequency, the $\overline{BQ}$ output remains at '0' for a longer period than AQ is at '1'. TR6 conducts for a longer period than TR7, the net charge on 1C1 increases and the VCO frequency rises towards the required value.

NOTE The waveforms illustrated are not to scale. The effective Q output pulses under normal operating conditions are about 50ns wide and appear once per millisecond. Under 'out-of-lock' conditions, such as when changing frequency, the effective Q (or Q) outputs are not more than a few tens of microseconds in width. Frequency drifts due to temperature changes etc. result in pulses only a fraction wider than the normal in-lock 50ns pulses. The 0,1μF d.c. blocking capacitors C15, C16 are virtually short circuits to pulses of this width so that there is very little attenuation of the pulses appearing at the bases of TR6 and TR7. There is one further output from the Q of each flip-flop. This feeds the remaining NAND gate (pins 4 and 5) of IC5.

Integrator

26. The main function of this circuit has been generally described. When transistor TR6 conducts capacitor IC1 charges through diode 1D1, and when transistor TR7 conducts IC1 discharges through 1D2. Integrated circuit 1IC2, which has a very high input impedance, acts as a voltage follower to provide the d.c. control voltage for application to the VCO. A high charge of 1C1 results in a high voltage output. This is reduced as the charge decreases. The range of the control voltage available is 0V to 20V.

Standard Frequency Generation.

27. The standard frequency generation circuits are described in the following paragraphs.

28. **Oscillators.** Two oscillators are used: a temperature compensated, crystal oscillator (TCXO) which provides an extremely accurate 5MHz signal, and the 5MHz crystal controlled oscillator, TR9, whose frequency can be varied a small amount from the VFO control on the front panel.

(i) The TCXO is a sealed unit which should not require servicing. A potentiometer is provided to enable frequency drift due to ageing to be corrected. **This adjustment must not be attempted without a frequency standard for comparison.**

(ii) The 5MHz crystal oscillator is of the Colpitts type with a varicap in series with the crystal. The voltage controlling the capacitance of the varicap is taken from a potentiometer in a series circuit between the regulated 15V supply and earth. The varicap is connected to the potentiometer moving contact and a control voltage in the range 7V to 14V allows the oscillator frequency to be varied by approximately ±100Hz.

29. **Diode switching.** Selection of the oscillator used is made at the front panel VFO control switch S1. For normal operation the switch is set to the OUT position (fully counter-clockwise). The 15V supply is then fed to diode switch circuit R37, D10, R40, the diode is forward biased and a path for the TCXO output amplifier TR10 is provided. Capacitors C31 and C33 provide d.c. blocking and give little attenuation to the 5MHz signal. With switch S1 set to OUT there is no 8,5V supply to oscillator transistor TR9. Hence there is no output from this circuit to TR10. The TCXO also feeds the 35,4MHz generator circuit which must run continuously. For this reason the TCXO is not switched off when the front panel VFO control is turned clockwise. In this position the 8,5V supply is disconnected from the diode switch described above and is connected to the 5MHz crystal oscillator and two other diode switches. These are R35, R36, D9 and R39, D11, R40. In the first switch D9 is forward biased and provides a path to earth for the TCXO output appearing thorugh R33. As a precautionary measure the diode in the second switch, D11 is also forward biased, the resulting voltage at the junction of D11, R40 reverse biasing D10 to ensure that the path between TCXO and TR10 is effectively open circuited. The output from the selected oscillator is fed through amplifier TR10 to pluse shaper TR11, whose square wave output is fed as clock pulses to divider chain IC6 to IC9 which forms the reference divider.

30. **Reference divider.** This is a chain of four series connected counters each of which contain the usual four flip-flops. One flip-flop is used as a coventional divide-by-two section while the other three are internally connected to give a divide-by-five section. To obtain a divide-by-ten-counter the two sections are connected externally (pins 1 and 12 linked). The purpose of the reference divider is to provide the 1kHz standard pulse train fed to the JK flip-flop in the Phase Discriminator. To do this, the chain must give a 0-going output pulse after every 5000 inputs from the TCXO. In the first counter (IC6) the divide-by-two section is not used, the clock pulses from the shaper being fed directly to the divide-by-five section. The remaining three counters are connected as divide-by-ten devices, the final output from the complete chain being a 1kHz train of pulses with 1:4 mark-space ratio. When the interpolate oscillator (VFO) is selected the output from the reference divider is a similar train of pulses at 1kHz ± 0,03Hz.

35,4MHz Generator

31. The 35,4MHz signal is generated in a crystal oscillator circuit comprising a 35,4MHz crystal XL2, transistors TR20, TR21, TR23, TR24, TR26 and associated components. Frequency control is exercised by varicap diode D15.

32. The d.c. control signal applied to D15 is generated in the control circuit comprising TR18, TR19 and IC25. The generator signal developed at TR24 collector is coupled via C96 to TR18. Here it is sampled and compared with a reference signal derived from the TCXO 5MHz output via dividers IC22, IC23 and IC24.

33. TR18 output controls the current flowing in TR19 and hence IC25 inverting input. Potentiometer R117 is adjusted to set the reference voltage applied to IC25 non-inverting input, so that when a 35,400MHz signal is generated the level of the d.c. signal developed at IC25 pin 6 and applied via LK5 and R120 to D15 is such to maintain the generator output at the correct frequency.

Power Supplies

Refer to Fig. 3, Sht 2.

34. The 12V input is fed via PL30, pin 22 through a 2A fuse and a decoupling circuit to three independant regulator circuits that are described in the following sub-paragraphs:

(a) **5V Supply Circuit**
The regulator for the 5V supply is an integrated circuit, IC1. The 12V input is connected to the input pin and the regulated supply is taken from the output pin. Smoothing additional to that in the package is provided by C106.

(b) **8,5V Supply Circuit**
The regulator for the 8,5V supply is an integrated circuit, IC2. The output is adjusted to the correct value by resistor R3. Capacitor C107 provides extra smoothing.

(c) **20V Generator and Regulator Circuit**
A simple blocking oscillator is used to provide the 20V supply. The positive-going pulses at the collector of TR1 (on load these will be about 23V amplitude) are rectified by D1 and smoothed through the capacitor-choke and capacitor-resistor circuit following.

The output is kept at a reasonably constant level by regulator transistor TR2. This transistor is controlled by an output from potential divider R6, R7 to its base which in turn, control the d.c. potential at the base of oscillator TR1. Should the potential on the 20V line tend to rise the potential at the base of TR2 also rises towards the fixed 5V potential at its emitter. Conduction through the transistor decreases to lower the potential at the base of TR1 and so reduce the oscillator frequency. Since the level of the d.c. output is a function of frequency this level will fall to the design value.

GENERATOR PCB

GENERAL DESCRIPTION

35. A simplified block diagram of the frequency hopping microprocessor-based system is given in Figure 5.

36. The basic blocks of the system comprise a read-only memory (ROM), in this case an erasable and electrically programmable ROM (EPROM), to hold the program of instructions, a random-access memory (RAM) to hold results and variable data, and an input/output (I/O) controller for connections to the Synthesiser and the microprocessing unit (MPU), which itself manipulates the data in a manner defined by the program of instructions.

Random–Access Memory (RAM)

37. Two 1024 bit RAMs (each organised into 256 x 4 bit locations) are connected in parallel. These RAM 's are of the static operation type which do not require periodical replenishment or refreshment as with the dynamic type. However complete loss of supply voltage causes all memory contents to be erased.

38. Addressing of the RAM 's has to be accomplished at two levels as the address bus consists of 8 lines, sufficient for addressing 256 memory locations. This is achieved by strobing the higher-order byte of the 16 bit memory address, which appears on the address lines first, into an external address latch by the timing pulse TPA which occurs once per machine cycle. The lower-order byte or the 16– bit address appears on the address lines at the termination of TPA.

39. Data is written into the RAM from the 8 line bi-directional bus by the MWR signal from the microprocessor and data is retrieved from the RAM by the MRD signal from the microprocessor. These functions also require chip select inputs CS_1 and CS_2 to be active.

Erasable And Electrically Programmable Read–Only Memory (EPROM)

40. The EPROM which holds the program instructions is a 16 384 bit, ultra-violet erasable and electrically programmable read-only memory which can be easily re-programmed in the field. There are six modes of device operation:

(a)	Read Mode	-	data is available at the output in the read mode
(b)	Deselect Mode	-	used when two or more EPROMs are used together
(c)	Power Down Mode	-	outputs held at high impedance to reduce active power consumption
(d)	Programming, Program Inhibit and Program Verify	-	these modes used for reprogramming the EPROM

41. Unlike the RAM, the ROM is non-volatile; that is, the contents of the memory are not lost when the power supply is removed.

Input/Output (I/0) Controller

42. In practice the microprocessor and its memories form only a part of the total system, therefore, the way in which interface, interaction and communication with other devices is conducted is of major importance. The various techniques which are used to implement these interconnections are generally termed Input/ Output (I/0) techniques. Similary the device used to carry out these interconnections is termed the I/0 Controller .

43. Input/output information generally fits into two categories:

(a) data which has been generated or is to be processed by the microprocessor unit.
(b) control signals which perform a diversity of control or status functions.

44. The microprocessor generates 4-bit function address codes which are decoded in a 4/16—bit decoder, thereby providing up to 16 functions designated S0 to S15. In this particular system only 14 functions are used.

45. Input functions include:

(a) Allowing frequency switch data from the Synthesiser on to the 8 line data bus.
(b) Detecting the FAM position of the FUNCTION switch.

46. Output functions include:

(a) Allowing code frequency data to be sent to the Synthesiser.
(b) Initiating and releasing SYNC. pulses and activating the transmitter PTT line.
(c) Illuminating the SYNC LED.
(d) Inhibiting Synthesiser FREQUENCY switch data to the data bus.

47. Four I/O flags (E1 – E4) are used to transfer status information to the microprocessor. These status signals are:

(a) $\overline{E1}$ FAM positon of the FUNCTION switch
(b) $\overline{E2}$ Not used
(c) $\overline{E3}$ Incoming sync. pulse detected
(d) $\overline{E4}$ 10MHz bit from the Synthesiser

The four flags can be tested by certain instructions. Only when tested by an instruction is the information acted on.

48. When the FUNCTION switch is put to the SYNC position an $\overline{\text{INTERRUPT}}$ signal is generated which causes the microprocessor to complete its current instruction and then service the interrupt. This takes the form of generating a stream of logic '0' and logic '1' pulses from the microprocessor Q output which in turn shifts the frequency of the SYNC FSK tone oscillator. The interrupt line is sampled at the beginning of every S1 cycle.

Microprocessor Unit (MPU)

49. A full description of the MPU, including an instruction summary and timing diagram, is contained in the data sheet for the RCA CDP1802D microprocessor. This is not included in this handbook.

50. The MPU is driven by the 1MHz clock derived from the Synthesiser TCXO. The RESET position of the FUNCTION switch causes logic '0's to be placed on all the data bus lines and the suppression of the machine cycle timing pulse TPA. The CPU is left in the execute instruction mode. When the RESET signal is removed an initialization cycle is performed which resets internal registers before returning to the normal program.

MICROPROCESSOR DATA

51. Before a functional description of the μP system is given descriptions of the microprocessor signals and simplified timing diagrams are included.

Signal Descriptions

52. Figure 6 gives the terminal assignment of the CDP1802 microprocessor and the direction of signal flow. A description of each signal and its functions is given in TABLE 1.

TABLE 1: SIGNAL DESCRIPTIONS

	Signal Name	Pin No's	Function
1.	BUS 0 to BUS 7	15 - 8	8-bit bi-directional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor and I/0 devices.
2.	NO to N2 (I/0 command)	19 - 17	3-bit N code generated by an I/0 instruction. These lines can be used to issue command codes or device selection codes to I/0 devices. Not used in this system.
3.	$\overline{EF1}$ to $\overline{EF4}$ (4 flags)	24 - 21	These levels enable the I/0 controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/0 devices to " call the attention " of the processor, as in this system, in which case the program must routinely test the status of these flags (active condition logic '0'). $\overline{EF1}$ Active when the FUNCTION switch, S13, is in the FAM position. $\overline{EF2}$ Not used, held permanently at logic '1' $\overline{EF3}$ Active when a SYNC signal has been detected. (switched by train of logic '0' and logic '1' pulses). $\overline{EF4}$. Not used, held permanently at logic '1'. These flags are tested at the beginning of every S1 cycle (refer to signal No. 5)
4.	$\overline{INTERRUPT}$ $\overline{DMA-OUT}$ $\overline{DMA-IN}$ (I/0 requests)	36 - 38	These signals are sampled during the interval between the leading edge of timing pulse TPB and the leading edge of TPA. In this system only the $\overline{INTERRUPT}$ signal is used, the action being as follows: When $\overline{INTERRUPT}$ is active ('0') FUNCTION switch S13 is in the SYNC position. The current main instruction is completed and the interrupt request is serviced. This consists of releasing a stream of logic '0' and logic '1' pulses from the Q output to modulate the SYNC oscillator. On completion of the interrupt the main program resumes at its next instruction.
5.	SC0, SC1 (state code lines)	6, 5	These lines indicate that the CPU is: (a) fetching an instruction (S0), or (b) executing an instruction (S1), or (c) processing a DMA request (S2) or (d) acknowledging an interrupt request (S3) These outputs are not used in this system
6.	TPA, TPB timing pulses)	34, 33	Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/0 controllers to interrupt codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher order byte of the 16-bit memory address. TPA is suppressed in IDLE when the CPU is in the load mode. TPB is not used in this system.

TABLE 1 (Cont.): SIGNAL DESCRIPTIONS

Signal Name	Pin No's	Function
7. MA0 to MA7 (memory address lines)	25 - 32	The higher order byte of a 16-bit memory address appears on the memory address lines MA0–MA7, first. Those bits required by the memory system are strobed into external address latches by timing pulse TPA. The low order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 64k bytes.
8. $\overline{\text{MWR}}$ (write pulse)	35	A negative pulse apppearing in a memory-write cycle, after the address lines have stabilized.
9. $\overline{\text{MRD}}$ (read level)	7	A low level on $\overline{\text{MRD}}$ indicates a memory-read cycle. It can be used to control three state outputs from the addressed memory which may have a common data input and output bus as in this system.
10. Q	4	Single bit output from the CPU which can be set or reset under program control. During SET Q and RESET Q instructions execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB. (See $\overline{\text{INTERRUPT}}$ for Q output).
11. CLOCK	1	Input for externally generated single phase clock. In this system a 1MHz clock from the Synthesizer is used. The clock is counted down internally to 8 clock pulses per machine cycle.
12. $\overline{\text{XTAL}}$	39	Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized. Not used in this system.
13. $\overline{\text{WAIT}}$ $\overline{\text{CLEAR}}$ (Control lines)	2, 3	Provides four control modes as listed in the following truth table: $\overline{\text{CLEAR}}$ $\overline{\text{WAIT}}$ MODE L L Load L H Reset H L Pause H H Run In this system the $\overline{\text{WAIT}}$ signal is held permanently at logic '1', thus only two modes, RESET and RUN are available. The functions of these modes are as follows: (a) RESET – certain internal registers are reset and logic '0's are placed on all data bus lines. TPA and TPB are suppressed while reset is held and CPU is placed in S1 (execute). The first machine cycle after termination is an initialization cycle. During this cycle the CPU remains in S1 and other internal registers are reset. Interrupt and DMA servicing are suppressed during the initialization cycle.

TABLE 1 (Cont.) SIGNAL DESCRIPTION

Signal Name	Pin No's	Function
		The next cycle is an S0 (fetch), S1 or an S2 (DMA) but never an S3 (INT REQ). Reset is achieved by setting the FUNCTION switch S13 to the RESET position which applies logic '0' to the CLEAR input.
		(b) RUN – Initiated from RESET position by returning S13 to OFF or FAM position. The first cycle following RESET is always the initialization cycle. The initialization cycle is then followed by fetch (S0) from location 0000 in memory.
14. V_{DD}, V_{SS}, V_{CC}	40, 20, 16	The internal supply voltage V_{DD} is isolated from the input/output supply VCC so that the processor may operate at maximum speed while interfacing with various external circuit technologies including TTL at 5V. V_{CC} must be less than or equal to VDD. All outputs swing from V_{SS} to V_{CC}. In this system V_{CC} equals V_{DD}.

Microprocessor Timing

53. Figure 7, the microprocessor timing diagram, illustrates the four separate areas of system control.

54. **General Timing**

(a) Clock - the basic clock frequency is 1MHz (T = 1μs) taken from the divider circuits in the Synthesiser. As this clock is derived from the 5MHz TCXO the stability is within 2p.p.m. The clock is divided down within the microprocessor to 8 clock pulses per machine cycle.

(b) TPA - a positive timing pulse produced once per machine cycle of duration T.

(c) TPB - a positive timing pulse produced once per machine cycle, after TPA, and of duration T.

(d) MACHINE CYCLE - a period of 8 clock pulses (8T) in which the program instruction is carried out. With two exceptions each instruction consists of two machine cycles. The first cycle is the fetch cycle and the second - and third if necessary – are execute cycles.

55. **Memory Timing**

(a) MA - the high-order byte of a 16– bit memory address appears on the memory address lines MA0–MA7 first. The three least significant bits are strobed into a 4-bit address latch, with the most significant bit, and the remaining 4-bits are strobed into a 4 to 16– bit address decoder. All bits are strobed by timing pulse TPA. The low–order address byte appears on the MA0–MA7 lines after the high-order bits have been strobed into the address latches.

(b) $\overline{MWR}$, $\overline{MRD}$ - the state of the $\overline{MWR}$ and $\overline{MRD}$ lines determines whether a byte is to be read from the addressed memory location, written into it or neither operation performed. Note that both lines are active logic '0'. The truth table is:

CPU LINES	MEMORY READ	MEMORY WRITE	NON–MEMORY OPERATION
$\overline{MWR}$	1	0	1
$\overline{MRD}$	0	1	1

The state of the $\overline{MWR}$ and $\overline{MRD}$ lines also determines, together with data from the address latch, when the outputs from the address decoder are gated.

(c) CPU DATA I/P - during a READ cycle data is released from the addressed memory location after a period defined by the memory system access time. The CPU controls the destination of the memory output when it appears on the data bus.

(d) CPU DATA O/P - during a WRITE cycle the memory output is in a high impedance state. A negative going $\overline{MWR}$ pulse causes the data byte, placed on the data bus by the CPU or I/O controller, to be written into the addressed memory location.

NOTE: The above timing refers to the random access memory (RAM). The EPROM does not require the write cycle but the read cycle is achieved by gating an output from the address decoder.

56. **I/O Timing**

(a) $N_0 - N_2$ - These lines which are used for I/O command or device selection codes are not used in this system.

(b) Q - The Q output is set/reset during an S1 (execute) cycle. In this system the Q output is caused to modulate the SYNC FSK oscillator as a result of an interrupt request performed by setting the FUNCTION switch, S13, to SYNC.

57. **I/O Request Timing**

(a) $\overline{DMA–IN}$ (not used)

(b) $\overline{DMA–OUT}$ (not used)

(c) $\overline{INTERRUPT}$ - when the $\overline{INTERRUPT}$ line is taken to logic '0' an interrupt routine is initiated. The interrupt causes the microprocessor to suspend its current program sequence and execute a predetermined sequence of operations designed to respond to the interrupt condition (Table 1 Signal No-4). The interrupt line can be activated at any time and is sampled during S1, S2 or S3 cycles under program control.

FUNCTIONAL DESCRIPTION

58. The μP base system functional description is given in terms of the block diagram, Figure 5, and the flow diagram, Figure 8.

59. **Clock Generation.** The clock for the system is derived from the 5MHz TCXO in the Synthesiser, a divided output at 1MHz being used. This clock is counted down in the μP to provide 8 clock pulses per machine cycle. Timing pulse TPA, generated once per machine cycle, is used together with the 1MHz clock to provide clock pulses for various other elements of the circuit.

60. **Microprocessor Reset.** Before the μP can receive the synchronisation signal and carry out its program of instructions it must be reset as described in 13 of Table 1. This is achieved automatically by the power-up reset circuit when power is first applied. The RESET position of the FUNCTION switch also resets some output latches and sets all address decoder outputs to logic '0'.

61. **NORMAL Mode of Operation.** In the NORMAL mode of operation the output frequency of the Synthesiser is constant as set by the FREQUENCY switches. The data from these switches is available at the input to tri-state buffers for used by the μP when in the hopping mode. The FUNCTION switch S13 is in OFF position placing a short circuit across the ON LED.

62. **Frequency Agile Mode of Operation.** When the FUNCTION switch is set to FAM, this condition is indicated to the μP on flag $\overline{EF1}$. AT the same time the short circuit is removed from the ON LED causing it to illuminate.

63. At this stage the steps illustrated on the flow diagram are described, starting at the reset condition.

Reset and Initialise (1)

64. When power is first applied the μP is automatically reset by the power-up reset circuit which applies a logic '0' to the $\overline{CLR}$ input. An initialization cycle is carried out by the μP as described in Table 1.13 (a).

65. The reset condition is also applied to the address decoder setting all outputs to logic '0'. Output latch 4 is reset which:

(a) Applies a logic '1' to the common line of the Synthesiser FREQUENCY switches thus enabling their output data.
(b) Applies a logic '1' to the tri-state driver of output latches 3 and 5 causing their outputs to go to a high impedance state (OFF).
(c) Applies a logic '1' to the disable lines of output latches 6 to 9 causing their outputs to go to a high impedance state (OFF).

66. When the RESET condition is removed ($\overline{CLR}$ = logic '1') the μP goes into the RUN condition as described in Table 1.13 (b), and commences to carry out the program of instruction held in the EPROM. Each time the address decoder output S0 is active an instruction is read from a previously addressed location in the EPROM.

Activate Flag EF1 (2)

67. When the FAM position of FUNCTION switch S13 is selected, flag $\overline{EF1}$ is taken to logic '0'. When next tested by the relevant μP instruction a slave sync, routine is initiated.

Slave Sync. Routine (3)

68. During the slave sync. routine the μP tests the $\overline{EF3}$ flag, which is not used in this system.

Disable Interrupt (4)

69. After sync. has been achieved no further interrupt requests are serviced, i.e. if the MODE switch is set to SYNC the μP ignores the request and no SYNC signal is generated.

Read FREQUENCY Switch Data and Store (100kHz, 1MHz) (5)

70. The μP outputs data to the 8-bit address bus lines, the data being strobed into the address latch and address decoder as described in Paragraph 55 (a). The decoded output (S14) is enabled by timing pulse TPA when the memory write signal is active ($\overline{MWR}$ = '0'). S14 output is now active enabling two of the four tristate buffers. Data from the 100kHz and 1MHz Synthesiser FREQUENCY switches is allowed onto the data bus and written into the RAM location, previously addressed, when address decoder output S1 and memory write signals are active.

Output FREQUENCY Switch Data to Output Latches (1MHz, 100kHz) (6)

71. The μP addresses the RAM location into which the 1MHz and 100kHz frequency switch data was previously written. When the memory read signal $\overline{MRD}$ goes to logic '0' the data is read onto the data bus.

72. Address decoder output S1 is enabled by $\overline{MRD}$ at the same time and a logic '1' strobe pulse transfers the data to output latches 8 and 9. The outputs of the latches are held OFF by a logic '1' on the disable inputs.

Read FREQUENCY Switch Data and Store (10kHz, 1kHz) (7)

73. The 10kHz and 1kHz Synthesiser FREQUENCY switch data is read by decoding address S13, which enables the tri-state buffers for the appropriate data. The data is written into a RAM location as before by $\overline{MWR}$.

Output FREQUENCY Switch Data to Output Latches (1MHz, 100kHz)

74. The data is read from the RAM location as in Paragraph 71 and is strobed into output latches 6 and 7 by address decoder output S3.

Read FREQUENCY Switch Data and Store (10MHz) (9)

75. The data from the 10MHz FREQUENCY switch is on flag $\overline{EF4}$ and when active (logic '0') signifies to the μP that the switch is in the 10MHz position.

Output FREQUENCY Switch Data to Output Latch (10MHz) (10)

76. Data bus line Do is set to logic '1' by the μP for 10MHz position or logic '0' for 0MHz position. Address decoder output S9 clocks the data on Do into output latch 5.

Enables Output Drivers (11)

77. When address decoder output S8 is active output latch 1 is clocked, setting its output to logic '0'. This has the following effects:

(a) Applies logic '1' to the common line of the Synthesiser FREQUENCY switches thus disabling the data outputs.
(b) Applies a logic '0' to the enable input of output latch 2, tri-state buffer, allowing the 10MHz bit to be sent to the Synthesiser.
(c) Applies logic '0' to the disabling inputs of output latches 6 to 9, allowing the FREQUENCY switch data to be sent to the Synthesiser.

Switch On SYNC LED (12)

78. When address decoder output S11 is active, 0V is applied to the cathode of the SYNC LED causing it to illuminate. This informs the operator that the Synthesiser is now in the 'hopping' sequence. The Synthesiser remains in this sequence until the system is RESET.

Read and Store CODE Switch Data (S8 and S9) (13)

79. When the address decoder output S4 is active, logic '0' is applied to the wipers of CODE switches S8 and S9 releasing the 4-bit data from each switch on to the data bus.

80. A memory write cycle (S1 and $\overline{MWR}$ active) writes the data into the previously addressed RAM location.

Read and Store CODE Switch Data (S10 and S11) (14)

81. Data from CODE switches S10 and S11 is allowed onto the data bus by decoder output S5 and is written into store as previously described.

Read and Store CODE Switch Data (S6 and S7) (15)

82. Data from CODE switches S6 and S7 is allowed onto the data bus by address decoder output S6 and is written into store as previously described.

Random Generator Routine (16)

83. The microprocessor, using the fixed program contained in the EPROM, commences to generate a random number.

Round Off Random Number to Selected Bandwidth (17)

84. When address decoder output S7 is active data from the bandwidth/dwell time switch SA is released on to the data bus. The μP uses this data to round off the random number to the selected bandwidth.

Subtract Random Number from Set Frequency (18)

85. The μP subtracts the random number from the Synthesiser FREQUENCY set previously and stored.

Output New Frequency Data to Output Latches (19 - 21)

86. The new frequency Data is strobed into the output latches in three stages as described in Paragraphs 70, 73 and 75

Wait Dwell Time (22)

87. The output frequency of the Synthesiser is changed by the new frequency data over the bandwidth selected. The μP, using the data from the dwell time switch SA , now waits the dwell time and then recommences the 'hopping' routine by generating new random number.

88. The 'hopping' sequence continues until the FUNCTION switch is put to the RESET position.

Synchronizing Signal Transmission.

89. When the system is acting as the master in a communications network it must transmit a synchronizing signal so that all distant ends start the frequency hopping sequence at exactly the same time. This is achieved by setting the FUNCTION switch S13 to SYNC.

90. This action causes two functions to be performed:

(a) Activates, the $\overline{INTERRUPT}$ line of the μP, which initiates an interrupt routine.
(b) Applies, a logic '1' to FREQUENCY switches COMMON line which returns control of the Synthesiser frequency to its own switches and disables the output latches thus preventing data held being passed to the Synthesiser.

Interrupt Routine (23)

91. When a interrupt request is allowed by the program the current instruction is completed and the location of the next instruction is stored for use on completion of the interrupt. The interrupt instruction is now read.

Activate PTT and Sync. Modulator (24)

92. The interrupt instruction causes the address decoder to activate output S10 which applies logic '0' to the SYNC Modulator which switches on the power.

Modulate Sync. TX Modulator (25)

93. A further instruction causes an internal flip-flop to toggle. The resultant Q output modulates the tone oscillator which generates a train of 1:1 Mark/Space tones. These tones represent the SYNC signal.

Deactivate PTT and Sync. Modulator (26)

94. After a predetermined period of time the S10 output returns to logic '0' causing the modulator power switch to be de-activated.

Jump to Next Instruction in Main Program

95. At the conclusion of the interrupt an instruction causes a jump to Point A in the main program.

CIRCUIT DESCRIPTION

96. Refer to Figure 9.

97. **The operation of the microprocessor (μP) and the function of signals have already been described, together with the timing and sequencing of the system.** Further detailed information on various circuit elements is given here, but for an understanding of the complete system this must be read in conjunction with the functional description.

Clock Generation

98. Refer to Figure 10 (a). The μP 1MHz clock **1**, supplied from the Synthesiser, is connected to IC21 pin 1 from p.c.b. pin 2. Timing pulse TPA **2**, generated by the μP at IC21 pin 34 once per machine cycle (every 8 clock pulses), provides the following:

(a) logic '1' reset pulses at D type flip-flop IC14a pin 4 and IC14b pin 10.
(b) logic '1' clock pulses at address latch IC23 pin 5.
(c) logic '1' strobe pulse at address decoder IC10 pin 1.

99. The 1MHz clock and TPA are fed to NOR gate IC9c, the output **3** consisting of a negative pulse which inhibits the clock pulse at D type flip-flop IC14b pin 11 for a period of 1,5T (1,5μs). Pulse **3** is inverted by IC2 which produces a 1,5T positive pulse **4** used to clock IC14a pin 3.

Address Decoder Output Gating

100. Refer to Figure 10 (b). The address decoder output gates, IC1d, IC3c, IC11a, b, c, d, IC12a, b, c, d, IC17a, b, c, d, are all enabled at the same time via the logic shown in the diagram.

101. Initially IC14a is clocked by waveform 4 causing waveform 5, to appear as a logic '1' at the Q output. This output, 5, is maintained at logic '1' until both flip-flops are reset by timing pulse TPA 2. Both Q outputs and hence 5 go to logic '0', this condition being maintained for 2μs (2T) i.e. the 1μs duration of TPA + 1μs to clock both flip-flops, returning 5 to logic '1'.

102. The negative going pulse 5 inhibits NAND gate IC1b thus allowing the address lines to stabilize before a memory read or write cycle is initiated.

103. When a memory write ($\overline{MWR}$) or memory read ($\overline{MRD}$) signal becomes active (logic '0') the output at IC1c pin 10 goes to logic '0' and providing waveform 5 is at logic '1' — i.e. the data on the address lines has had time to settle — IC1b pin 4 goes to logic '0'. When the data from address latch IC23 pin 1 is at logic '0', IC9a pin 3 goes to logic '1' enabling the decoder output gates.

Reset Logic

104. Refer to Figure 10 (c). Resetting of the system, **as described in Table 1.13,** is achieved as follows:

(a) MANUAL — when the FUNCTION switch S13 is set to the RESET position a logic '0' (0V) is applied via PL32, pin 5 to pin 11 of Inverter IC24e. A second inversion by IC24d produces a logic '0' at the μP $\overline{CLEAR}$ input IC21 pin 3. A third inversion provides logic '1' reset levels to the D type flip-flop output latches IC4a, b and IC13a. A logic '1' is also fed to the address decoder INHIBIT input IC10 pin 23.

Sync. FSK Modulator

105. Refer to Figure 11. The sync. FSK modulator comprises a standard operational amplifier, IC20, which functions as an active bandpass filter having a centre frequency determined by the RC feedback loop network R35/R30/C23/C24 and resistor chain R26/R27/R28/R29. When TR1 conducts (due to a logic '1' applied to the base) R28 and R29 are shorted and the centre frequency, F1, is adjusted by R27 to 1900Hz + 425Hz. When TR1 ceases to conduct (due to a logic '0' at the base) R28 and R29 are connected into the frequency determining network to give a centre frequency F2 of 1900Hz — 425Hz, determined by the adjustment of R28.

106. The gain of an amplifier with positive feedback is given by:

$$G = \frac{A}{1 + A\beta} \quad \text{where } A = \text{gain without feedback}, \ \beta = \text{gain of feedback path}$$

If the feedback is of such magnitude and phase that $A\beta = -1$ then the gain of the amplifier is infinite. Thus the amplifier can produce an output without external input, i.e. the circuit oscillates.

107. The gain of IC20d is approximately 0,5 and the feedback gain, defined by R34/R32 is −2,2 (negative feedback). Therefore $A\beta = -1$ and the circuit oscillates.

108. The 12V power supply to the oscillator is switched on by the logic '0' applied to the base of TR2 when the FUNCTION switch is set to SYNC as described in TABLE 2, S10. A stream of logic '0' and logic '1' pulses from the μP Q output (IC21 pin 4) then modulates the oscillator producing a FSK output at F1 = 1475Hz and F2 = 2325Hz respectively. IC20a is a voltage follower which couples the output to PL34, pin 7 via R41, C28 and L1.

FSK Sync. Demodulator

109. Refer to Figure 11. The sync. demodulator receives a FSK signal (as described in Paragraph 85) at PL34, pin 1. which is coupled by C31 via the buffer amplifier IC28 to the limiting amplifier IC8a. IC8b and IC8c are active filters, similar to IC20b in the sync. modulator but without the feedback path. IC8c is adjusted for a centre frequency F2 = 1475 Hz by R11 and IC8d is adjusted for a centre frequency of F1 = 2325Hz by R14. The output of each filter is rectified by D10 and D11 respectively.

The output filter components are optimised for a 50 baud input signal. The two rectified outputs are fed to the comparator IC8b, the output of which produces the logic '0' /logic '1' pulse train encoded in the FSK signal.

110. The output is fed to μP flag $\overline{EF3}$, IC21 pin 22.

Address Decoder Outputs

111. The address decoder decodes addresses from the μP. Each output (S0 – S14) being used to perform a particular function. Refer to Figure 12 for a circuit of each address decoder output gate. For simplicity each output function is described in numerial order in Table 2. It must be remembered, however that this is not necessarily the order in which the functions are performed.

112. Output gates IC1d, IC3c, IC11a, b, c, d, IC12a, b, c, d, IC17a, b, c, d are enabled simultaneously as described in Paragraph 100. Each decoder output is at logic '1' when active.

TABLE 2: INSTRUCTION DETAILS

Instruction	IC10 pin No.	Function
S0	11	Logic '1' applied to IC12c pin 8 gives a logic '0' at IC22 (EPROM) pin 18 and 20 enabling a read cycle.
S1	9	Logic '1' applied to IC7d pin 12 gives a logic '0' strobe level at output latches IC18a pin 14 and IC18b pin 2. This locks the data, on the bus lines (D0–D7), into the latches. It also applies a RESET pulse to IC5a so that the SEGMENT FLAG is set to logic '1' if S9 is not active.
S2	10	Logic '1' applied to IC12d pin 12 gives a logic '0' at IC15 and IC16 (RAMs) pins 10 and 15, thus activating the chips. This logic '0' is also used via LINK 1 as a RAM strobe level, when using an IM6561 RAM.
S3	8	Logic '1' applied to IC3c pin 8 gives a logic '0' strobe level at output latches IC25a pin 14 and IC25b pin 2. This locks the data on the bus lines (D0–D7) into the latches.
S4	7	Logic '1' applied to IC17c pin 8 gives a logic '1' via inverter IC24a to the common line of CODE switches 8 and 9, allowing data onto the data bus.
S5	6	As for S4 but via IC17a and IC24c to CODE switches 10 and 11.
S6	5	As for S4 but via IC17b and IC24b to CODE switches 6 and 7.
S7	4	Logic '1' applied to IC3d pin 12 gives a logic '0' via IC9b to switch SA common, which enables the bandwidth and dwell time of frequency 'hop' onto the data bus (D0–D7).
S8	18	(a) When the system is reset the Q output of D type flip-flop IC13a is at logic '0'. This disables IC3a so that regardless of the FUNCTION switch IC3a, output is at logic '0'. This is inverted in IC2b so that the following conditions apply.

TABLE 2 (Cont.)

Instruction	IC10 pin No.	Function
		(i) the HOPPING FLAG output is at logic '1' (ii) logic '1' applied to tri-state buffers IC6a and IC6b causes pins 3 and 7 to assume high impedances thus disabling the 10MHz (A) and 10MHz (B) outputs. (iii) logic '1' applied to output latches IC18a, IC18b, IC25a and IC25b DISABLE inputs cause latch outputs to assume high impedance. (iv) Assuming that the Transceiver is operating in a local mode, ie. TR5 cut off +5V is applied to the COMMON circuit of the front panel FREQUENCY selectors. (b) When S8 is active D type flip-flop IC13a CLOCK input is taken to logic '0'. There is then no change in IC13a Q output which remains at logic '0'. (c) When S8 is de-activated IC13a CLOCK input is taken to logic '1' and the Q output is switched to logic '1'. If the FUNCTION switch is switched to FAM so that the FAM INITIATE input is at logic '0', the following conditions apply. (i) the HOPPING FLAG is at logic '0' (ii) a logic '0' is applied to tri-state buffers IC6a and IC6b so that IC13b and IC5b Q outputs are enabled to the 10MHz (A) and 10MHZ (B) outputs. (iii) + 5V is removed from the front panel FREQUENCY selectors which are therefore disabled (iv) logic '0' applied to the DISABLE inputs of latches IC18a, IC18b, IC25a, IC25b removes the high impedance state of the outputs thus allowing data to be output when the latches are strobed.
S9	17	Logic '1' applied the IC11c pin 8 sets D type flip-flops IC13b and IC5b CLOCK inputs to logic '0'. Logic '1' applied to D type flip-flop IC5a SET input sets the SEGMENT FLAG to logic '0'. When S9 is de-activated, IC13b and IC5b clock inputs are taken to logic '1'. The data on data bus D0 and D1 lines is then switched via tri-state buffers IC6b and IC6a to the 10MHz (A) and 10MHz (B) outputs respectively. At the same time the SEGMENT FLAG returns to logic '1'.
S10	20	The logic '1' applied to IC11a pin 1 sets D type flip-flop IC4b CLOCK input to logic '0'. When S10 is de-activated IC4b CLOCK input is switched to logic '1' and data bus D0 information appears at IC4b 'Q' output.

TABLE 2 Cont.)

Instruction	IC10 pin No.	Function
		When the Q output is logic '1' the inverter IC2f applies a logic '0' to the PTT LINE via TR3 and to the base of the sync. modulator power switch TR2, ie. a sync. signal can be transmitted. If the Q output is logic '0' the PTT LINE and sync. modulator are de-activated. When the system goes to RESET the Q output is set to logic '0'.
S11	19	When the system is RESET D type flip-flop IC4a is reset by a logic '1' applied to pin 4. IC4a logic '0' Q output is inverted in IC24f and 5V is applied to the SYNC LED which is then non conducting. When S11 is active a logic '1' is applied to IC11b pin 5. Hence D type flip-flop IC4a CLOCK input is at logic '0'. When the system is operating in the hopping mode, ie. Sync. achieved, S11 is de-activated. IC4a CLOCK input is then switched to logic '1' and the 5V D input appears at the Q output. This is inverted in IC24f to present a logic '0' to the SYNC LED which is illuminated. The system remains in this condition until RESET, ie. when the μP system is in the hopping mode it remains in this mode even if the FUNCTION switch is set to OFF or SYNC.
S12	14	Logic '1' is applied IC1d pin 13. Tri-state buffers IC6d and IC6e are then enabled allowing 10MHz (A) and 10MHz (B) data from the FREQUENCY selectors onto the data bus.
S13	13	Logic '1' is applied to IC12b pin 6. Tri-state buffers IC7 and IC19 are then enabled allowing 1kHz and 10kHz FREQUENCY selector data onto the data bus.
S14	16	Logic '1' is applied to IC12a pin 1. Tri-state buffers IC19 and IC26 are then enabled allowing 100kHz and 1MHz FREQUENCY selector data onto the data bus.

Address Latch

113. Address latch IC23 comprises four separate latches each with their own data inputs (D0–D3) and complementary Q outputs (Q0 – Q3, $\overline{Q0}$ – $\overline{Q3}$). The latches share a common clock (pin 5) derived from μP timing pulse TPA. The polarity input (pin 6) is held at logic '1' which means that data input is transferred to the Q output during the high clock level. When the clock returns to logic '0' the 4 bits (MA0, 1, 2,7) of the higher order address, on the address bus, are latched.

Address Decoder

114. Address decoder IC10 is a 4 to 16 line decoder with latched inputs, (MA3, 4, 5, 6 of the higher order address bits), which presents a logic '1' at the selected output. Data is held in the latches when the strobe (pin 1) is at logic '1' and is decoded and output during the strobe transition to logic '0'. During system reset the inhibit input (pin 23) is at logic '1' and all outputs are set to logic '0'.

Output Latches

115. Two types of output latches are used. IC4, 5 and IC13 conventional dual D type flip-flops, their operation being described in TABLE 2, and IC25 and IC18 are dual 4-bit latches. Each latch has separate strobe, reset and output disable control, when the strobe line (pins 2 and 14) is at logic '1' the data on the data input lines (D0—D3) are transferred to the corresponding Q outputs, providing the disable line (pins 3 and 15) is at logic '0'. If the disable line is at logic '1' the outputs are forced to a high impedance state. The reset line (pins 1 and 13) is held permanently at logic '0' and is therefore inoperative.

Tri—State Buffers

116. IC6, 7, 19 and 26 are hex non-inverting buffers with three state outputs. The three state output of each buffer is controlled by two enable inputs ($\overline{E0}_4$, pin 1 and $\overline{E0}_2$, pin 15). A logic '1' on $\overline{E0}_4$ causes the outputs of four of the six buffers to assume a high impedance or OFF state, regardless of other input conditions, and a logic '1' on $\overline{E0}_2$ causes the outputs of the other two buffers to assume a high impedance or OFF state.

RAMS

117. One of two types of random access memories may be used (IC16 and 17):

(a) IM6561
(b) P2111

118. Two 1024 bits static RAM's, each organised into 256 by 4 bits, are connected in parallel. Each RAM has an 8-bit address input ($A_0 - A_7$) and a 4-bit output.

119. The IM6561 loads addresses on the falling edge of strobe signal STR and an output latch maintains the data when STR returns to logic '1'. A read cycle is performed when the R/$\overline{W}$ input is a logic '1' which causes memory data to be output. When $\overline{CS1}$ = $\overline{CS2}$ = STR = R/$\overline{W}$ = logic '0' a write cycle is performed which causes the outputs to go to a high impedance state. A memory functions table is shown below:

STR	$\overline{CS1}$	$\overline{CS2}$	R/$\overline{W}$	OPERATION	OUTPUT
0	0	0	0	WRITE	HIGH IMPEDANCE
0	0	0	1	READ	MEMORY DATA
X	0	1	X	HOLD	HIGH IMPEDANCE
X	1	0	X	HOLD	HIGH IMPEDANCE

The strobe (STR) and chip select ($\overline{CS1}$, $\overline{CS2}$) inputs are derived from address decoder output S2, STR being connected via link LK1.

120. The P2111 RAM is identical to the IM6561 except that pin 9 is an output disable pin. With a P2111 in circuit, pin 9 is connected to the $\overline{MRD}$ line of the μP via link LK1, thus enabling the output drivers of the P2111 when data is to be read from the RAM, and disabling the output when data is to be written into the RAM.

Bandwidth/Dwell Time Switch

121. SA is an 8-bit data switch, each bit being set manually to give a specific binary output. When enabled by a logic '0' from the address decoder (S7) the data is placed on the data bus. The data contained in the switch is the bandwidth and dwell time for the frequency ' hop '.

122. Bits 1—4 provide 15 sets of dwell time data. A switch closure represents logic '0' and a swtich operating represetns logic '1'. The dwell time is equal to the binary output X 70ms (approx.), where bit 1 is the L.S.B. All switches closed ('0' s) is a forbidden state.

123. Bits 5—7 provide 4 bandwidths over which the Synthesiser can hop:

000 : 16kHz (2^4)
100 : 32kHz (2^5)
110 : 64kHz (2^6)
111 : 100kHz (2^7)

124. Test switch SB is a similar switch used for testing the data bus lines.

Function Switch

125. FUNCTION SWITCH S13 is a four position rotary switch. The four positions are:

1. RESET
2. OFF
3. FAM
4. SYNC.

The SYNC position is spring biased to the FAM position.

Code Switch

126. The CODE switches are standard thumbwheel switches mounted on the front panel. The internal coding of the switch is such that it produces the complement of 9's complement code at its outputs for every number selected.

Power Supply

127. All the ICs are fed with + 5V from the regulator IC27 except for IC8 and IC20 in the sync. demodulator/modulator circuits. These are supplied directly from +12V line derived from the Synthesiser, as is the +5V regulator.

SERVICING AND TEST INSTRUCTIONS

128. Procedures are given in the following paragraphs for testing the FPU together with the Synthesiser.

TEST EQUIPMENT

129. The following items of test equipment are required:

Oscilloscope (Tektronics 465)
Multimeter (AVO Model 8)
Frequency Counter (Racal 9839)
Spectrum Analyser (HP 141)
Power Supply, 12V at 1,5A (Kinghill 18V 10)
Digital Voltmeter (HP)
Hopping Synthesiser Test Jig
Resistor, 51 ohms, 0,25W.

Note: If a Tektronix 465 oscilloscope is used, the frequency counter may be connected to the Ch.1 output of the 465. All frequency measurement can then be made via Ch.1 of the oscilloscope.

PRELIMINARY OPERATIONS

130. The following preliminary operations should be made prior to performing the Test Procedures detailed later.

1. Set MODE Switch to RESET position.
2. Set VFO Switch to OFF position.

TEST PROCEDURES

Power Supplies

131. 1. Measure resistance of pins 21 and 22 of PL30, to frame.
Check that the resistance is greater than 200k.
2. Remove Links 1 – 3 on the Synthesiser PCB.
3. Apply 12V to PL30 of the Synthesiser PCB, +ve to pin 22, –ve to pin 21.
4. Measure voltages as follows:
(a) Link 1 : 5V ±0,2V
(b) Link 2 : 8,5V set with R3 to within ±0,2V of 8,5V
(c) Link 3 : 20V Min
5. Replace Links 1 – 3.

Checking Synthesiser Frequencies.

132. 1. Connect the frequency counter to test point (TP) 5, on the Synthesiser.
Adjust R34 to give 5MHz ± 1Hz.

2. Connect oscilloscope to PCB pin 8.
Check for 1 MHz ±1 Hz, 4V p to p ±0,5V p to p square wave.

3. Connect the oscilloscope to TP 3, or IC9.11 or IC4.5
Check for 1kHz ±1 Hz.

4. Set FREQUENCY switches to 1,6MHz.

5. Ensure Link 4 is connected.

6. Connect the frequency counter to PCB pin 13 (earth lead to pin 14).
Check frequency is 37MHz ±2 Hz.

7. Set FREQUENCY Switches to 29,999MHz.

8. Measure the voltage across Link 4 with the digital meter.
Check the voltage is 16V ±0,5V.
Adjust L3 as necessary.

9. Using the frequency counter check the frequency at PCB pin 13.
This should be 65,399MHz ± 20Hz.
Adjust as necessary with R34 of the TXCO.

10. Connect the Spectrum Analyser to pins 13 and 14.

11. Measure the 1kHz switching side bands at :

(a) 29,999MHz
(b) 16MHz
(c) 1,6MHz.
Check that these are more than 45dB below the main signal.

12. Connect 51 ohm resistor across PCB pins 13 and 14.

13. Measure output level at the following frequencies:

    (a) 29,999 MHz

    (b) 16 MHz

    (c) 1,6 MHz

    The levels should be 800mV, peak-to-peak, ±50mV.

14. Remove resistor and spectrum analyser.

VFO

133. 1. Select 1,6 MHz on FREQUENCY Switches.

    2. Switch VFO Control ON (Fully clockwise).

    3. Connect the frequency counter to PCB pins 13 and 14.
    Adjust C36 for a frequency of 37,000520 MHz.

    4. Turn VFO control fully counter-clockwise (NOT OFF).
    Check that output frequency is 36,999500 MHz or lower.

    5. Adjust C36 so that the variation above and below 37 MHz is approximately equal.

    6. Set VFO Control to give an output of 37 MHz ±20 Hz.
    Check that the pointer on the VFO Control is within 30° of vertical.

    7. Set VFO to OFF.

35,4 MHz Loop

134. 1. Remove Link 5.

    2. Connect the frequency counter to TP13.
    Adjust L5 to give 35,4 MHz ±10 kHz.

    3. Connect the 51 ohm resistor across PCB pins 12 and 11.

    4. Connect oscilloscope to pins 12 and 11 (ground clip of scope).
    Tune T3 and T4 for maximum output.

    5. Connect Link 5.
    Short emitter to base of TR20.

    6. Measure the d.c. voltage on Link 5.
    Adjust R117 for 5V d.c.

    7. Measure the output level across the 51 ohms.
    Check the level is 420mV, peak-to-peak, ±50mV.
    Remove short from TR20.

    8. Connect the oscilloscope to Link 5.
    Adjust L5, if necessary, to give 5V ±0,5V.
    Measure output frequency and level at pins 11 and 12.
    Frequency must be 35,4 MHz ±10 Hz.
    Level must be 420mV p to p ±50mV across 51Ω.

FSK Adjustment

135. 1. Connect a 22k resistor from + 12V to the base of TR1 on the Generator PCB.

    2. Connect + 12V d.c. to collector of TR2, or short emitter to collector.

3. Connect counter to pin 1 of IC20.
Adjust R27 to give 2 325Hz ± 2Hz.

4. Remove the 22k resistor from the base of TR1.
Adjust R28 to give 1 475Hz ± 2Hz.

5. Connect 100k resistor across pins 1 and 4 on SK19 of the Decoupling PCB.

6. Connect the counter to pin 8 of IC8.
Adjust R11 for maximum output.

7. Reconnect +12V d.c. via 22k resistor to base of TR1.

8. Connect oscilloscope to pin 14 of IC8.
Adjust R14 for maximum output.

9. Remove 12V from collector of TR2, the 22k resistor from, TR1 and the 100k resistor from PL19.

Generator

136. 1. Set SB 1-8 to ON.

2. Set SA 1, 2, 4 and 8 to ON and 3, 5 ,6 and 7 to OFF.

3. Set MODE switch to RESET.

4. Connect oscilloscope to pin 16 (TPB), IC21.33
Check for a Low on oscilloscope .
Check on front panel that no LED's are illuminated.

5. Set MODE switch to OFF.
Check the output on pin 16 toggles.
Check that no LED's are illuminated on front panel.

6. Set MODE switch to FAM.
Check the output on pin 16 toggles.
Check that the ON LED is illuminated.

7. Set the MODE switch to SYNC.
Check the SYNC LED illuminates after approximately 2s.

8. Connect the Synthesiser to the test jig as follows:
25 way socket SK5 to the corresponding connector on the test jig.
9 way socket SK19 to the corresponding connector on the test jig.

9. Set the frequency on the test jig and the Synthesiser to 2 MHz and the code to 123021.

10. Set both MODE switches to FAM.

11. Initiate sync. on the test jig.
Check that both SYNC. LED's take more than 2s to illuminate.
Check that no ERROR LED's illuminate.

12. Switch Synthesiser and test jig to RESET.

13. Change both CODE switches to 210312.

14. Set both MODE switches to FAM.

15. Initiate sync. on the Synthesiser under test.
Check that both SYNC. LED's take longer than 2s to illuminate.
Check that no ERROR LED's illuminate.
Check that PTT LED on test jig illuminates when sync. is initiated and that it is extinguished when sync. is completed.

16. Switch off and disconnect all equipment.

PARTS LIST

137. The component tolerances and ratings given in this parts list are optimum. However if such components are not immediately available alternatives with closer tolerances and/or higher wattage or voltage ratings may be used in manufacture or supplied as replacements.

138. When ordering replacements please quote the full description including the circuit reference and the Order Number.

FREQUENCY PROCESSING UNIT

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
		1100-0871		**UNIT**	**FREQUENCY PROCESSOR**	
				Sub-Assemblies		
		1300-0868			Synthesiser PCB	
		1300-0966			Generator PCB	
		1300-0990			Code Switch PCB	
		1300-0991			Frequency Switch PCB	
		1300-1057			Decoupling PCB	
				Capacitors		
	C1	2600-3293			Ceramic 100nF 10p.c. 100V	
	C2	2600-3293			Ceramic 100nF 10p.c. 100V	
				Cable Assemblies		
		1400-1035			Cable, Flat Assembly 26W	
	SK29	3300-1600			Ansley Socket, F, 609-2600M 26W	
	SK30	3300-1600			Ansley Socket, F, 609-2600M 26W	
	SK31	3300-1600			Ansley Socket, F, 609-2600M 26W	
		4100-5784			Flat Tape, 0,128M 26W	
		1400-1036			Cable, Flat Assembly 10W	
	SK33	3300-1598			Ansley Socket, F, 609-1001M 10W	
	SK34	3300-1598			Ansley Socket, F, 609-1001M 10W	
		4100-5783			Flat Tape, 0,073M 10W	
		1400-1037			Cable, Flat Assembly 20W	
	SK32	3300-1591			Ansley Socket, F, 609-2600M 20W	
		3300-2817			Ansley Soldr. Conn. 609-2003 20W	
		3300-5785			Flat Tape, 0,048M 40W	
					(Split to form 2 x 20W Cables)	

FREQUENCY PROCESSOR UNIT (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
		1400-1037			Cable, Flat Assembly 20W	
	SK35	3300-1591			Ansley Socket, F, 609-2600M 20W	
		3300-1817			Ansley Soldr. Conn. 609-2003 20W	
		3300-5785			Flat Tape, 0,048M 40W	
					(Split to form 2 x 20W Cables)	
				Diodes		
	D1	3600-1321			LED YL INT MTG Black 406-Y	
	D2	3600-1322			LED GN INT MTG Black 406-G	
	D3	3600-0404			1N 4153	
				Resistors		
	R1	2200-0424			Variable (with switch) 10k	
	R2				Not Used	
	R3	2000-0334			Carbon 560 ohms 5p.c. 0,25W	
	R4	2000-0313			Carbon 10 ohms 5p.c. 0,25W	
				Switches		
	S12				Part of R1	
	S13				Rotary 4P4W OAK 10-01/000-091	

SYNTHESISER PCB

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION			NO/UNIT
		1300-0868		**PCB**	**SYNTHESISER**			
				Sub-Assembly				
		1300-1233			Integrator Assembly (Potted)			
				Capacitors				
	C1				Not Used			
	C2	2600-3123			Ceramic	100nF	10p.c. 100V	
	C3	2500-3616			Tantalum	47uF	35V	
	C4	2500-6064			Tantalum	1uF	20 35V	
	C5	2500-6064			Tantalum	1uF	20p.c. 35V	
	C6	2600-3123			Ceramic	100nF	10p.c. 100V	
	C7	2500-3616			Tantalum	47uF	35V	
	C8	2500-6057			Tantalum	33uF	20p.c. 25V	
	C9	2600-2535			Ceramic	10nF	10p.c. 200V	
	C10	2500-6057			Tantalum	33uF	20p.c. 25V	
	C11	2600-9212			Ceramic	47nF	10p.c. 100V	
	C12	2500-6064			Tantalum	1uF	20p.c. 35V	
	C13				Not Used			
	C14				Not Used			
	C15	2600-3123			Ceramic	100nF	10p.c. 100V	
	C16	2600-3123			Ceramic	100nF	10p.c. 100V	
	C17	2600-9212			Ceramic	47nF	10p.c. 100V	
	C18	2600-9212			Ceramic	47nF	10p.c. 100V	
	C19	2600-1563			Ceramic	330pF	5p.c. 200V	
	C20	2600-3227			Ceramic	220nF	20p.c. 50V	
	C21	2600-0204			Ceramic	6,8pF	5p.c. 200V	

SYNTHESISER PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	C22	2600-1086			Ceramic 56pF 5p.c. 200V	
	C23	2600-2026			Ceramic 1nF 10p.c. 100V	
	C24	2600-2026			Ceramic 1nF 10p.c. 100V	
	C25	2600-2026			Ceramic 1nF 10p.c. 100V	
	C26	2500-4014			Tantalum 100uF 16V	
	C27	2600-2535			Ceramic 10nF 10p.c. 200V	
	C28	2500-4014			Tantalum 100uF 16V	
	C29	2600-2912			Ceramic 47nF 10p.c. 100V	
	C30	2600-2912			Ceramic 47nF 10p.c. 100V	
	C31	2600-1709			Ceramic 470pF 10p.c. 200V	
	C32	2600-2912			Ceramic 47nF 10p.c. 100V	
	C33	2600-1709			Ceramic 470pF 10p.c. 200V	
	C34	2600-2912			Ceramic 47nF 10p.c. 100V	
	C35	2600-1244			Ceramic 120pF 5p.c. 200V	
	C36	2800-0029			Variable, Single, 4,5-20pF	
	C37	2600-1308			Ceramic 150pF 5p.c. 200V	
	C38	2600-1308			Ceramic 150pF 5p.c. 200V	
	C39	2600-1709			Ceramic 470pF 10p.c. 200V	
	C40	2500-6070			Tantalum 10uF 20p.c. 35V	
	C41	2600-2912			Ceramic 47nF 10p.c. 100V	
	C42	2600-1563			Ceramic 330pF 5p.c. 200V	
	C43	2600-2912			Ceramic 47nF 10p.c. 100V	
	C44	2600-2912			Ceramic 47nF 10p.c. 100V	
	C45	2600-2912			Ceramic 47nF 10p.c. 100V	
	C46	2600-2912			Ceramic 47nF 10p.c. 100V	
	C47	2600-2912			Ceramic 47nF 10p.c. 100V	
	C48	2600-2912			Ceramic 47nF 10p.c. 100V	
	C49	2600-2535			Ceramic 10nF 10p.c. 200V	

SYNTHESISER PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	C50	2600-2535			Ceramic 10nF 10p.c. 200V	
	C51	2600-3123			Ceramic 100nF 10p.c. 100V	
	C52	2600-3123			Ceramic 100nF 10p.c. 100V	
	C53	2600-3123			Ceramic 100nF 10p.c. 100V	
	C54	2600-3123			Ceramic 100nF 10p.c. 100V	
	C55	2600-3123			Ceramic 100nF 10p.c. 100V	
	C56	2600-3123			Ceramic 100nF 10p.c. 100V	
	C57	2600-2535			Ceramic 10nF 10p.c. 200V	
	C58	2600-2535			Ceramic 10nF 10p.c. 200V	
	C59	2600-2535			Ceramic 10nF 10p.c. 200V	
	C60	2600-0414			Ceramic 10pF 5p.c. 200V	
	C61	2600-1709			Ceramic 470pF 10p.c. 200V	
	C62	2600-3123			Ceramic 100nF 10p.c. 100V	
	C63	2600-0718			Ceramic 22pF 5p.c. 200V	
	C64	2600-3123			Ceramic 100nF 10p.c. 100V	
	C65	2600-2535			Ceramic 10nF 10p.c. 200V	
	C66	2600-2535			Ceramic 10nF 10p.c. 200V	
	C67	2600-2026			Ceramic 1nF 10p.c. 100V	
	C68	2600-2912			Ceramic 47nF 10p.c. 100V	
	C69	2600-0718			Ceramic 22pF 10p.c. 200V	
	C70	2600-2535			Ceramic 10nF 10p.c. 200V	
	C71	2600-2912			Ceramic 47nF 10p.c. 100V	
	C72	2600-2912			Ceramic 47nF 10p.c. 100V	
	C73	2600-2912			Ceramic 47nF 10p.c. 100V	
	C74	2600-2535			Ceramic 10nF 10p.c. 200V	
	C75	2600-2535			Ceramic 10nF 10p.c. 200V	
	C76	2600-0414			Ceramic 10pF 5p.c. 200V	

SYNTHESISER PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	C77	2600-2535			Ceramic 10nF 10p.c. 200V	
	C78	2600-1107			Ceramic 68pF 5p.c. 200V	
	C79	2600-0983			Ceramic 39pF 5p.c. 200V	
	C80	2600-3123			Ceramic 100nF 10p.c. 100V	
	C81	2600-0718			Ceramic 22pF 10p.c. 200V	
	C82	2600-2535			Ceramic 10nF 10p.c. 200V	
	C83	2600-2535			Ceramic 10nF 10p.c. 200V	
	C84	2600-0906			Ceramic 33pF 5p.c. 200V	
	C85	2600-0906			Ceramic 33pF 5p.c. 200V	
	C86	2600-2535			Ceramic 10nF 10p.c. 200V	
	C87	2600-2535			Ceramic 10nF 10p.c. 200V	
	C88	2600-0906			Ceramic 33pF 5p.c. 200V	
	C89	2600-2535			Ceramic 10nF 10p.c. 200V	
	C90	2600-2535			Ceramic 10nF 10p.c. 200V	
	C91	2600-2535			Ceramic 10nF 10p.c. 200V	
	C92	2600-0906			Ceramic 33pF 5p.c. 200V	
	C93	2500-6064			Tantalum 1uF 20p.c. 35V	
	C94	2600-2912			Ceramic 47nF 10p.c. 100V	
	C95	2600-3123			Ceramic 100nF 10p.c. 100V	
	C96	2600-2535			Ceramic 10nF 10p.c. 200V	
	C97	2600-2912			Ceramic 47nF 10p.c. 100V	
	C98	2600-2912			Ceramic 47nF 10p.c. 100V	
	C99	2600-2912			Ceramic 47nF 10p.c. 100V	
	C100	2600-2912			Ceramic 47nF 10p.c. 100V	
	C101	2600-2912			Ceramic 47nF 10p.c. 100V	
	C102	2600-2912			Ceramic 47nF 10p.c. 100V	

SYNTHESISER PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	C103	2600-2912			Ceramic 47nF 10p.c. 100V	
	C104	2600-2912			Ceramic 47nF 10p.c. 100V	
	C105	2600-2912			Ceramic 47nF 10p.c. 100V	
	C106	2500-6057			Tantalum 33uF 20p.c. 25V	
	C107	2500-6064			Tantalum 1uF 20p.c. 35V	
				Diodes		
	D1	3600-0404			IN4153	
	D2	3600-0404			Not Used	
	D3	3600-0404			Not Used	
	D4	3600-0404			Not Used	
	D5	3600-0421			VARICAP ZC806 Matched Pair	
	D6	3600-0421			VARICAP ZC806	
	D7	3600-0404			IN4153	
	D8	3600-0404			IN4153	
	D9	3600-0404			IN4153	
	D10	3600-0404			IN4153	
	D11	3600-0404			IN4153	
	D12	3600-0419			VARICAP ZC806	
	D13	3600-1275			HP 5082-2835	
	D14	3600-1275			HP 5082-2835	
	D15	3600-8282			VARICAP BB709	
	D16	3600-0404			IN4153	
	D17	3600-0404			IN4153	
				Resistors		
	R1	2000-0317			Carbon 22 ohm 5p.c. 0,25W	
	R2	2000-0329			Carbon 222 0hm 5p.c. 0,25W	

SYNTHESISER PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	R3	2200-0143			Variable 5k	
	R4	2000-0329			Carbon 220 ohm 5p.c. 0,25W	
	R5	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R6	2000-0352			Carbon 22k 5p.c. 0,25W	
	R7	2000-0345			Carbon 4k7 5p.c. 0,25W	
	R8	2000-0319			Carbon 33 ohm 5p.c. 0,25W	
	R9	2000-0365			Carbon 220k 5p.c. 0,25W	
	R10	2000-0365			Not Used	
	R11	2000-0365			Not Used	
	R12	2000-0328			Carbon 180 ohm 5p.c. 0,25W	
	R13	2000-0334			Carbon 560 ohm 5p.c. 0,25W	
	R14	2000-0349			Carbon 10k 5p.c. 0,25W	
	R15	2000-0349			Carbon 10k 5p.c. 0,25W	
	R16	2000-0327			Carbon 150 ohm 5p.c. 0,25W	
	R17	2000-0334			Carbon 560 ohm 5p.c. 0,25W	
	R18	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R19	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R20	2000-0329			Carbon 220 ohm 5p.c. 0,25W	
	R21	2000-0339			Carbon 1k5 5p.c. 0,25W	
	R22	2000-0345			Carbon 4k7 5p.c. 0,25W	
	R23	2000-0349			Carbon 10k 5p.c. 0,25W	
	R24	2000-0359			Carbon 68k 5p.c. 0,25W	
	R25	2000-0325			Carbon 100 ohm 5p.c. 0,25W	
	R26	2000-0325			Carbon 100 ohm 5p.c. 0,25W	
	R27	2000-0341			Carbon 2k2 5p.c. 0,25W	
	R28	2000-0353			Carbon 22k 5p.c. 0,25W	
	R29	2000-0353			Carbon 22k 5p.c. 0,25W	
	R30	2000-0321			Carbon 47 ohm 5p.c. 0,25W	

SYNTHESISER PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	R31				Not Used	
	R32	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R33	2000-0341			Carbon 2k2 5p.c. 0,25W	
	R34	2200-0147			Variable 10k	
	R35	2000-0336			Carbon 820 ohm 5p.c. 0,25W	
	R36	2000-0346			Carbon 5k6 5p.c. 0,25W	
	R37	2000-0340			Carbon 1k8 5p.c. 0,25W	
	R38	2000-0349			Carbon 10k 5p.c. 0,25W	
	R39	2000-0339			Carbon 1k5 5p.c. 0,25W	
	R40	2000-0342			Carbon 2k7 5p.c. 0,25W	
	R41	2000-0341			Carbon 2k2 5p.c. 0,25W	
	R42	2000-0337			Carbon 1k 5p.c. 0,25W	
	R43	2000-0325			Carbon 100 ohm 5p.c. 0,25W	
	R44	2000-0355			Carbon 33k 5p.c. 0,25W	
	R45	2000-0337			Carbon 1k 5p.c. 0,25W	
	R46	2000-0353			Carbon 22k 5p.c. 0,25W	
	R47	2000-0347			Carbon 6k8 5p.c. 0,25W	
	R48	2000-0332			Carbon 390 ohm 5p.c. 0,25W	
	R49	2000-0336			Carbon 820 ohm 5p.c. 0,25W	
	R50	2000-0342			Carbon 2k7 5p.c. 0,25W	
	R51				Carbon S.O.T. 5p.c. 0,25W	
	R52	2000-0355			Carbon 33k 5p.c. 0,25W	
	R53	2000-0343			Carbon 3k3 5p.c. 0,25W	
	R54	2000-0344			Carbon 3k9 5p.c. 0,25W	
	R55	2000-0350			Carbon 12k 5p.c. 0,25W	
	R56	2000-0343			Carbon 3k3 5p.c. 0,25W	
	R57	2000-0325			Carbon 100 ohm 5p.c. 0,25W	
	R58	2000-0337			Carbon 1k 5p.c. 0,25W	

SYNTHESISER PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	R59	2000-0331			Carbon 330 ohm 5p.c. 0,25W	
	R60	2000-0355			Carbon 33k 5p.c. 0,25W	
	R61	2000-0325			Carbon 100 ohm 5p.c. 0,25W	
	R62	2000-0337			Carbon 1k 5p.c. 0,25W	
	R63	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R64	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R65	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R66	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R67	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R68	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R69	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R70	2000-0345			Carbon 4k7 5p.c. 0,25W	
	R71	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R72	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R73	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R74	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R75	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R76	2000-0349			Carbon 10k 5p.c. 0,25W	
	R77	2000-0343			Carbon 3k3 5p.c. 0,25W	
	R78	2000-0343			Carbon 3k3 5p.c. 0,25W	
	R79	2000-0339			Carbon 1k5 5p.c. 0,25W	
	R80	2000-0339			Carbon 1k5 5p.c. 0,25W	
	R81	2000-0339			Carbon 1k5 5p.c. 0,25W	
	R82	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R83	2000-0336			Carbon 820 ohm 5p.c. 0,25W	
	R84	2000-0341			Carbon 2k2 5p.c. 0,25W	

SYNTHESISER PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	R85	2000-0337			Carbon 1k 5p.c. 0,25W	
	R86	2000-0337			Carbon 1k 5p.c. 0,25W	
	R87	2000-0319			Carbon 33 ohm 5p.c. 0,25W	
	R88	2000-0317			Carbon 22 ohm 5p.c. 0,25W	
	R89	2000-0328			Carbon 180 ohm 5p.c. 0,25W	
	R90	2000-0325			Carbon 100 ohm 5p.c. 0,25W	
	R91	2000-0330			Carbon 270 ohm 5p.c. 0,25W	
	R92	2000-0325			Carbon 100 ohm 5p.c. 0,25W	
	R93	2000-0347			Carbon 6k8 5p.c. 0,25W	
	R94	2000-0341			Carbon 2k2 5p.c. 0,25W	
	R95	2000-0336			Carbon 820 ohm 5p.c. 0,25W	
	R96	2000-0337			Carbon 1k 5p.c. 0,25W	
	R97	2000-0337			Carbon 1k 5p.c. 0,25W	
	R98	2000-0350			Carbon 12k 5p.c. 0,25W	
	R99	2000-0342			Carbon 2k7 5p.c. 0,25W	
	R100	2000-0325			Carbon 100 ohm 5p.c. 0,25W	
	R101	2000-0337			Carbon 1k 5p.c. 0,25W	
	R102	2000-0331			Carbon 330 ohm 5p.c. 0,25W	
	R103	2000-0355			Carbon 33k 5p.c. 0,25W	
	R104	2000-0325			Carbon 100 ohm 5p.c. 0,25W	
	R105	2000-0337			Carbon 1k 5p.c. 0,25W	
	R106	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R107	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R108	2000-0349			Carbon 10k 5p.c. 0,25W	
	R109	2000-0313			Carbon 10 ohm 5p.c. 0,25W	
	R110	2000-0349			Carbon 10k 5p.c. 0,25W	
	R111	2000-0325			Carbon 100 ohm 5p.c. 0,25W	
	R112	2000-0349			Carbon 10k 5p.c. 0,25W	

SYNTHESISER PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	R113	2000-0349			Carbon 10k 5p.c. 0,25W	
	R114	2000-0353			Carbon 22k 5p.c. 0,25W	
	R115	2000-0338			Carbon 1k2 5p.c. 0,25W	
	R116	2000-0353			Carbon 22k 5p.c. 0,25W	
	R117	2200-0147			Variable 10k	
	R118	2000-0345			Carbon 4k7 5p.c. 0,25W	
	R119	2000-0361			Carbon 100k 5p.c. 0,25W	
	R120	2000-0361			Carbon 100k 5p.c. 0,25W	
	R121	2000-0332			Carbon 390 ohm 5p.c. 0,25W	
	R122	2000-0351			Carbon 15k 5p.c. 0,25W	
	R123	2000-0352			Carbon 18k 5p.c. 0,25W	
	R124	2000-0325			Carbon 100 ohm 5p.c. 0,25W	
	R125	2000-0332			Carbon 390 ohm 5p.c. 0,25W	
	R126	2000-0324			Carbon 82 ohm 5p.c. 0,25W	
	R127	2000-0325			Carbon 100 ohm 5p.c. 0,25W	
	R128	2000-0354			Carbon 27k 5p.c. 0,25W	
	R129	2000-0349			Carbon 10k 5p.c. 0,25W	
	R130	2000-0341			Carbon 2k2 5p.c. 0,25W	
	R131	2000-0341			Carbon 2k2 5p.c. 0,25W	
	R132	2000-0353			Carbon 22k 5p.c. 0,25W	
	R133	2000-0349			Carbon 10k 5p.c. 0,25W	
	R134	2000-0339			Carbon 1k5 5p.c. 0,25W	
	R135	2000-0339			Carbon 1k5 5p.c. 0,25W	
	R136	2000-0349			Carbon 10k 5p.c. 0,25W	
	R137	2000-0341			Carbon 2k2 5p.c. 0,25W	
	R138	2000-0345			Carbon 4k7 5p.c. 0,25W	
	R139	2000-0349			Carbon 10k 5p.c. 0,25W	
	R140	2000-0345			Carbon 4k7 5p.c. 0,25W	
	R141	2000-0313			Carbon 10 ohm 5p.c. 0,25W	

SYNTHESISER PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	R142	2000-0346			Carbon 5k6 5p.c. 0,25W	
	R143	2000-0346			Carbon 5k6 5p.c. 0,25W	
	R144	2000-0325			Carbon 100 ohm 5p.c. 0,25W	
	R145	2000-0337			Carbon 1k 5p.c. 0,25W	
	R146	2000-0334			Carbon 560 ohm 5p.c. 0,25W	
	R147	2000-0349			Carbon 10k 5p.c. 0,25W	
	R148	2000-0342			Carbon 2k7 5p.c. 0,25W	
	IRA1	2300-0989			R-Network, 22k x 9, 1 Comm. 10SIL Package	
	IRA2	2300-0989			R-Network, 22k x 9, 1 Comm. 10SIL Package	
				Integrated Circuits		
	IC1	3600-0534			LM309 K, V.Reg. +5V	
	IC2	3600-6061			LM 317 T, V.Reg. Var.	
	IC3	3600-6606			78 L15 A, V.Reg. + 15V	
	IC4	3600-0489			7473, TTL, Dual JK Flip-Flop	
	IC5	3600-0507			74500, Schottky TTL, Quad 2 I/P NAND	
	IC6	3600-0491			7490, TTL, Divide-by-10 Counter	
	IC7	3600-0491			7490, TTL, Divide-by-10 Counter	
	IC8	3600-0491			7490, TTL, Divide-by-10 Counter	
	IC9	3600-0491			7490, TTL, Divide-by-10 Counter	
	IC10	3600-0507			74500, Schottky TTL, Quad 2 I/P NAND	
	IC11	3600-0487			7430, TTL, 8 I/P NAND Gate.	
	IC12	3600-0504			74176, TTL, 4 Bit ALU	
	IC13	3600-0504			74176, TTL, 4 Bit ALU	
	IC14	3600-0504			74176, TTL, 4 Bit ALU	
	IC15	3600-0504			74176, TTL, 4 Bit ALU	
	IC16	3600-0504			74176, TTL, 4 Bit ALU	
	IC17	3600-0507			74500, Schottky TTL, Quad 2 I/P NAND	
	IC18	3600-6169			SP8690, 10/11 Divider	

SYNTHESISER PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	IC19	3600-0631			4049, HEX INV/BUFFER	
	IC20	3600-0631			4049, HEX INV/BUFFER	
	IC21	3600-0631			4049, HEX INV/BUFFER	
	IC22	3600-0491			7490, TTL, Divide-by-10 Counter	
	IC23	3600-0491			7490, TTL, Divide-by-10 Counter	
	IC24	3600-0630			4027, CMOS, Dual K Flip-Flop	
	IC25	3600-0599			CA3130 Op. Amp.	
				Miscellaneous		
	FS1	2900-0029			Fuse 2A FB, 5 x 20mm	
	L1	3100-0126			Inductor	
	L2	3100-0125			Inductor	
	L3	3100-0671			Inductor, Variable	
	L4	3100-1033			Choke, 47μH, 10%, Sub-Min. BS 9751	
	L5	3100-0670			Inductor, Variable	
	T1	3100-0673			Transformer, 14t = 2t	
	T2	3100-0829			Transformer, 3t = 1t	
	T3	3100-0672			Transformer, 9t = 1t	
	T4	3100-0672			Transformer, 9t = 1t	
	XI	3700-0015			TXCO, 5MHz, 9V, 0,5ppm.	
	XL1	3700-0011			Crystal, 5MHz	
	XL2	3700-0083			Filter, Crystal, 35,4 MHz, Spec. B1557	
	PL30	3300-9508			Connector, 26way, Ansley 609-2602M	
				Transistors		
	TR1	3600-0185			2N3904, Si, NPN	
	TR2	3600-0027			BC261B, Alt : BC 1778, CN 41546	
	TR3				Not Used	

SYNTHESISER PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	TR4				Not Used	
	TR5				Not Used	
	TR6	3600-0027			BC261B, Alt. BC1778, CN 41546	
	TR7	3600-0144			2N2369 , NPN	
	TR8	3600-2987			FET 3N202	
	TR9	3600-0144			2N2369 , NPN	
	TR10	3600-0144			2N2369 , NPN	
	TR11	3600-0144			2N2369 , NPN	
	TR12	3600-0185			2N3904, Si, NPN	
	TR13	3600-0144			2N2369, NPN	
	TR14	3600-0144			2N2369, NPN	
	TR15	3600-0144			2N2369, NPN	
	TR16	3600-0144			2N2369, NPN	
	TR17	3600-0144			2N2369, NPN	
	TR18	3600-3016			FET SD211	
	TR19	3600-3016			FET SD211	
	TR20	3600-3029			BF240, NPN	
	TR21	3600-0144			2N2369, NPN	
	TR22	3600-0185			2N3904 , Si, NPN	
	TR23	3600-6729			BF440, 7092, PNP	
	TR24	3600-6729			BF440, 7092, PNP	
	TR25	3600-0185			2N3904, Si, NPN	
	TR26	3600-6729			BF440, TO 92, PNP	
	TR27	3600-0187			2N3906, Si, PNP	
	TR28	3600-0185			2N3904 , Si, NPN	
	TR29	3600-0185			2N3904 , Si, NPN	

GENERATOR PCB

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
		1300-0966		**PCB**	**GENERATOR**	
				Capacitors		
	C1	2500-6064			Tantalum 1uF 20p.c. 35V	
	C2	2500-6042			Tantalum 10uF 20p.c. 16V	
	C3	2600-2535			Ceramic 10nF 10p.c. 200V	
	C4	2500-6064			Tantalum 1uF 20p.c. 35V	
	C5	2600-2535			Ceramic 10nF 10p.c. 200V	
	C6	2600-3123			Ceramic 100nF 10p.c. 100V	
	C7	2600-2026			Ceramic 1nF 10p.c. 100V	
	C8	2500-6042			Tantalum 10uF 20p.c. 16V	
	C9	2600-2026			Ceramic 1nF 10p.c. 100V	
	C10	2600-2026			Ceramic 1nF 10p.c. 100V	
	C11	2500-6042			Tantalum 10uF 20p.c. 16V	
	C12	2600-2410			Ceramic 6n8 5p.c. 100V	
	C13	2600-2410			Ceramic 6n8 5p.c. 100V	
	C14	2600-2410			Ceramic 6n8 5p.c. 100V	
	C15	2600-2410			Ceramic 6n8 5p.c. 100V	
	C16	2500-6042			Tantalum 10uF 20p.c. 16V	
	C17	2500-6042			Tantalum 10uF 20p.c. 16V	
	C18	2600-2645			Ceramic 22nF 10p.c. 100V	
	C19	2600-2645			Ceramic 22nF 10p.c. 100V	
	C20	2600-3123			Ceramic 100nF 10p.c. 100V	
	C21	2600-3123			Ceramic 100nF 10p.c. 100V	
	C22	2600-2026			Ceramic 1nF 10p.c. 100V	
	C23	2600-2410			Ceramic 6n8 5p.c. 100V	
	C24	2600-2410			Ceramic 6n8 5p.c. 100V	

GENERATOR PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	C25				Tantalum 10uF 20p.c. 16V	
	C26	2600-2026			Ceramic 1nF 10p.c. 100V	
	C27	2600-2026			Ceramic 1nF 10p.c. 100V	
	C28	2500-6042			Tantalum 10uF 20p.c. 16V	
	C29	2600-3123			Ceramic 100nF 10p.c. 100V	
	C30	2600-2535			Ceramic 10nF 10p.c. 200V	
	C31	2600-2535			Ceramic 10nF 10p.c. 200V	
				Connectors		
	PL31	3300-9508			26-way Ansley Rt. Angle 609-2602M	
	PL32	3300-1581			20-way HDR Rt. Angle 609-2002M	
	PL34	3300-1588			10-way Rt. Angle 609-1002M	
	PL35	3300-1581			20-way HDR Rt. Angle 609-2002M	
				Diodes		
	D1	3600-0404			IN4153	
	D2	3600-0404			IN4153	
	D3	3600-0404			IN4153	
	D4	3600-0404			IN4153	
	D5	3600-0404			IN4153	
	D6	3600-0404			IN4153	
	D7	3600-0404			IN4153	
	D8	3600-0404			IN4153	
	D9	3600-0340			Zener, 6V8, 5p.c., 0,4W, Do35, BZX79	
	D10	3600-0404			IN4153	
	D11	3600-0404			IN4153	
	D12	3600-0404			IN4153	
				Integrated Circuits		
	IC1	3600-0551			4011 B, Quad 2IP Nand Gate	
	IC2	3600-0631			4049 B, Quad, Inverting Buffer	

GENERATOR PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	IC3	3600-0740			4081 B, Quad 2 Input AND Gate	
	IC4	3600-0737			4013 B, Dual D-type Flip-flop	
	IC5	3600-0737			4013 B, Dual D-type Flip-flop	
	IC6	3600-6100			40097/80C97, 3-State Buffer	
	IC7	3600-6100			40097/80C97, 3-State Buffer	
	IC8	3600-0626			LM 324N, Op-Amp	
	IC9	3600-0614			4001 B, Quad 2 Input NOR Gate	
	IC10	3600-0742			14514 B Decoder	
	IC11	3600-0551			4011 B, Quad 2 Input NAND Gate	
	IC12	3600-0551			4011 B, Quad 2 Input NAND Gate	
	IC13	3600-0737			4013 B, Dual D-type Flip-flop	
	IC14	3600-0737			4013 B, Dual D-type Flip-flop	
	IC15	3600-0741			6561, RAM	
	IC16	3600-0741			6561, RAM	
		3600-0776			P211, Alternative for IC15 and IC16	
	IC17	3600-0740			4081 B, Quad 2 Input AND Gate	
	IC18	3600-0744			4508 B, 4 Bit Dual Latch	
	IC19	3600-6100			40097/80C97, 3-State Buffer	
	IC20	3600-0626			LM 324N, Op-Amp	
	IC21	3600-6078			CDP 1802, μProcessor, 40 DIL	
	IC22	6600-0009			2716 EPROM – Programmed	
	IC23	3600-0689			4042 B, Quad Latch CN2776	
	IC24	3600-0631			4049 B – Use Motorola Only	
	IC25	3600-0744			4508, 4 Bit Dual Latch	
	IC26	3600-6100			40097/80C97, 3-State Buffer	
	IC27	3600-0534			LM309K V. Reg, + 5V	
	IC28	3600-6284			LF441, Op-Amp	
				Inductors		
	L1	3100-1049			Choke, 1mH	
	L2	3100-1049			Choke, 1mH	

GENERATOR PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
				Resistors		
	R1	2000-0361			Carbon 100k 5p.c. 0,25W	
	R2	2000-0313			Carbon 10 ohms 5p.c. 0,25W	
	R3	2000-0337			Carbon 1k 5p.c. 0,25W	
	R4	2000-0361			Carbon 100k 5p.c. 0,25W	
	R5	2000-0350			Carbon 12k 5p.c. 0,25W	
	R6	2000-0361			Carbon 100k 5p.c. 0,25W	
	R7	2000-0330			Carbon 270 ohm 5p.c. 0,25W	
	R8	2000-0361			Carbon 100k 5p.c. 0,25W	
	R9	2000-0361			Carbon 100k 5p.c. 0,25W	
	R10	2000-0339			Carbon 1k5 5p.c. 0,25W	
	R11	2200-0194			Variable, 500 ohm	
	R12	2000-0361			Carbon 100k 5p.c. 0,25W	
	R13	2000-0334			Carbon 560 ohm 5p.c. 0,25W	
	R14	2200-0194			Variable, 500 ohm	
	R15	2000-0363			Carbon 150k 5p.c. 0,25W	
	R16	2000-0363			Carbon 150k 5p.c. 0,25W	
	R17	2000-0342			Carbon 2k7 5p.c. 0,25W	
	R18	2000-0342			Carbon 2k7 5p.c. 0,25W	
	R19	2000-0357			Carbon 47k 5p.c. 0,25W	
	R20	2000-0357			Carbon 47k 5p.c. 0,25W	
	R21	2000-0357			Carbon 47k 5p.c. 0,25W	
	R22	2000-0357			Carbon 47k 5p.c. 0,25W	
	R23	2000-0376			Carbon 2M2 5p.c. 0,25W	
	R24	2000-0341			Carbon 2k2 5p.c. 0,25W	
	R25	2000-0353			Carbon 22k 5p.c. 0,25W	
	R26	2000-0334			Carbon 560 ohm 5p.c. 0,25W	
	R27	2200-0233			Variable, 250 ohm	
	R28	2200-0194			Variable, 500 ohm	
	R29	2000-0336			Carbon 820 ohm 5p.c. 0,25W	

GENERATOR PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	R30	2000-0363			Carbon 150k 5p.c. 0,25W	
	R31	2000-0349			Carbon 10k 5p.c. 0,25W	
	R32	2000-0349			Carbon 10k 5p.c. 0,25W	
	R33	2000-0349			Carbon 10k 5p.c. 0,25W	
	R34	2000-0353			Carbon 22k 5p.c. 0,25W	
	R35	2000-0361			Carbon 100k 5p.c. 0,25W	
	R36	2000-0330			Carbon 270 ohm 5p.c. 0,25W	
	R37	2000-0337			Carbon 1k 5p.c. 0,25W	
	R38	2000-0341			Carbon 2k2 5p.c. 0,25W	
	R39	2000-0341			Carbon 2k2 5p.c. 0,25W	
	R40	2000-0337			Carbon 1k 5p.c. 0,25W	
	R41	2000-0361			Carbon 100k 5p.c. 0,25W	
	R42	2000-0336			Carbon 820 5p.c. 0,25W	
	R43	2000-0353			Carbon 22k 5p.c. 0,25W	
	R44	2000-0365			Carbon 220k 5p.c. 0,25W	
	R45	2000-0353			Carbon 22k 5p.c. 0,25W	
	IRA1	2300-0989			R. Net, 22k x 9, 1 Com. IOSIL 4310R-10-223	
	IRA2	2300-0988			R. Net, 22k x 5, 1 Com. 6SIL, 4306R-101-223	
				Switches		
	SA	3200-2697			SW, DIL, 16W, STNFRD ENG, 1008-692	
	SB	3200-2697			SW, DIL, 16W, STNFRD ENG, 1008-692	
				Transistors		
	TR1	3600-0971			MPSA –18, NPN	
	TR2	3600-0027			BC261, Alt. BC177B, PNP	
	TR3	3600-0027			BC261, Alt, BC177B, PNP	
	TR4	3600-0185			2N3904, Si, NPN	
	TR5	3600-0215			2N5306	

Code Switch PCB

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
		1300-0990		**PCB**	**Code Switch**	
				Diodes		
	D1	3600-0404			IN4153	
	D2	3600-0404			IN4153	
	D3	3600-0404			IN4153	
	D4	3600-0404			IN4153	
	D5	3600-0404			IN4153	
	D6	3600-0404			IN4153	
	D7	3600-0404			IN4153	
	D8	3600-0404			IN4153	
	D9	3600-0404			IN4153	
	D10	3600-0404			IN4153	
	D11	3600-0404			IN4153	
	D12	3600-0404			IN4153	
	D13	3600-0404			IN4153	
	D14	3600-0404			IN4153	
	D15	3600-0404			IN4153	
	D16	3600-0404			IN4153	
	D17	3600-0404			IN4153	
	D18	3600-0404			IN4153	
	D19	3600-0404			IN4153	
	D20	3600-0404			IN4153	
	D21	3600-0404			IN4153	
	D22	3600-0404			IN4153	
	D23	3600-0404			IN4153	
	D24	3600-0404			IN4153	

Code Switch PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	D25	3600-0404			IN4153;	
				Resistors		
	R1	2000-3274			Carbon 560 ohm 5p.c. 0,25W	
	R2	2000-3274			Carbon 560 ohm 5p.c. 0,25W	
				Switches		
	S6	1600-5719			Thumbwheel (Modified)	
	S7	1600-5719			Thumbwheel (Modified)	
	S8	1600-5719			Thumbwheel (Modified)	
	S9	1600-5719			Thumbwheel (Modified)	
	S10	1600-5719			Thumbwheel (Modified)	
	S11	1600-5719			Thumbwheel (Modified)	

Frequency Switch PCB

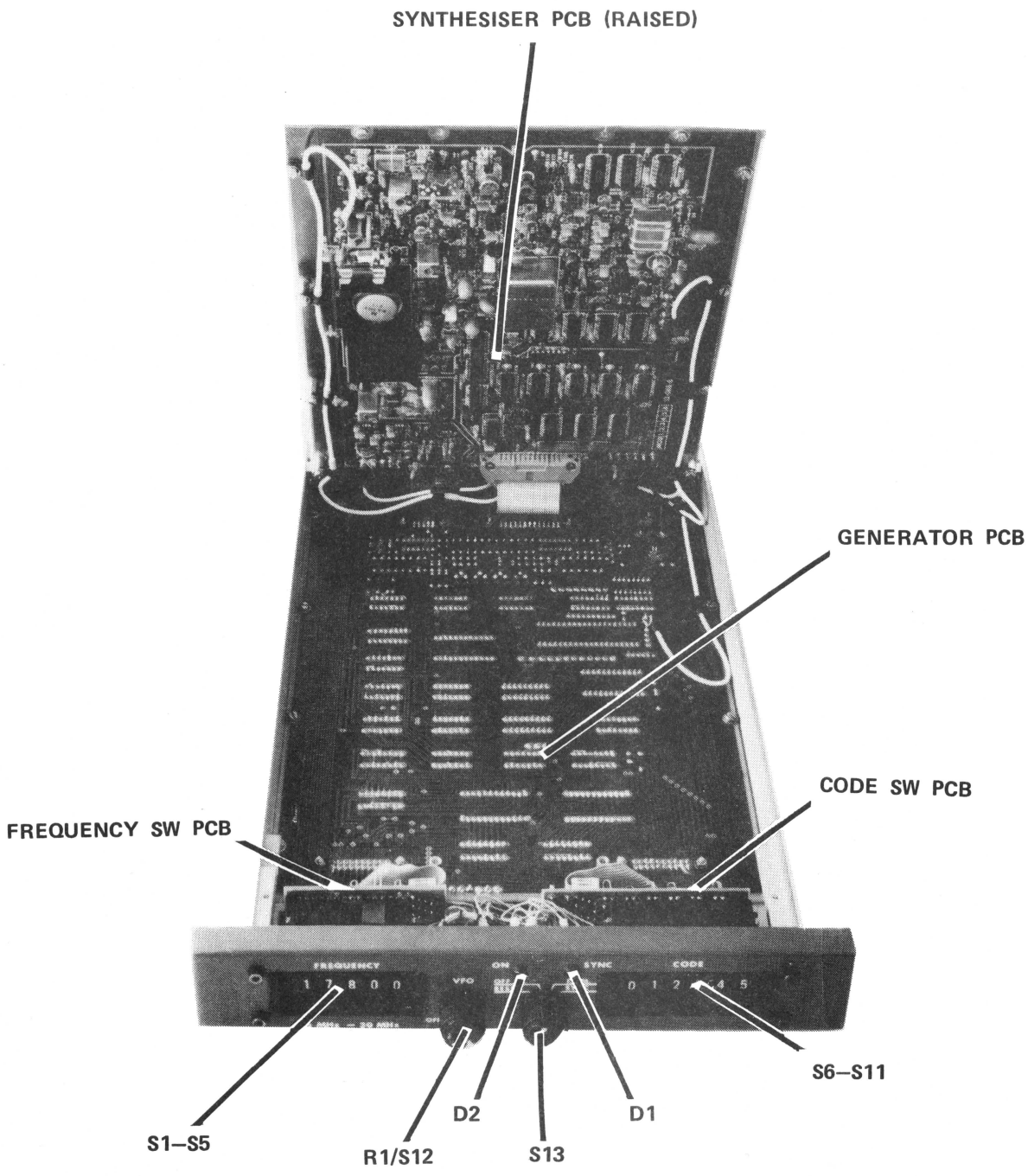
FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
		1300-0991		PCB	Frequency Switch	
				Diodes		
	D1	3600-0404			IN4153	
	D2	3600-0404			IN4153	
	D3	3600-0404			IN4153	
	D4	3600-0404			IN4153	
	D5	3600-0404			IN4153	
	D6	3600-0404			IN4153	
	D7	3600-0404			IN4153	
	D8	3600-0404			IN4153	
	D9	3600-0404			IN4153	
	D10	3600-0404			IN4153	
	D11	3600-0404			IN4153	
	D12	3600-0404			IN4153	
	D13	3600-0404			IN4153	
	D14	3600-0404			IN4153	
	D15	3600-0404			IN4153	
	D16	3600-0404			IN4153	
	D17	3600-0404			IN4153	
	D18	3600-0404			IN4153	
				Switches		
	S1	1600-5719			Thumbwheel (Modified)	
	S2	1600-5719			Thumbwheel (Modified)	
	S3	1600-5719			Thumbwheel (Modified)	
	S4	1600-5719			Thumbwheel (Modified)	
	S5	1600-5719			Thumbwheel (Modified)	

Decoupling PCB

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
		1300-1057		**PCB**	**Decoupling**	
				Capacitors		
	C1	2600-2534			Ceramic 10nF 10p.c. 100V	
	C2	2600-2534			Ceramic 10nF 10p.c. 100V	
	C3	2600-2534			Ceramic 10nF 10p.c. 100V	
	C4	2600-2534			Ceramic 10nF 10p.c. 100V	
	C5	2600-2534			Ceramic 10nF 10p.c. 100V	
	C6	2600-2534			Ceramic 10nF 10p.c. 100V	
	C7	2600-2534			Ceramic 10nF 10p.c. 100V	
	C8	2600-2534			Ceramic 10nF 10p.c. 100V	
	C9	2600-2534			Ceramic 10nF 10p.c. 100V	
	C10	2600-2534			Ceramic 10nF 10p.c. 100V	
	C11	2600-3125			Ceramic 100nF 20p.c. 50V	
	C12	2600-2534			Ceramic 10nF 10p.c. 100V	
	C13	2600-2534			Ceramic 10nF 10p.c. 100V	
	C14	2600-2534			Ceramic 10nF 10p.c. 100V	
	C15	2600-2534			Ceramic 10nF 10p.c. 100V	
	C16	2600-2534			Ceramic 10nF 10p.c. 100V	
	C17	2600-2534			Ceramic 10nF 10p.c. 100V	
	C18	2600-2534			Ceramic 10nF 10p.c. 100V	
	C19	2600-2534			Ceramic 10nF 10p.c. 100V	
	C20	2600-2534			Ceramic 10nF 10p.c. 100V	
	C21	2600-2534			Ceramic 10nF 10p.c. 100V	
	C22	2600-2534			Ceramic 10nF 10p.c. 100V	
	C23	2600-2534			Ceramic 10nF 10p.c. 100V	
	C24	2600-3125			Ceramic 100nF 20p.c. 50V	

Decoupling PCB (Cont.)

FIG. NO.	REF.	ORDER NO.	CODIFICATION	ITEM	DESCRIPTION	NO/UNIT
	C25	2600-2534			Ceramic 10nF 10p.c. 100V	
	C26	2600-2534			Ceramic 10nF 10p.c. 100V	
	C27	2600-2534			Ceramic 10nF 10p.c. 100V	
	C28	2600-2534			Ceramic 10nF 10p.c. 100V	
	C29	2600-2534			Ceramic 10nF 10p.c. 100V	
	C30	2600-2534			Ceramic 10nF 10p.c. 100V	
	C31	2600-2534			Ceramic 10nF 10p.c. 100V	
	C32	2600-2534			Ceramic 10nF 10p.c. 100V	
				Plugs		
	PL5	3300-1131			DB 25P-OL2, 25-way	
	PL19	3300-1132			DE 9P-OL2, 9-way	
	PL29	3300-1589			609-2622, 26-way	
	PL35	3300-1567			609-1022, 10-way	



FREQUENCY PROCESSOR UNIT

DECOUPLING CAPACITORS

10 n

PLUG 5, PINS 1-10, 12-24

PLUG 19, PINS 2, 3, 5 - 9

100 n

PLUG 5, PINS 11, 25

PL 19

PINS 1 AND 4 ARE NOT DECOUPLED

* A SOLDER CONNECTION IS USED TO TERMINATE THE CABLE ON THE PCB.

P/O DECOUPLING PCB

TO MAINFRAME LOOM SK20 (RECITER)

SK 19

PL 19

C26

C32

PL 33

SK 33

AUDIO (Rx)

GND

GND

AUDIO(SYNC)TO Tx

HOPPING FLAG

PTT

N/C

N/C

SEGMENT FLAG

N/C

SK 34

PL 34

CODE SWITCH PCB

6 7 8 9 10 11

D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25

R1 560

D1 SYNC LED

D1 RESET

R2 560

OFF

FAM

SYNC

*

D2 ON LED

S12a

S13

R4 10

S13

S12b

R3 560

D3

R1 10k

SK 32

PL 32

BANK A MSD

BANK B MSD

BANK C LSD

DATA BUS

SYNC LED

+5V

GND

RESET

FAM INT.

SYNC. INIT.

23 21 22 20 18 19

VFO

VFO

VFO WIPER

1kHz

VFO ENABLE

VFO INHIBIT

TO MAINFRAME LOOM SK6 (INTERFACE PCB)

SK 5

PL 5

C1

C25

PL 29

SK 29

CONNECTED IN PARALLEL TO SK30

P/O DECOUPLING PCB

TO BALANCED MODULATOR SK 22

TO RECITER SK 21

PL 22

PL 21

C2 100n

C1 100 n

11 12 35,4 MHz

14 13 37 MHz - 65,399 MHz

CONNECTED IN PARALLEL TO SK29

SK 31

SK 30

PL 31

PL 30

1kHz

10kHz

100 kHz

1 MHz

10 MHz

FREQ. SEL (LOCAL/REMOTE)

0V COMM

9V Tx

9V AM Rx

+5V (FREQ. SW. COMM)

12 V

9V Rx

N/C

SYNTHESISER PCB

14 1kHz 1

16 VFO 2

12 VFO INHIBIT 3

17 VFO WIPER 4

13 VFO ENABLE 5

15 VFO 6

2 1 MHz 8 7

FREQUENCY SWITCH PCB

COM S1 D1 D2 D3 D4 1 2 4 8

COM S2 D5 D6 D7 D8 1 2 4 8

COM S3 D9 D10 D11 D12 1 2 4 8

COM S4 D13 D14 D15 D16 1 2 4 8

COM S5 D17 D18 1 2 4 8

SK 35

PL 35

1kHz

10kHz

100 kHz

1 MHz

10 MHz

+5V

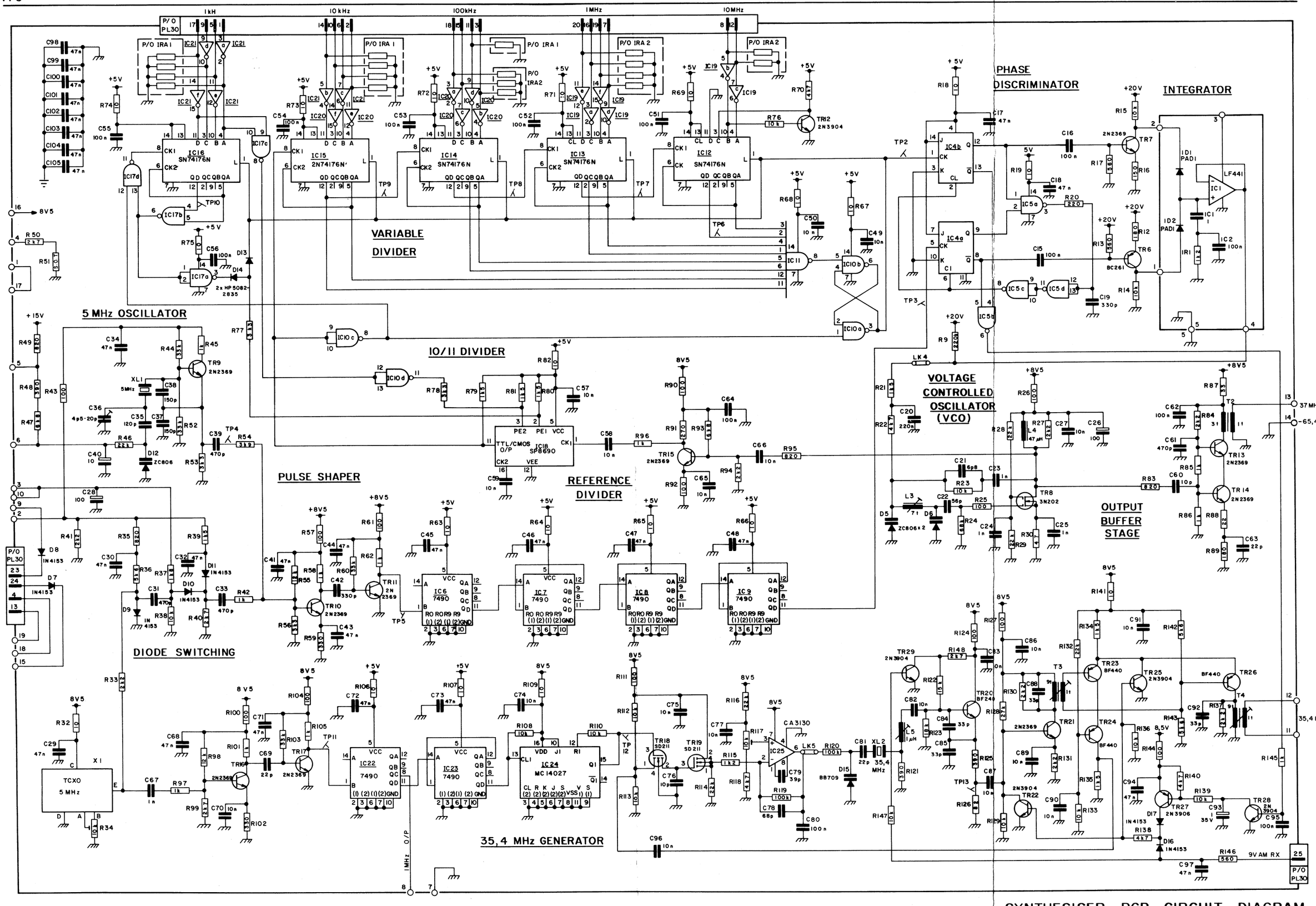
GENERATOR PCB

3 4 5 6 7 8

FREQUENCY PROCESSOR UNIT
CIRCUIT DIAGRAM

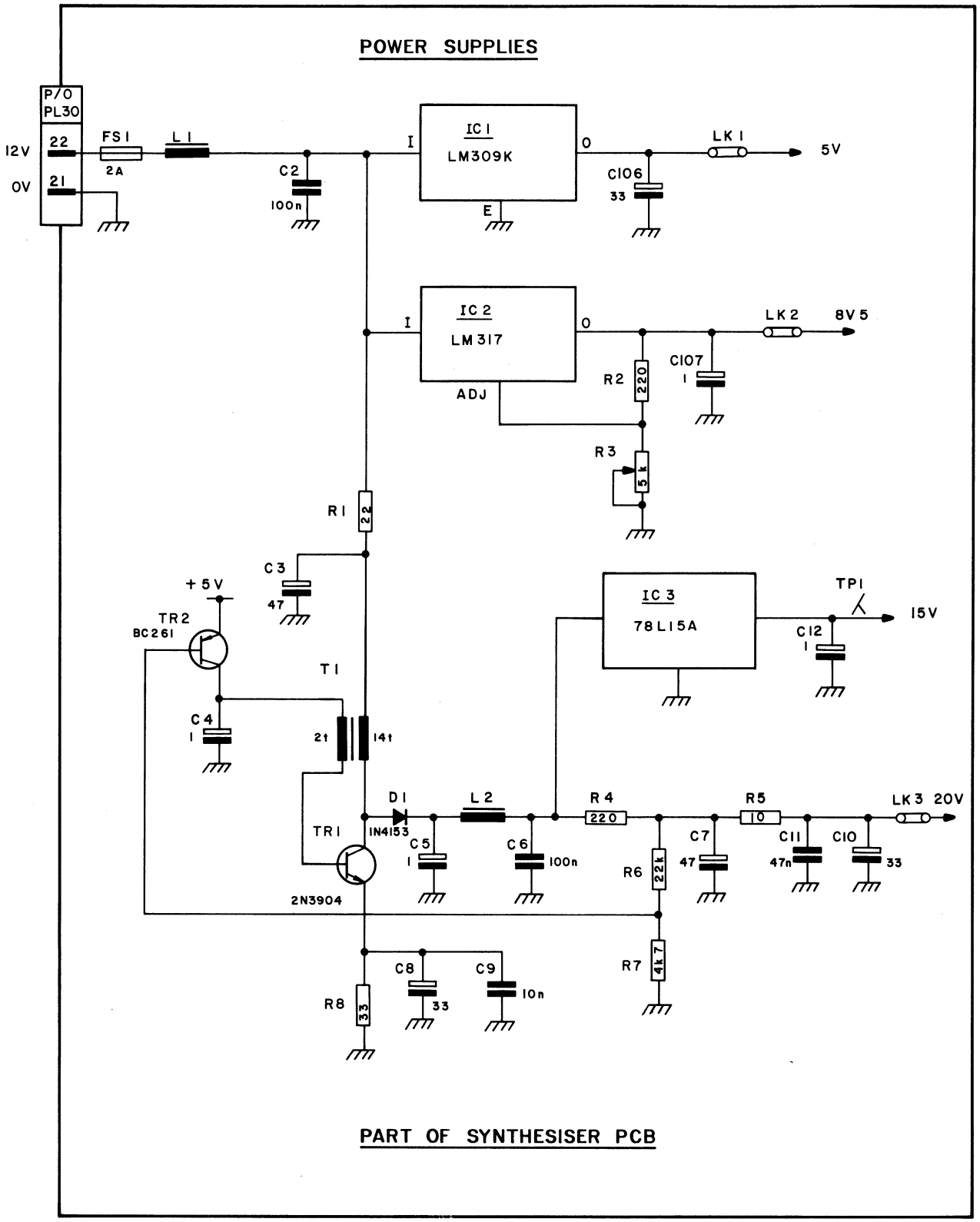
GE003.1085

FIG. 2

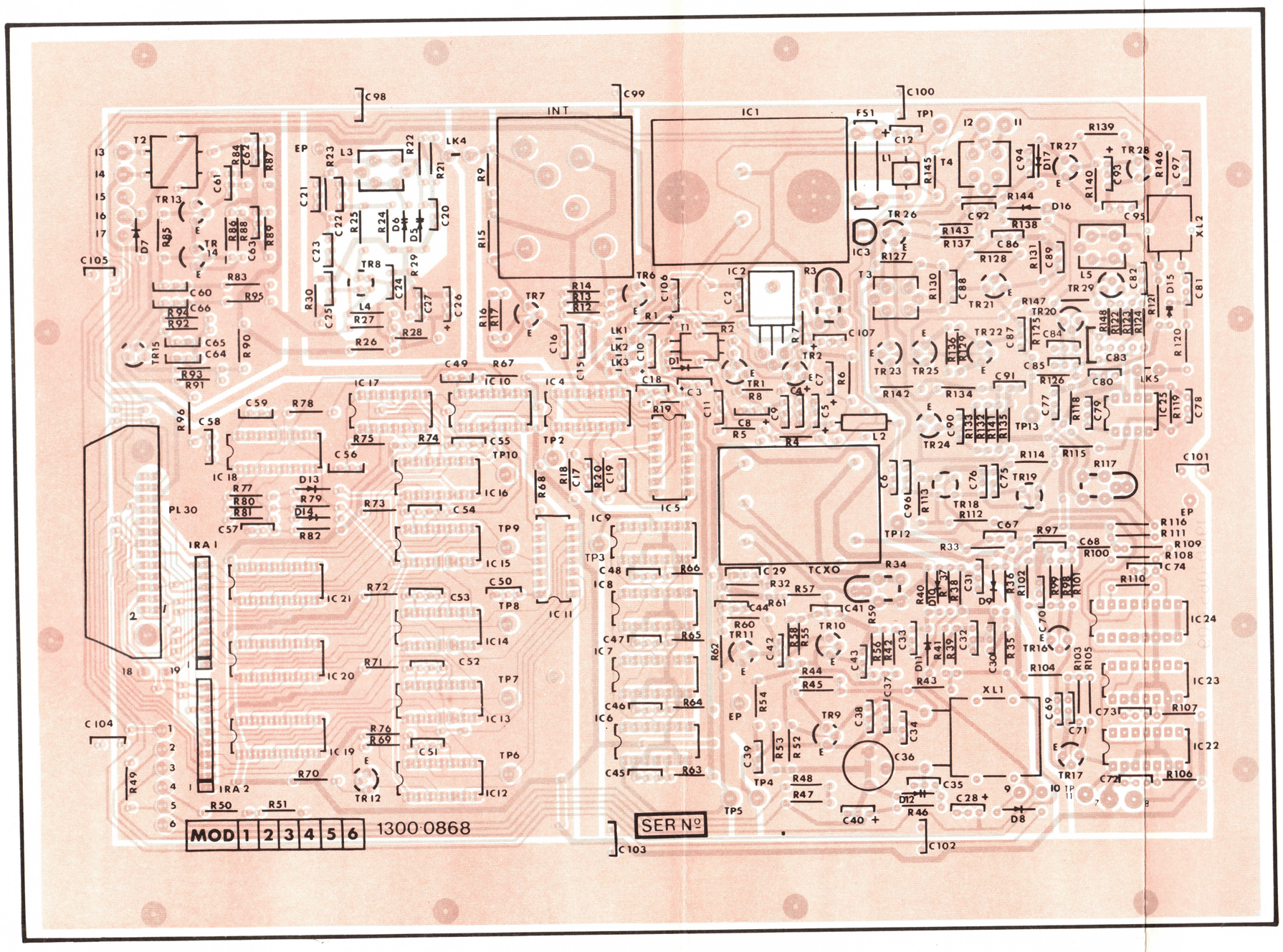


GE003.1085

FIG. 3 SHT. 1



SYNTHESISER PCB
CIRCUIT DIAGRAM



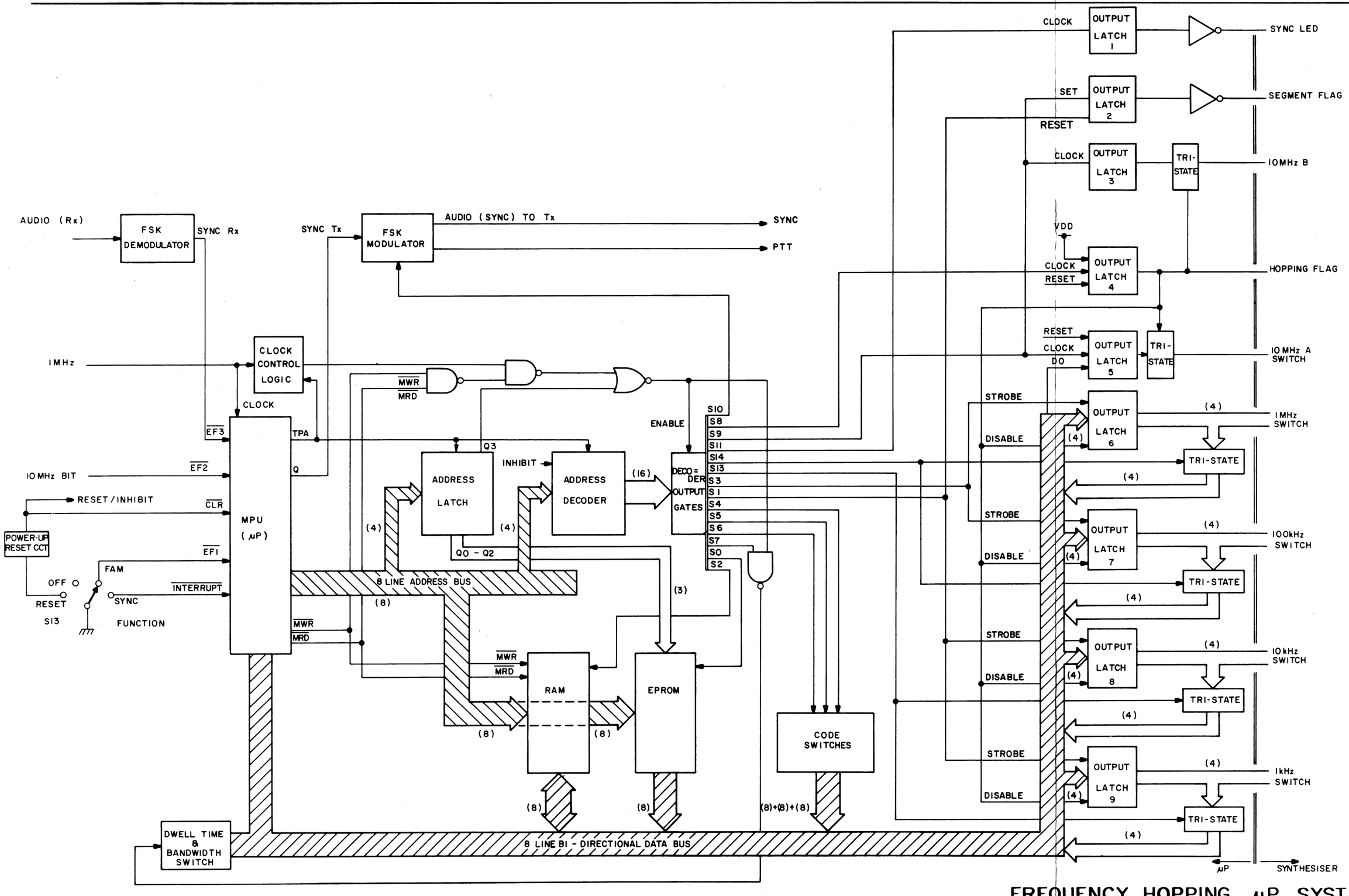
PCB Component Side :

PCB Track Side :

SYNTHESISER PCB
COMPONENT LOCATION

GE003.1085

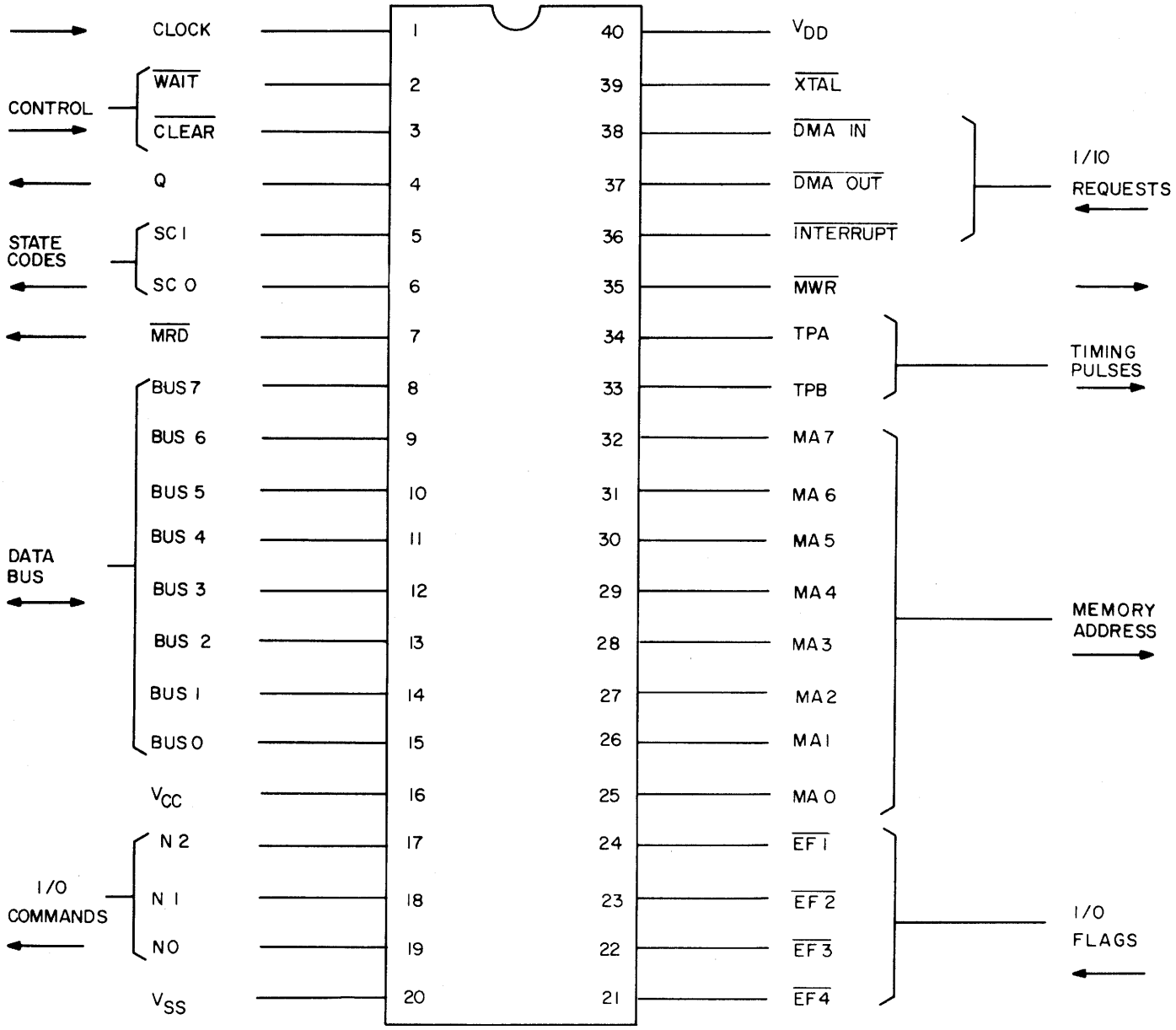
FIG. 4



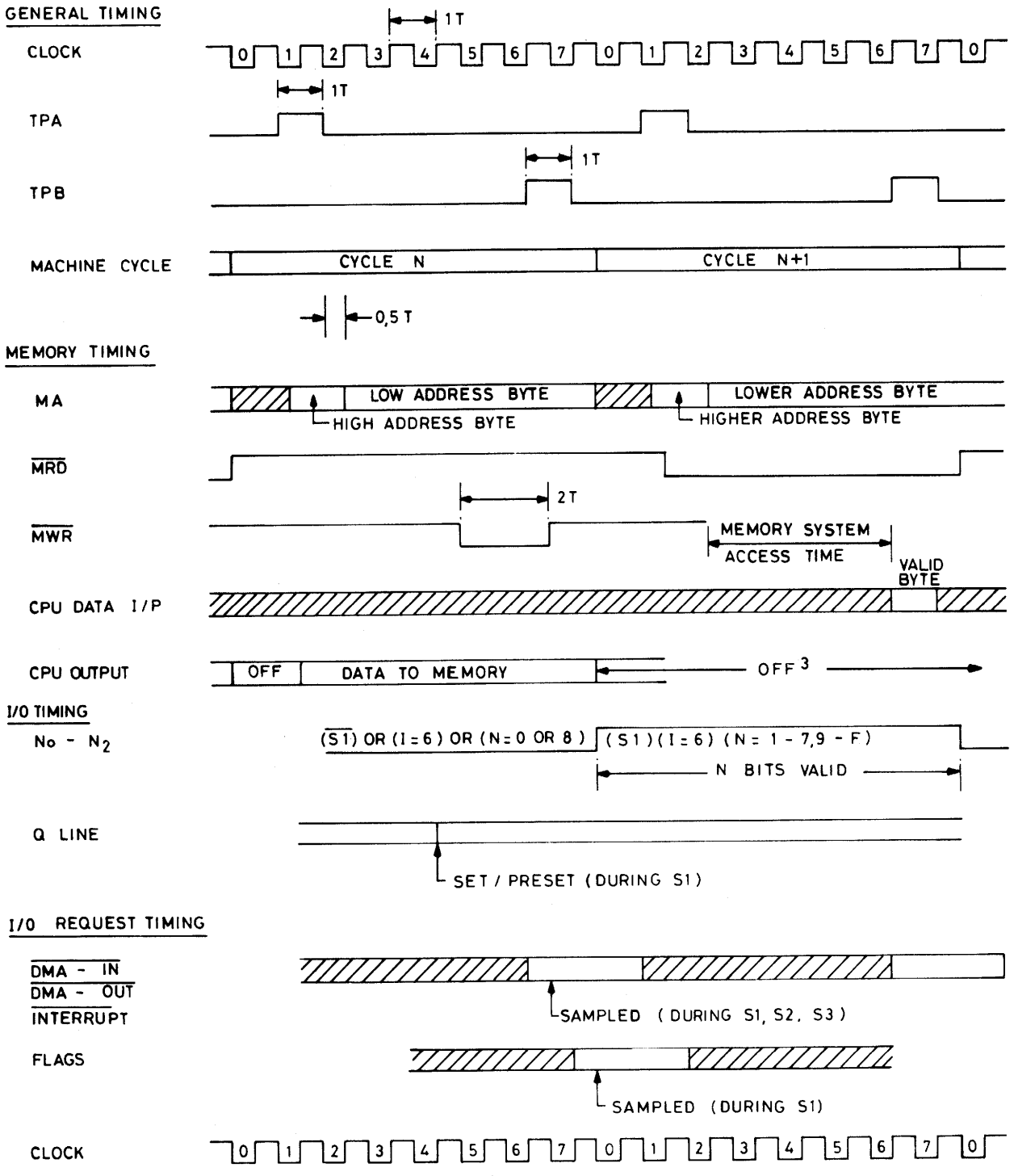
FREQUENCY HOPPING μP SYSTEM
FUNCTIONAL DIAGRAM

GE0031085

FIG. 5

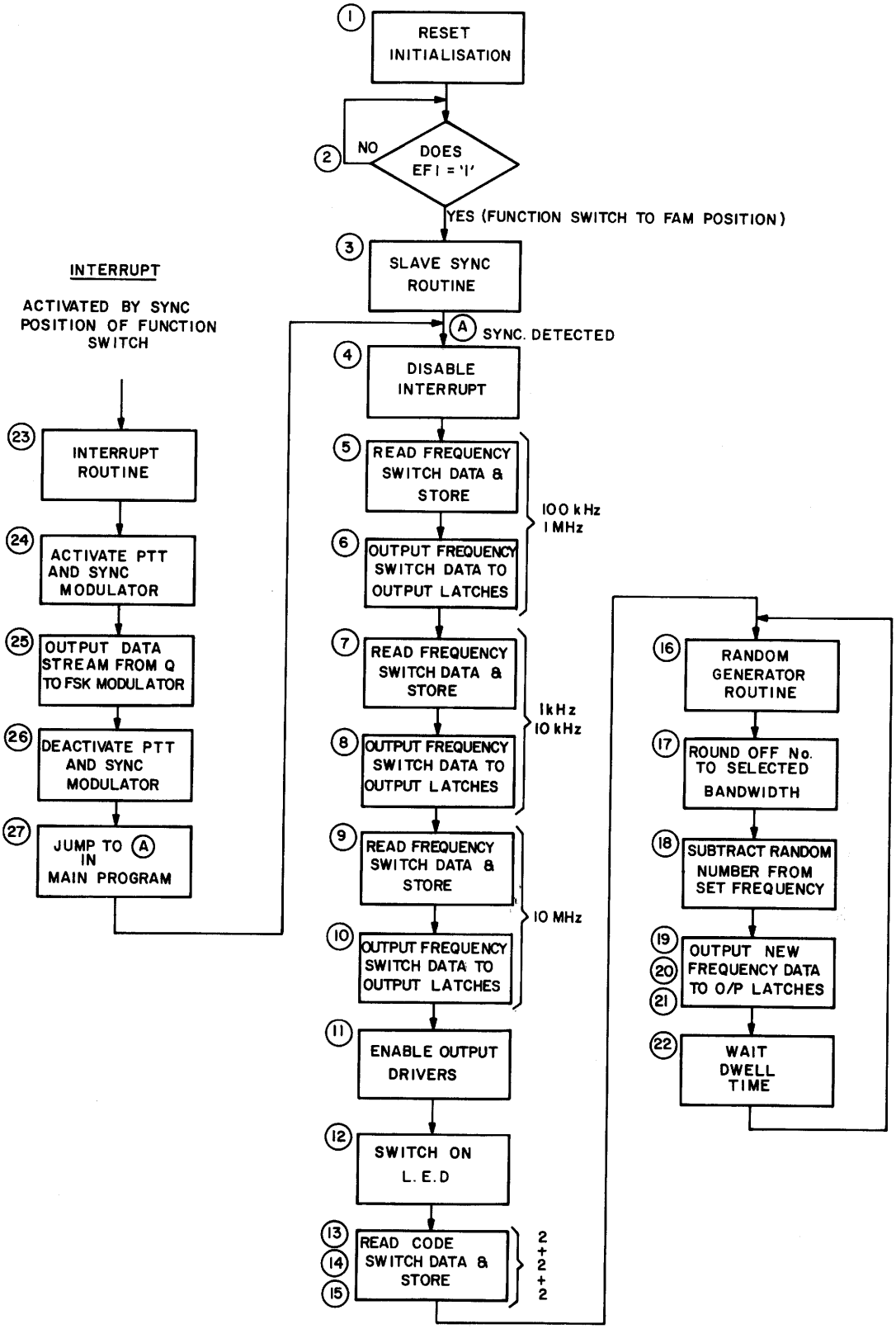


CDP1802 – TERMINAL ASSIGNMENT



NOTES
1. USER GENERATED SIGNALS
2. SHADING INDICATES 'DONT CARE' OR INTERNAL DELAY
3. OFF INDICATES HIGH-IMPEDANCE STATE

CDP1802 – TIMING DIAGRAM



FREQUENCY HOPPING
FLOW DIAGRAM

IC No.	1, 11, 12	2, 24	3	17	6	7	19, 26
TYPE	4011	4049	4081	4081	40097	40097	40097
VDD PIN	14	1	14	14	16	16	16
VSS PIN	7	8	5,6,7	7	4,8,10	8,12,14	8

NOTE: 1. LK BETWEEN PINS 10 & 9 FOR P2111 AND, BETWEEN PINS 10 & 11 FOR IM6561

2. ALL DIODES ARE IN4153

ADDRESS DECODER

ADDRESS LATCH

μP

IC21 CDP1802

IC23 4042

IC10 4514

IC22 EPROM 2716

RAM 2 x IM6561 (OR P2111)

IC15, IC16

FSK MODULATOR REFER TO FIG. 11

FSK DEMODULATOR REFER TO FIG. 11

IC27 REG LM309K

IRA1, IRA2 R1-R5, R7-R15

ADDRESS BUS TEST POINTS

DATA BUS TEST POINTS

SB TEST SWITCH

SA BANDWIDTH/DWELL TIME SWITCH

PL35 CONNECTED IN PARALLEL TO PINS 1-20 OF PL31

P/O PL34: AUDIO (SYNC) TO Tx; PTT; AUDIO (Rx); RESET; SYNC INITIATE; FAM INITIATE; 10 MHz BIT; SYNC DETECT; P/B; 1 MHz

P/O PL31: +12V; +5V; SYNC LED; SEGMENT FLAG; 10 MHz B; HOPPING FLAG; FREQ. SW COMM.; FREQ. SEL (LOCAL/REM); 10 MHz A; 100kHz A B C D; 1MHz A B C D; 1kHz A B C D; 10kHz A B C D; 9V Tx; 9V Rx; 9V AM Rx

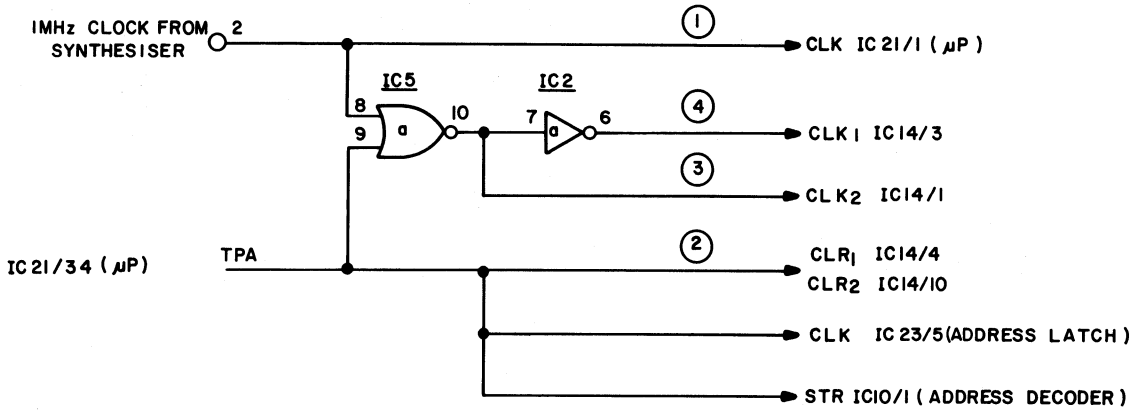
P/O PL32: TO CODE SWITCHES ON FRONT PANEL; ENABLE CODE SWITCHES

VFO; VFO WIPER; VFO; 1 kHz; VFO INHIBIT; VFO ENABLE — TO SYNTH. PCB

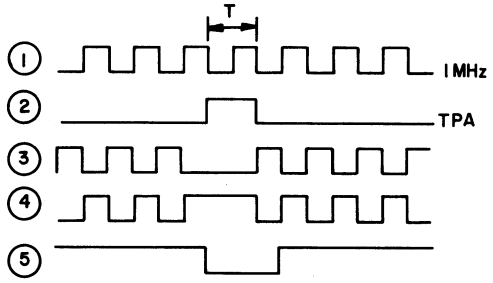
GE003J085

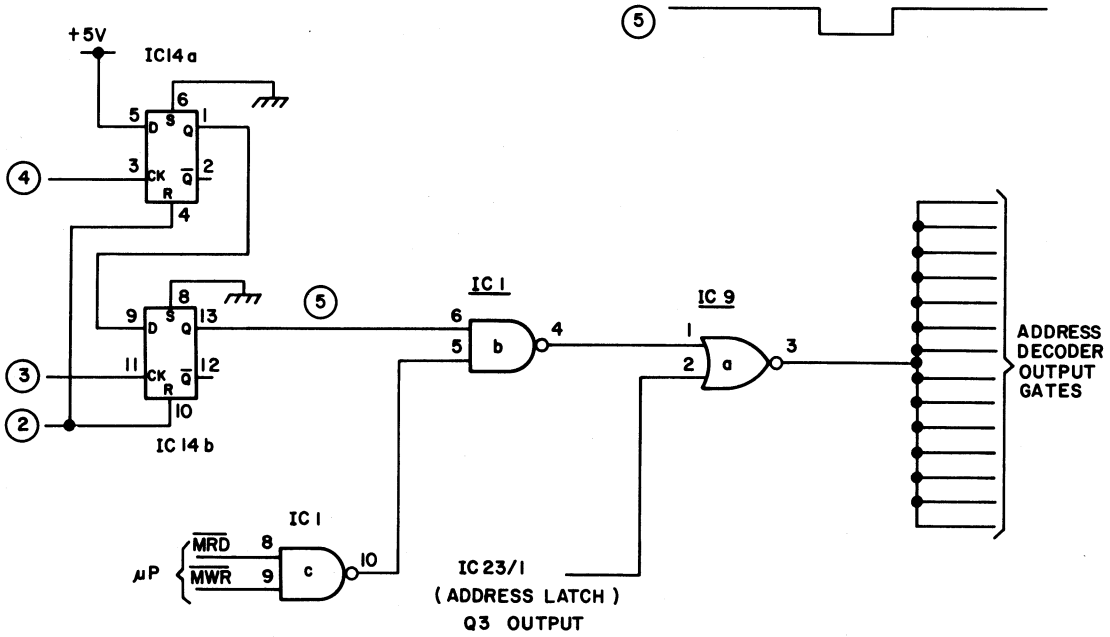
GENERATOR PCB CIRCUIT DIAGRAM

FIG. 9

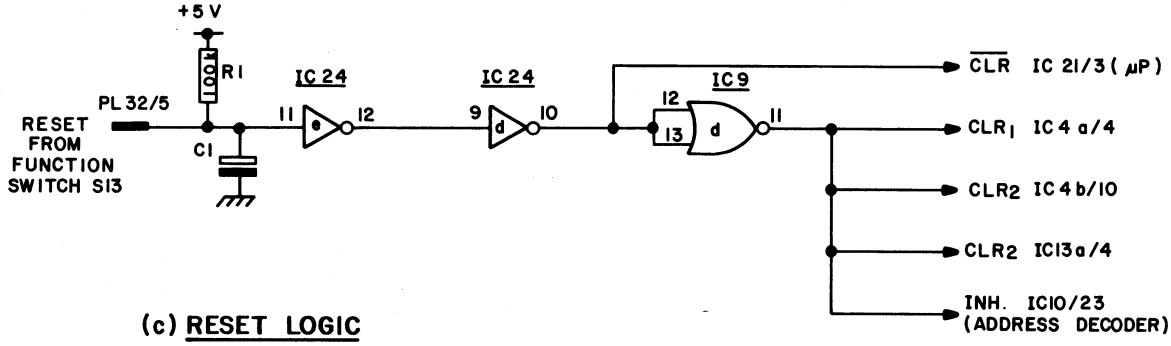


(a) CLOCK GENERATION





(b) ADDRESS DECODER OUTPUT GATING

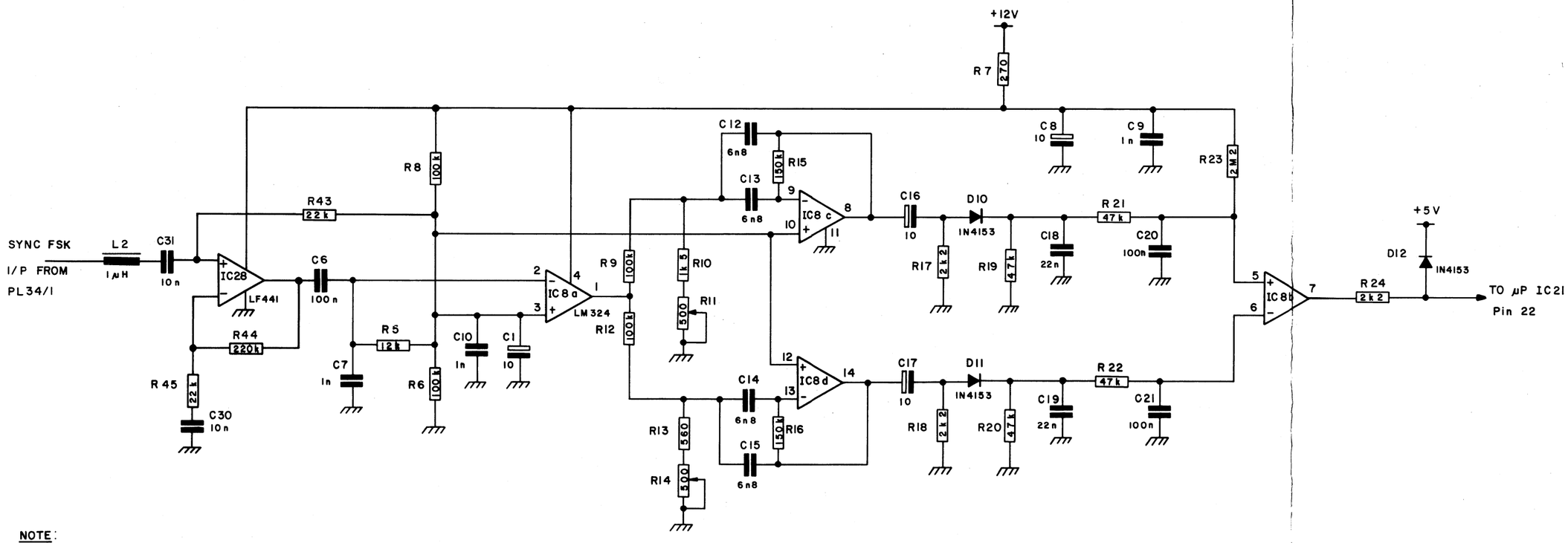


(c) RESET LOGIC

CLOCK, ADDRESS DECODER OUTPUT GATING AND RESET LOGIC

GE003.1085

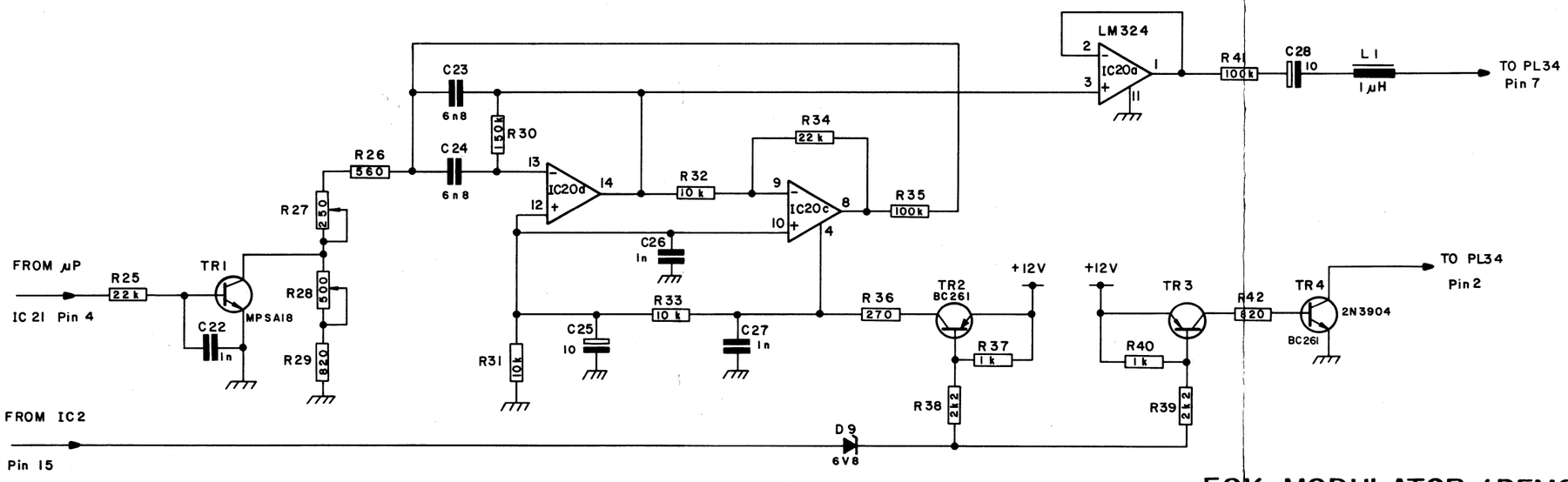
FIG.10



NOTE:

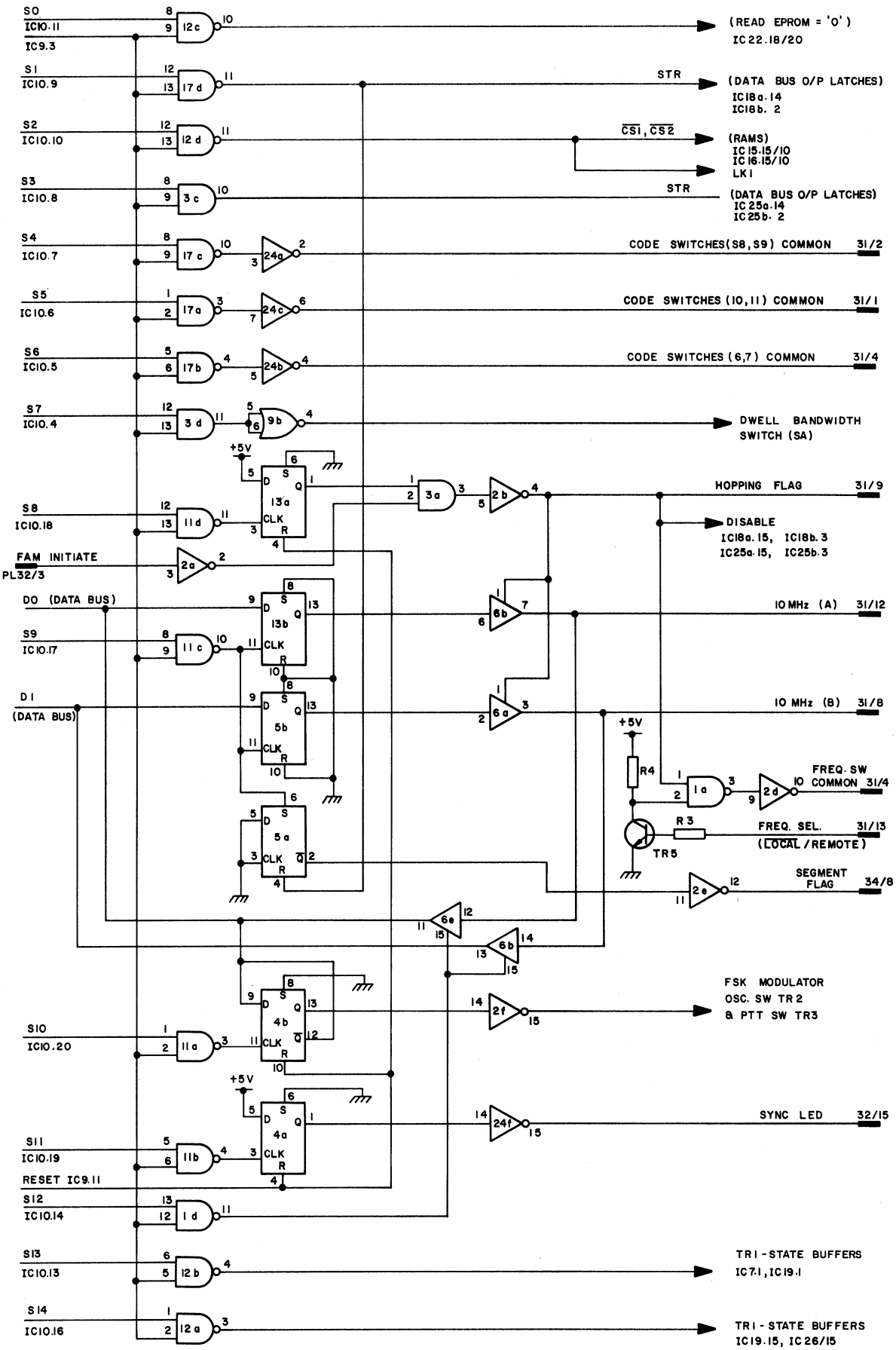
IC28 AND ASSOCIATED COMPONENTS ARE NOT INCORPORATED ON THE GENERATOR PCB IN EARLY MODELS.

SYNC. FSK DEMODULATOR

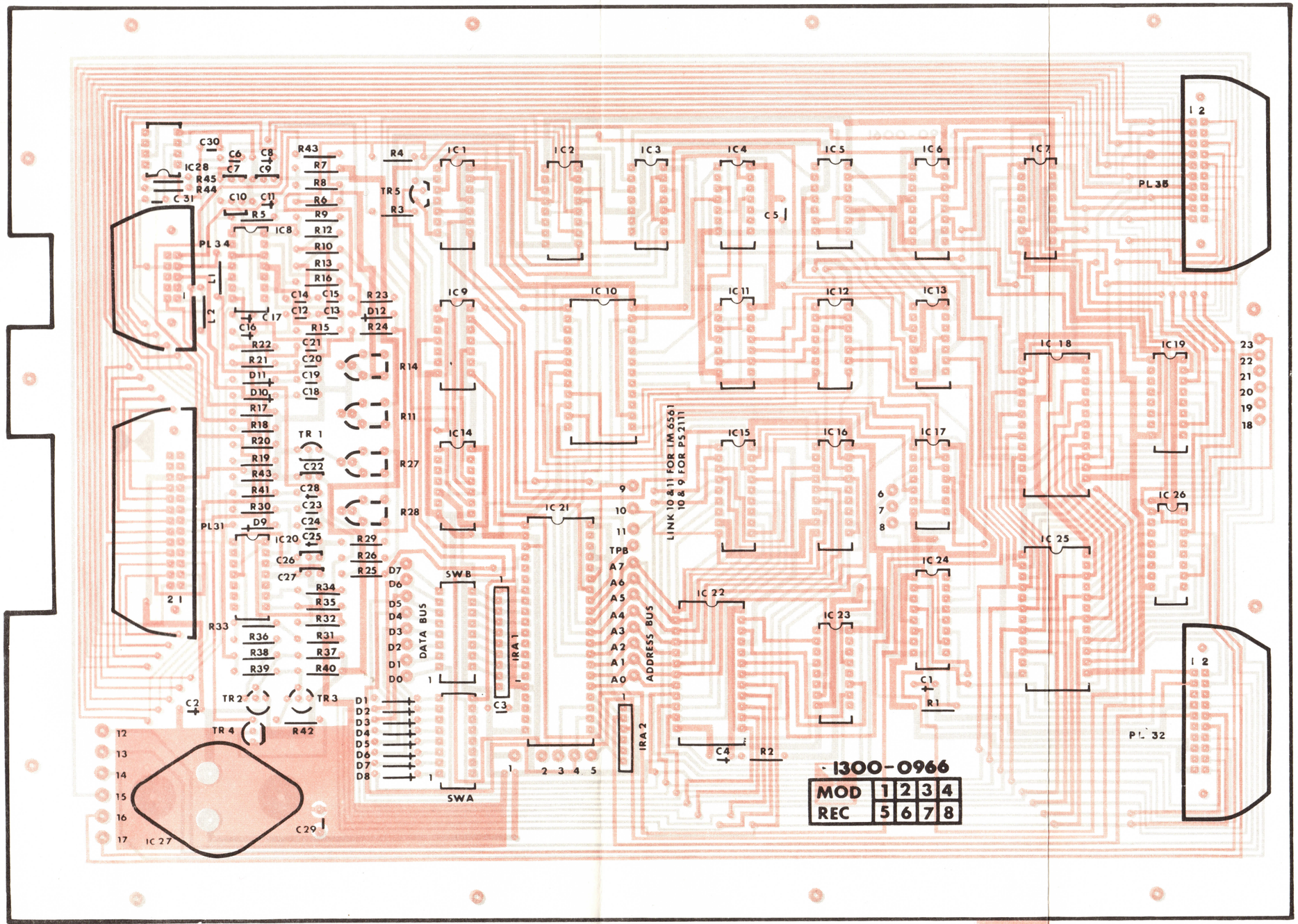


SYNC. FSK MODULATOR

FSK MODULATOR / DEMODULATOR
CIRCUIT DIAGRAMS



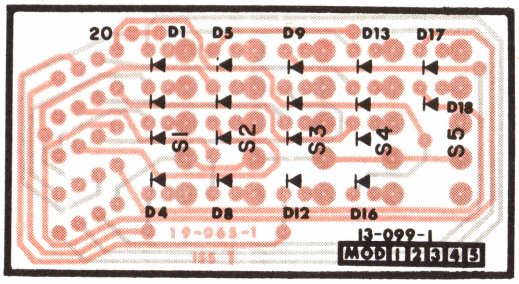
ADDRESS DECODER OUTPUTS



PCB Component Side:

PCB Track Side:

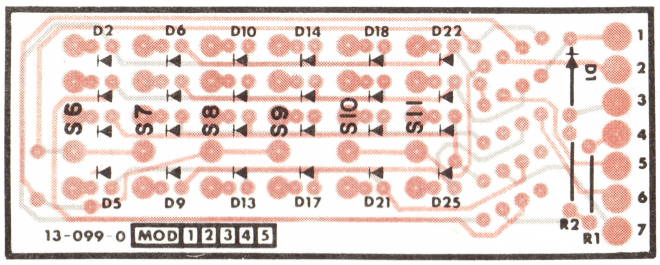
GENERATOR PCB COMPONENT LOCATION



PCB Component Side:

PCB Track Side:

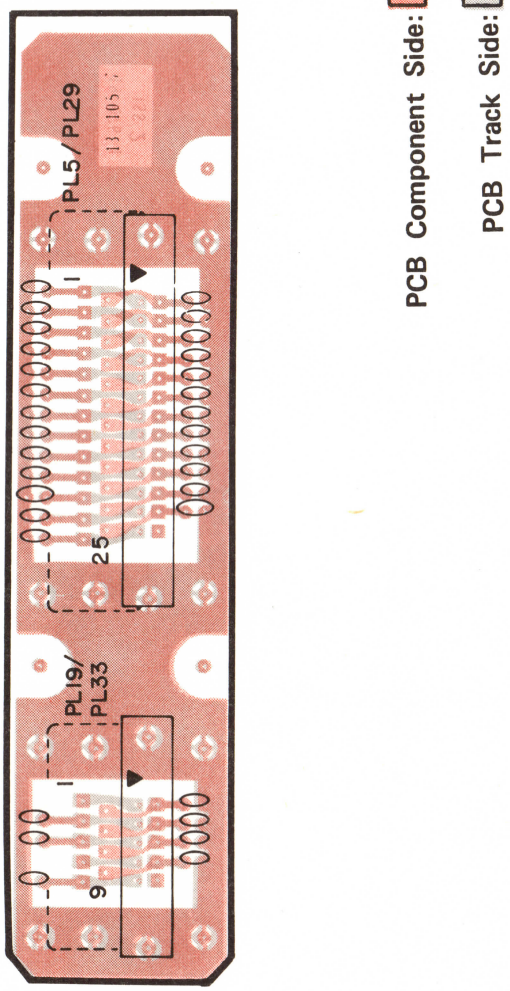
FREQUENCY SWITCH PCB
COMPONENT LOCATION



PCB Component Side:

PCB Track Side:

CODE SWITCH
COMPONENT LOCATION



DECOUPLING PCB
COMPONENT LOCATION