ITT Mackay

# Operation and Maintenance Manual

## Antenna Coupler MSR 4030

## Control Unit AT6211

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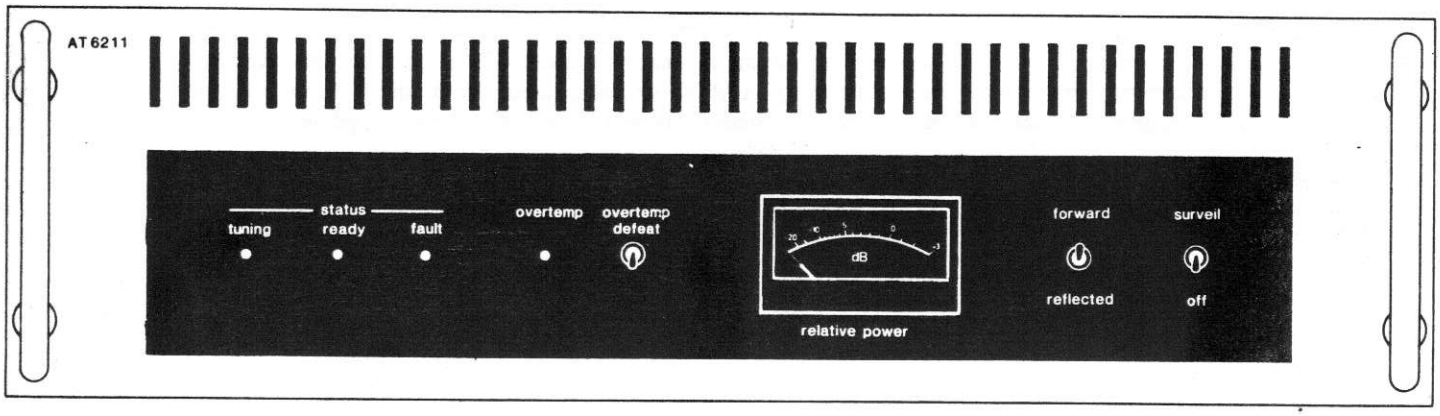
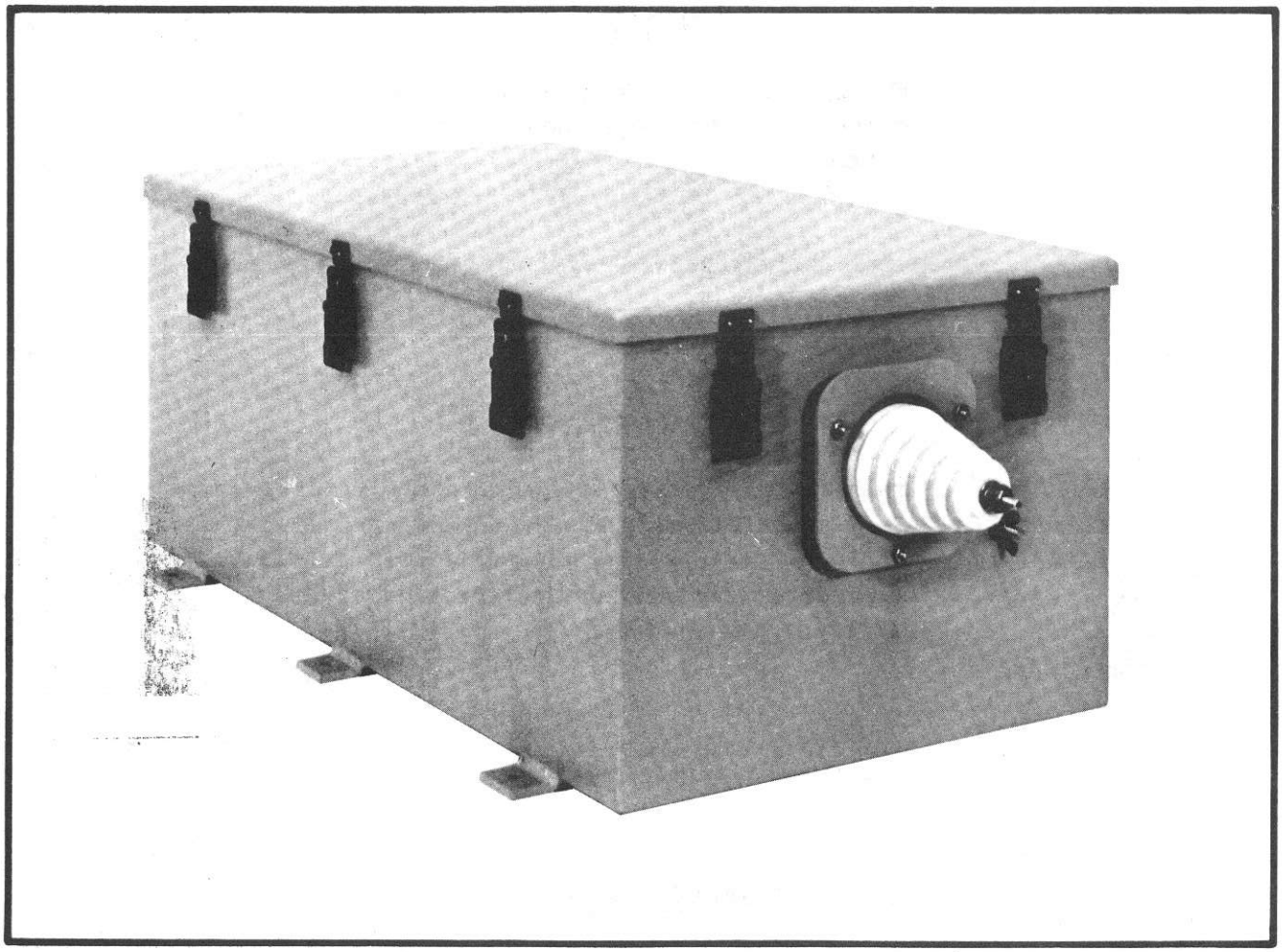



# Control Unit AT6211

ITT Mackay



# MSR - 4030

## 1kw Automatic Antenna Coupler

Issue 4

Publication No. 600236-823-001

## NOTICE

ITT MACKAY reserves the right to make changes to the equipment without notice.

## PROPRIETARY STATEMENT



## SAFETY NOTICE

This equipment has dangerous RF voltages which can cause BURNS and INJURY. Do not touch the antenna connector, long wire antenna or metal portion of whip antennas when transmitting. When practicable, maintenance should be performed with the equipment de-energized. If power-on maintenance is required, use caution. Do not touch high voltage or RF components.

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# SECTION 1
# INTRODUCTION

## 1.1 SCOPE

This instruction manual contains information necessary for the installation, operation, and maintenance of the Automatic Antenna Coupler.

## 1.2 DESCRIPTION

### 1.2.1 General

The MSR 4030 is a 1 kW antenna coupler for use when connecting whip or wire antennas to a transmitter designed to match a 50 ohm load from 1.6-30 MHz. Although particularly suitable for use with Mackay transmitters incorporating the MSR 1020 1 kW Linear Power Amplifier, an optional model MSR 6408 control unit is available to facilitate interface of the antenna coupler with other transmitters.

The MSR 4030 is designed for easy installation and features an automatically switched series capacitor to provide the capability of matching a wide range of antennas without use of optional external networks or internal field adjustments. Additionally, all the high reliability electronic control circuits are located in a compartment adjacent to the tuning circuits. This "single package" concept eliminates the need for a separate electronics unit and simplifies installation and troubleshooting. The MSR 4030 uses plug-in modular construction and can be quickly disassembled with only basic tools. Built in Test Equipment (BITE) facilites are provided for testing and maintenance of some assemblies without special test equipment.

The Antenna Coupler is housed inside a fully gasketed and water-tight case. In this way, it is designed for outside mounting near the antenna.

A memory module is provided to expand the capabilities of the basic coupler tuning functions. With this module, the tuning information can be stored automatically and retained in memory for up to 96 communication channels. Upon command, the memory will rapidly guide the MSR 4030 tuning elements to their preset positions without an RF carrier or any manual tuning controls. This feature provides extra convenience and a very rapid method of tuning many frequencies without the necessity of radiating RF power.

The Antenna Bypass Kit is available as an option that can provide the user with a convenient method of receiving out of band signals. It is designed to bypass the coupler network during receive so that the tuned circuits will not degrade out of band received signals.

Although the MSR 4030 is designed to withstand severe shock and vibration conditions, an optional shock mount kit is available for additional protection. With this kit, the coupler can withstand the severe shock and vibration of the environment as defined by MIL-STD-810C.

## 1.3 SPECIFICATIONS

1.3.1 Frequency Range: 1.6 - 30 MHz

1.3.2 Antenna Matching Capability:

| | |
|---|---|
| 24' Whip (7.9m) | 2.0 - 30 MHz |
| 35' Whip (10.7m) | 1.6 - 30 MHz |
| Longwire 35' to 150' (11-50m) | 1.6 - 30 MHz |

1.3.3 Power Handling Capability:

1 kW PEP: 24' whip to 150' Long-Wire Antenna

1 kW Average: 35' whip to 150' Long-Wire Antenna

1.3.4 Input Impedance:

50 ohm nominal

1.3.5 Tuning Accuracy:

1.5:1 VSWR Maximum

1.3.6 Remote Capability:

May be located up to 250 feet (80m) from the Power Amplifier or antenna coupler control unit.

1.3.7 RF Tune Power Requirement:

100 Watts Nominal
40 Watts Minimum
250 Watts Maximum

1.3.8 Tuning Time:

Typically 5 - 15 seconds

1.3.9 Channel Capacity:

96 Channels (May be limited by associated Transmitter)

1.3.10 Power Supply Requirements:

115/230 VAC ±15%, Single Phase, 48-63 Hz

1.3.11 Power Consumption:

60 watts, coupler tuned. 130 watts, tuning (average)

1.3.12 Operating Temperature:

−30 °C to +55 °C (to +65 °C with reduced performance)

1.3.13 Vibration/Shock:

MIL-STD-810C; (when fitted with optional Isolators) Vibration-Method 514-2, Fig. 6, curve V, 20-200 Hz Shock - Method 516.2, Procedure 2, Fig. 2

1.3.14 Enclosure:

Splash proof for exposed installations per MIL-STD-108E, Table II

1.3.15 Humidity:

95% RH, 50 °C

1.3.16 Enclosure only (Less mounting feet, latches, connectors, antenna post — Length -28" (71 cm) Width - 15" (38 cm) Height -11" (28 cm)

1.3.17 Weight:

72 lbs. (33 kg)

## 1.4 EQUIPMENT SUPPLIED

1.4.1 COUPLER, MSR 4030 - Part Number 698002-000-XXX (Specify color - Grey or Olive Drab)

1.4.2 MANUAL, OPERATION/MAINTENANCE - Part Number 600236-823-001

1.4.3 KIT, ACCESSORY Part Number 698002-017-001 consisting of the following:

1.4.3.1 CONNECTOR, PLUG - Part Number 600375-606-005 (MS3106A-28-21S)

1.4.3.2 SEALANT, COAXIAL - Part Number 600033-115-001 (Three Rolls)

1.4.3.3 CONNECTOR, RF, UG-21D - Part Number 600028-606-001

1.4.3.4 CLAMP, CABLE - Part Number 600376-606-004 (AMPHENOL - AN3057-12)

1.4.3.5 FUSE,3A

1.4.3.6 FUSE,6A

## 1.5 OPTIONAL EQUIPMENT - NOT SUPPLIED

1.5.1 KIT, SHOCK MOUNTING - Part Number 600095-700-001

1.5.2 CONTROL UNIT, MSR-6408 - Part Number 699016-000-XXX (Specify Color - Grey, Olive Drab, or Light Grey)

1.5.3 KIT, ANTENNA BYPASS - Part Number 600067-700-001

1.5.4 KIT, DEPOT SPARES - Part Number 600065-700-001

1.5.5 KIT, SPARE P.C. BOARDS - Part Number 600066-700-001

1.5.6 KIT, LONGWIRE, 150 FT - Part Number 600233-817-007

1.5.7 WHIP, 23 FT, SELF-SUPPORTING - Part Number 600019-398-002

1.5.8 WHIP, 32 FT - Part Number 600018-398-001

1.5.9 BASE, MOUNT, 32 WHIP - Part Number 600018-398-007 (Use with 1.5.8)

1.5.10 CABLE, RF, RG-213U - Part Number 600017-102-001 (Specify length in feet)

1.5.11 CABLE, CONTROL - Part Number 600069-102-010 (Specify length in feet)

1.5.12 KIT, COMPREHENSIVE SPARES,-Part Number 600123-700-001

1.5.13 CABLE, CONTROL, PREASSEMBLED - Part Number 600530-540-XXX (Complete Assembly with connectors):

| | |
|---|---|
| 3 FT ±3 IN. | = 600530-540-001 |
| 6 FT ±3 IN. | = 600530-540-002 |
| 10 FT ±3 IN. | = 600530-540-003 |
| 20 FT ±6 IN. | = 600530-540-004 |
| 30 FT ±6 IN. | = 600530-540-005 |
| 40 FT ±1 FT | = 600530-540-006 |
| 50 FT ±1 FT | = 600530-540-007 |
| 75 FT ±1 FT | = 600530-540-008 |
| 100 FT ±2 FT | = 600530-540-009 |
| 150 FT ±2 FT | = 600530-540-010 |
| 200 FT ±2 FT | = 600530-540-011 |
| 250 FT ±2 FT | = 600530-540-012 |

1.5.14 KIT, EXTENDER, PC BOARD - Part Number 600068-700-001

consisting of:

| | |
|---|---|
| 601316-536-001 | Control Board |
| 601317-536-001 | Interface Board |
| 601318-536-001 | Memory Board |

**NOTE**

*The MSR-4030 Antenna Coupler has been specifically designed for use with the MSR-1020 1 kW Amplifier. However, the optional MSR-6408 control unit will allow the user to interface the MSR-4030 with other types of transmitters.*

# SECTION 2
# INSTALLATION

## 2.1 GENERAL

This section describes the installation procedures for the antenna coupler. Included within this section are procedures for unpacking, inspection and, if necessary, reshipping.

## 2.2 UNPACKING AND INSPECTION

Unpack the MSR-4030 Antenna Coupler and make certain that all equipment outlined in Section 1.4 is present. Retain the carton and packing materials until the contents have been inspected. If there is evidence of damage, do not attempt to use the equipment. Contact the shipper and file a shipment damage claim.

## 2.3 RESHIPPING

If return of the Antenna Coupler should become necessary, a Returned Material (RM) number must first be obtained. This number must be clearly marked on the outside of the shipping carton.

## 2.4 INSTALLATION

Thoroughly plan the transmitter/coupler/antenna locations and carefully follow the installation considerations given below. Satisfactory system performance depends upon the care and attention taken prior to and during installation.

The protective connector cover installed for shipping should remain in place until the antenna coupler is installed.

### 2.4.1 Installation Consideration

#### 2.4.1.1 Antenna Site Location

For optimum characteristics and safety, the antenna should be mounted high enough to clear any surrounding obstructions. The antenna should also be located as far as possible from nearby objects such as power lines, buildings, etc. Figure 2.1 and 2.2 show typical whip and longwire installations.

#### 2.4.1.2 Adequate Ground

Provide the best possible RF ground for the transmitter and the coupler. Use a flat copper strap, 25 mm wide or number 6 gauge or larger wire and connect it to the ground terminal at the rear of the transmitter and on the coupler case. The coupler ground must be attached to the antenna ground. Leads to the ground system should be as short as possible.

**NOTE**

*Good grounding cannot be over emphasized. The coupler and antenna must be well grounded to prevent RF system problems.*

#### 2.4.1.3 Separation

Provide maximum separation between the coupler output (antenna) and the transmitter. The coupler may be mounted up to 250 feet (80 meters) from the transmitter.

#### 2.4.1.4 Antenna Lead-In

The lead-in from the antenna coupler to the antenna must be insulated for at least 15 kV potential. The lead-in should not run parallel to metal objects which are bonded to the system ground. The tuner should be as close to the antenna as possible and never further away than 3 feet (1 meter), as this will decrease antenna efficiency.

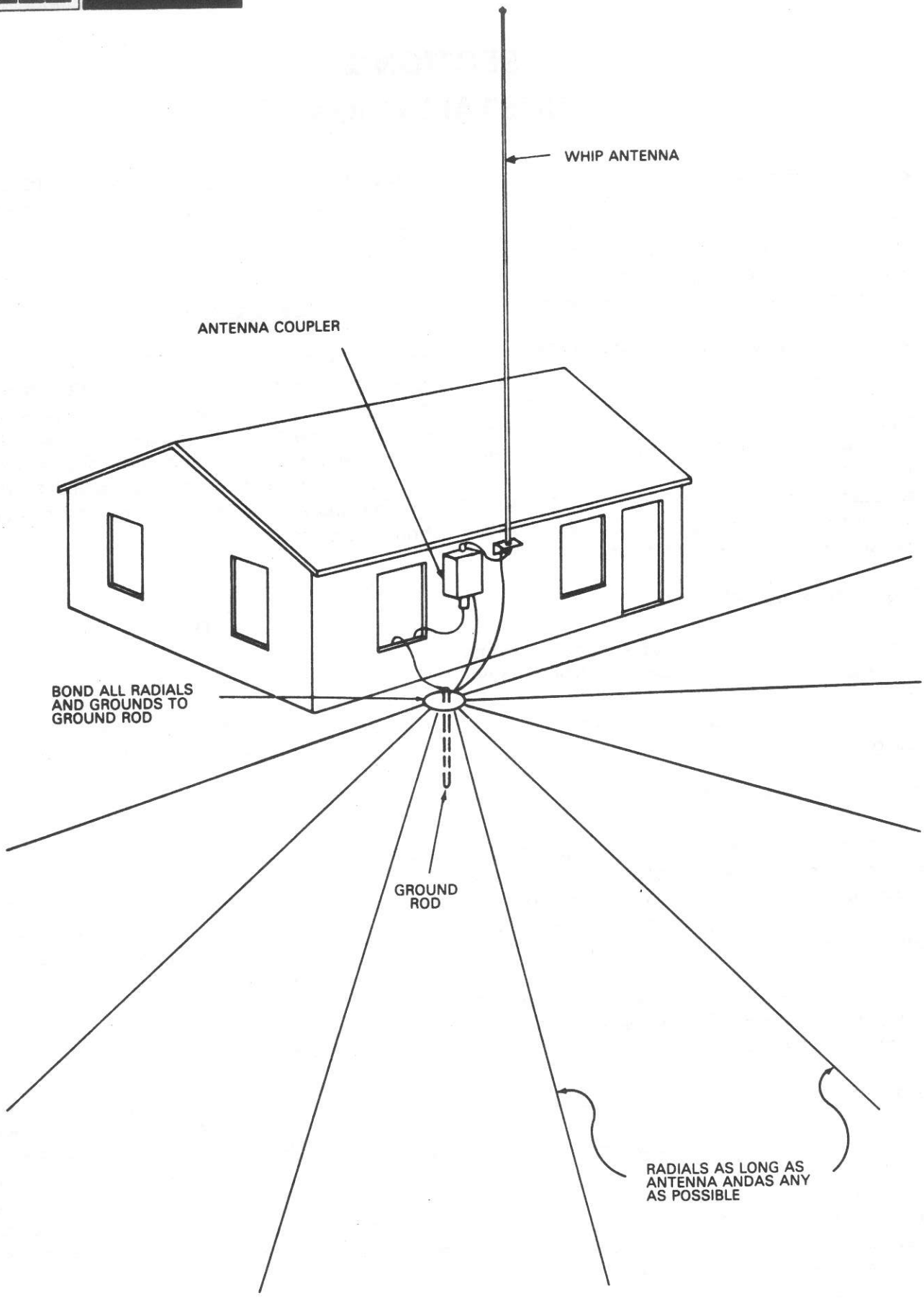



Figure 2.1 Typical Whip Antenna Installation

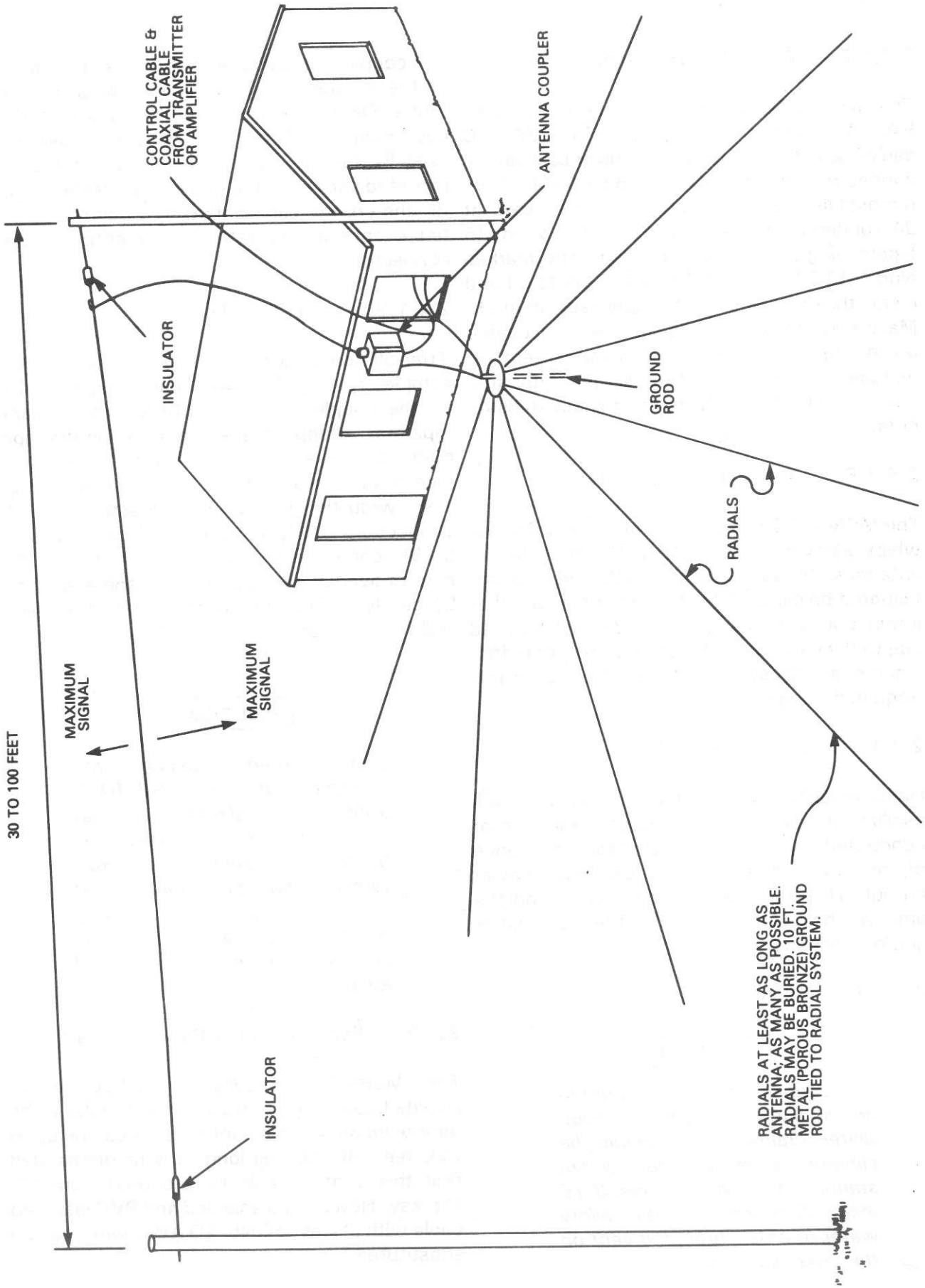



**Figure 2.2 Typical Longwire Antenna Installation**

2.4.1.5 Power Requirements

The MSR-4030 requires a source of 115/230 VAC (48-63 Hz) power. Either 115 or 230 VAC can be selected inside of the coupler case on the connector board (601164-536-001). Two removable plugs are supplied on this board at J4 (underneath the power switch), or at J5 (spare plug). Just insert the correctly marked plug ("115 VAC" or "230 VAC") onto J4 and install the other one into the spare socket at J5. Make sure that the double sided AC tag located on the outside of the case has the correct AC voltage showing. If not, unscrew both stop nuts, reverse the tag face, and replace the stop nuts.

2.4.1.6 Antenna Compatibility

The MSR-4030 can be used with 24 or 35 foot whips as well as with 35-150 foot longwire antennas. If operation at 1 kW levels is anticipated below 2 MHz, it is recommended that a minimum antenna length of 35 feet be used due to the excessive RF voltages and poor efficiency characteristic of shorter antennas in this frequency range.

2.4.1.7 Low Level Modulation

Linear amplifiers with low level modulation will oscillate if the RF power output is radiated or conducted into the low level stages. Evidence of this situation is erratic or excessive power output. This is caused by the coupler and the antenna being too close to the transmitter and/or inadequate RF grounds.

2.4.1.8 Coupler Mounting

**CAUTION**

*The coupler should be mounted on a surface providing good water drainage and should be elevated over surfaces where standing water may exceed 3/16 inch. Submersion may allow water to enter through a vent on the lower case wall.*

The coupler can be bolted to mounts at the base of the antenna in any position except upside down. Six 1/4-20 bolts are used to secure the case mounting feet to the mounting surface. (See Figures 2.3 and 2.4.) If the coupler is mounted vertically, the end of the case with the RF and control cables should be pointed down to prevent the possibility of water entry into the connectors.

2.4.1.9 After Installation

After all connections are made to the coupler, completely wrap the control cable plug and J11 on the coupler case with the coaxial sealant tape that is supplied (see 1.4.4). Wrap the tape completely against the case and at least one inch beyond the rubber sleeving on the plug. Also, wrap the ground lug connection, the RF connection (J10), and the tip of the insulator (J19), completely covering all hardware. Be sure to overlap each winding of tape and finish by gently kneading to form a smooth surface and force out any air.

**CAUTION**

*Under certain conditions, the voltages on the MSR-4030 antenna terminal may be as great as 15 kV. Extreme caution must be taken to isolate this "Hot" terminal from personnel and at least 6 inches from any nearby objects such as guy wires, cables, brackets, or ground leads.*

2.4.2 Remote Control Cable Fabrication

The MSR-4030 requires a 37-conductor, shielded cable for controlling the coupler at its remote location. This control cable can be up to 250 feet (80 meters) long. It is recommended that this control cable be procured from ITT Mackay. However, a shielded and PVC jacketed cable with at least 36 No. 20 AWG wires can be substituted.

NOTES:

1. DIMENSIONS ARE IN INCHES AND (CENTIMETERS)
2. RESERVE SEVEN INCHES FROM THE ENCLOSURE FOR CABLE BEND AT J11.
3. UNIT WEIGHT 72 LBS. (33 KG).

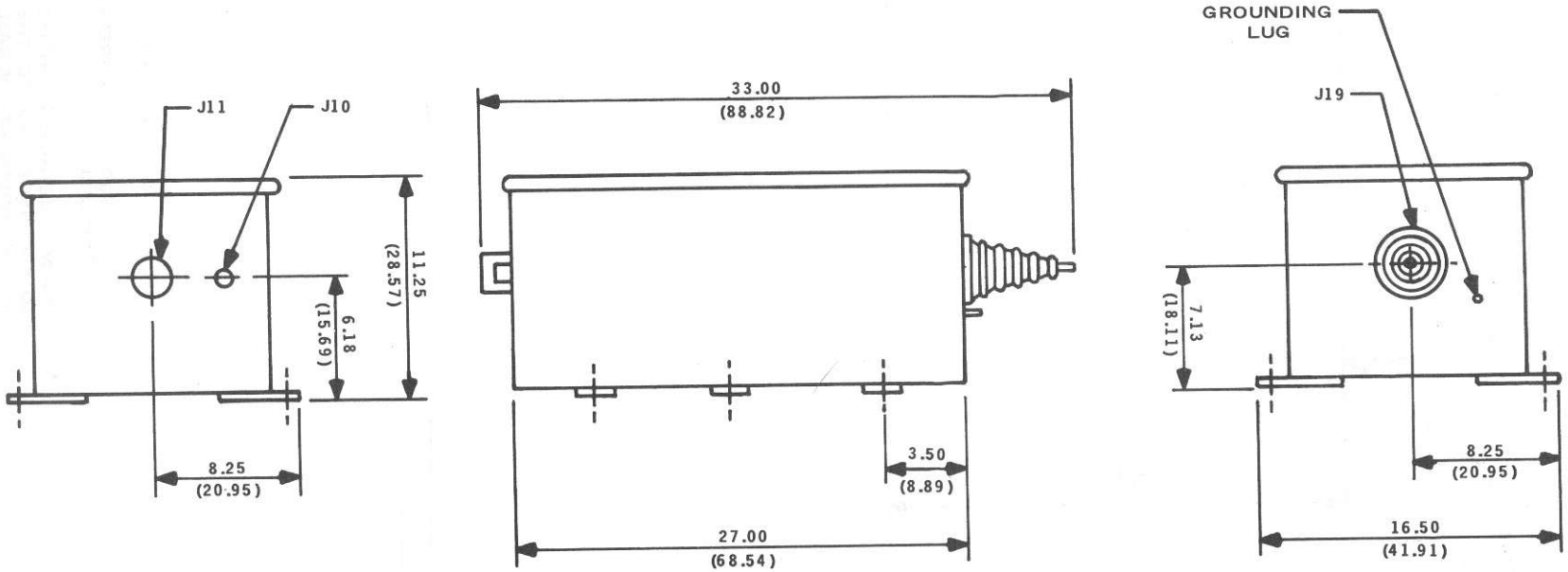
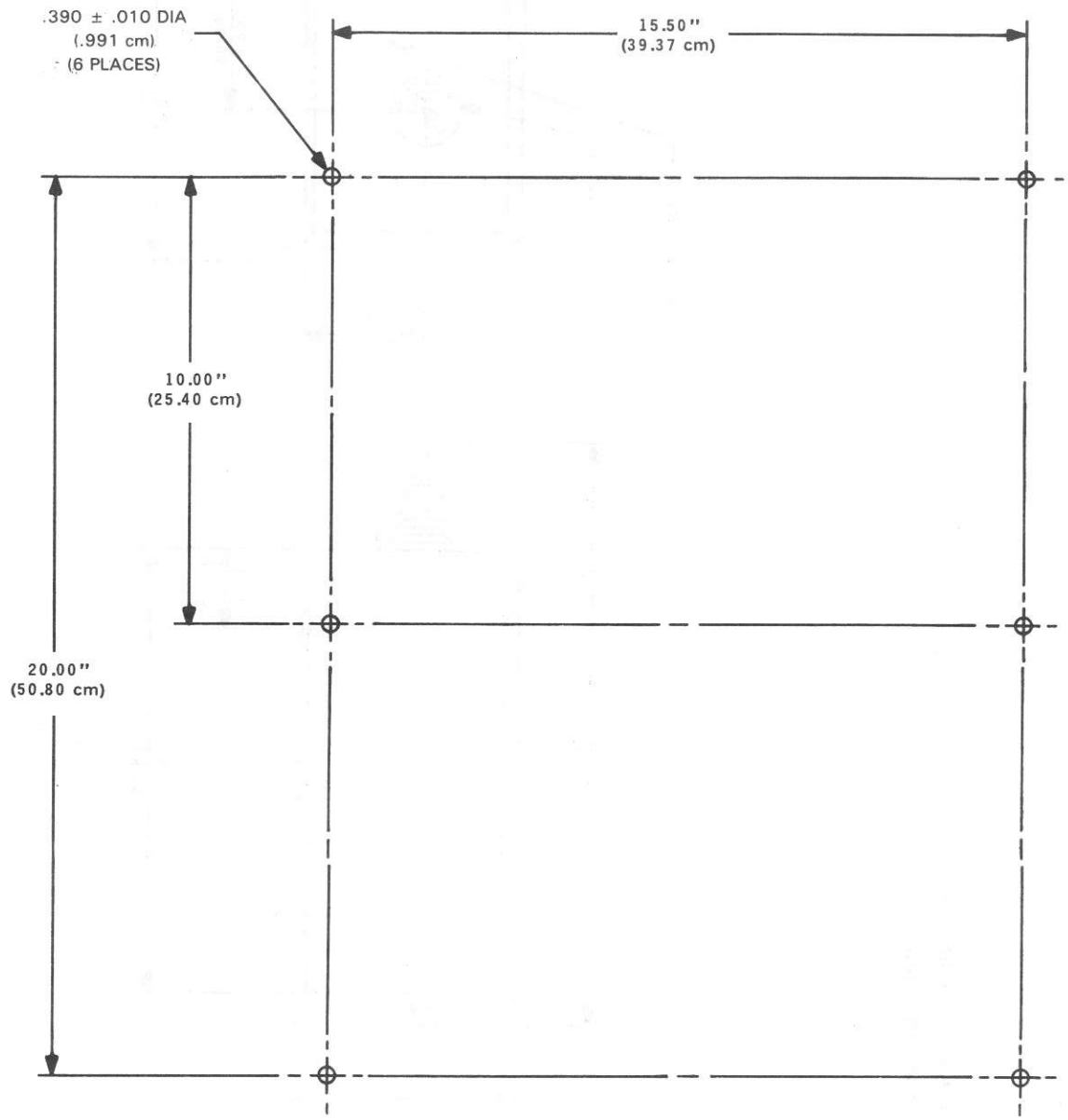


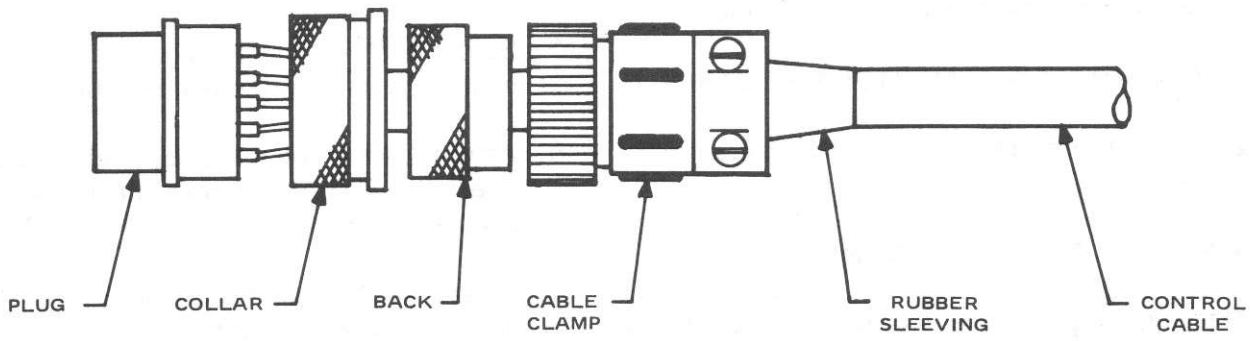

Figure 2.3 MSR-4030 Case Outline

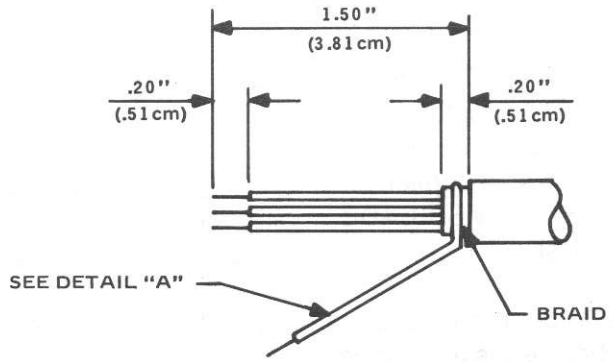


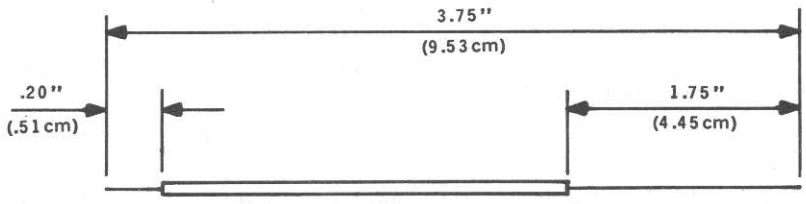

NOTES:

1. USE 3/8 MOUNTING HARDWARE (NOT SUPPLIED).
2. A METAL SURFACE IS PREFERRED FOR MOUNTING THE COUPLER CASE.
3. IF A NON-METALIC MOUNTING SURFACE IS USED, BE SURE TO SECURELY GROUND THE COUPLER CASE DIRECTLY TO THE GROUND AT THE BASE OF THE ANTENNA.

**Figure 2.4 Mounting Hole Pattern Dimensions**




DETAIL A

Figure 2.5 Control Cable Assembly

2.4.2.1 Material Supplied

The following material is required and supplied for fabricating the coupler control cable:

1. Connector, plug (MS3106A-28-215) - 1 each
2. Cable Clamp (Amphenol AN3057-12) - 1 each

2.4.2.2 Material Not Supplied

The following material is required, but not supplied for fabricating the coupler control cable:

1. Solder
2. Wire, Insulated, 3 3/4 inches long, No. 20 AWG
3. Cable, control (see 1.5.11)
4. Connector, plug, MS3106A-28-21 P (supplied in the MSR-1020 Amplifier or MSR-6408 Control Unit accessory kits)
5. Cable clamp, MS-3057-16A (Supplied in the MSR-1020 Amplifier or MSR-6408 Control Unit accessory kits)

As a convenience for installation, preassembled cables with connectors on both ends are provided as an option. These cables are factory assembled in lengths from 10 to 250 feet (see 1.5.12).

2.4.2.3 Cable Fabrication

1. Slide the cable clamp, back piece, and collar on the control cable as detailed by Figure 2.5.

2. Cut the cable PVC sleeving back 1.5 inches.

3. Cut the braid off the end leaving only .20 inches exposed.

4. Find the black wire and cut it back at least one inch (this wire is not used).

5. Strip and tin solder .20 inches off of the other wires.

6. Prepare the wire as shown in detail A. Solder the long stripped end completely around the braid.

7. Solder each wire into the solder sockets in each plug as diagrammed in table 2.1.

8. After all wires are soldered, push the collar over the plug and screw the back piece securely into the collar.

9. Loosen the screws on the cable clamp and securely screw it onto the back piece. Tighten both screws securely against the rubber sleeving and the cable.

2.4.3 Additional Material Required for Installation

2.4.3.1 Material required and supplied for the coupler installation:

1. Sealant, coaxial (see 1.4.3.2)
2. Connector, UG-21D (see 1.4.3.3) used with RF-213U cable.

2.4.3.2 Material required but not supplied for the coupler installation:

1. Six 3/8 bolts (and nuts if required)
2. RG-213U cable (see 1.5.10)
3. Up to 3 feet of antenna cable as referenced by 2.4.1.4
4. Ground strapping material as referenced by 2.4.1.2
5. Antenna, such as 1.5.6, 1.5.7, or 1.5.8.

## 2.5 CHECKS AFTER INSTALLATION

2.5.1 General Installation

Make sure that the coupler is well secured to its mounting platform. There should be good metal to metal bonding between the case and the antenna ground. The connections to the case should be well covered with the coaxial sealant to insure adequate waterproofing and to prevent corrosion. The coupler itself should be as close as possible to the antenna and the anten-

na lead-in should be well secured and no more than 3 feet (1 meter) in length. The RF and control cables should be no more than 250 feet (80 meters) long and tightly connected.

2.5.2 Functional Checks

1. After all connections are complete, turn on the MSR-1020 kW amplifier and all of its associated equipment. Do not turn on the antenna coupler power switch that is on the MSR-6212 Power Supply.

2. Note that the red antenna fault light on the transmitter (MSR-8000 or MSR-6700) is not lit.

3. Turn on the antenna coupler power switch at the MSR-1020 and note that the antenna fault light comes on.

4. Terminate the RF output from the amplifier into a 2 kW 50 ohm load.

5. On the transmitter, push the antenna tune button. The fault light should go out and the tuning/not tuned (yellow) light should come on. Note that there is approximately 100 watts output as indicated by the amplifier test meter.

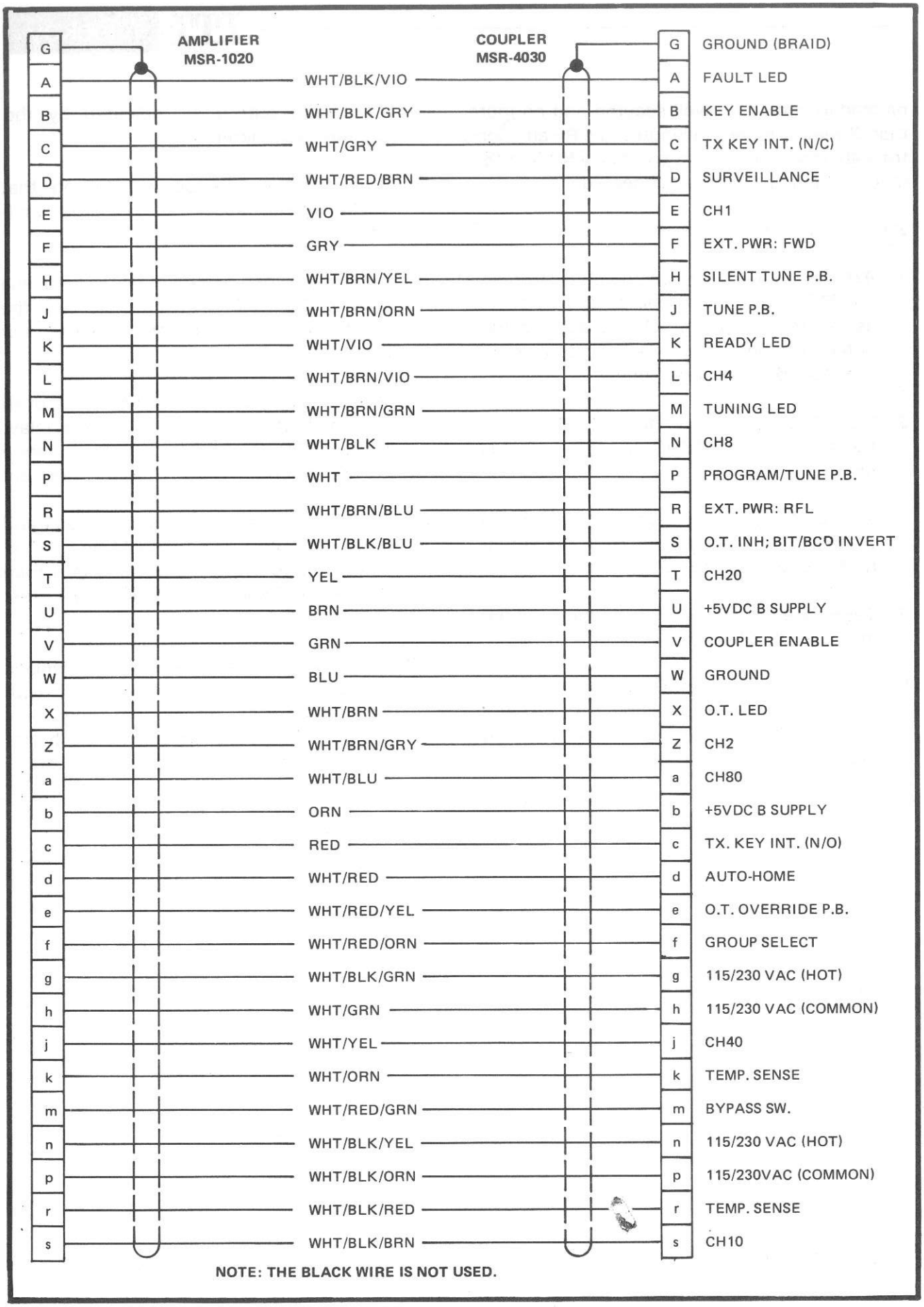
6. Turn off the coupler power and note that the tuning light goes out and the transmitter unkeys.

7. Remove the load and reconnect the RF line back to the MSR-4030 coupler. Turn the coupler power on and note a steady fault light.

8. Select a low operating frequency and push the tune button again. After a short delay, the MSR-4030 should tune the antenna and the green ready light should come on.

9. Place the transmitter in the CW mode and depress the key. There should be approximately 1000 watts output and less than 50 watts reflected on the MSR-1020 test meter.

10. Tune several other operating frequencies to see that a good tune is achieved with the antenna used. Check and correct any arcing or RF related problems by better grounding, more antenna clearance, etc.




**NOTE: THE BLACK WIRE IS NOT USED.**

Table 2.1 Counpler Control Cable

# SECTION 3
# OPERATION

## 3.1 GENERAL

This section contains information and instructions required for proper operation of the MSR-4030 antenna coupler. The MSR-4030 antenna coupler is used as a slave unit to the MSR-1020 in the 1 kW system. Refer to the Technical Manual for the 1 kW amplifier (MSR-1020) and the transmitter (MSR-8000 or MSR-6700) for a complete technical description of their operation with the 1 kW system.

## 3.2 OPERATING CONTROLS

The following controls and indicators are located on the front panel of the companion transmitter:

### 3.2.1 Tune

Depressing this button initiates a tuning cycle. A momentary depression of this button is the only action required.

### 3.2.2 Fault

This red light is illuminated for the following conditions:

1. When the antenna coupler power is initially turned on, a steady, non-blinking light comes on.

2. If the tuning time delay runs out (approximately 30 seconds after initiation of a tune command) the light will blink.

3. Anytime the VSWR exceeds 2:1 for more than 1 second, except during a tuning cycle, the light will blink on and off.

### 3.2.3 Tuned/Not Tuned

This yellow light is illuminated only during a tuning cycle.

### 3.2.4 Ready

The green light is illuminated after a tuning cycle has been completed and the coupler has tuned to an acceptable VSWR.

### 3.2.5 TX Power

1. **FWD:** Indicates relative forward RF power at the input to the antenna coupler.

2. **RFL:** Indicates relative reflected RF power at the input to the antenna coupler. A null or low reading indicates the antenna is correctly matched to the transceiver.

### 3.2.6 Coupler Fault

This red light is turned on continuously at the MSR-1020 for the following conditions:

1. Whenever the amplifier senses a coupler VSWR of more than 2:1

2. Whenever an over-temperature condition exists in the MSR-4030

### 3.2.7 Tuning Mode Controls

1. **Normal Tune** - By depressing the tune button (refer to 3.2.1), the MSR-4030 will accept a 100-250 watt carrier and tune its elements to an acceptable match.

2. **Surveillance Tune** - This tuning feature is selected by a dip switch mounted under the cover of the MSR-8000 or MSR-6700.

If the coupler has tuned and in the surveillance mode this feature allows the coupler to sample the RF carrier and automatically retune for small VSWR changes.

3. **Silent Tune** - This feature is available on the front panel of the MSR-6700, initiated by the coupler silent tune and program pushbuttons. On the MSR-8000, the "CHECK TX" pushbutton initiates a silent tune cycle. It is also available in the accessory MSR-6408 control unit (see accessories, section 6). It allows the coupler to store position information derived from the standard tunes, into designated channels and upon command the coupler will retune to the programmed frequency quickly and without an RF carrier.

4. **MSR-8000** - When using the MSR-8000 in the silent tune mode, ten channels can be programmed on the "CHANNEL/FREQ" knob on the front panel of the transceiver. Every time the antenna coupler is tuned in one of the ten channels, the tuning information is stored in that particular channel. To use the silent tune mode, pick a channel that has already been tuned and push the "CHECK TX" pushbutton. The coupler will automatically position the tuning elements from memory and the "READY" LED will come on. Because no RF carrier is used, the "TX" LED on the meter will not light and there will be no forward power during the tuning sequence in the silent tune mode. However, there may be a reflected power indication on the meter during tuning due to logic voltages.

   It is recommended that the MSR-4030 be turned off when programming frequencies into the MSR-8000 since use of the "CHECK TX" button will cause the coupler to attempt silent tuning. Also, the surveillance feature should be enabled when using the silent tune feature to ensure a low VSWR.

5. **MSR-6700** - The MSR-6700 has the capability of storing 95 channels (01-95) in the MSR-4030. Programming is done from the exciter's front panel by depressing "CHAN," the channel number, "ENTER" and then the coupler "TUNE" pushbutton. The tuning information is then stored in the channel selected. To check the memory channels, program several different operating frequencies into different channels. Go back to the first channel and frequency that was programmed and push the coupler "SIL TUNE" pushbutton. The coupler will automatically tune from memory without any RF carrier. The "TX" LED will not light and only some reflected power will be indicated by the meter due to logic voltages out of the MSR-4030. When the green "READY" LED comes on, check the VSWR with a CW carrier. A low reflected power reading on the meter indicates a good antenna coupler tune. The surveillance feature should be enabled for silent tuning to ensure a low VSWR.

6. **MSR-6408** - Referring to Figure 6.3, make sure that J1 and J2 are securely connected and that all system wiring and transmitter connections are complete. Turn on all of the equipment and note that the MSR-6408 "FAULT" LED is on. This indicates that the antenna coupler has power and is in the correct standby condition. Terminate the RF output from the amplifier into a 2 kW 50 ohm load with a 1000 watt wattmeter in series for measurement purposes. With all of the switches in the positions as indicated by Figure 6.4, push the "TUNE" button and the "FAULT" LED should go out and the "TUNING" LED should come on. Note that there is 150-250 watts output during tuning on the wattmeter. If not, the transmitter should be adjusted for this output during the tuning mode. Turn off the AC power switch on the control unit. Remove the load and reconnect the RF line back to the MSR-4030. Turn the MSR-6408 power on

and a steady "FAULT" LED should be indicating. Select a low operating frequency and push the "TUNE" button again. After a short delay, the antenna coupler should tune the antenna and the green "READY" LED should come on. Place the transmitter in the CW mode and depress the key. Check the relative power meter on the control unit in the "FWD" position and it should indicate forward power output. Put the meter in the "RFL" position and there should be very little reflected power, indicating a good antenna coupler tune.

### 3.3 LOW TUNE POWER OPERATION

If necessary, the MSR 4030 may be tuned and operated with the MSR 1020 LPA power switch in the STANDBY position. This will allow the coupler to tune on 40 watts nominal RF tune power from the MSR 8000 or MSR 6700. Such bypass operation is advantageous in the event emergency standby AC power reserve is insufficient for operating the MSR 1020 LPA.

### 3.4 ACCESSORY OPERATION

Refer to accessories and addendums (Section IV of this manual for detailed operating information on these accessories:

1. MSR-6408 control unit (699016-000-XXX)
2. Antenna By-Pass Kit (600067-7000-001)
3. Shock Mount Kit (600095-700-001)

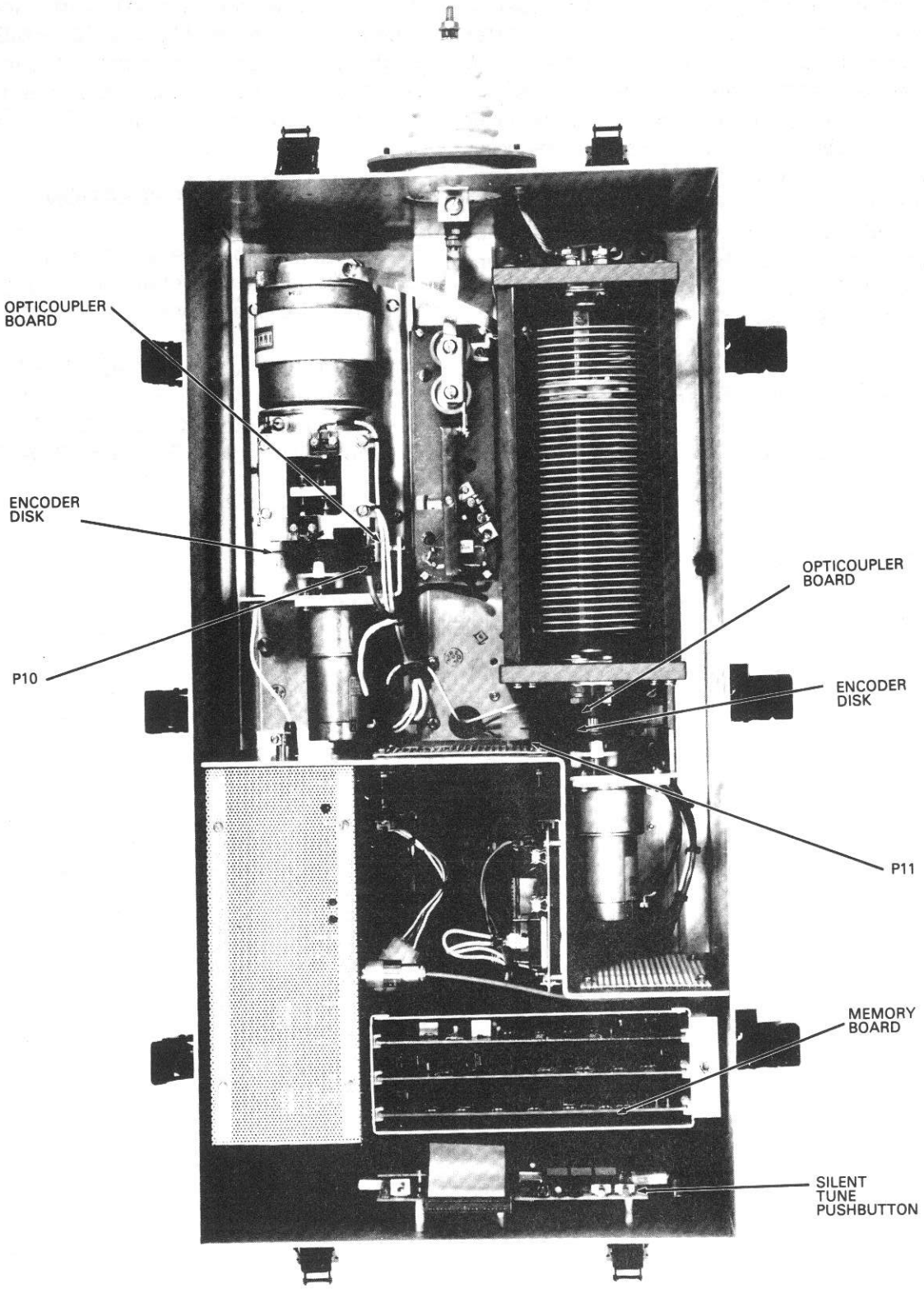



Figure 3.1 Silent Tune Features

# SECTION 4
# FUNCTIONAL DESCRIPTION

## 4.1 GENERAL

The MSR-4030 is a reliable 1 kW automatic antenna tuner that is designed to tune a variety of antennas from 1.6-30 MHz. Whenever possible, the major sections of this coupler have been made into modules of removable boards for ease of maintenance and serviceability. This section describes these major sections as well as the two main packaging levels - the case and coupler chassis assemblies.

Figure 4.1 is a functional block diagram that shows the basic interfacing of all of the boards and module level assemblies.

## 4.2 SUBASSEMBLIES

The antenna coupler consists of nine major P.C. board or module level assemblies that are packaged into two major mechanical assemblies.

### 4.2.1 RF Module

The RF Module contains the RF Board (601169-536-001) in a removable chassis with the RF input at J17 on the Circuit Board and the RF output at J18 on the Chassis.

The RF Module contains the following five separate functions:

1. The 6 dB attenuator pad is made up of six (6) 45 watt resistors that are used during tuning to limit the VSWR as seen by the transmitter.

2. The power detectors provide forward and reflected voltage outputs that indicate VSWR conditions.

3. The magnitude detector samples the RF and provides error signals that control the tuning of the inductor in the coupler tuning network.

4. The phase detector also samples the RF and provides the error signals that control the capacitor in the tuning network.

5. A four to one impedance transformer is used to transform the 50 ohm input to a 12.5 ohm output from the RF Module.

### 4.2.2 Capacitor Chassis Assembly

The capacitor chassis assembly is the series element, C1, of the basic series C, Shunt L coupler tuning network. C1 is a 12-500 pf, 15 kV variable capacitor that is used to tune out the phase error in the coupler network. In addition, an opticoupler board (601170-536-002) and a shaft driven disk are used to transmit location data to the MSR-4030 logic. In this way, the location of the variable capacitor as it tunes from 12-500 pf can be digitally tracked with the addition of the Memory Module (see Section VI).

### 4.2.3 Opticoupler Board

This board is made up of two groups - 601170-526-002 in the capacitor chassis assembly and 601170-536-001 which is located in the inductor chassis assembly. This board provides digital information to the Memory Module (601166-536-001). Refer to the Memory Module information in Section V for a complete technical description.

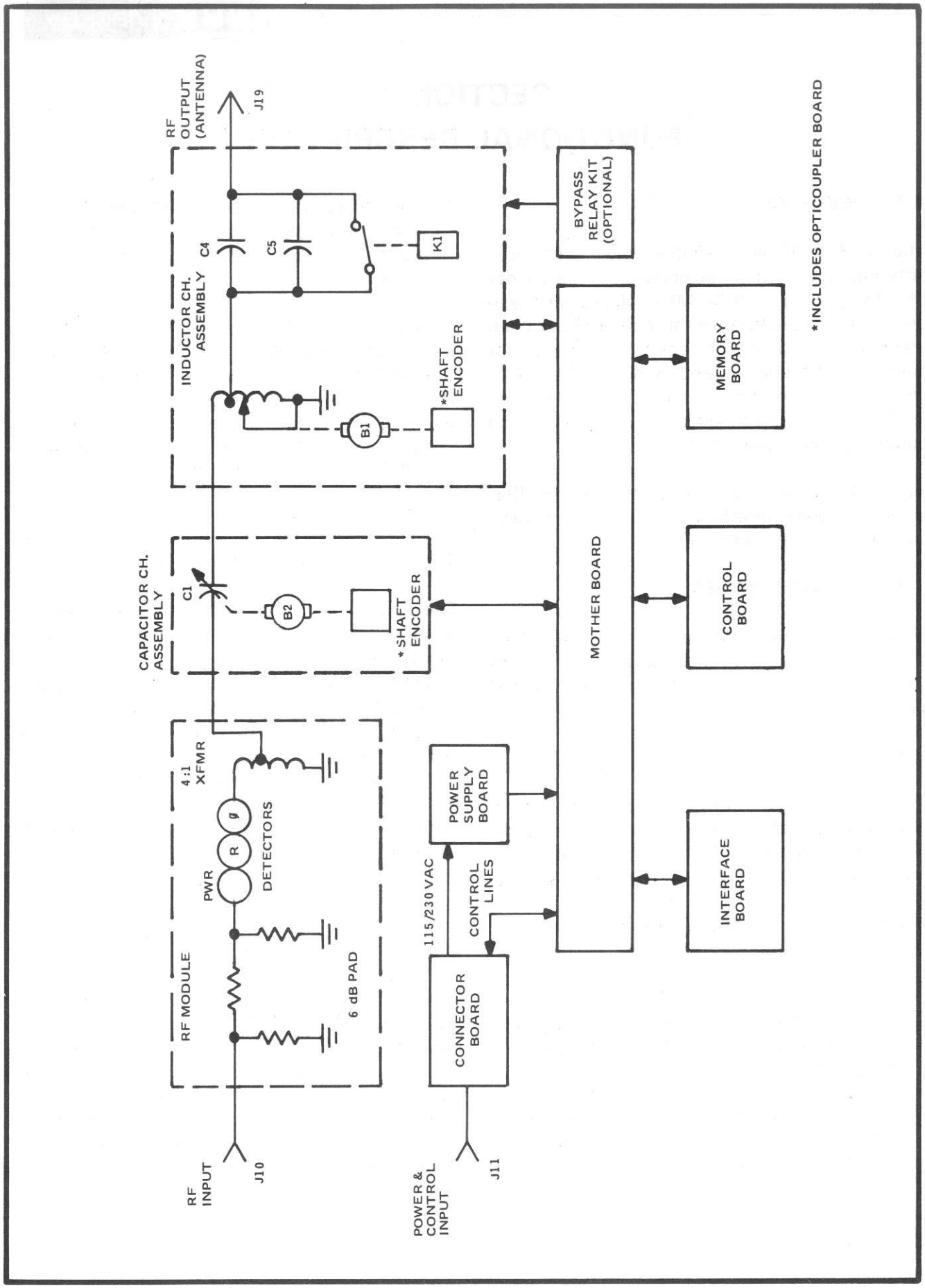



Figure 4.1 MSR-4030 Block Design

### 4.2.4 Interface Board (601165-536-001)

The interface board contains the electronic circuitry required to interface the control board (601282-536-001) to the memory board. In addition, circuitry for other functions such as coupler by-pass, transmit interlock, over-temperature, etc. is included.

### 4.2.5 Control Board (601282-536-001)

The control board contains all of the active coupler logic circuits, servo amplifiers, and the +8 VDC regulator for the logic supply. It contains all of the tuning logic required to convert error signals from the RF board into pulsed DC from the servo transistors to drive the tuning motors during normal and surveillance tune modes.

### 4.2.6 Memory Board

The memory board expands the basic antenna coupler tuning functions. With this board, the tuning information can be stored automatically and retained in memory for up to 96 communication channels. Upon command, the memory will rapidly guide the MSR-4030 tuning elements to their positions without an RF carrier or any manual tuning controls. This feature provides the extra convenience of channelized operation for a very rapid method of tuning many frequencies without radiating any RF power.

### 4.2.7 Coupler Mother Board (601168-536-001)

The MSR-4030 uses a mother board for all under-chassis wiring. This circuit board provides connectors to plug-in and interconnect five boards to each other and to external wiring. The external (above chassis) wiring is terminated into three plugs and connected into the mother board through three PC mounted connectors. Another connection is provided to interconnect the connector board (601164-536-001) to the mother board through a ribbon cable.

### 4.2.8 Power Supply Board (601175-536-001)

The power supply board provides all of the voltages required by the MSR-4030 coupler. These DC voltage outputs are +28 unregulated, +15 unregulated, +5 "A" supply, and +5 "B" supply. The +28 VDC and the +15 VDC outputs are fused and have LED BUS indicators that light when the voltage is present. In addition, the +5 VDC outputs are over voltage protected and the 5 volt regulators are mounted on a heatsink for added reliability.

### 4.2.9 Inductor Chassis Assembly (600360-713)

The inductor chassis assembly contains L1, the shunt element of the basic series C, Shunt L coupler tuning network. L1 is a 50 uh variable inductor specially designed to operate with the high voltages and currents encountered in a 1000 watt antenna coupler. It is motor driven from the control board by the magnitude error signals to tune the antenna to 50 ohms. In addition, an opticoupler board (601170-536-001) and a shaft driven disk are used to transmit location data to the MSR-4030 logic. In this way, the location of the variable inductor can be digitally tracked as it tunes.

The inductor chassis also includes a solenoid activated switch that shorts across capacitors C4 and C5. These capacitors are in series with the coupler tuning network and are automatically switched into the circuit when needed for additional tuning range.

### 4.2.10 Coupler Chassis Assembly (600426-705)

This chassis is used as a mounting platform that houses all of the sub-level boards and modules. It is secured in the coupler case by six captive fastener screws for easy removal and installation.

### 4.2.11 Connector Board (601164-536-001)

The connector board provides AC power and control line interconnections between the external control cable and the coupler circuitry. The control line connector is mounted on the PC board and is secured to the case by 6-32 threaded studs. The connector board is connected to the mother board by a plug-on 40-conductor ribbon cable. All lines are bypassed by either axial-lead capacitors or a buffered inverter circuit on the connector board. The connector board also provides on-board features to operate the coupler and determine its status locally. Additionally, it incorporates an AC switch and a 115/230 VAC option plug.

### 4.2.12 Case Assembly

The case, along with its cover, is designed for outdoor mounting, and is fully gasketed and splash-proof. The connector board is installed into the case and provides an interconnection at J11 for control line inputs. The case is used to house the coupler chassis assembly and to provide the necessary input/output connections.

# SECTION 5
# MAINTENANCE

## 5.1 GENERAL

This section provides information for routine maintenance, repair and evaluation of the overall performance of the MSR-4030. Modular construction of the Antenna Coupler lends itself to a logical and straightforward troubleshooting procedure. By referring to the overall and individual block diagrams, and using related level information, a trouble can be quickly localized to a particular assembly.

After establishing the existence of a trouble in a particular assembly, refer to the servicing information for that assembly located elsewhere in this section of the manual.

**WARNING**

*This MSR-4030 is extremely hazardous when operated with the cover off. Precaution must be taken to avoid the AC and RF voltages that are present inside the case.*

### 5.1.1 PC Board Repair

To avoid damaging the PC boards during the replacement of components, extreme care should be used in soldering and component removal. A low wattage soldering iron (25-50 watts) with a narrow tip should be used.

A low wattage iron is necessary to prevent the application of excessive heat to the copper foil of the PC board. Excessive heat may cause the foil to separate from the board, rendering the board unrepairable. Only a high quality electronic grade rosin solder should be used in making repairs.

**CAUTION**

*Do not use an acid core solder.*

Due to the circuit density of the boards, solder "bridges" or short circuits between adjacent full runs are possible if care is not used during soldering operations. After soldering is completed, the area around the connection should be closely inspected for excess solder or "bridges" between adjacent runs or connection. Any "bridges" or excess solder between connections must be removed before reinstalling the board. Because of the double sided construction used on the PC boards, a components lead may be soldered to printed circuit areas on top and bottom of the board. Consequently, when a component lead is removed, the replacement component should be resoldered, top and bottom, as applicable.

### 5.1.2 CMOS Device Handling Precautions

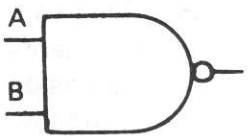
CMOS devices can be damaged by static voltages, and therefore the following is recommended:

a) All MOS devices should be placed on a grounded work bench surface, and the repair operator should be grounded prior to handling MOS devices, since a person can be statically charged with respect to the work bench surface.
b) Nylon clothing should not be worn while handling MOS circuit or devices.
c) Do not insert or remove MOS devices from sockets while power is applied.
d) When soldering MOS devices, insure the soldering iron used is a grounded type.

### 5.1.3 Logic Interpretation

Several types of digital devices are used in the coupler. The following descriptions are presented to explain their basic operation and symbolic notation. The digital devices used (gates, flip-flops, inverters, etc.) are binary in nature, that is, the output voltage of each can be only in two permissible states. The two possible states are called logic "1" and logic "0." The assignment of voltage levels to these states is arbitrary. However, in the manual positive logic is standardized, which means we define the logic states as shown in Table 5.1.

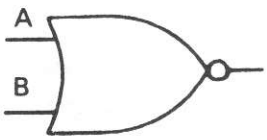
#### 5.1.3.1 NAND Gate




| INPUTS | | OUTPUT |
|---|---|---|
| A | B | |
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

The outputs of the NAND gate are the opposite of the AND gate. If any input is 0, the output will be 1.

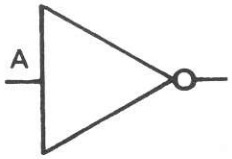
#### 5.1.3.2 NOR Gate




| INPUTS | | OUTPUT |
|---|---|---|
| A | B | |
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

The output of the NOR gate is the opposite of the OR gate. The output is 0 if any input is 1.

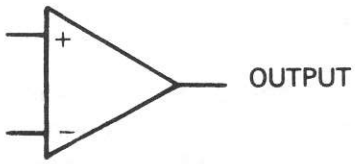
#### 5.1.3.3 Inverter




| INPUT | OUTPUT |
|---|---|
| 0 | 1 |
| 1 | 0 |

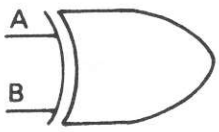
The inverter has a single input. The output level is the opposite of the input level.

#### 5.1.3.4 Voltage Comparator




The voltage comparator has two inputs, V+ and V−. The V+ input is normally connected to a fixed or reference voltage. The V− input is usually variable. As the V− input becomes more positive and exceeds the V+ input level, the output switches low. If the V− input voltage becomes less positive than the V+ reference input, the output switches to a high level once again.

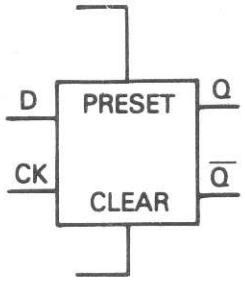
#### 5.1.3.5 Exclusive OR Gate




| INPUTS | | OUTPUT |
|---|---|---|
| A | B | |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

The Exclusive OR gate only has a high output when its inputs are different.

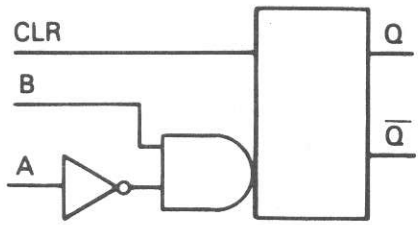
5.1.3.6 D-Type Flip-Flop




| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| PRESET | CLEAR | CLOCK | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | No Change | |

The D-Type Flip-Flop may be set or reset independently of D and clock inputs. However, when both preset and clear inputs are high, the level present at the D input will be clocked to the Q output as the clock input goes high.

5.1.3.7 Retriggerable Monostable Multivibrator (One-Shot)




| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| CLEAR | A | B | Q | $\overline{Q}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | | |
| H | ↓ | H | | |
| ↑ | L | H | | |

The One Shot produces output pulses when certain inputs have level transitions.

| | | TTL | CMOS |
|---|---|---|---|
| LOGIC 1: | Normally greater than | 2.0 Volts | 7.0 Volts |
| LOGIC 0: | Normally less than | 0.8 Volts | 3.0 Volts |

**Table 5.1 Logic States**

## 5.2 MAINTENANCE EQUIPMENT AND SUPPLIES

The Antenna Coupler requires a minimum of tools for assembly and disassembly for maintenance. The MSR-4030 has been designed for reliability and serviceability and requires very little test equipment or maintenance supplies.

5.2.1 Required Test Equipment

The following test equipment or equivalent is required for troubleshooting and repair of the MSR-4030 antenna coupler:

1) Companion transceiver or equivalent source of 100 watts of RF Power.
2) Wattmeter - Bird Model 43 with 1000 H and 100 H elements.

3) 2 kW, 50 ohm dummy load - Bird Model 329
4) VTVM - Hewlett Packard 410B
5) Volt-Ohm Meter - Simpson 260
6) RF Module cable assembly (see Figure 5.8)

### 5.2.2 Maintenance Tools

To disassemble and adjust the MSR-4030, the following tools are required:

1) Slotted and insulated alignment tool, such as the JFD 5284 or 7104-5
2) 12" long, medium sized, flat-bladed screwdriver
3) Small adjustable wrench

### 5.2.3 Maintenance Supplies

The antenna coupler should be checked yearly and the following supplies are required for this maintenance:

1) Cramolin Red Paste - Part No. 600011-112-001 (1/2 lb. can)
2) Cramolin Red Liquid - Part No. 600011-112-002 (2 oz. bottle)
3) Coaxial Sealant Tape - Part No. 600033-115-001 (1 roll)

## 5.3 ASSEMBLY AND BOARD IDENTIFICATION

Table 5.2 lists the major assemblies and boards that are located in the MSR-4030. The sub-assemblies are listed underneath the main assemblies with their part numbers. Schematics for each major assembly and circuit board, parts lists, and circuit descriptions are contained in this chapter of the manual.

## 5.4 DISASSEMBLY OF THE COUPLER

Refer to Figure 5.1 and 5.2 for information regarding the disassembly of the coupler (shown with the cover removed). If routine maintenance or servicing is required, the following steps can be taken to get to all boards and assemblies:

1) Loosen all ten latches on the case and remove the cover.
2) Disconnect the ribbon cable connector and plug P16 from the connector board.
3) Unscrew P17 from J17, disconnect the strap at E5, and disconnect the strap going to the antenna terminal at E4.
4) Unscrew six captive fasteners located around the main chassis.

**NOTE**

*When reinstalling the coupler chassis into the case, first apply Blue Loctite (P/N 600018-115-001) to the threads of the six fastener mounts located on the case floor.*

5) Pull the main chassis straight out.
6) Unscrew the two captive fasteners on the RF module, remove P17 from J17, and pull the RF module from the main chassis.
7) To remove the power supply board, remove the two screws on the top, remove P14, and unplug the two clips on the bridge rectifier (P12 and P13). Pull the board straight out.
8) The capacitor chassis assembly can be removed by loosening four captive screws, removing the strap at E2, disconnecting P9 from the mother board, and lifting the capacitor chassis off the main chassis.
9) To remove the inductor chassis assembly, unplug P8 and P5 from the mother board, loosen the four captive screws on the chassis, and remove the inductor chassis from the main chassis.
10) The connector board can be removed from the case by removing the eight nuts that secure the board to the case studs and pulling the board off of these studs.
11) To remove the interface, memory, or the control board, loosen the captive screw on the card cage, pull the lid up, and pull the board straight out.
12) The mother board can be removed by turning the main chassis upside down, removing the ribbon cable at J1, unscrew the 15 retaining screws, and pulling the mother board off of the main chassis.

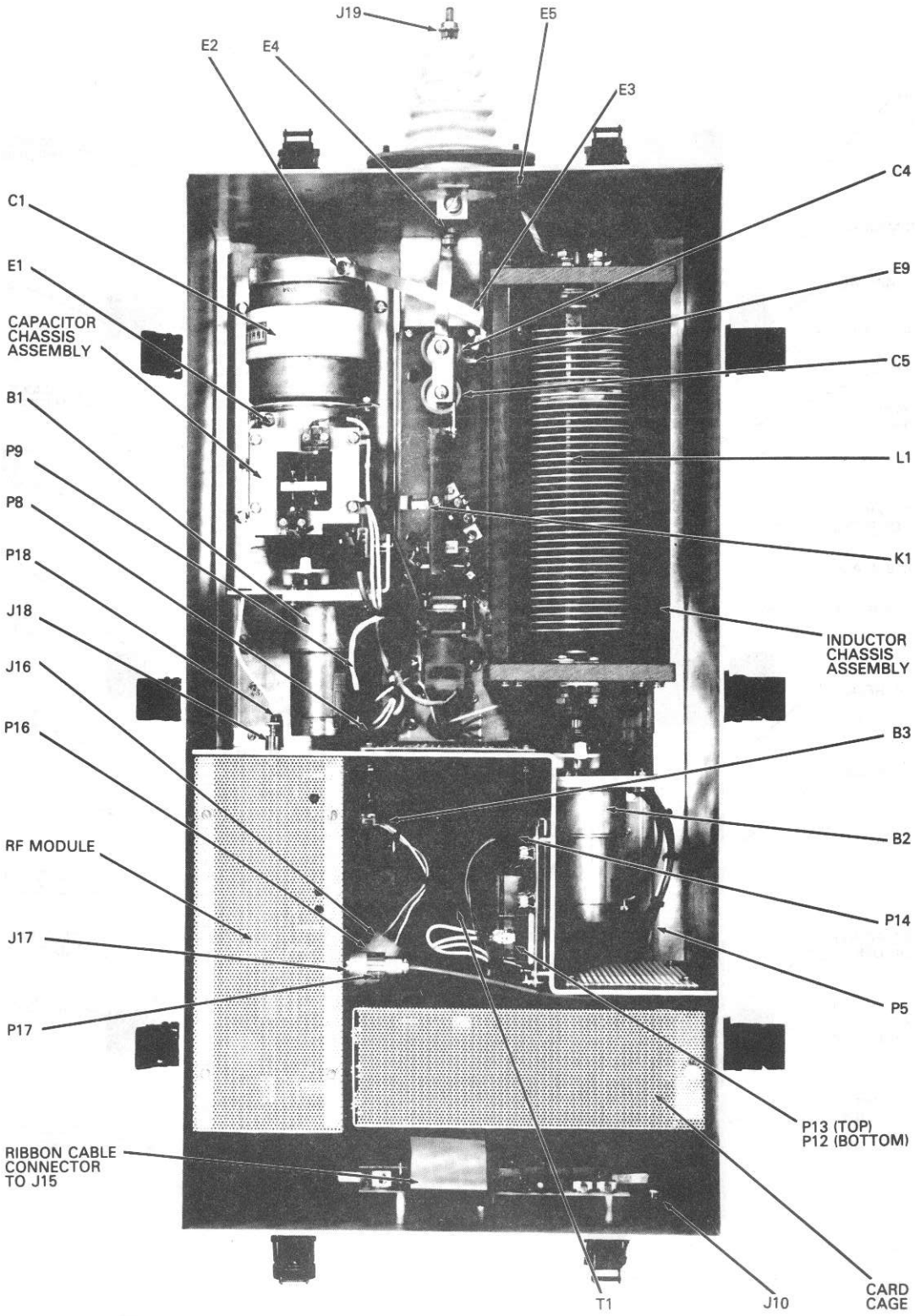



Figure 5.1 Major Parts, Connections and Modules

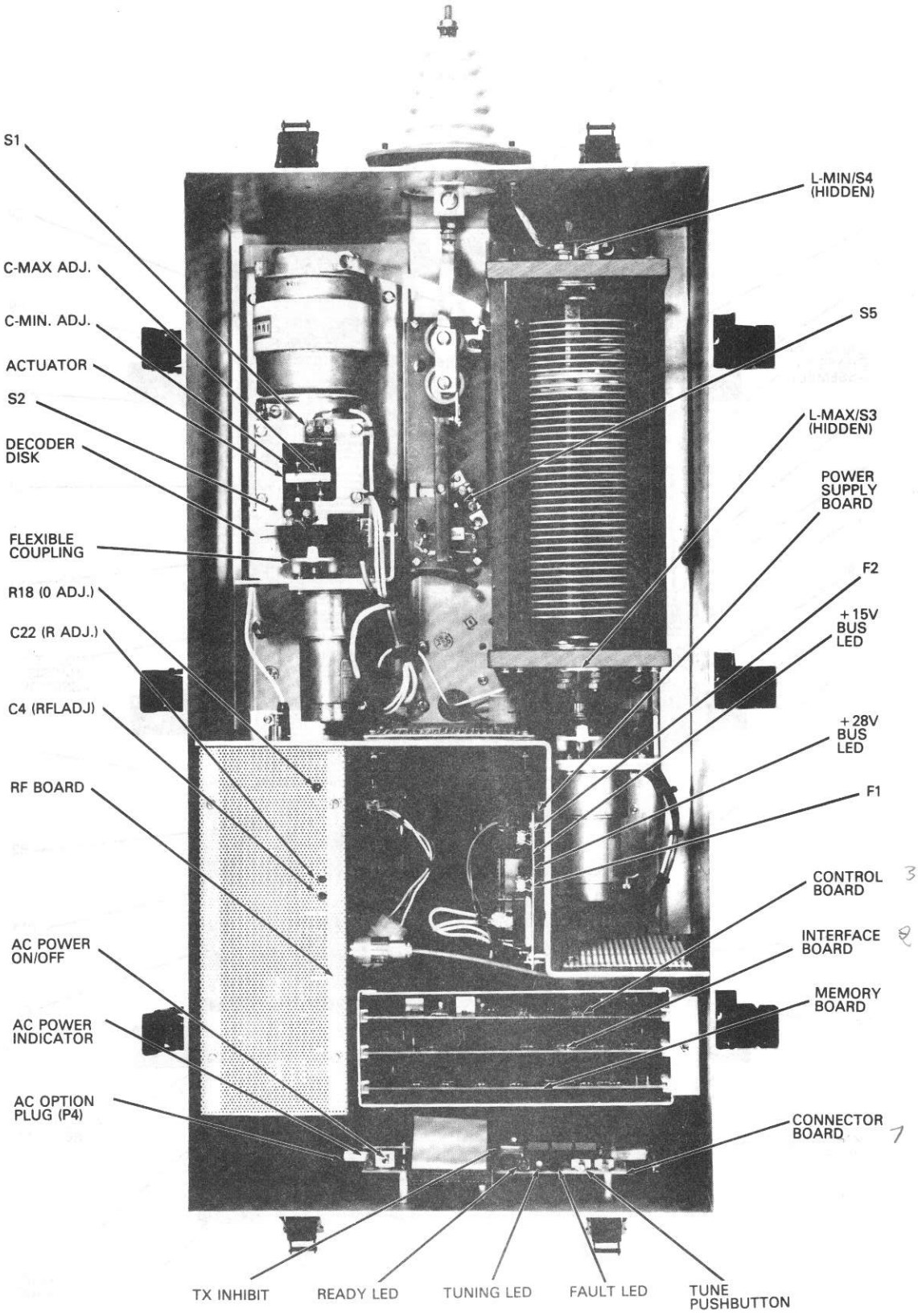



**Figure 5.2 Adjustments, Indicators, Boards and Switches**

| DESCRIPTION | PART NUMBER |
|---|---|
| Case Assembly, Grey | 600359-713-001 |
| Case Assembly, O.D. | 600369-713-002 |
| Antenna Insulator Assembly | 600386-713-001 |
| Gasket, Insulator to Case | 600086-628-001 |
| Gasket, Insulator to Mounting Plate | 600092-628-001 |
| Connector, RF Input (J10) | 600146-606-001 |
| Connector Hood for J10 | 600206-606-001 |
| Gasket for J10 | 600070-628-001 |
| Coax, J10 to P17 (1.5 Ft.) | 600109-102-001 |
| Connector, Coax (P17) | 600244-606-001 |
| Reducer for P17 | 600244-606-002 |
| Latch, Case | 600246-618-003 |
| Can, Breather | 600702-612-001 |
| Filter, Breather | 600029-641-001 |
| Gasket, Breather | 600090-628-001 |
| Antenna Insulator Mounting Plate, Grey | 603128-602-001 |
| Antenna Insulator Mounting Plate, O.D. | 603128-602-002 |
| Gasket, Connector Board to Case (J11) | 600077-628-002 |
| Voltage Tag, 115/230 VAC | 600519-626-001 |
| Cover Assembly, Grey | 600197-708-001 |
| Cover Assembly, O.D. | 600197-708-002 |
| Gasket, 14 Inch | 600084-628-001 |
| Gasket, 26.5 Inch | 600085-628-001 |
| Keeper (Latch) | 600246-618-004 |
| Coupler Chassis Assembly | 600426-705-001 |
| Ribbon Cable (Connector Bd. to Mother Bd.) | 600315-540-107 |
| Fan (B3) | 600019-387-001 |
| Fan Screen | 600010-641-001 |
| Ground Strap, C1 to L1 | 600245-608-001 |
| Cover, P.C. Card Case | 600155-704-001 |
| Transformer, Mod., T1 (Prewired w/Connectors) | 600156-512-001 |
| Transformer, T1 | 600149-512-001 |
| Plug, 6 Pin (P11) | 600264-606-004 |
| Pins, (P11) | 600265-230-002 |
| Plug, 3 Pin (P14) | 600287-606-004 |
| Pins (P11) | 600277-230-001 |
| Terminal, Crimp (P12, 13) | 600245-230-001 |
| Connector Board Assembly | 601164-536-001 |
| RF Module | 600414-705-001 |
| RF P.C. Board | 601169-536-001 |
| RF Transformer Assembly (4:1) | 650125-513-001 |
| Capacitor Chassis Assembly (C1) | 600355-713 |
| Capacitor Assembly (C1, and Mounts) | 600382-713-001 |
| Opticoupler P.C. Board (Capacitor) | 601170-536-002 |
| Opticoupler P.C. Board (Inductor) | 601170-536-001 |
| Control P.C. Board | 601282-536-001 |
| Mother P.C. Board | 601168-536-001 |
| Power Supply P.C. Board | 601171-536-001 |
| Inductor Chassis Assembly (L1) | 600360-713-001 |
| Interface P.C. Board | 601165-536-001 |
| Memory Board | 601166-536-002 |

**Table 5.2 MSR-4030 Coupler Assemblies**

## 5.5 COUPLER MAINTENANCE AND ADJUSTMENTS

All modules, boards, and assemblies in the MSR-4030 are of high reliability, solid state design, and adjustment or repair is seldom required. The coupler should, however, be checked yearly and certain preventive maintenance functions performed. In this way, the reliability of the coupler can be assured and any potential problems can be corrected.

### 5.5.1 Servicing Coupler With BITE Facilities

The MSR-4030 contains built-in test equipment (BITE) which is a maintenance feature contained on the connector board. By removing the case cover, the service technician has access to many of the same coupler controls that are at the transmitter site, but can now be controlled locally at the coupler location. These functions are the AC ON/OFF switch and the normal tune and silent tune pushbuttons. Additionally, there is a TX Inhibit switch and the fault, tuning, and ready LED indicators. The TX Inhibit is a safety feature that prevents the transmitter from keying when the switch is placed in the inhibit position and the red LED is on. See Section 5.13 for further information on the operation of the connector board.

### 5.5.2 Annual Maintenance

The coupler should be checked yearly and maintenance performed as necessary to assure years of reliable operation. The following steps are recommended for this maintenance check:

**CAUTION**

*The Transmitter and all AC power to the coupler should be shut off before performing these steps.*

1) Remove the cover and check to see that the gasket is in good shape. Replace any deteriorated gasket material and make sure that the gasket is clean and free from dust.
2) Refer to Section 5.4 and remove the main chassis from the coupler case.
3) Check for loose hardware and tighten as necessary.
4) Refer to Figure 5.3 and remove the hardware and cover holding the foam filtering material. Clean this foam with plain soap and water. After the filter is dry, place it back into position, replacing the cover and the hardware.
5) Clean and remove any corrosion and replace or refinish affected parts.
6) If necessary, clean the outside of the case, antenna insulator, and cover with soap and water.
7) Make sure that the case mounting bolts are tight and secure.
8) Check the ground connections and clean off any existing corrosion and make sure these connections are secure and making a good ground.
9) Make sure that the RF and control line connections are secure and waterproof. If not, remove the sealant material, clean off the connections, and reapply the sealant tape.
10) Pad Relay Lubrication (K1)
    Remove the RF Module from the chassis by disconnecting the cable connection at J17 and loosening the two captive fasteners securing the module to the chassis and divider panel. Remove the hardware from the module top and side covers to allow access to the RF Board. Lubricate the Attenuator Pad Relay K1 using a small brush to apply Cramolin liquid. Brush the lubricant on all metal parts and contacts of the relay to protect against corrosion. Wipe excess lubricant from the relay and surrounding areas with a cloth. Replace the top and side covers of the module and reinstall on the chassis. Tighten all hard ware and reconnect the cable at J17.
11) Replace the coupler chassis inside the case and secure all connections. Leave the cover off the case.

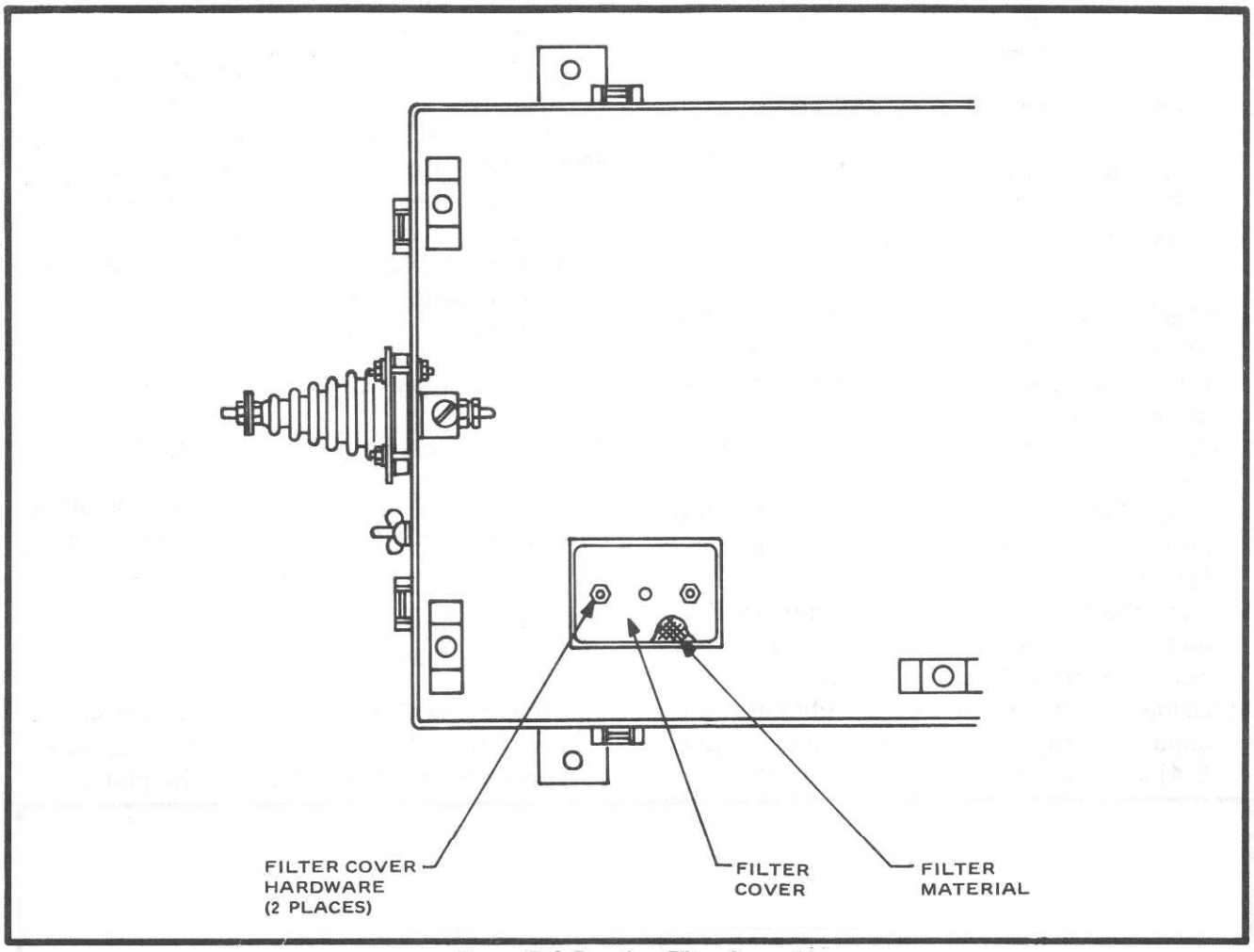



Figure 5.3 Breather Filter Assembly

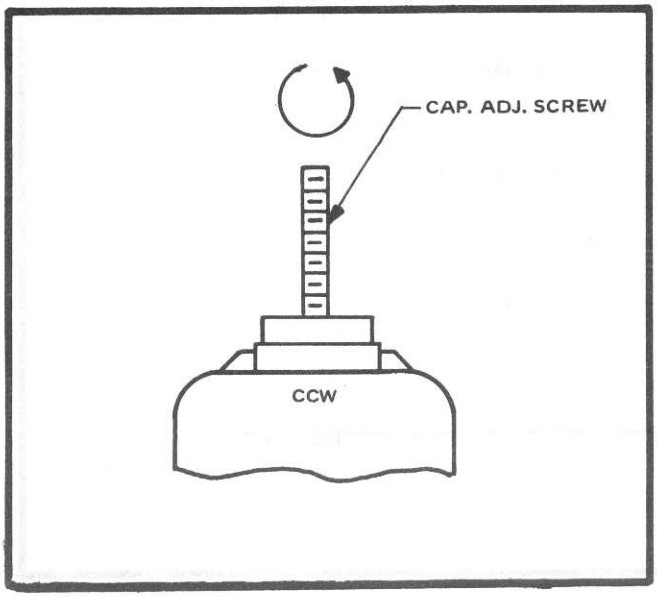



Figure 5.4 Vacuum Variable Capacitor (C-Max)

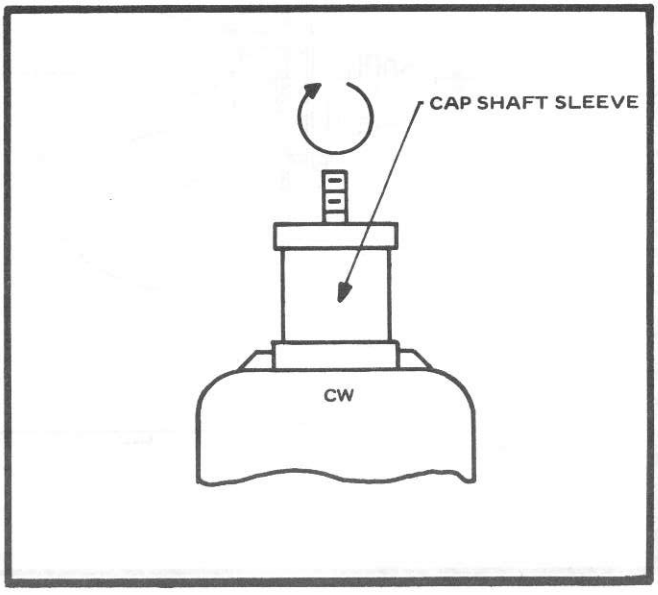



Figure 5.5 Vacuum Variable Capacitor (C-Min)

**CAUTION**

*The transmitter and the AC power will be applied to the coupler for the following steps. Be careful to avoid the high voltages within the coupler.*

12)Make sure that the Tx inhibit is in the enabled position and the transmitter is set for a low operating frequency. Turn all power back on.

13)The neon light, fault LED, and Tx inhibit LED on the connector board should be on. Also, both LED BUS indicators on the power supply board should be lit and the fan should be running.

14)Push the tune pushbutton and the inductor and the variable capacitor should go to the home position. Turn off the AC switch.

15)Using the cramolin paste, lubricate the capacitor adjustment screw (see Figure 5.4) and the variable inductor shaft.

16)Turn the AC switch back on, put the Tx inhibit switch to normal and tune the coupler at a frequency in the 20-30 Mhz range.

17)After the coupler goes ready, turn the AC off and the Tx inhibit to enable.

18)The capacitor should be towards the C-Min position (see Figure 5.5). Lubricate the sleeve with the cramolin liquid.

19)Turn the AC back on, place the Tx inhibit to normal, and latch the cover in place back on the case.

5.5.3 Coupler Adjustments

5.5.3.1 Capacitor C-Min and C-Max Adjust

Refer to Figure 5.2 for the adjustment locations and Figures 5.4 and 5.5 for positioning information.

1) Loosen the two screws on the motor side of the flexible coupling to the capacitor.

2) Loosen the C maximum adjustment screw away from S1. Hand rotate the capacitor shaft counterclockwise until the plunger is

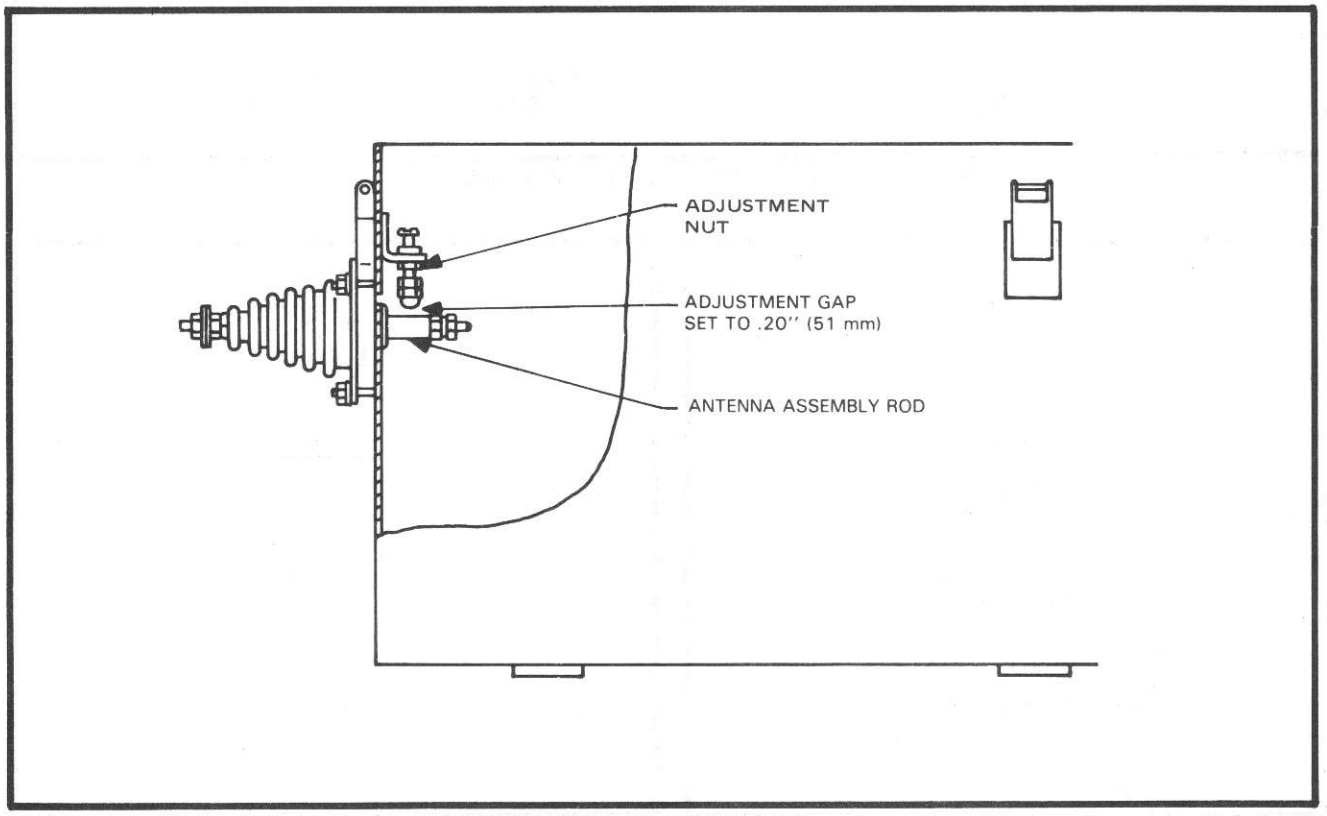



**Figure 5.6 Ball Gap Adjustment**

all the way into the body of the capacitor and the actuator is flush against the capacitor body. Do not use the decoder disk to rotate the shaft. Back the plunger out about 1 turn and adjust the limit switch adjustment screw to just close the switch. A switch closure may be observed by a distinct clicking sound or by an open circuit reading on an ohmmeter connected between terminal 1 of the switch and chassis ground. Tighten down the adjustment screw and back the plunger out until the switch opens. Rotate the shaft counterclockwise again until the switch closes. There should be a small amount of play between the actuator and capacitor body of about .05 inches (1-2 mm). Read just if necessary.

3) From the maximum capacitance position (plunger in and C maximum switch just closed), rotate the shaft 23 1/2 turns in the clockwise direction. Set the other adjustment screw to just close the switch. Ohmmeter connections to this switch are also between terminal 1 and chassis ground. (This adjustment is not as critical as that for the C maximum limit.)

5.5.3.2 Ball Gap Adjustment

Make sure that the spacing on the ball gap shown in Figure 5.6 is .20 inches (51 mm). If not, loosen the adjustment nut and turn the screw shaft until the acorn nut is the proper distance from the spacer. Carefully tighten the adjustment nut to secure the adjustment.

5.5.3.3 RF Module Adjustment

**NOTE**

*Do not adjust RF Module unless it is definitely determined that it is defective or misaligned.*

The RF module contains three adjustments - forward and reflected power, phase, and magnitude. These are very critical voltage adjustments that affect the tuning accuracy of the MSR-4030 Antenna Coupler. A flat-bladed and insulated alignment tool (see Section 5.2.2) is required for the following alignment steps:

1) Remove the RF module from the main chassis.
2) Remove the top and side covers from the module chassis.
3) Remove the lugged wire from E6 and hook up the test set-up as shown in Figure 5.7.
4) Apply 100 watts of RF at 15 MHz into J17.
5) Adjust C22 for a DC null (0 VDC) on Pin No. 12.
6) Adjust R18 for a DC null on Pin No. 6. If a compensating capacitor is not available for the cable assembly (Figure 5.8), adjust the R18 for −75 mV DC instead of the DC null.
7) Adjust C4 for 0 VDC at Pin No. 16.
8) Check Pin No. 12 for 0 VDC ±150 mV at 2 MHz and 25 MHz.
9) Check Pin No. 6 for 0 VDC ±150 mV at 2 MHz and 25 MHz.
10) Check Pin No. 16 for less than 75 mV at 2, 15, and 25 MHz. Readjust as necessary.
11) Check Pin No. 18 for 4-5 VDC at 2, 15, and 25 MHz.
12) Unhook the test set-up, rehook T1 to E6, replace the covers, and reinstall the RF module into the main chassis.

## 5.6 COUPLER MOTHER BOARD

The MSR-4030 uses a mother board to connect all circuit boards and discrete wiring together. It is a printed circuit board that is located underneath the main chassis. This circuit board provides connectors to plug-in and interconnect five boards to each other and to external wiring. The external (above chassis) wiring is terminated into three plugs and connected into the mother board thru three PC mounted connectors. Another connection is provided to interconnect the connector board (601164-536-001) to the mother board through a ribbon cable.

Since the mother board is only used for interconnection, it has no active parts. To identify these point to point connections, use the following four charts for any troubleshooting that involves the mother board.

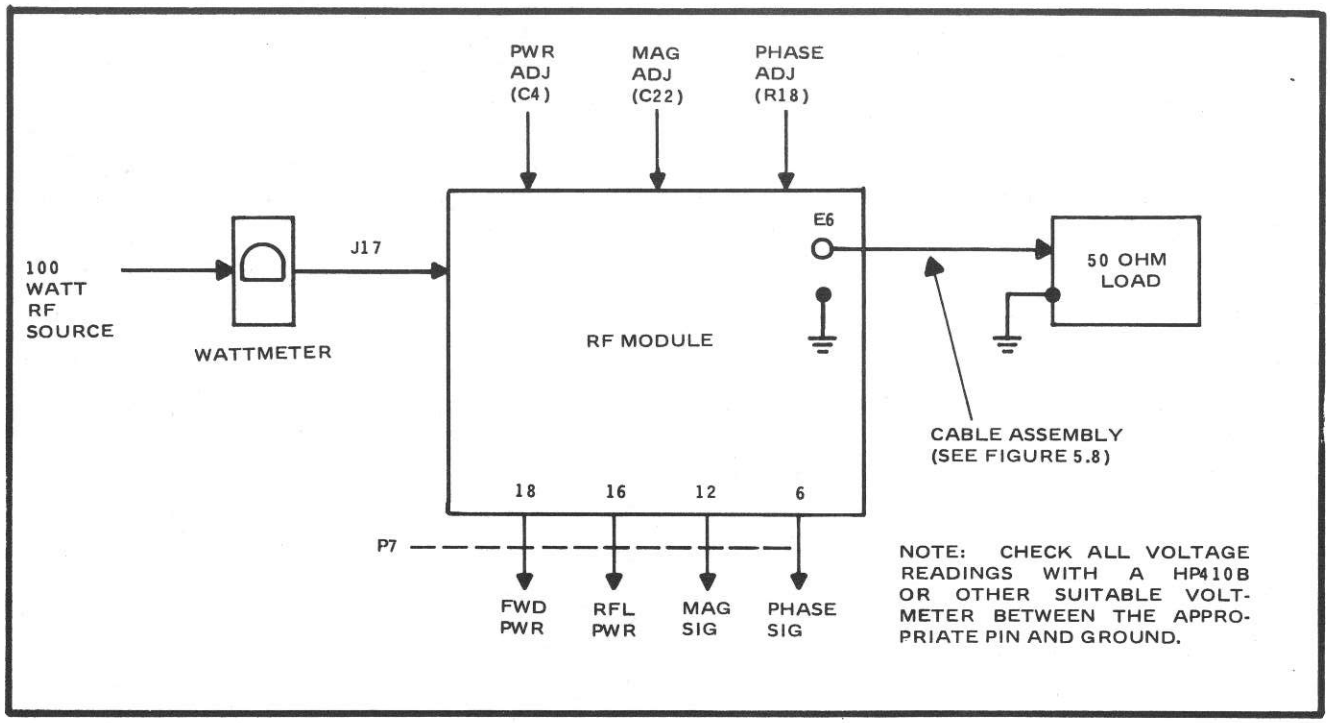



**Figure 5.7 RF Module Test Set-Up**

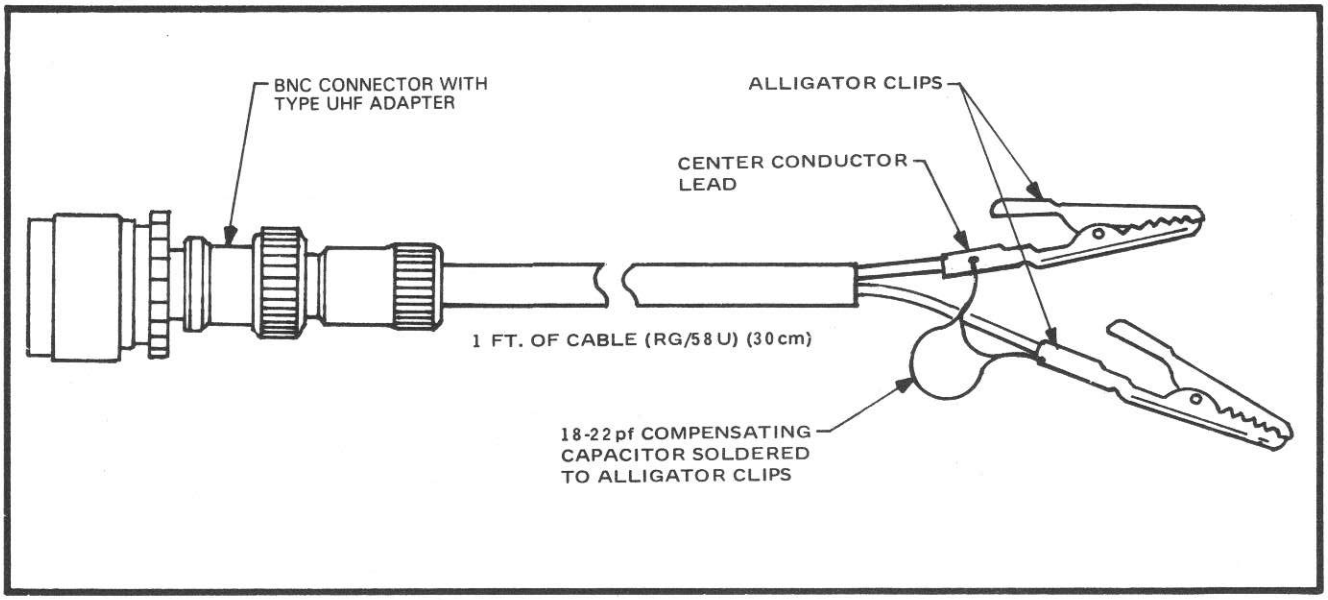



**Figure 5.8 RF Module Cable Assembly**

## MOTHER BOARD CONNECTOR/PIN NUMBERS

| SIGNAL NAME | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | P1 | P2 | P3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | 9 | 1 | 41 | 1 | 7 | 1 | 1 | 10 | 3 | 1 | 1 | E |
| GND | 25 | - | 42 | 2 | 10 | 2 | 2 | 7 | 4 | 2 | 2 | F |
| GND | - | 3 | 43 | 3 | 1 | 3 | 39 | 11 | 7 | 19 | 3 | H |
| GND | - | 4 | 44 | 4 | 4 | 4 | 40 | 1 | 5 | 20 | 4 | J |
| GND | - | 41 | - | 5 | - | 35 | 41 | 4 | - | - | - | K |
| GND | - | - | - | 6 | - | 36 | 42 | - | - | - | - | L |
| GND | - | 43 | - | - | - | 37 | 43 | - | - | - | - | 10 |
| GND | - | 44 | - | - | - | 38 | 44 | - | - | - | - | - |
| GND | - | - | - | - | - | 39 | - | - | - | - | - | - |
| GND | - | - | - | - | - | 40 | - | - | - | - | - | - |
| GND | - | - | - | - | - | 41 | - | - | - | - | - | - |
| GND | - | - | - | - | - | 42 | - | - | - | - | - | - |
| GND | - | - | - | - | - | 43 | - | - | - | - | - | - |
| GND | - | - | - | - | - | 44 | - | - | - | - | - | - |
| O.T.OVERRIDE | 1 | - | - | 35 | - | - | - | - | - | - | - | - |
| TXINT (N/C) | 19 | - | - | 15 | - | - | - | - | - | - | - | - |
| ONES CH. 2 | 3 | - | - | 26 | - | - | - | - | - | - | - | - |
| | - | - | - | - | - | - | - | - | - | - | - | - |
| O.T. LED | 5 | - | - | 36 | - | - | - | - | - | - | - | - |
| TENS CH4 | 6 | - | - | 17 | - | - | - | - | - | - | - | - |
| RFL PWR MTR | 7 | - | - | - | - | - | - | - | - | - | 5 | - |
| RFL PWR MTR | - | - | - | - | - | - | - | - | - | - | 6 | - |
| TENS CH1 | 8 | - | - | 19 | - | - | - | - | - | - | - | - |
| BYPASS SW | 10 | - | - | 33 | - | - | - | - | - | - | - | - |
| TUN PB | 11 | - | - | 32 | - | - | - | - | - | - | - | - |
| GPS ELECT | 12 | - | - | 37 | - | - | - | - | - | - | - | - |
| TUNE/STORE PB | 13 | - | - | 38 | - | - | - | - | - | - | - | - |
| SURV SW | 15 | - | - | 34 | - | - | - | - | - | - | - | - |

**MOTHER BOARD CONNECTOR/PIN NUMBERS (CONTINUED)**

| SIGNAL NAME | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | P1 | P2 | P3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TX INT (N/O) | 4 | - | - | 16 | - | - | - | - | - | - | - | - |
| ONES CH 8 | 21 | - | - | 22 | - | - | - | - | - | - | - | - |
| KEY ENABLE | 23 | - | - | 12 | - | - | - | - | - | - | - | - |
| FORCE INHIBIT | - | - | 36 | - | - | - | - | - | - | - | - | - |
| FAULT LED | 27 | - | - | - | - | - | - | - | - | - | 13 | - |
| FAULT LED | - | - | - | - | - | - | - | - | - | - | 14 | - |
| FWD PWR MTR | 29 | - | - | - | - | - | - | - | - | - | 7 | - |
| FWD PWR MTR | - | - | - | - | - | - | - | - | - | - | 8 | - |
| ONES CH 1 | 31 | - | - | 28 | - | - | - | - | - | - | - | - |
| TUNE LED | 33 | - | - | - | - | - | - | - | - | - | 17 | - |
| TUNE LED | - | - | - | - | - | - | - | - | - | - | 18 | - |
| TENS CH2 | 34 | - | - | 20 | - | - | - | - | - | - | - | - |
| READY LED | 35 | - | 9 | - | - | - | - | - | - | - | 15 | - |
| READY LED | - | - | - | - | - | - | - | - | - | - | 16 | - |
| TENS CH 8 | 36 | - | - | 18 | - | - | - | - | - | - | - | - |
| ONES CH 4 | 37 | - | - | 24 | - | - | - | - | - | - | - | - |
| +5V - BSUP | 38 | - | 37 | - | - | 5 | - | - | - | - | - | - |
| +5V - BSUP | 40 | - | 38 | - | - | 6 | - | - | - | - | - | - |
| +5V - BSUP | - | - | 39 | - | - | 7 | - | - | - | - | - | - |
| +5V - BSUP | - | - | 40 | - | - | 8 | - | - | - | - | - | - |
| SILENT TUNE | 17 | 5,6 | - | 30 | - | - | - | - | - | - | - | - |
| ANTENNA MOD. | - | - | - | 13 | - | - | - | - | - | 3 | - | - |
| ANTENNA MOD. | - | - | - | - | - | - | - | - | - | 4 | - | - |
| KEY ENABLE | - | - | 35 | - | - | - | - | - | - | - | 19 | - |
| KEY ENABLE | - | - | - | - | - | - | - | - | - | - | 20 | - |
| $\overline{CS3}$ | - | 9 | 3 | - | - | - | - | - | - | - | - | - |
| A = B,L | - | 10 | - | 42 | - | - | - | - | - | - | - | - |
| WRITE ENABLE | - | 11 | - | 39 | - | - | - | - | - | - | - | - |
| ST CLOCK | - | 12 | - | 40 | - | - | - | - | - | - | - | - |
| A<B,L | - | 13 | - | 43 | - | - | - | - | - | - | - | - |
| $\overline{READ\ ENABLE}$ | - | 14 | - | 41 | - | - | - | - | - | - | - | - |
| $\overline{CS2}$ | - | 15 | 6 | - | - | - | - | - | - | - | - | - |
| $\overline{CS1}$ | - | 16 | 4 | - | - | - | - | - | - | - | - | - |
| A6 | - | 17 | 10 | - | - | - | - | - | - | - | - | - |
| A7 | - | 18 | 8 | - | - | - | - | - | - | - | - | - |
| A3 | - | 19 | 14 | - | - | - | - | - | - | - | - | - |
| A5 | - | 20 | 12 | - | - | - | - | - | - | - | - | - |
| FAULT′ | - | - | 7 | - | - | - | - | - | - | - | 10 | - |

## MOTHER BOARD CONNECTOR/PIN NUMBERS (CONTINUED)

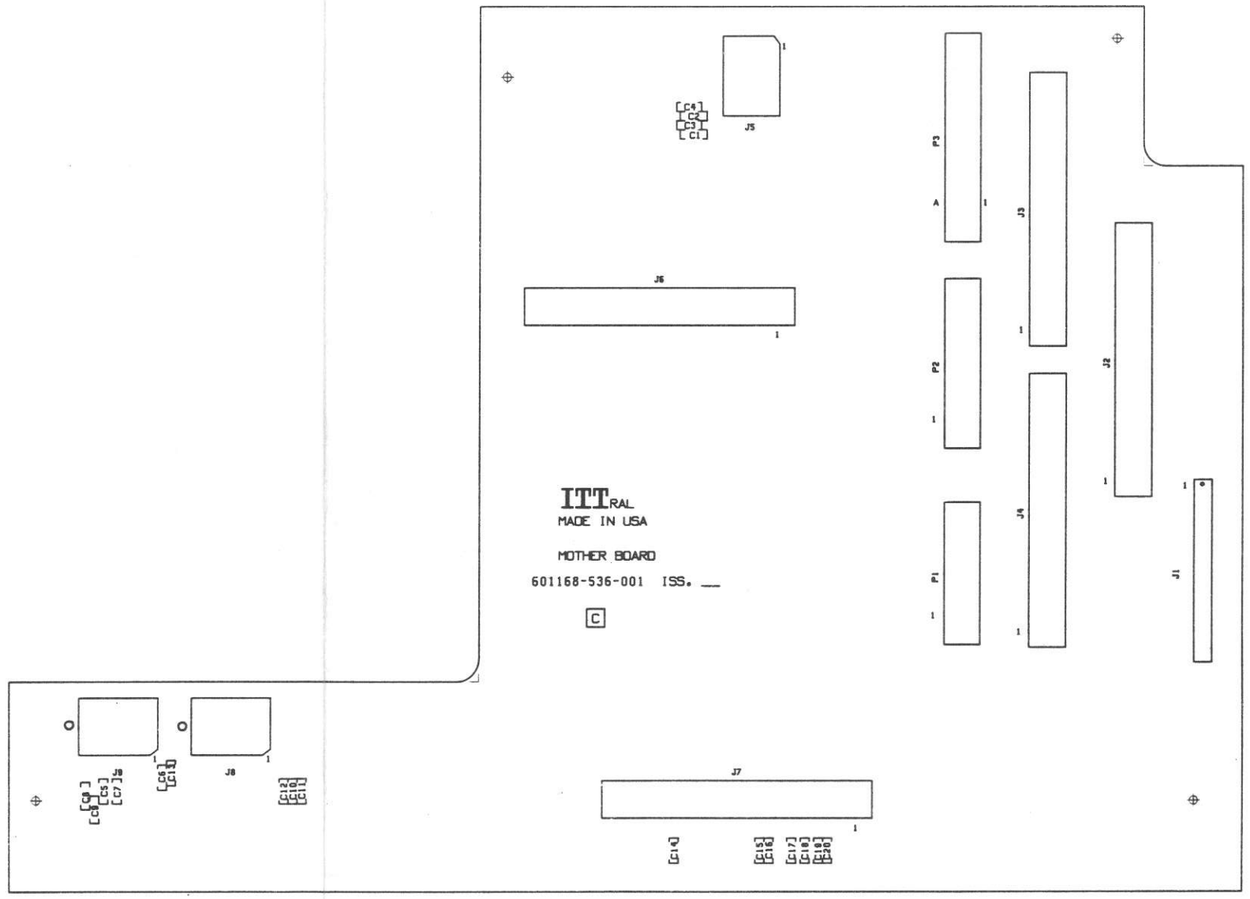
| SIGNAL NAME | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | P1 | P2 | P3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ANT. MOD WT | - | 21 | 16 | - | - | - | - | - | - | - | - | - |
| A>B,L | - | 22 | - | 44 | - | - | - | - | - | - | - | - |
| INPUT 1 | - | 23 | - | - | 3 | - | - | - | - | - | - | - |
| A4 | - | 24 | 18 | - | - | - | - | - | - | - | - | - |
| CCTR RESET | - | 25 | 19 | - | - | - | - | - | - | - | - | - |
| LCTR RESET | - | 26 | 17 | - | - | - | - | - | - | - | - | - |
| C INPUT 1 | - | 29 | - | - | - | - | - | - | 2 | - | - | - |
| L INPUT 2 | - | 30 | - | - | 2 | - | - | - | - | - | - | - |
| A<B,C | - | 31 | - | - | - | - | - | - | - | - | - | - |
| C INPUT 2 | - | 32 | - | - | - | - | - | - | 1 | - | - | - |
| A>B,C | - | 33 | 23 | - | - | - | - | - | - | - | - | - |
| A=B,C | - | 34 | 24 | - | - | - | - | - | - | - | - | - |
| 6TH CLK. CYCLE | - | 35 | 11 | - | - | - | - | - | - | - | - | - |
| ANT. MOD. READ | - | 36 | 26 | - | - | - | - | - | - | - | - | - |
| 5V-ASUP | - | 37 | - | - | 5 | 9 | - | - | 6 | - | - | - |
| 5V-ASUP | - | 38 | - | - | - | 10 | - | - | - | - | - | - |
| 5V-ASUP | - | 39 | - | - | - | 11 | - | - | - | - | - | - |
| 5V-ASUP | - | 40 | - | - | - | 12 | - | - | - | - | - | - |
| +28V UNREG | - | - | - | - | - | 21 | 3 | 3 | - | - | 23 | - |
| +28V UNREG | - | - | - | - | - | 22 | 4 | 6 | - | - | 24 | - |
| +28V UNREG | - | - | - | - | - | 23 | - | 9 | - | - | 25 | - |
| +28V UNREG | - | - | - | - | - | 24 | - | - | - | - | 26 | - |
| +28V UNREG | - | - | - | - | - | 25 | - | - | - | - | - | - |
| +28V UNREG | - | - | - | - | - | 26 | - | - | - | - | - | - |
| +28V UNREG | - | - | - | - | - | 27 | - | - | - | - | - | - |
| +28V UNREG | - | - | - | - | - | 28 | - | - | - | - | - | - |
| +15V UNREG | - | - | - | - | - | 15 | - | - | - | - | - | B |
| +15V UNREG | - | - | - | - | - | 16 | - | - | - | - | - | - |
| +15V UNREG | - | - | - | - | - | 17 | - | - | - | - | - | - |
| +15V UNREG | - | - | - | - | - | 18 | - | - | - | - | - | - |
| $\overline{\text{L MIN}}$ | - | - | 32 | - | - | - | - | - | - | - | - | 3 |
| $\overline{\text{L MAX}}$ | - | - | 31 | - | - | - | - | - | - | - | - | C |
| $\overline{\text{C MAX}}$ | - | - | 34 | - | - | - | - | - | 9 | - | - | 4 |

## MOTHER BOARD CONNECTOR/PIN NUMBERS (CONTINUED)

| SIGNAL NAME | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | P1 | P2 | P3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{\text{C MIN}}$ | - | - | - | - | - | - | - | - | 8 | - | - | D |
| | - | - | - | - | - | - | - | - | - | - | - | - |
| L RUN MIN | - | - | - | - | 12 | - | - | - | - | - | - | 6 |
| L RUN MAX | - | - | - | - | 11 | - | - | - | - | - | - | 7 |
| C RUN MAX | - | - | - | - | - | - | - | - | 11 | - | - | 8 |
| C RUN MIN | - | - | - | - | - | - | - | - | 12 | - | - | 9 |
| Ø SIG | - | - | - | 23 | - | - | 6 | - | - | 5 | - | - |
| Ø SIG | - | - | - | - | - | - | - | - | - | 6 | - | - |
| Ø REF | - | - | - | 21 | - | - | 8 | - | - | 7 | - | - |
| Ø REF | - | - | - | - | - | - | - | - | - | 8 | - | - |
| R REF | - | - | - | 25 | - | - | 10 | - | - | 9 | - | - |
| R REF | - | - | - | - | - | - | - | - | - | 10 | - | - |
| R SIG | - | - | - | 27 | - | - | 12 | - | - | 11 | - | - |
| R SIG | - | - | - | - | - | - | - | - | - | 12 | - | - |
| RFL PWR | - | - | - | 29 | - | - | 16 | - | - | 15 | - | - |
| RFL PWR | - | - | - | - | - | - | - | - | - | 16 | - | - |
| FWD PWR | - | - | - | 31 | - | - | 18 | - | - | 17 | - | - |
| FWD PWR | - | - | - | - | - | - | - | - | - | 18 | - | - |
| SURVEILLANCE | - | - | - | - | - | - | - | - | - | - | 11 | - |
| SURVEILLANCE | - | - | 5 | - | - | - | - | - | - | - | 12 | - |
| TUNE INIT | - | - | 15 | - | - | - | - | - | - | - | 21 | - |
| TUNE INIT | - | - | - | - | - | - | - | - | - | - | 22 | - |
| PAD RELAY/ATTN | - | - | - | - | - | - | 33 | - | - | - | - | 5 |
| PAD RELAY/ATTN | - | - | - | - | - | - | 34 | - | - | - | - | 5 |
| AUTO-HOME | 32 | - | - | 10 | - | - | - | - | - | - | - | - |
| OT INHIBIT | | | | | | | | | | | | |
| BCD INVERT | 39 | - | - | 9 | - | - | - | - | - | - | - | - |
| BYPASS R | - | - | - | 11 | - | - | - | 2 | - | - | - | - |
| BYPASS R | - | - | - | - | - | - | - | 5 | - | - | - | - |
| | - | - | - | - | - | - | - | - | - | - | - | - |
| ANT MOD RELAY | - | - | - | 7 | - | - | - | 8 | - | - | - | - |
| ANT MOD RELAY | - | - | - | 8 | - | - | - | - | - | - | - | - |
| L MIN | - | - | 30 | - | - | - | - | 12 | - | - | - | - |
| L MAX | - | - | 29 | - | 8 | - | - | - | - | - | - | - |

**MOTHER BOARD**
**(601168-536)**

| Symbol | Description | Part Number |
|---|---|---|
| C1,2,8,9 | Capacitor, .01 uF, 50V | 600272-314-002 |
| C3,4,5-7,10-20 | Capacitor, .1 uF, 50V | 600272-314-001 |
| J1 | Connector, 40P | 600174-608-024 |
| J2-4,6,7 | Connector, 22P | 600147-605-001 |
| J5,8,9 | Connector, 12P | 600237-608-001 |
| P1 | Connector, 10P | 600128-605-001 |
| P2 | Connector, 13P | 600128-605-002 |
| P3 | Connector, 10P | 600128-605-003 |
| — | Key Connector | 600219-227-003 |




**Mother Board Assembly**

CONNECTOR BD. HEADER (TO RIBBON CABLE ASSY)
MEMORY BD.
INTERFACE BD.
INDUCTOR CHASSIS ASS'Y.
CONTROL BD.
POWER SUPPLY BOARD
R.F. MODULE

J1
FAULT LED
TUNE LED
FWD PWR MTR
READY LED
BCD INVERT
AUTO-HOME
SILENT TUNE
RFL. PWR. MTR.
-TENS CH 8
-TENS CH 2
-ONES CH 1
-KEY ENABLE
-ONES CH 8
-TX. INT. (N/C)
-SURV. SW.
-TUNE/STORE P.B.
-GRP. SELECT
-TUNE P.B.
-BYPASS SW.
-TENS CH 1
-TENS CH 4
-O.T. LED
-TX. INT. (N/O)
-ONE'S CH 2
-OT OVERIDE
-ONE'S CH 4
GND
TO: J3, J6 & J15 +5V, -B SUP
C INPUT 1
C INPUT 2

J2
READ ENABLE
A<B, L
ST. CLOCK
WRITE ENABLE
A=B, L
A>B, L
A5
A3
A7
A6
CS1
CS2
CS3
ANT. MOD. READ
6TH CLOCK CYC.
A=B, C
A>B, C
LCTR RESET
CCTR RESET
A4
ANT MOD WT
L INPUT 2
INPUT 1
A<B, C

J3
READ ENABLE
A<B, L
ST. CLOCK
WRITE ENABLE
A=B, L
A>B, L
GND
L MAX
READY LED
C3 0.1
TENS CH. 8
TENS CH. 2
ONE'S CH. 1
KEY ENABLE
ONE'S CH. 8
TX. INT. (N/C)
SURV. SW.
TUNE/STORE PB.
GRP. SELECT
TUNE P.B.
BYPASS SW.
TENS CH. 1
TENS CH. 4
O.T. LED
TX. INT. (N/O)
ONE'S CH2
O.T. OVERIDE
ONE'S CH4
SURVEIL.
TUNE INIT.

J4
BCD INVERT
AUTO-HOME
GND
Ø SIG
Ø REF
R REF
R SIG
RFL PWR
FWR PWR
BYPASS R
ANT. MOD RELAY
GND
ANT. MOD
L INPUT 2
INPUT 1

J5
FAULT
TUNE
GND

FORCE INHIBIT
KEY ENABLE
C MIN
L MIN
L MAX
L MIN.
C4 0.1
GND
5V A SUP

P3
C MIN
C RUN MAX.
C RUN MIN.
L RUN MAX.
L RUN MIN.
PAD RELAY/ATTN.
+15V UNREG.
GND
+28V UNREG.

P2
GND
TUNE
GND
BYPASS R
ANT. MOD RELAY
ANT. MOD
L INPUT 2
INPUT 1

P1
Ø SIG
Ø REF
R REF
R SIG
RFL PWR
FWR PWR
GND

J6
+28V
TO: J1, J3, & J15 +5V, -B SUP
GND

J7
CAPS. C15-20 ARE .1uf
C14 .1
C20
C19
C18
C17
C16
C15
Ø SIG
Ø REF
R REF
R SIG
RFL PWR
FWR PWR
+28V
GND

INDUCTOR CHASSIS ASS'Y
CAPACITOR CHASSIS ASS'Y.
ANT. MOD.
BYPASS R
+28V
GND

J8
C MIN.
C RUN MAX.
C RUN MIN.
C10 0.1
C11 0.1
C12 0.1
C13 0.1
C5 0.1
C INPUT 1
C INPUT 2
GND

J9
C7 0.1
C8 0.1
C9 0.1
C6 0.1
GND

Mother Board Schematic

## 5.7 CAPACITOR CHASSIS ASSEMBLY

### 5.7.1 General

The capacitor chassis assembly is an integral part of the MSR-4030. It contains C1, the series element of the basic series C, shunt L coupler tuning network. C1 is a 12-500 pf variable capacitor capable of handling the voltages required of a 1000 watt antenna coupler. In addition, an opticoupler board (601170-536-002) and a shaft driven disk are used to transmit location data to the MSR-4030 logic. In this way, the location of the variable capacitor as it tunes from 12-500 pf can be digitally tracked.

### 5.7.2 Tuning Capacitor

C1 is a 12-500 pf vacuum variable capacitor that is rated at 15 kilovolts. It is the series element in the coupler tuning network and is directly driven by a DC motor mounted on the capacitor chassis assembly. It is controlled by a servo system located on the control board (601282-536-001) which moves the capacitor according to the phase of the tuning network. The capacitor is provided with two plunger activated switches that act as limit stops to prevent capacitor damage. These switches are S1 for the "C-Max" limit (500 pf) and S2 for the "C-Min" limit (12 pf).

### 5.7.3 Opticoupler Board

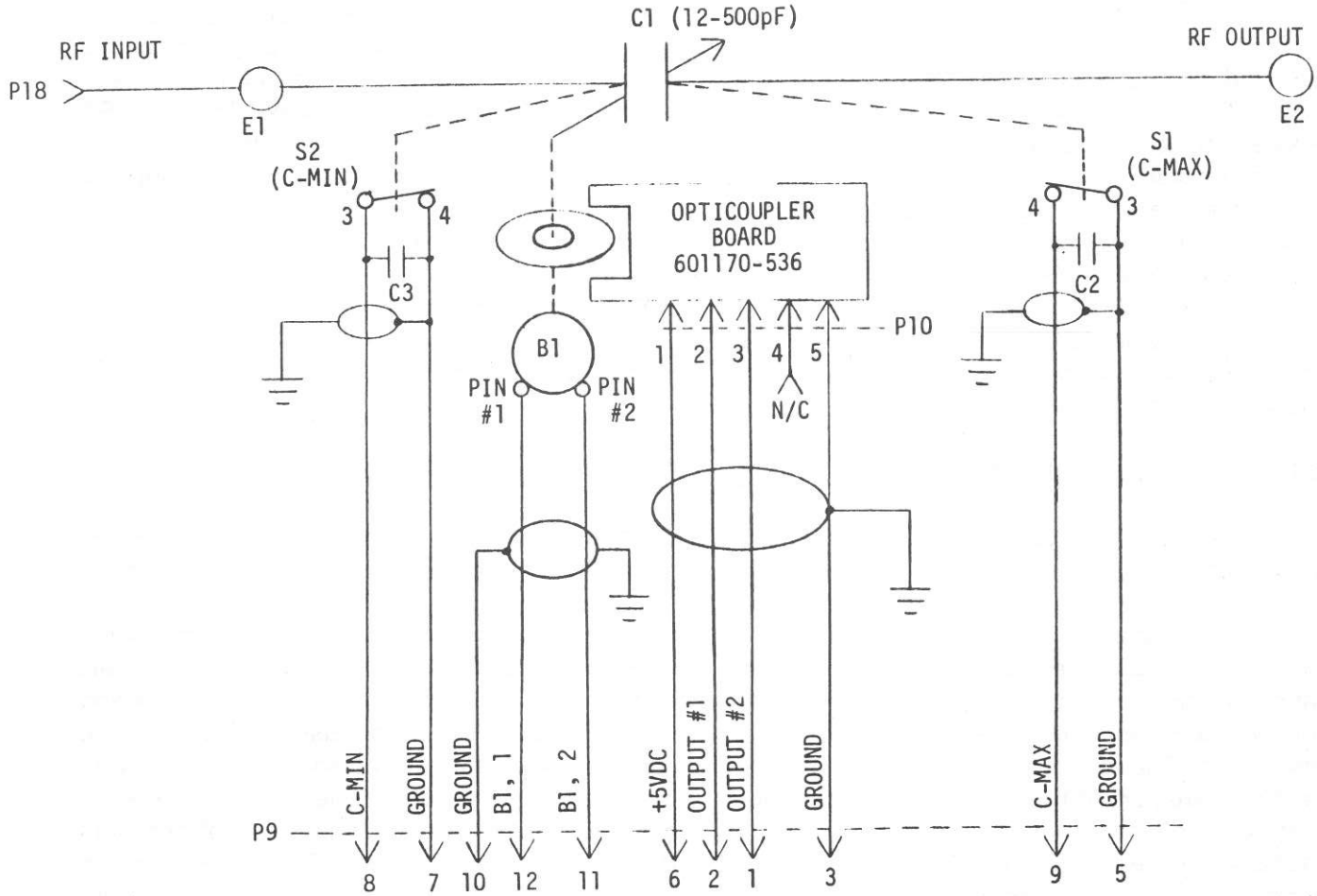
See Section 5.14.

### 5.7.4 Input and Output Connections

RF input into the capacitor chassis assembly is through P18 and the output is by way of terminal E2. The two motor connections and the wiring for the limit switches are routed through the main cable bundle and are terminated in the plug P9. The opticoupler board is hooked up through plug P10 which also goes into the main cable bundle and is terminated at P9. P9 is a 12-Pin Molex plug used to connect the input/output connections of the capacitor chassis assembly to the coupler mother board (601168-536-001).

### 5.7.5 Input and Output Specifications

| Pin | Input/Output | Function | Specification |
|---|---|---|---|
| P9-1 | Output | Output No. 2 | Opticoupler Board pulsed waveform (J1-3) |
| P9-2 | Output | Output No. 1 | Opticoupler Board pulsed waveform (J1-2) |
| P9-3 | — | Ground | GND for Opticoupler Board (J1-5) |
| P9-4 | — | Ground | GND |
| P9-5 | — | Ground | GND for switch S1 (C-Max) |
| P9-6 | Input | +5 VDC | +5 VDC ±.3V to Opticoupler Board (J1-1) |
| P9-7 | — | Ground | GND for switch S2 (C-Min) |
| P9-8 | Output | C-Min | Disable = Ground, Enable = Open Circuit |
| P9-9 | Output | C-Max | Disable = Ground, Enable = Open Circuit |
| P9-10 | — | Ground | Shield GND for Motor B1 |
| P9-11 | Input | C-Run to Max | +28 VDC, C1 moving to maximum |
| P9-12 | Input | C-Run to Min | +28 VDC, C1 moving to minimum |
| P18 | Input | RF Input | |
| E2 | Output | RF Output | |




**CAPACITOR CHASSIS ASSEMBLY BLOCK DIAGRAM**

**CAPACITOR CHASSIS ASSEMBLY**
**(600355-713)**

| Symbol | Description | Part Number |
|---|---|---|
| B1 | Motor, Gear | 600023-387-002 |
| C1 | Capacitor, 12-500 pF, 15kV | 600382-713-001 |
| — | Insulated Coupling | 600106-240-001 |
| — | Encoder Disc Assembly | 600357-713-001 |
| C2,3 | Capacitor, .1uF, 50V | 600226-314-008 |
| P9 | Connector, 12 Pin | 600357-606-001 |
| — | Male Pin (P9) | 600237-230-002 |
| — | Female Pin (P9) | 600223-230-002 |
| P10 | Connector, 5 Pin | 600283-606-005 |
| — | Pins, Connector (P10) | 600259-230-003 |
| P18 | RF Cable Assembly | 600474-540-001 |
| S1,2 | Microswitch | 600275-616-001 |

## 5.8 INDUCTOR CHASSIS ASSEMBLY

### 5.8.1 General

The Inductor Chassis Assembly is an integral part of the MSR-4030. It contains L1, the shunt element of the basic series C, Shunt L coupler tuning network. L1 is a 50 uh variable inductor capable of handling the voltages required of a 1000 watt antenna coupler. In addition, an Opticoupler Board (601170-536-001) and a shaft driven disk are used to transmit location data to the MSR-4030 logic. In this way, the location of the variable inductor can be digitally tracked as it tunes.

### 5.8.2 Variable Inductor

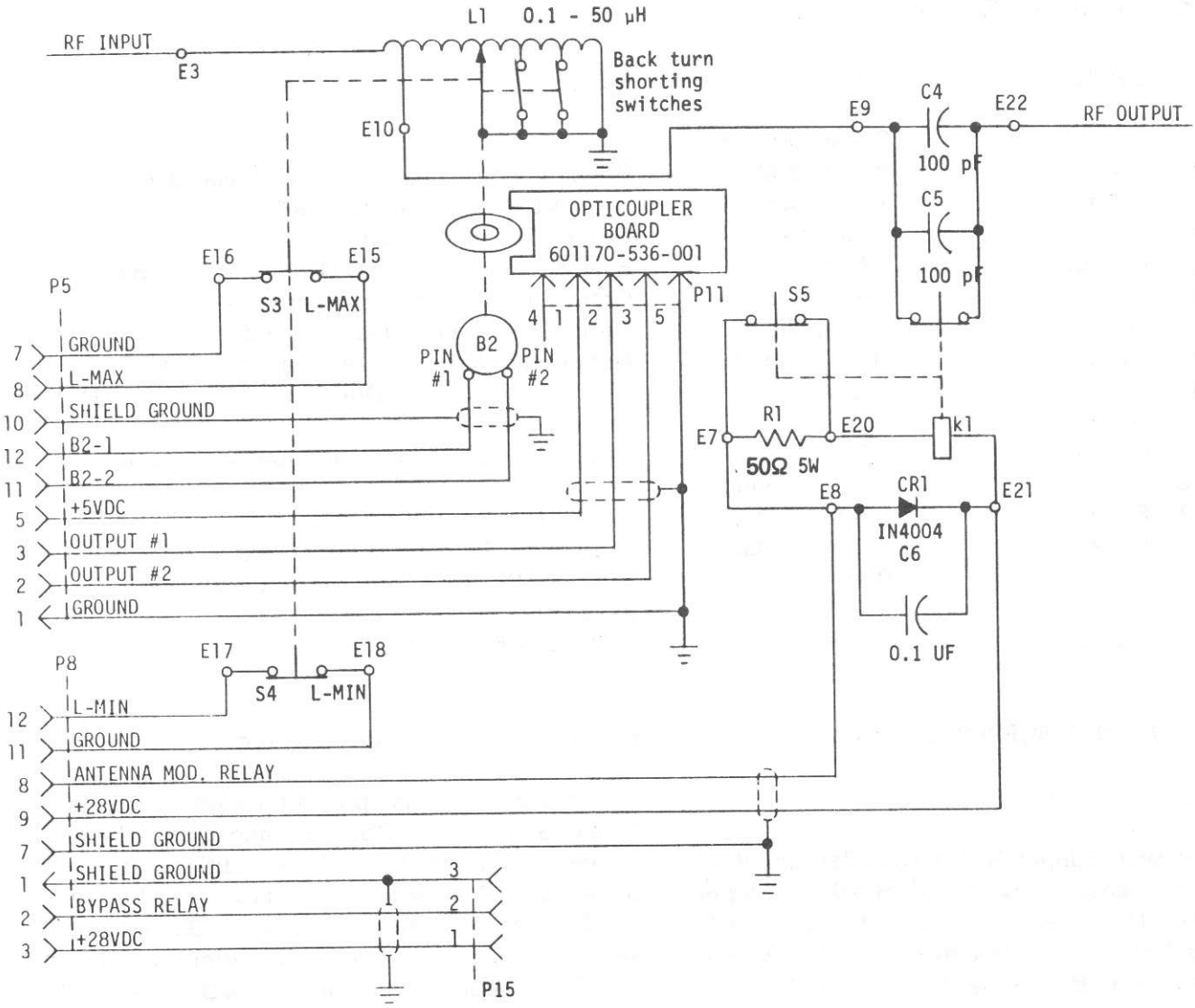
L1 is a 50 uh, rotary-tuned inductor with a Q of 175 at 2 MHz. It is the shunt L element of the tuning network that controls the impedance matching of the antenna. It is tapped at the "Hot" end to provide a small amount of inductance to the series tuning capacitor, to make the vacuum capacitor "Look" much larger at resonance. The inductor contains two shorting bars that are part of the "Back Turns Shorting" feature of this coil; they are strategically placed to short out the unused turns of the inductor in order to reduce unwanted voltage build-up. The variable inductor is directly driven by a shaft coupled D.C. motor that is mounted on the chassis holding the Inductor Assembly. It is controlled by a Servo system located on the Control Board (601282-536-001) which moves the inductor according to the magnitude of the tuning network. The inductor is provided with two plunger activated switches that act as limit stops to prevent inductor damage. These switches are S3 for the "L-Max" limit and S4 for the "L-Min" limit. "L-Min" is the "Homing" or minimum inductance point on the inductor while "L-Max" is towards the "Tuning" or maximum inductance of the variable inductor.

### 5.8.3 Opticoupler Board

See Section 5.14.

### 5.8.4 Antenna Modification Capacitors

C4 and C5 are 100 pf capacitors that are wired in parallel on the inductor chassis. They are in series with the coupler tuning network and are automatically switched into the network when needed for additional tuning capacitance. (This happens whenever the conditions of L-Max and C-Max occur simultaneously or when the capacitor element returns to its home position more than once during a tune cycle.) Relay K1 is made up of a solenoid operated set of contacts that short across C4 and C5. Whenever K1 is energized, the relay arm opens the contact across the capacitors and in turn pushes switch S5 open. This places R1 in series with the coil winding and reduces the coil current for sustained operation.




**INDUCTOR CHASSIS ASSEMBLY SCHEMATIC**

**INDUCTOR CHASSIS ASSEMBLY**
**(600360-713)**

| Symbol | Description | Part Number |
|---|---|---|
| — | Insulated Shaft Coupling | 600106-240-001 |
| — | Opticoupler Board Assembly | 601170-536-001 |
| — | Inductor Encoder Disc Assy | 600358-713-001 |
| — | Contact, Bottom (C4,5) | 600249-608-001 |
| — | Contact, Top (C4,5) | 600250-608-001 |
| — | Mounting Plate (C4,5) | 600433-705-001 |
| B2 | Motor, Gear | 600023-387-002 |
| C4,5 | Capacitor, 100 pF, 15KV | 600244-314-007 |
| C6 | Capacitor, .1 uF, 50V | 600272-314-001 |
| CR1 | Diode, 1N4004 | 600011-416-002 |
| L1 | Inductor, Variable | 600217-376-001 |
| P5,8 | Connector, 12P | 600357-606-001 |

| Symbol | Description | Part Number |
|---|---|---|
| — | Male Pins (P5,8) | 600237-230-002 |
| — | Female Pins (P5,8) | 600223-230-002 |
| P11 | Connector, 5P | 600283-606-005 |
| — | Pins, Connector (P11) | 600259-230-003 |
| P15 | Connector, 3P | 600197-606-001 |
| — | Pins, Connector (P15) | 600229-230-001 |
| — | Contact, Spring (C4,5) | 600248-608-001 |
| — | Solenoid Contact Arm | 600026-619-001 |
| — | Solenoid, Rotary | 600028-387-001 |
| — | Gnd Strap, Ant. Insulator | 600244-608-001 |
| — | Gnd Strap, L1 to Case | 600517-540-001 |
| R1 | Resistor, 50 ohms, 5 watts | 600096-340-500 |
| S5 | Microswitch | 600275-616-001 |

5.8.5 Input and Output Specifications

| Pin | Input/Output | Function | Specification |
|---|---|---|---|
| P8-7 | — | Shield Ground | — |
| P8-8 | Input | Antenna Mod. | Provides Logic ground to close relay K1 |
| P8-9 | Input | K1 Voltage | +28 VDC (±5V) to relay K1 |
| P8-11 | — | Ground | Ground for S2 (L-Min) |
| P8-12 | Output | L-Min | Enable = Open Circuit, Disable = Ground |
| P5-1 | — | Ground | Ground for Opticoupler Board (J1-5) |
| P5-2 | Output | Output No. 2 | Opticoupler Board pulsed waveform (J1-3) |
| P5-3 | Output | Output No. 1 | Opticoupler Board pulsed waveform (J1-2) |
| P5-5 | Input | +5 VDC | +5 VDC (±.3V) to Opticoupler Board (J1-1) |
| P5-7 | — | Ground | Ground for S1 (L-Max) |
| P5-8 | Output | L-Max | Enable = Open Circuit, Disable = Ground |
| P5-10 | — | Shield Ground | — |
| P5-11 | Either | L-Run to Min | +28 VDC, L1 moving to L-Min |
| P5 | Either | L-Run to Max | +28 VDC, L1 moving to L-Max |
| E3 | Input | RF Input | Provides RF input from capacitor chassis assembly |
| E22 | Output | RF Output | Provides RF output to Antenna |

## 5.9 POWER SUPPLY BOARD

5.9.1 General

The Power Supply Board provides all of the voltages required by the MSR-4030 Coupler. These DC voltage outputs are +28 unregulated, +15 unregulated, +5 "A" supply, and +5 "B" supply. The +28 VDC and the +15 VDC outputs are fused and have LED BUS indicators that light when the voltage is present. In addition, the +5 VDC outputs are crowbar protected and the 5 volt regulators are mounted on a heatsink for additional heat dissipation.

5.9.2 +28 VDC Unregulated

20 VAC (nominal) is applied to the Power Supply Board across the AC terminals of CR1. CR1 is a full wave bridge rectifier that rectifies this AC voltage, which in turn is filtered by C1. This voltage is fused by F1 (6 amp) and indicated by DS1. R1 and R2 limit the current going to the LED indicator light. The +28 VDC goes out on Pins 21-28 of P6 where it is filtered for RF by C11.

5.9.3 +15 VDC Unregulated

12 VAC (nominal) is applied through J14, Pins 1 and 3 to CR2, CR6, CR7 and CR8. These diodes make a full wave bridge rectifier that rectifies this AC voltage, which is filtered by C2 and C3. This voltage is fused by F2 (3 amp) and indicated by DS2. R3 limits the current going to the LED indicator light. The +15 VDC goes out on Pins 15-18 of P6 where it is further filtered by C9 (for RF) and C10.

5.9.4 +5 VDC

The Power Supply Board has two +5 VDC outputs which share the current loads required by the MSR-4030. These two outputs are the +5V "A" supply and the +5 "B" supply, both of which are electrically identical. The +15 VDC is supplied to U1 and U2 (5 volt regulators) and filtered for stability at the regulator inputs by C4. The +5 supply has outputs at Pins 9-12 of P6 and is filtered by C7 (for RF) and C8. The +5V "B" supply has outputs at Pins 5-8 of P6 and is filtered by C5 (for RF) and C6.

### 5.9.5 +5 VDC Crowbar Circuit

Both of the +5 VDC outputs are protected against over-voltage by a crowbar circuit that shorts F2 to ground, shutting off the +15 VDC supply to the regulators. The 5V "A" supply is sampled by CR4 with R4 providing a stable Zener current path. Whenever the BUS voltage increases enough to cause CR4 to conduct, CR10 is biased and causes the SCR Q1 to fire when the gate voltage reaches .65 volts. R6 limits the gate current to Q1. The protection circuit for the 5V "B" supply is identical to that for the "A" supply. Diodes CR9 and CR10 allow each circuit to fire SCR Q1 independently. This blows fuse F2, which protects the +5 VDC outputs from an over-voltage condition.

### 5.9.6 AC Input Voltages

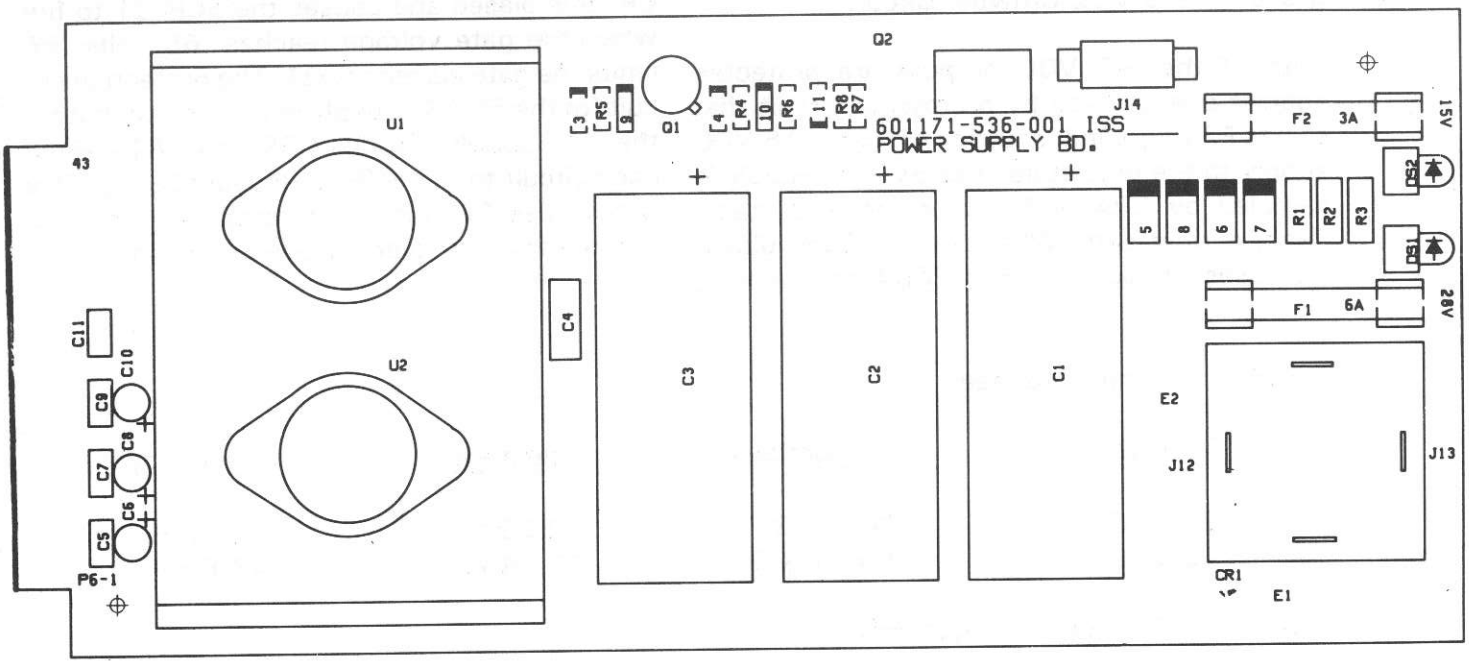
| Voltage | Pin Numbers | Tolerance | Frequency |
|---|---|---|---|
| 20 VAC | J12, J13 | 19-23 VAC | 48-63 Hz |
| 12 VAC | J14, 1 & 3 | 11-14 AC | 48-63 Hz |

### 5.9.7 DC Output Voltages (P6)

| Voltage | Pin Numbers | Tolerance | Load |
|---|---|---|---|
| +28V | 21-28 | 22.0-33.0V | 1 Amp |
| Unregulated | | 23.0-34.0V | Unloaded |
| +15V | 15-18 | 11.0-19.0V | 100 ma |
| Unregulated | | 12.0-20.0V | Unloaded |
| +5V | 9-12 | 4.7-5.3V | 500 ma |
| "A" supply | | 4.7-5.3V | Unloaded |
| +5V | 5-8 | 4.7-5.3V | 500 ma |
| "B" supply | | 4.7-5.3V | Unloaded |

### 5.9.8 Output Ripple

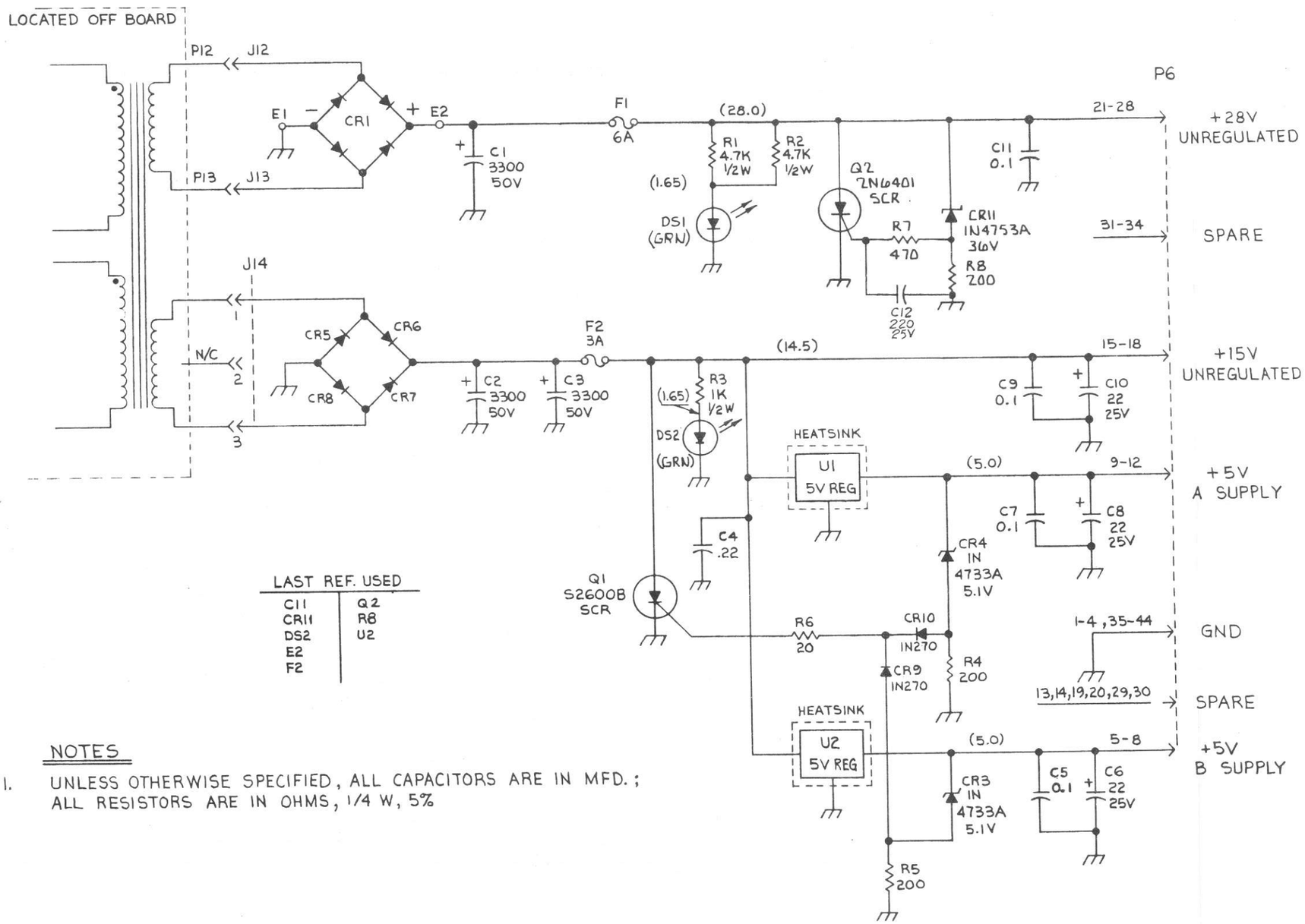
| Voltage | Max. Ripple (p-p) | Load |
|---|---|---|
| +28V Unregulated | 1.5V | 1 Amp |
| +15V Unregulated | 1.5V | 100 ma |
| +5V "A" supply | 15 mv | 500 ma |
| +5V "B" supply | 15 mv | 500 ma |




POWER SUPPLY BOARD SCHEMATIC

**POWER SUPPLY BOARD**
**(601171-536)**

| Symbol | Description | Part Number |
|---|---|---|
| C1,2,3 | Capacitor, 3300 uF, 50V | 600259-314-116 |
| C4 | Capacitor, .22 uF, 100V | 600204-314-019 |
| C5,7,9,11 | Capacitor, .1 uF, 50V | 600226-314-008 |
| C6,8,10 | Capacitor, 22 uF, 25V | 600297-314-016 |
| C12 | Capacitor, 220 uF, 25V | 600297-314-041 |
| CR1 | Bridge Rect. | 600028-416-001 |
| CR3,4 | Diode, 1N4733A, 5.1V | 600006-411-006 |
| CR5,8 | Diode, MR851 | 600042-416-001 |
| CR9,10 | Diode, 1N270 | 600052-410-001 |
| CR11 | Diode, 1N4752A, 33V | 600006-411-055 |
| DS1,2 | Led, Green | 600043-390-001 |
| F1 | Fuse, 6A | 600004-396-017 |
| F2 | Fuse, 3A | 600004-396-014 |
| Q1 | SCR, 7A, S2600B | 600051-416-001 |
| Q2 | SCR, 16A, 2N6401 | 600055-416-001 |
| R1,2 | Resistor, 4.7K, 1/2W, 5% | 647014-341-205 |
| R3 | Resistor, 10K, 1/2W, 5% | 610014-341-205 |
| R4,5,7 | Resistor, 200, 1/4W, 5% | 600004-341-075 |
| R6 | Resistor, 20, 1/4W, 5% | 620094-341-075 |
| R8 | Resistor, 470, 1/4W, 5% | 647004-341-075 |
| U1,2 | Reg., LM309K | 600064-415-001 |




| LAST REF. USED | |
|---|---|
| C11 | Q2 |
| CR11 | R8 |
| DS2 | U2 |
| E2 | |
| F2 | |

NOTES

1. UNLESS OTHERWISE SPECIFIED, ALL CAPACITORS ARE IN MFD.; ALL RESISTORS ARE IN OHMS, 1/4 W, 5%

POWER SUPPLY BOARD SCHEMATIC

5.9.9 Crowbar Specifications

Both the 5 volt "A" supply and the "B" supply outputs are protected from an over-voltage condition.
When either output reaches a minimum voltage of 5.5-7.5 VDC, Q1 will conduct and blow fuse F2.

5.9.10 +28V Crowbar Circuit
Overvoltage protection for this supply voltage is provided by CR11, R7, R8, and Q2. Should the supply voltage become excessive, CR11 will begin conducting through R8. As the supply voltage approaches 38 volts, R7 will supply enough gate voltage to Q2 causing it to conduct and blow F1.

## 5.10 R.F. MODULE

5.10.1 General

The RF Module contains the RF Board (601169-536) is an aluminum chassis with an RF input at J17 on the circuit board and an RF output at J18 on the chassis. This module is a series connection between the RF connector to the case and the input to the capacitor chassis assembly (600355-713-001). It is designed to withstand the RF voltage encountered in a 1 kW antenna coupler in the 1.6-30 MHz frequency range. The RF Module contains five separate elements - a six DB attenuator pad, power detectors, magnitude detector, phase detector, and a 4 to 1 impedance transformer.

When the antenna has been properly tuned or matched by the reactive elements in the antenna coupler, the coupler will present a purely resistive 50 ohm load to the transmitter. If the antenna is not properly tuned, the impedance at this point may be something other than 50 ohms and either inductive or capacitive. The detector circuits on the RF board sense these conditions and direct the coupler's tunable elements to achieve a proper match. The 6 dB pad is used during coupler tuning to limit reflected power and the 4 to 1 transformer is used to transform the nominal 50 ohm input to 12.5 ohm output.

5.10.2 6 dB Attenuator Pad

The 6 dB pad on the RF Board consists of six 75 ohm/45 watt non-inductive resistors (R1-R6) and a high voltage relay (K1). They are used in a TT-Pad configuration that gives approximately 6 dB of loss and limits worst case VSWR. The pad has a total power handling capability of 270 watts.

5.10.3 Forward and Reflected Power Detectors

The function of the power detector is to provide voltage samples of forward and reflected power for metering purposes and for use with the VSWR comparator on the control board.

Voltage samples proportional to and in phase with the line voltage are made by C5/C6 for the Forward Power line and by C3/C4/L9/C27 for the Reflected Power line.

Transformer T1 samples the line current and produces outputs through CR3 and CR4. When the line impedance is 50 ohms resistive, the voltage sample from C5/C6 will add in phase with the current sample through CR3 to produce an output on the Forward Power line P7-18. The voltage sample from C3/C4/L9/C7 will also add with the current sample through CR4. However, no output will result because the voltage and current sample will be 180 out of phase. This results in a minimum voltage on the Reflected Power line P7-16.

Whenever the line impedance is different from 50 + j0 ohms, a voltage on the Reflected Power line P7-16 will result.

R30-R33 form voltage dividers to scale the Power Detector outputs while L3/L4 and C16/C17/C25/C26 serve to remove RF from the error voltage on these lines.

5.10.4 Magnitude or R Detector

The function of the magnitude detector is to sense the resistive component of the line impedance and to provide a proportional DC out-

put to the servo system that will drive the variable inductor to achieve a resistive component of 50 ohms.

The detector circuit is constructed such that the antenna current induces a voltage in transformer T2. The combination of C2 with C22 and C8 form a divider which produces a voltage sample in phase with and proportional to the line voltage. L1 is provided for frequency compensation. This voltage is detected by CR6, peak filtered by C10, and will produce a positive voltage across R12 at the output. L2 is used strictly as a DC return path to ground. The voltage induced in T2 is such that when the line impedance is 50 ohms resistive the voltage across T2 is twice the amplitude and 180° out of phase with the voltage sample produced by the RF voltage divider. The vector sum of the outputs from T2 and the divider is detected by CR5, filtered by C9, and appears as a negative voltage across R11. Thus, when the line impedance is 50 ohms resistive, the positive voltage across R12 and the negative voltage across R11 are equal and opposite and the magnitude detector output on pin 12 will be at a null (zero volts), as in a tuned condition. If the load impedance is higher than 50 ohms, a lower antennna current will result causing a lower voltage across T2 and less negative voltage across R11. The output from the discriminator will then be positive and cause the servo system to drive the variable inductor toward minimum inductance. Likewise, if the load impedance is less than 50 ohms, a higher antenna current will result causing a higher voltage across T2 and more negative voltage across R11. The output from the detector will go negative and cause the servo system to drive the variable inductor toward minimum inductance.

### 5.10.5 Phase Detector

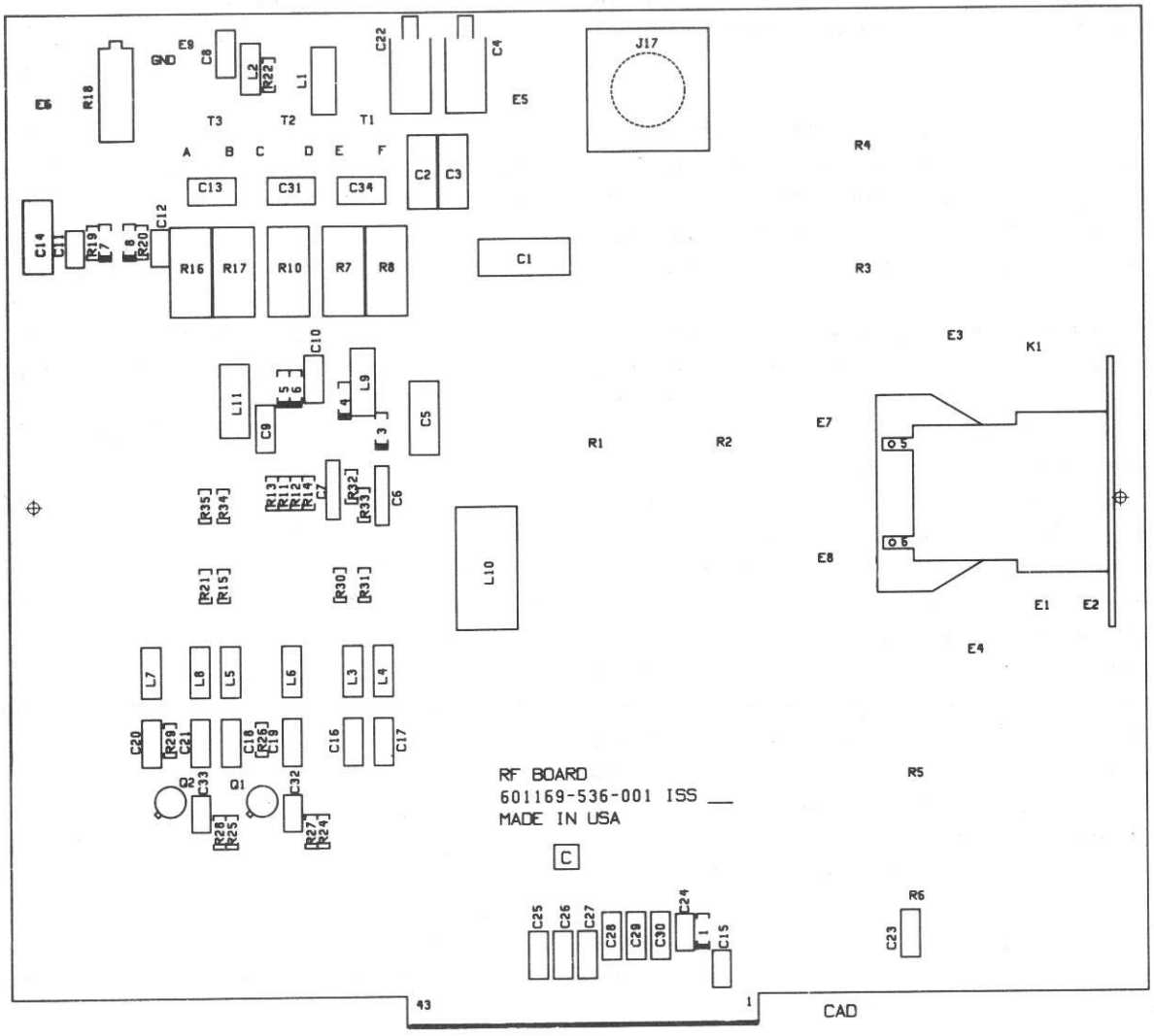
The function of the phase detector is to sense the reactive component and to provide a proportional DC output to the servo system that will drive the variable capacitor such that the condition is corrected.

The detector circuit is constructed such that the antenna current induces a voltage in transformer T3. The combination of C14 with L11, R34, and R35 form a divider that produces a reference voltage at the junction of R16 and R17 which is 90° out of phase with the line voltage. The vector sum of the reference voltage and the induced voltage in T3 are detected by CR8 and CR7, filtered by C12 and C11 respectively, and summed in potentiometer R18. R18 is adjusted such that the circuit is perfectly symmetrical.

When adjusted properly, the phase detector output on pin 6 will be at a null (zero volts) when the antenna impedance presents a purely resistive load, as in a tuned condition. If the load is capacitive, a positive output results and causes the servo system to drive the vacuum capacitor toward maximum capacitance. If the load is inductive, the output is negative and the vacuum capacitor is driven toward minimum capacitance.

### 5.10.6 Impedance Transformer

An impedance matching transformer, T1, is used at the output of the RF module to normally transform the 50 ohms RF input to a 12.5 ohms output. This lowered impedance provides a wider tuning range for the given L & C values used in the Antenna Coupler. The RF impedance transformer (650125-513-001) is mounted directly to the RF Module enclosure to provide thermal conduction for cooling.



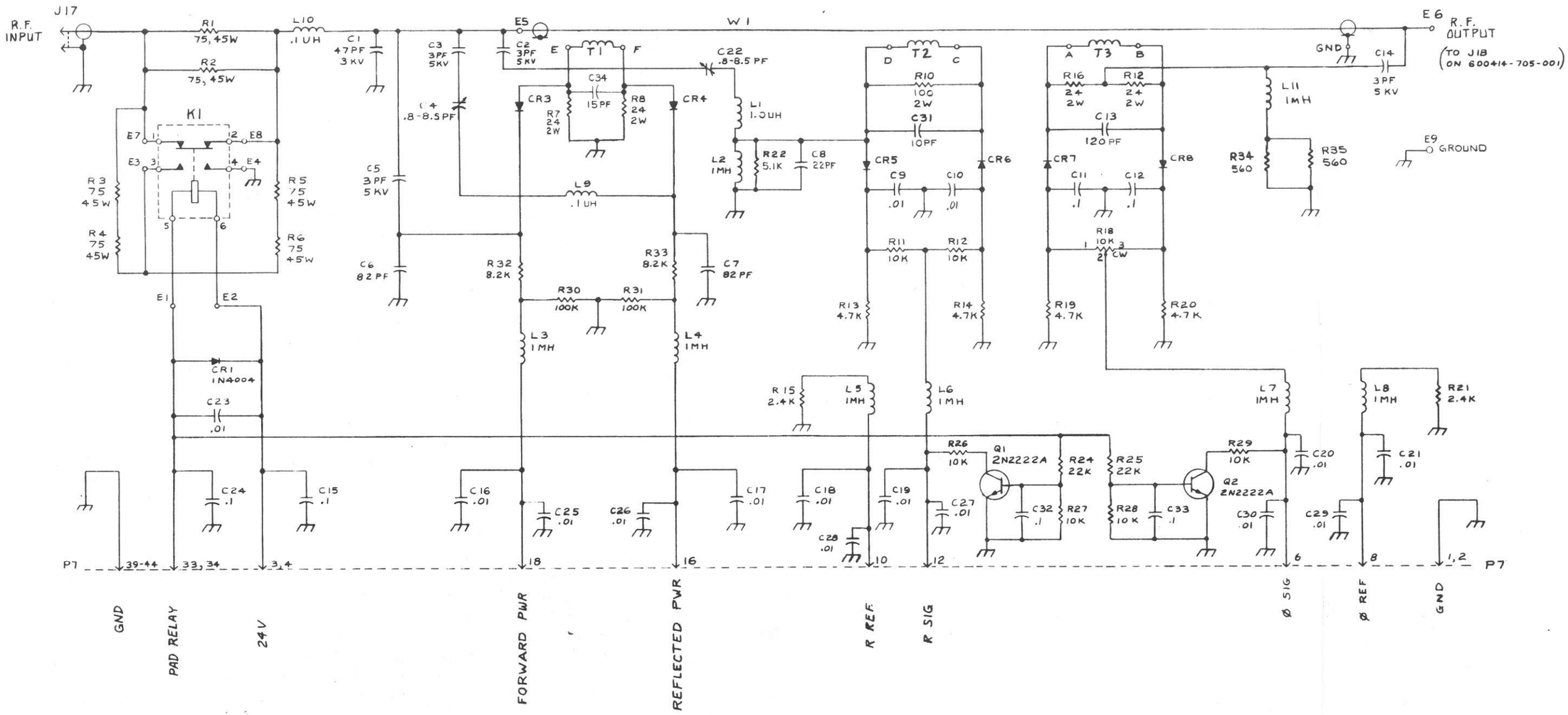

**RF BOARD**
**(601169-536)**

| Symbol | Description | Part Number |
|---|---|---|
| C1 | Capacitor, 47 pF/3 KV | 600301-314-003 |
| C2,3,5,14 | Capacitor, 3 pF/5 KV | 600246-314-001 |
| C4,22 | Capacitor, .8-8.5 pF | 600058-317-001 |
| C6,7 | Capacitor, 82 pF NPO | 600269-314-028 |
| C8 | Capacitor, 22 pF NPO | 600269-314-014 |
| C9,10,16-21, 23,25-30 | Capacitor, 0.1 uF | 600189-014-002 |
| C11,12,15, 24,32,33 | Capacitor, 0.01 uF, 50V | 600266-314-008 |
| C13 | Capacitor, 120 pF, Mica | 612003-306-501 |
| C31 | Capacitor, 10 pF, Mica | 610093-306-501 |
| C34 | Capacitor, 15 pF, Mica | 615091-306-501 |
| CR1 | Diode, 1N4004 | 600011-416-002 |
| CR3-8 | Diode, HSCH-1001 | 600145-410-001 |
| K1 | Relay, 24V | 600050-403-001 |
| L1,11 | Coil, 1 uH | 600072-376-013 |

**RF BOARD**
**(601169-536)**

| Symbol | Description | Part Number |
|---|---|---|
| L2-8 | Coil, 1 mH | 600034-376-001 |
| L9 | Coil, .1 uH | 600072-376-001 |
| L10 | Coil, .1 uH | 670119-513-009 |
| Q1,2 | Trans., Pad | 600025-419-001 |
| R1-6 | Resistor, 75 ohm, 45W | 600081-340-005 |
| R7,8,16,17 | Resistor, 24 ohm, 2% | 624094-341-425 |
| R10 | Resistor, 100 ohm, 2W | 610004-341-425 |
| R11,12,26-29 | Resistor, 10K, 1/4W, 5% | 610024-341-075 |
| R13,14,19,20 | Resistor, 4.7K, 1/4W, 5% | 647014-341-075 |
| R15,21 | Resistor, 2.4K, 1/4W, 5% | 624014-341-075 |
| R18 | Resistor, Var., 10K | 600063-360-010 |
| R22 | Resistor, 5.1K, 1/4W, 5% | 651014-341-075 |
| R24,25 | Resistor, 22K, 1/4W, 5% | 622024-341-075 |
| R30,31 | Resistor, 100K, 1/4W, 5% | 610034-341-075 |
| R32,33 | Resistor, 8.2K, 1/4W, 5% | 682014-341-075 |
| R34,35 | Resistor, 560 ohm, 1/4W, 5% | 656004-341-075 |
| T1,2,3 | Toroid, Detector | 600161-512-001 |
| W1 | Assy, Coaxial | 600514-540-001 |

(6 DB PAD) | (POWER DETECTOR) | (MAGNITUDE DETECTOR) | (PHASE DETECTOR)




NOTES:

1. UNLESS OTHERWISE NOTED: ALL RESISTORS ARE IN OHMS, 1/4 W, ±5%; CAPACITORS ARE IN MICROFARADS; DIODES ARE HSCH-1001.

**RF BOARD SCHEMATIC**

5.10.7 Input and Output Specifications

| Pin | Input/Output | Function | Specification |
|---|---|---|---|
| J18 | Output | RF Output | Provides RF path out of module |
| J17 | Input | RF Output | Provides RF path into module |
| P7,1&2 | — | Ground | |
| P7,3&4 | Input | +28 VDC | +28 VDC (±5V) to relay K1 |
| P7,6 | Output | signal | −4 VDC to +4 VDC, proportional to phase error (no error = 0 VDC) |
| P7,8 | Output | reference | 0 VDC - used for noise cancellation purposes |
| P7,10 | Output | R reference | 0 VDC - used for noise cancellation purposes |
| P7,12 | Output | R signal | −4 VDC to +4 VDC, proportional to magnitude error (no error = 0 VDC) |
| P7,16 | Output | Forward Power | 0 −4 VDC determined by RF power |
| P7,18 | Output | Reflected Power | 0 −4 VDC determined by RF power |
| P7,33&34 | Input | PAD relay | Ground to close relay K1 |
| P7,39-44 | — | Ground | |

## 5.11 INTERFACE BOARD

### 5.11.1 General

The Interface Board contains the circuitry required to interface the Control Board to the Memory Board. In addition, circuitry for other functions such as Coupler Bypass, Transmit Interlock, Overtemperature, etc. is included. Descriptions/operations of these circuits follow.

### 5.11.2 BCD to Binary Converter

The BCD (Binary-Coded Decimal) Converter converts the 2 digit BCD channel address at the coupler control point (Channel switch positions 0-95) to a 5-bit address for the Silent Tune Memory. The Converter circuitry has several associated functions:

#### 5.11.2.1 BCD Inverter

The BCD Inverter consists of U25 and U26. It is required when the MSR-4030 is used with the Auxiliary Control Unit. The channel lines are inverted by the Connector Board and must be inverted again for normal operation. This is accomplished by a logic 1 on the BCD Invert/OT Inhibit line P4-9.

Channel lines from the MSR-8000 or MSR-6700 are BCD complement and the inversion by the Connector Board is sufficient. A logic 0 is on P4-9 when the MSR-4030 is used with these units.

The Ones Digit lines of the channel switch (CH1, CH2, CH4, and CH8) enter the board on P4 pins 28, 16, 14, and 22. The Tens Digit lines (CH10, CH20, CH40, and CH80) enter on P4 pins 19, 20, 17, and 18. These lines are inverted if required by U25 and U26 and processed by the Converter IC's U23 and U24.

#### 5.11.2.2 Converter/Chip Select Decoder IC's

The channel lines from the BCD Inverters U25 and U26 are connected to the inputs of the BCD/Binary Converter IC's U23 and U24, except for CH1 which does not require processing and is connected to P3-14 (A3). The remaining Binary address outputs (A4, A5, A6, and A7) are routed to P3 pins 18, 12, 10, and 8 respectively.

The Binary address appearing on A3-A7 ranges from 0 to 31. As the BCD channel switch changes from 0 to 31, the Binary address cor-

responds directly. However, at BCD 32, the Binary address returns to 0 and again counts up to 31 as the BCD switch progresses to BCD 63. Again, at BCD 64, the Binary address starts over at zero and becomes 31 for BCD 95.

U22 is a 3 to 8 decoder IC and selects the required Memory Chip on the Memory Board depending on the Channel Address. CS1 (Chip Select 1) on P3-4 is in positions 0-31. CS2 is at a logic 0 for positions 32-63. Similarly, CS3 is a logic 0 for positions 65-95. Again, at BCD 64, the Binary address starts over at zero and becomes 31 for BCD 95.

The Group Select line (P4-37) when at a logic 0, pulls pins 1 and 2 of U22 low. This results in CS1 going to logic 0. This action is required when the MSR-4030 is used with the MSR-8000. The MSR-8000 channel switch has a range of BCD 1 to 10 on a 4-bit line. BCD 10 requires 2 digits (8 bits) and is illegal for the converter IC's and results in all logic 1's on the Binary address output lines.

The Memory Board accommodates this address but the Chip Select Decoder U21 functions improperly unless the Group Select line is low to force CS1 to a logic 0.

Resistors R1, R2, and network Z3 provide pull-ups for the open collector outputs of U22 and U23.

### 5.11.3 Tune Initiate

The Tune Initiate function is provided by NOR Gate U16A and one-shot U10A. Normally, both inputs to U16A are at a logic 0 resulting in U10A pin 1 being at logic 1. U16A pin 12 (Tune Store) is connected P4-32 and receives a positive-going pulse from the Connector Board whenever a Tune Cycle has been initiated and a memory storage operation is required.

U16A pin 11 receives a positive-going pulse on P4-38 when a Tune Cycle has been initiated and no memory storage is required.

In either case, a negative-going pulse from U16A-13 will trigger U10A and set the Tune Flip-Flop. The Q output provides a pulse that is series gated through U9A, U18B, U19D, and U21A, and puts the control board circuitry into a tune cycle.

### 5.11.4 Tune Flip-Flop

A pulse from U10A into the clock input of Tune Flip-Flop U4A pin 3 will cause it to be set unless the Silent-Tune Flip-Flop U3A has been set. The Data and Q outputs of U3A and U4A are cross-counted to prevent simultaneous Tune and Silent Tune cycles from occurring. The Q output of U4A controls the Key Enable function.

The Tune Flip-Flop is reset by a negative-going pulse on pin 1 that may come from the Ready One-Shot, Fault One-Shot, or the Power-Up reset function.

### 5.11.5 Silent Tune Initiate

Operation of the Silent Tune Initiate circuitry is identical to that of the Tune Initiate with 2 exceptions: the Silent Tune Initiate One-Shot U8A only receives a positive-going pulse from the Silent Tune line P4-30, and it has an inhibit function.

The inhibit function detects when the Channel Switch on the MSR-8000 control panel is in the Manual Position (non-memory channel) and prevents a Silent Tune Cycle from being initiated. Diodes CR10, 11 and 12 are connected to the CH1, CH2, and CH8 lines. When the MSR-8000 channel switch is in the Manual Channel position, these lines will all be at logic 1. The anodes of these diodes are connected to both inputs of U15A which has pull-up resistor R21. With the cathodes of CR10, 11, and 12 at logic 1, the output of U15A puts a logic 0 on U8A disabling it.

During normal operation U8A will put out a positive pulse and set the Silent Tune Flip-Flop. The Q output of U8A is series-gated through

U9A, U188, U19D, and U21A. A Tune Initiate pulse on P3-15 will occur when U8A is triggered, and initiates a tune cycle on the control board.

5.11.6 Silent Tune Flip-Flop

The Silent Tune Flip-Flop U3A will be set by a positive pulse on its clock input provided the Tune Flip has not been set. The Silent Tune Flip-Flop outputs control several functions:

5.11.6.1 Read Enable

The Q output of U3A is connected to the Read Enable line P4-41 and holds this line at logic 0 to enable the Memory Read Latches on the Memory Board.

5.11.6.2 The Q output of U3A is inverted by U21E and puts a logic 0 on the Force/Retune Inhibit line P3-36 to disable the Force function on the Control Board during a Silent Tune Cycle.

5.11.6.3 Transmit Interlock

The Q output of U3A is connected to U6B pin 2 and enables the Transmit Interlock function to prevent the transmitter from being keyed during a Silent Tune Cycle. Operation of the Interlock Circuitry is discussed in section 5.11.16.

5.11.6.4 Silent Tune Servo Preamps, Forward and Reflected Power Circuits

The Q output of U3A enables the Silent Tune Power circuits during a Silent Tune Cycle. Operation of these circuits is covered in section 5.11.8.

5.11.6.5 Start Clock One-Shot

The Start Clock One-Shot U10B is triggered when the Silent Tune Flip-Flop U3A is set. The Q output of U3A goes to logic 0 when U3A is set and causes U10B to produce a negative-going pulse on its Q output to U11A pin 5. Since U11A pin 4 is normally high, a positive-going pulse will result on the Start Clock line P4-40. A start clock function is required at the beginning of a Silent Tune Cycle so a Memory Read Operation can occur.

The Silent Tune Flip-Flop is reset by a negative-going pulse on pin 1 that may come from the Ready One-Shot, Fault One-Shot, or the Power-Up reset function.

5.11.7 Ready One-Shot

The Ready One-Shot U8B is triggered when it receives a log 0 on the Ready line P3-9 from the Control Board.

A positive pulse from U8B pin 13 allows the Antenna Modification Flip-Flop U17B to be set if required.

A negative-going pulse from U8B pin 4 resets the Tune and Silent Tune Flip-Flops through U11B and U12A.

5.11.8 Fault One-Shot

The Fault One-Shot U13A is triggered by a logic 0 on the Fault line P3-7.

A positive-going pulse from U13A pin 13 enters NOR gate U12B and causes the Power-Up Home Flip-Flop to be reset.

A negative-going pulse from U13A pin 4 causes the output of U19A to produce a positive pulse that resets the Write Enable Flip-Flop through U18A. The negative pulse from pin 4 also causes the output of U11B to produce a positive pulse to U12, allowing the Tune and Silent Tune Flip-Flops to be reset.

5.11.9 Sixth Clock Cycle One-Shot

The Sixth Clock Cycle One-Shot U13B is triggered by a logic 0 on the Sixth Clock Cycle line P3-11. This occurs at the end of a Memory operation on the Memory Board. A negative-going pulse from U13B is gated through U19A and U18A and resets the Write Enable Flip-Flop U17A.

### 5.11.10 Write Enable Flip-Flop

The Write Enable Flip-Flop puts a logic 1 on the Write Enable line P4-39. This occurs when a Tune Cycle is initiated and the information is to be stored into Memory.

U17A is set when its clock input pin 3 receives a positive pulse from the Tune Store line P4-32.

U17A is reset by the Sixth Clock Cycle One-Shot upon completion of a successful tune cycle. Otherwise, it is reset by the Fault One-Shot or by the Power-Up Reset Function.

### 5.11.11 Power-Up Reset Function

U29B, R28, C41, and CR13 comprise the Power-Up Reset Function. When the Coupler power is switched on C41 holds both inputs of U19B at logic 0 until R28 can charge C41. When C41 charges sufficiently, U19B's output will go to a logic 0. This delay results in the outputs of U12A, B, C, and D and U13A remaining at a logic 0 for a short time after the power is switched on. These gates cause all Flip-Flops on the interface board to be reset.

### 5.11.12 Power-Up Home Flip-Flop

U3B is the Power-Up Home Flip-Flop and must be set to enable the Key Enable, Silent Tune Servo Preamps, and Forward and Reflected Power circuits used in the Silent Tune Mode.

The Power-Up Home Flip-Flop causes the elements to go to their home positions when it has been cleared prior to initiating a tune cycle. This occurs since the Key Enable line is held at logic 1 and prevents the transmitter from being keyed. With no RF power, the Home Cycle on the Control Board will not be interrupted until the elements reach home positions. This also occurs during a Silent Tune Cycle since U3B will not enable the Silent Tune Servo Preamps or Forward/Reflected Power circuits until U3B is set.

Forcing the elements to home positions is necessary at initial power up to reset the Element Counters on the Memory Board. The Counters are reset by the element limit switches. A Fault also homes the elements to reset the Counters since the Fault may have resulted from loss of Counter synchronization during a Silent Tune Cycle.

U3B is also cleared when the Antenna Modification Flip-Flop is set (during a Tune Cycle when L reach L Max). This allows the Coupler elements to home and attempt tuning with the Antenna Modification Capacitor in series with the Antenna.

U3B is set by the Elements Home signal from U15C. When both elements are at their home positions a logic 1 will appear on the C Max and L Min lines, P3-34 and 30. Both lines are inverted and applied to NOR gate U15B, inverted again, and used to set the Power-Up Home Flip-Flop with a logic 0.

When the Antenna Modification Flip-Flop is set, a negative-going pulse from U19C pin 8 will pull the clear input of U3B low through CR16. U12B receives positive-going pulses from the Fault Flip-Flop or the Power-Up Reset Function. R29 provides pull up current to U3B's clear input.

### 5.11.13 Antenna Modification Flip-Flop

U17B is set whenever the Antenna Modification Capacitor is required. During a Tune Cycle (with RF power) if the Antenna Modification Capacitor is required, a logic 1 is applied to U17B's clock input. U17B's Data input is held at logic 1. Consequently, U17B changes state.

During a Silent Tune Cycle, a logic 1 will appear on U9D pin 5 from the Antenna Modification Read line P3-26 if the Antenna Modification Capacitor is required. A logic 0 from U9D pin 6 is inverted by U14D and gated with a Ready pulse by U14A. This results in a logic 0 pulse on U17B's Preset input and sets U17B.

When U17B has been set during a Tune Cycle, the Q output is connected to the Antenna Modification Write line (P3-16) and allows the Memory Board to store this information for a Silent Tune Cycle. The Q output of U17B is gated through NOR gate U6A to drive Q6 and Q11 to energize the Antenna Modification Relay. U6A is connected to the Bypass line P4-33 and prevents the output of U6A from going to logic 1 (to energize the Antenna Modification Relay) whenever the Bypass function is enabled (logic 1 on P4-33).

The Q output of U17B is also connected to NAND gate U19C through R21 and C26. U19C's other input is connected to the Antenna Mod.'s line P4-13. When this line goes to logic 1 to set the Antenna Modification Flip-Flop U17B, U19C pin 9 will be at a logic if U17B is not already set. This results in U19's output going to logic 0 causing a Tune initiate pulse (logic 0) on P3-15 through U19D and U21A. At the same time, U17B will be set. R21 and C26 provide a time delay to keep U19C pin 9 at a logic 0 since U17B pin 8 will go to logic 0 when U19C pin 10 goes to logic 1 and U19's output could not go to logic 0. Once U17B is set, U19C pin 9 will remain a logic 1 to prevent another Tune initiate pulse from occurring if the coupler fails to tune with the Antenna Modification Capacitor. Otherwise the coupler could cycle indefinitely.

### 5.11.14 Key Enable

The Key Enable Time P4-12 will go to a logic 0 to key the transmitter whenever the Tune Flip-Flop U4A and Power-Up Home Flip-Flop U3B have been set. The Q outputs of U4A and U3B are connected to the inputs of NOR gate U2D. When both flip-flops are set, U2D's output will go to logic 1. U2B inverts this and puts a logic 0 on U2C pin 5. U2C pin 6 is connected to the Key Enable line P3-35 and receives a logic 0 from the Control Board. This results in a logic 1 on U2C pin 4 to turn on Q2 and Q7 to put a logic 0 on the Key Enable line P4-12.

### 5.11.15 Bypass Function

A logic 1 on P4-33 (Bypass line) causes the transmitter to be interlocked (disabled) and energizes the Bypass Relay. This signal is connected to U5A pin 12 and 13 through R30 and C44. R30 and C44 hold U5A pin 13 at logic 0 for a short time and delay U5A's output from going to logic 0 when the Bypass line goes to logic 1. This delay allows the transmitter to be interlocked and prevents the Bypass from energizing before the RF has decayed.

U6C inverts the logic 0 from U5A and turns on Q5 and Q10 to energize the Bypass Relay.

### 5.11.16 Transmit Interlock

The Transmit Interlock (Tx Interlock) function prevents the transmitter from being keyed by putting a logic 1 on the Tx Interlock N/C (normally closed) line P4-15 or a logic 0 on the Tx Interlock N/O (normally open) line P4-16. Complementary outputs are provided for various transmitter requirements.

The TX Interlock function is enabled during a Silent Tune Cycle, during an Over-temperature condition, or when the Bypass function is enabled.

The Q output of the Silent Tune Flip-Flop U3A puts a logic 1 on U6B (pin 3). In either case, U6B's output will go to logic 0. This causes the output of U5C to put a logic 1 on U6D pin 9 and also to pin 8 through R34 and C47. R34 and C47 provide a delay that holds the Tx Interlock function for a short time to allow the Bypass Relay to return to its normal position before the transmitter can be keyed. U6D's output turns off Q3, Q8, and Q9 and turns on Q4 to provide the required states on the Interlock lines to cause the exciter to be disabled.

If the Overtemperature condition occurs, U5B's inputs will go to logic 1 resulting in a logic 1 on

U6D's output to enable the Tx Interlock function.

### 5.11.17 Overtemperature

When the internal air temperature of the Coupler reaches +80 degrees C, the Overtemperature function will disable the transmitter. Some Mackay exciters do not use the Overtemperature feature but use a sensor located on the Connector Board to sense temperature and provide a signal to reduce transmitter power proportionally to temperature. In this case, the Overtemperature function is inhibited by a logic 0 on the OT Inhibit BDC/Invert line P4-9.

Temperature reference diode CR3 provides a voltage proportional to the temperature into the non-inverting input of op amp U20. R3 provides operating current to CR3. R4 and R5 form a voltage divider to put a 3.5 volt reference on the inverting input of U20. When the Temperature increases to +80 degrees C, the voltage on the non-inverting input of U20 will be 3.5 volts and U2D's output will go to a logic 1 and interlock the transmitter and turn on the LED Flasher U1. Note that CR4 will hold the non-inverting input of U26 at logic 0 if the OT Inhibit BDC/Invert line is at logic 3 and prevent U20's output from going to a logic 1.

Normally, the Overtemperature Flip-Flop U4B is held in the reset condition by a logic 0 on its clear input. When the output of U20 goes to logic 1, U4B's clear input goes to logic 1 allowing it to be set if an OT Override pulse from P4-35 is applied to its Clock input.

If the OT Override Function is not used, U4B will remain cleared and U1 will begin flashing the QT LED with a 1 Hz signal on its output pin 3. This will cause U2A to flash the $\overline{\text{OT LED}}$ Line P4-36. Also, U5B pin 4 will go to a logic 1 and cause the Transmit Interlock Function to occur.

When the OT Override button is pushed, a logic 1 sets U4B through its clock input. U4B's Q output puts a logic 1 on U2A pin 9 which causes the OT LED line to remain at logic 0 so the OT LED is lit and does not flash. U4B's $\overline{Q}$ output puts a logic 0 on U5B pin 5 and results in disabling the Tx Interlock Function so that the transmitter can be operated during an overtemperature condition.

### 5.11.18 Silent Tune Servo Preamps, Forward and Reflected Power Circuits

These circuits take information from the Memory Board and generate error signals to tune the elements and provide forward and reflected power signals to the Control Board. Essentially, the circuitry simulates the RF Module detector outputs so that the Control Board can function during a Silent Tune Cycle without RF power.

#### 5.11.18.1 Forward Power

During a Silent Tune Cycle, both inputs to NAND gate U9C will be at logic 1 if U3A and U3B have not been set. The Output of U9C is inverted by U11D and applied to the Forward Power line P4-31 through CR19. CR19 isolates the Forward Power Silent Tune Circuitry from this line during normal Tune Cycles with RF Power.

#### 5.11.18.2 Reflected Power

At the completion of a Silent Tune Cycle, both inputs to U11C (A=B, L and A=B, C) are at logic 1, resulting in a logic 0 on NOR gate U18C pin 11. The other input to U18C is connected to U9C pin 11 and will be at logic 0 when U3A and U3B have been set. This results in a logic 1 on U18D pins 8 and 9 so that U18D's output is at logic 0 and the Reflected Power line P4-29 is at logic 0.

During a Silent Tune Cycle, the output of U11C will be at logic 1 before both elements have been positioned. This results in a logic 1 at the output of U18D. R40 and R41 divide this voltage and it is applied to the Reflected Power line through CR18 which isolates it from the line when not being used. C48 holds the Reflected Power line at logic 0 for a short inter-

val so that the Home Cycle will be terminated on the Control Board at the start of a Silent Tune Cycle.

### 5.11.19 Servo Preamps

The L and C Servo Preamps process the digital comparator outputs from the Memory Board and convert them to variable analog signals to drive the Servo amplifiers on the Control Board. The L and C Servo Preamps are identical. Therefore only the L Servo Preamp operation is discussed.

#### 5.11.19.1 L Servo Preamp Enable

The Memory Board L Discriminator outputs (A > B, L and A < B, L) are gated through U16A and U16C, then divided by voltage dividers R46-R49 before being applied to the non-inverting inputs of U7A and U7B. As discussed in 19.2, the output of U9C will be logic 0 when U3A and U3B are set. This enables the outputs of U16B and U16C to go to logic 1 when the inputs go to logic 0. A greater than B, L (P4-44) will be a logic 1 when A less than B, L (P4-43) is at logic 0 and vice versa. When a Silent Tune Cycle is completed, both lines will be at logic 0.

The A = B, L (P4-42) line will be at logic 0 at the end of a Silent Tune Cycle. This signal is gated through U14C with the Q output of U3A and then inverted by U14B. This gating only allows the output of U14B to be logic if A = B, L is high and the Silent Tune Flip-Flop U3A has been set. This signal is connected to the non-inverting input resistors (R42 and R44) of U7A and U7B through CR20.

#### 5.11.19.2 L Servo Preamp

Operation of the L Servo Preamp is best explained by describing a typical Silent Tune Cycle. After the Preamps have been enabled as discussed in 20.1, the count on the L Memory Counter may be less than the count on the L Memory Read Latch. This results in a logic 0 on the A greater than B, L line and a logic 1 on the A less than B, L line. The A = B, L line will also be at a logic 0. This results in a voltage on U7A pin 3 near 0 volts on U7A pin 2 and U7B pins 5 and 6. U7A and U7B have a gain of approximately 2 so that U7A's output will produce a voltage with its input now high. This voltage goes through CR21 and appears on the R Ref line (P4-25) and cause the Inductor to run towards maximum.

As the Inductor crosses the tune point (L Memory Counter = L Memory Read Latch) the A = B, L line will go to logic 1 momentarily because the Inductor will overshoot the tune point. A greater than B, L and A less than B, L will change states, each assuming the previous state of the other.

The momentary pulse on the A = B, L line will cause C54 to charge slightly and raise the voltages on the inverting inputs of U7A and U7B. This reduces their gain. CR20 prevents C54 from discharging through its charge path.

Since A greater than B, L and A less than B, L have changed states, U7A pin 3 will be near zero volts and U7B pin 5 will have a positive voltage. U7B's output will now go to a positive voltage but it will be very small initially because of the gain reduction by the A = B, L signal. Since U7A's output is now low, C54 will discharge through R42 and R43. As this occurs, U7B's gain increases causing its output voltage to increase. It puts this voltage on the R signal line (P4-27) and causes the Inductor to run in the opposite (home) direction.

The inductor will again cross the tune point and overshoot and the process repeated. However, each time the overshoot becomes less until the Inductor rests on the tune point. When this happens, A = B, L will be logic 1 and A greater than B, L and A less than B, L will be logic 0. This results in a small but equal positive voltage on the R signal lines. The Servo Preamps are disabled when the Ready signal resets U3A. Diodes CR21 and CR22 isolates the Servo Preamps when they are not required.

5.11.20 Counter Reset Lines

5.11.20.1 The C Max Line P3-34 is used to reset the C Counter on the Memory Board. Q1 inverts this line to put a logic 0 on P3-19 to reset the counter on the memory board.

5.11.20.2 The L Counter is reset by a logic 0 on P3-17. U21D inverts the L Min line P3-30 and provides the reset signal to the Memory Board on P3-17.

5.11.21 Surveillance

The Surveillance feature on the Control Board requires a log 0 to be enabled. The TTL level signal from the Connector Board on P4-34 is inverted by U21D and output on P3-5. U21F's output will be at 8 volts CMOS levels when not at logic 0.

5.11.22 Inputs

| Connector/Pin No. | Line/Function | Specification |
|---|---|---|
| P4-28 | CH1 | BCD Ones Digit |
| P4-26 | CH2 | BCD Ones Digit |
| P4-24 | CH4 | BCD Ones Digit |
| P4-22 | CH8 | BCD Ones Digit |
| P4-19 | CH10 | BCD Tens Digit |
| P4-20 | CH20 | BCD Tens Digit |
| P4-17 | CH40 | BCD Tens Digit |
| P4-14 | CH80 | BCD Tens Digit |

Lines CH1-CH80 require a 2 digit BCD Complement Address with a change of 0 to 95.

| Connector/Pin No. | Line/Function | Specification |
|---|---|---|
| P4-33 | Bypass | Logic 1 for Bypass Mode |
| P4-32 | Tune Store | Logic 1 pulse to initiate an RF tune cycle and program a memory channel |
| P4-38 | Tune | Logic 1 pulse to initiate an RF tune cycle without programming a memory channel |
| P4-30 | Silent Tune | Logic 1 pulse to initiate a Silent Tune Cycle |
| P4-13 | Antenna Mod' | 30 msec logic 1 pulse during an RF tune cycle to switch in capacitors |
| P3-7 | $\overline{\text{Fault}}$ | Logic 0 during a coupler fault condition |
| P3-11 | Sixth Clock Cycle | Logic 1 for 6 msec during Memory Board Clock interval |
| P3-9 | $\overline{\text{Ready}}$ | Logic 0 when coupler is in a Ready condition |
| P4-35 | OT Override | Logic 1 pulse to reset the overtemperature circuitry |
| P4-10 | Auto Home | Logic 1 pulse to force elements home in the Auto-Home mode using the MSR-6408 |
| P4-9 | $\overline{\text{BCD Invert/}}$ OT Inhibit | Logic 0 required for MSR-8000 and MSR-6700; Logic 1 for other exciters |
| P4-37 | Group Select | Logic 0 required for MSR-8000 operation |
| P3-35 | Key Enable' | Logic 0 input from Control Board to request Tune Power from exciter |
| P3-34 | C Max | Logic 1 when capacitor element is at its home position |
| P3-29 | L Max | Logic 1 when Inductor element is at maximum inductance |
| P3-30 | L Min | Logic 1 when Inductor element is at its home position |
| P4-34 | Surveillance In | Logic 1 required to enable Surveillance feature |
| P4-42 | A = B, L | Logic 1 when Inductor element has completed tuning during a Silent Tune Cycle |
| P3-24 | A = B, C | Logic 1 when Capacitor element has completed tuning during a Silent Tune Cycle |
| P3-26 | Antenna Mod. Read | Logic 1 input from Memory Board during a Silent Tune Cycle allows switching of Antenna Mod. Capacitors |
| P4-44 | A > B, L | Logic 1 voltage from Memory Board to run Inductor towards its minimum value |
| P4-43 | A < B, L | Logic 1 voltage from Memory Board to run Inductor towards its maximum value |
| P3-23 | A > B, C | Logic 1 voltage from Memory Board to run Capacitor towards its minimum value |
| P3-21 | A < B, C | Logic 1 voltage from Memory Board to run Capacitor towards its maximum value |

| Connector/Pin No. | Line/Function | Specification |
|---|---|---|
| P3-38 | +5 Input | +5.0 ±.3 volts, 750 mA maximum |
| P3-40 | +5 Input | +5.0 ±.3 volts, 750 mA maximum |
| P3-25 | +5 Input | +5.0 ±.3 volts, 750 mA maximum |
| P3-28 | GND | Ground, 0v |
| P3-41 | GND | Ground, 0v |
| P3-42 | GND | Ground, 0v |
| P3-43 | GND | Ground, 0v |
| P3-44 | GND | Ground, 0v |
| P4-1 | GND | Ground, 0v |
| P4-2 | GND | Ground, 0v |
| P4-3 | GND | Ground, 0v |
| P4-4 | GND | Ground, 0v |
| P4-5 | GND | Ground, 0v |
| P4-6 | GND | Ground, 0v |

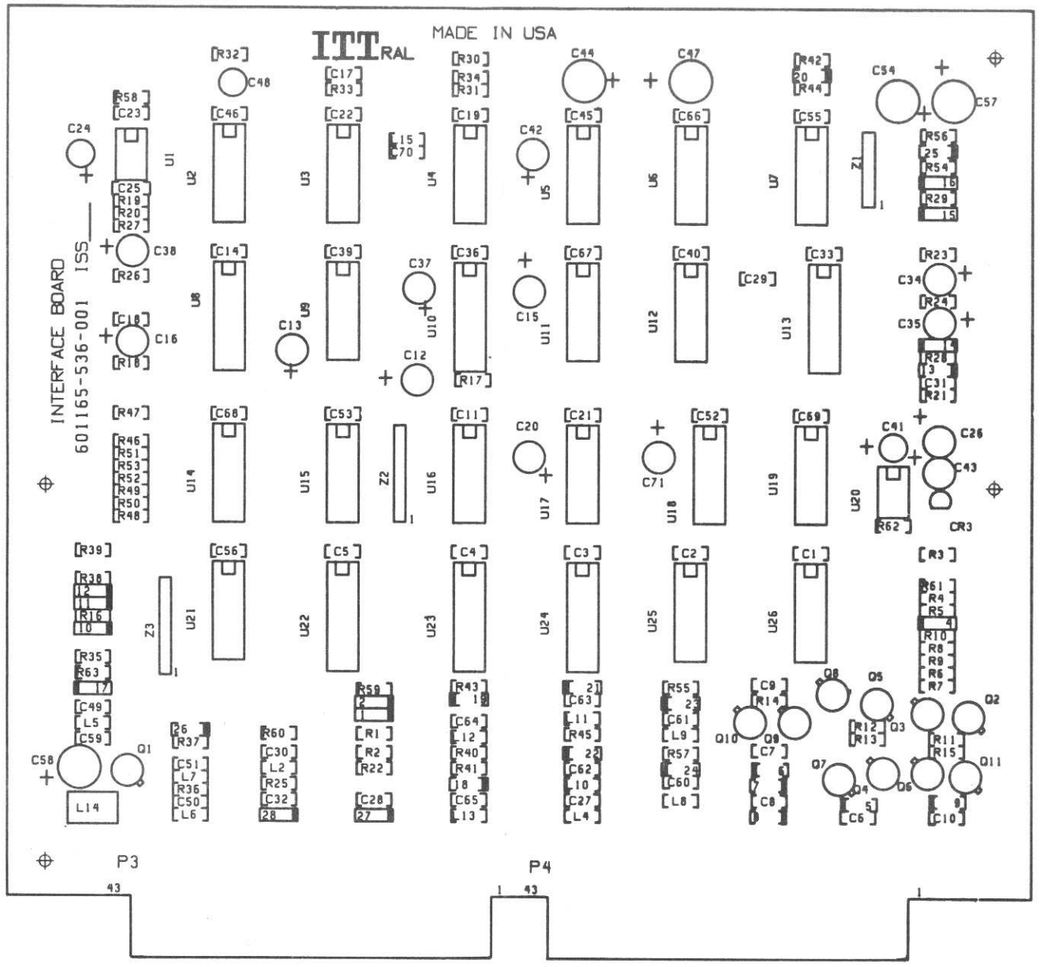
5.11.23 Outputs

| | | |
|---|---|---|
| P3-14 | A3 | Binary Channel Address |
| P3-18 | A4 | Binary Channel Address |
| P3-12 | A5 | Binary Channel Address |
| P3-13 | A6 | Binary Channel Address |
| P3-8 | A7 | Binary Channel Address |

(A3-A7 output a Binary Address with a range of 0-31.)

| | | |
|---|---|---|
| P3-4 | $\overline{CS1}$ | Logic 0 for channels 0-31 |
| P3-6 | $\overline{CS2}$ | Logic 0 for channels 32-63 |
| P3-3 | $\overline{CS3}$ | Logic 0 for channels 64-95 |
| P4-12 | Key Enable | Logic 0 during a Tune Cycle to request Tune Power from exciter |
| P4-15 | Tx Interlock N/C | Logic 0 for normal operation; logic 1 during a Silent Tune Cycle and when coupler is in Bypass mode or overtemperature condition |
| P4-16 | $\overline{\text{Tx Interlock N/O}}$ | Same as for Tx Interlock N/C but inverted |
| P4-11 | Bypass Relay | Logic 0 to energize Bypass Relay |
| P4-7,8 | Antenna Mod. Relay | Logic 0 to energize Antenna Mod. Relay |
| P3-16 | Antenna Mod. Write | Logic 1 when Antenna Mod. Relay is energized; provides status for a Memory Storage operation |
| P4-36 | $\overline{OT}$ LED | 1 Hz logic level square wave when temperature in coupler reaches 80 ±5 °C; goes to a logic 0 if OT Override button on MSR-6408 is depressed |

| Connector/Pin No. | Line/Function | Specification |
|---|---|---|
| P4-40 | Start Clock | 1 ±.5 msec logic 1 pulse occurs at beginning and end of a Silent Tune Cycle and completion of a Memory Storage operation |
| P4-39 | Write Enable | Logic 1 during a Silent Tune Cycle |
| P3-15 | Tune Initiate | 1 ±.5 msec logic 0 pulse at start of a Tune or Silent Tune Cycle; logic 0 pulse also occurs when Antenna Mod. Relay energizes during a Tune Cycle |
| P4-41 | $\overline{\text{Read Enable}}$ | Logic 0 during a Silent Tune Cycle |
| P4-21 | $\phi$ Ref | Logic 1 voltage during a Silent tune Cycle runs Capacitor element to its minimum value |
| P4-23 | $\phi$ Sig | Logic 1 voltage during a Silent Tune Cycle runs Capacitor element to its maximum value |
| P4-25 | R Ref | Logic 1 voltage during a Silent Tune Cycle runs Inductor element to its maximum value |
| P4-27 | R Sig | Logic 1 voltage during a Silent Tune Cycle runs Inductor element to its minimum value |
| P4-31 | FWD PWR | Logic 1 voltage during a Silent Tune Cycle |
| P3-31 | $\overline{\text{L Max}}$ | Logic 0 when Inductor element is at its maximum value |
| P3-19 | $\overline{\text{C Counter Reset}}$ | Logic 0 when Capacitor element is at its maximum value |
| P3-32 | $\overline{\text{L Min}}$ | Logic 0 when Inductor element is at its minimum value |
| P3-17 | $\overline{\text{L Counter Reset}}$ | Logic 0 when Inductor element is at its minimum value |
| P4-29 | RFL PWR | Logic 1 during a Silent Tune Cycle until elements have positioned, then logic 0 |
| P3-36 | $\overline{\text{Force/Retune Inhibit}}$ | Logic 0 during a Silent Tune Cycle |
| P3-5 | $\overline{\text{Surveillance Out}}$ | Logic 0 when Surveillance feature is enabled |

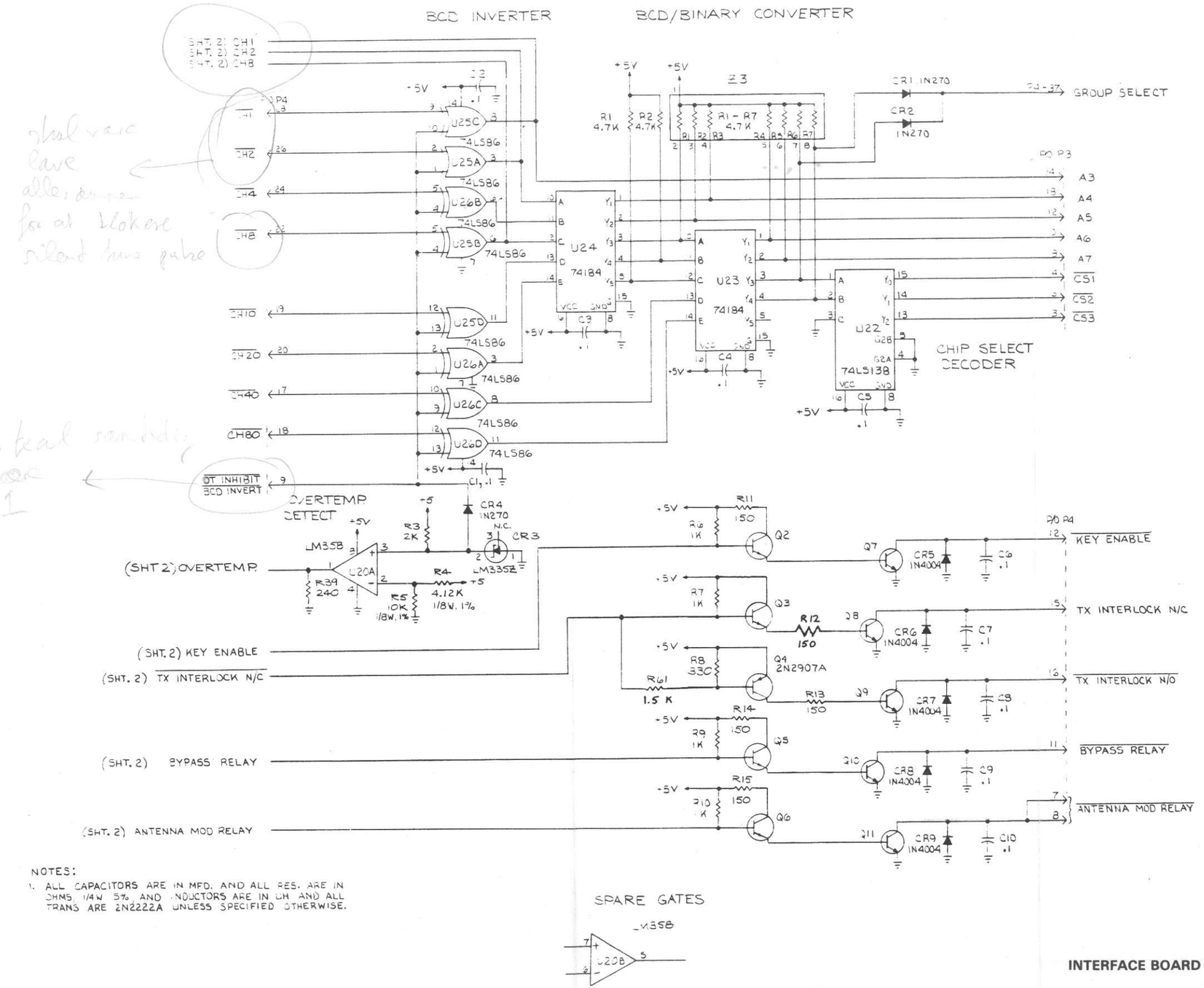



INTERFACE BOARD
(601165-536)

INTERFACE BOARD
(601165-536)

| Symbol | Description | Part Number |
|---|---|---|
| C1-11, 14, 17-19, 21-23, 27-33, 36, 39, 40, 45, 46, 49-53, 55, 56, 59-70 | Capacitor, .1 uF, 50V | 600272-314-001 |
| C12,20, 26,42, 43,71 | Capacitor, 1 uF, 35V | 600202-314-007 |
| C13,15, 16,34, 35,37,38 | Capacitor, .1 uF, 35V | 600202-314-001 |
| C24,41 | Capacitor, 10 uF, 50V | 600297-314-013 |
| C25 | Capacitor, .01 uF, 50V | 600272-314-002 |
| C44,47, 58 | Capacitor, 47 uF, 50V | 600297-314-026 |
| C48 | Capacitor, 4.7 uF, 50V | 600297-314-010 |
| C54,57 | Capacitor, 10 uF, 100V | 600297-314-014 |
| CR1,2,4, 10-12, 14-17, 27 | Diode 1N270 | 600052-410-001 |
| CR3 | Diode LM335Z | 600598-415-001 |
| CR5-9 | Diode 1N4004 | 600011-416-002 |
| CR13 | Diode 1N4148 | 600109-410-001 |
| L2, 4-13, 15 | Inductor 100 uH | 600125-376-002 |
| L14 | Inductor 4.7 uH | 600091-376-001 |
| Q1-3, 5-11 | XSTR 2N2222A | 600080-413-001 |
| Q4 | XSTR 2N2907A | 600154-413-001 |
| R1,2,16, 29-33, 35-38, 47,49, 51,53, 58,63,25 | Resistor, 4.7K, 1/4W, 5% | 647014-341-075 |
| R3 | Resistor, 2K, 1/4W, 5% | 620014-341-075 |
| R4 | Resistor, 4.12K, 1/8W, 1% | 641211-342-059 |
| R5 | Resistor, 10K, 1/8W, 1% | 610021-342-059 |
| R6,7,9, 10,19,62 | Resistor, 1K, 1/4W, 5% | 610014-341-075 |
| R8 | Resistor, 330 ohm, 1/4W, 5% | 633004-341-075 |
| R11,12, 13,14,15 | Resistor, 150 ohm, 1/4W, 5% | 615004-341-075 |
| R17,18, 23,24 | | |
| 26,27 | Resistor, 22K, 1/4W, 5% | 622024-341-075 |
| R20 | Resistor, 47K, 1/4W, 5% | 647024-341-075 |
| R21,34 | Resistor, 470 ohm, 1/4W, 5% | 647004-341-075 |
| R28,40, 41,59, 43,45, 46,48, 50,52, 55,57,60 | Resistor, 10K, 1/4W, 5% | 610024-341-075 |
| R39,22, | Resistor, 240 ohm, 1/4W, 5% | 624004-341-075 |
| R64 | Resistor, 0 Ω | 600000-341-075 |
| R42,44, 54,56 | Resistor, 20K, 1/4W, 5% | 620024-341-075 |

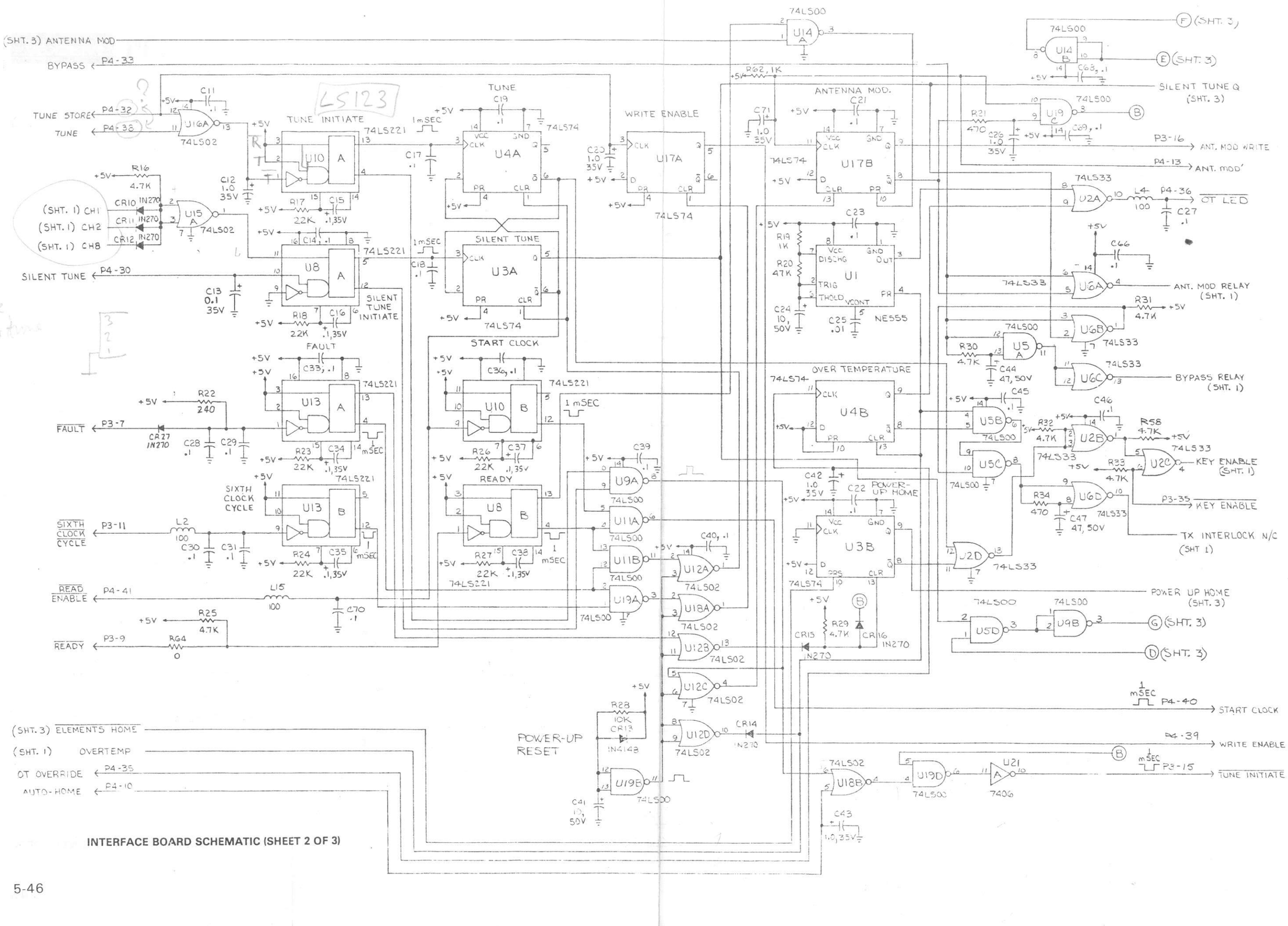
| Symbol | Description | Part Number |
|---|---|---|
| R61 | Resistor, 1.5K, 1/4W, 5% | 615014-341-075 |
| U1 | IC NE555 | 600074-415-001 |
| U2,6 | IC 74 LS33 | 600219-415-001 |
| U3,4,17 | IC 74 LS74 | 600113-415-001 |
| U5,9,11, 14,19 | IC 74 LS00 | 600114-415-001 |
| U8,10,13 | IC 74 LS221 | 600326-415-001 |
| U12,15, 16,18 | IC 74 LS02 | 600118-415-001 |
| U7 | IC LM324 | 600171-415-001 |
| U20 | IC LM358 | 600150-415-001 |
| U21 | IC 7406 | 600016-415-001 |
| U22 | IC 74 LS138 | 600309-415-001 |
| U23,24 | IC 74184 | 600119-415-001 |
| Z1 | Res Net 1K X5 | 600201-537-002 |
| Z2,3 | Res Net 4.7K X7 | 600201-537-001 |




NOTES:

1. ALL CAPACITORS ARE IN MFD. AND ALL RES. ARE IN OHMS, 1/4W 5% AND INDUCTORS ARE IN UH AND ALL TRANS ARE 2N2222A UNLESS SPECIFIED OTHERWISE.

**INTERFACE BOARD SCHEMATIC (SHEET 1 OF 3)**




**INTERFACE BOARD SCHEMATIC (SHEET 2 OF 3)**

## 5.12 CONTROL BOARD

### 5.12.1 General

The Control Board contains most of the active coupler logic circuits including the Servo Amplifiers, Forward and Reflected Power Comparators, Phase and Magnitude Comparators, and the 6 dB Attenuator control. In addition, the tune cycle timers and status indicator circuitry are contained on the Control Board.

### 5.12.2 Functional Description

The operation of the control board circuitry is described in this section. Refer to the schematic for the following discussion.

#### 5.12.2.1 Power Requirements

The control board has four associated DC voltages: +28, +12, +8, and −5.

##### 5.12.2.1.1 +28 VDC

The servo drive transistors require +28 VDC. This voltage enters on J2 pin 23-26.

##### 5.12.2.1.2 +12 VDC, 8 VDC

Power for the IC's is derived from 12 VDC that enters on J3 pin B. This voltage is regulated to +8 volts by U5 as required by the CMOS logic.

##### 5.12.2.1.3 −5 VDC

Comparators U20 and U23, and U26 require −5 VDC. This voltage is provided by a DC-DC converter circuit consisting of U17 and R84-85, C50-53, and CR30-31. This voltage may be measured on TP8 only when the RF present line TP2 is at logic 1. The converter runs only during transmit intervals to prevent RF interference in the station receiver.

#### 5.12.2.2 Servo Preamplifier

Control information for the variable capacitor servo originates in the phase discriminator or from the silent tune C servo preamps on the Interface Board. This control signal enters the control board on P1 -pins 5 and 6 and is applied to the non-inverting (+) input of differential amplifier U23C. The inverting (1) input of U23C is connected to ground through a resistor located on the RF board. In this manner, both inputs of U23C will be subject to the same amount of stray hum or noise pickup. Since U23C can respond only to differences between its two inputs, this unwanted noise will not be amplified.

Inductors L14 and L15, and capacitors C40 and C41 serve to remove any RF on the input lines to U23C.

The voltage gain of U23C is basically determined by the ratio of R73 to R70; therefore, the voltage gain of the preamplifier is 20. C42 and R71 comprise a damping network while C44 is used to insure that any AC on the preamp input is not amplified.

The control signal at the non-inverting input of U23C can be positive or negative as a function of the discriminator output. The output of U23C is applied through R74 to the inverting input of U20B. Since R74 and R75 are equal in value, U20B has unity gain; therefore, the voltage outputs from U23C and U20B will be equal but of opposite polarity. The outputs from U23C and U20B are also connected to the inverting inputs of comparators U23D and U20C.

R44/Q14/R50 and R48/Q15/R54 form "swamping" circuits to load down the discriminator inputs after the coupler has tuned due to the increased error voltages at high power operation. The $\overline{Q}$ output of U19A biases on Q14/Q15 through R50/R54 when a ready condition is reached. This places R44/R48 across each input to ground.

The servo oscillator, made up of U26D, U26A, and associated components, produces a triangular shaped waveform having a frequency of about 300 Hz. This signal is applied to the non-inverting inputs of comparators U23D and U20C. Whenever the error signal at the inverting input of U23D or U20C exceeds the

voltage at the non-inverting input, a low logic level is produced at the respective comparator's output.

A low logic level will be produced only during the period of time that the error signal exceeds the triangular signal. In this way, the analog error signal is converted into a time modulated signal whose pulse width is directly proportional to the error signal. Depending on the polarity of the error signal, this variable pulse width signal will be present on the output of either U23D or U20C. With no error signal, both outputs from U23D and U20C will be high. R86/CR26 and R88/CR29 serve to remove the negative voltage swing from the comparator's output to prevent damage to the inputs of the following CMOS IC's. Because −5 VDC is used in these circuits, they are operational only when RF power is present.

Signal input to the servo preamp for the variable inductor originates in the magnitude discriminator or from the Silent Tune L servo preamps on the interface board. Its operation is identical to that of the variable capacitor servo preamp with the exception of the RC damping network and a lower voltage gain.

5.12.2.3 Servo Control Logic

The servo control logic is used to force the servo amplifiers to drive the tuning elements in a particular direction in response to a homing or forcing signal, to disrupt the drive when the elements are at their limits, and to remove drive entirely in response to the limits or to the servo enable/disable signal. Under tuning conditions, the control logic routes the output signals from the preamplifier/comparators to the servo amplifiers.

The control logic for the capacitor servo is comprised of IC's U12A, U2A, and U7A. When a homing signal is received, the output of U7A is forced high while the output of U12A is forced low. Consequently, the output of U2B will be high and, assuming the servos are enabled and the capacitor is not at its maximum limit, the output of U2A will be low. These signals, applied to the C servo amplifier, will drive the capacitor toward its home position.

The control logic for the inductor servo is comprised of IC's U12B, U4, and U9. It is important to note that a homing and forcing function cannot occur simultaneously. By following the logic paths, it can be seen that when homing, the output from U9B is low while the output from U9A is high. Consequently, the output of U4B will be high and, assuming the servos are enabled and the inductor is not at its minimum limit, the output of U4A will be low. These signals, applied to the L servo amplifier, will drive the inductor toward its home position. When a forcing signal is applied, the output states of U4A and U4B are reversed and the inductor will be driven in the opposite direction, toward maximum inductance. Under tuning conditions, as with the capacitor servo logic, the output signals from the preamplifier/comparators are routed unchanged to the L servo amplifier.

5.12.2.4 Servo Amplifier (Motor Driver)

The capacitor servo amplifier consists of two complementary power transistor pairs, Q27/Q29 and Q33/Q35, that control the motor for the vacuum variable capacitor. Q28/Q30 and Q34/Q36 combine with the power transistors to form a darlington configuration. Q18 and Q32 translate the +8 volt CMOS logic levels up to Vcc for driving Q28/Q30 and Q34/Q36, respectively.

The two complementary transistor pairs from a bridge type circuit with the motor connected across the emitter junctions of Q27/Q29 and Q33/Q35. With no positioning signal, the bases of Q18 and Q32 are supplied with high logic levels through R62 and R90 respectively. With Q18 and Q32 turned on, no drive signals are applied to the bridge circuit and no voltage will appear across the motor.

Assuming Q18 is turned off and Q32 is turned on, then the bases of Q28/Q30 will be near Vcc potential and the bases of Q33/Q35 will be near ground potential. This will bias on power transistors Q27 and Q35 and bias off Q29 and Q33. The servo motor will then turn in the direction that runs the capacitor toward its home position of maximum capacitance. When Q18 is turned on and Q32 is turned off, the situation is reversed and the motor will run in the opposite direction.

During normal operation, the bases of Q18 and Q32 will often have time modulated drive voltages applied to them. The pulse width will control the speed, since the motor will integrate the pulses across it into an average voltage. By employing this type of servo, maximum motor efficiency and proportional control are maintained, even at low error voltage levels.

Operation of the servo amplifier for the variable inductor is identical to that of the capacitor servo just described.

5.12.2.5 Power on Reset Pulse Generator

Upon an initial application of power, capacitor C27 charges through resistor R34. During this time, the outputs of U14D, U21A, U18A, U21C, U14B, and U1C are high and are used to reset all flip-flops. After approximately 400 ms, the voltage across C27 becomes high enough to cause these outputs to go low, thus terminating the reset pulse. Diode CR14 is used for fast recovery in the event of a momentary power disruption.

5.12.2.6 Tune Initiate

A tune cycle is initiated by a negative-going pulse on the tune initiate line J2-22, 22. This causes a short, positive pulse to be generated that sets some flip-flops and resets others:

5.12.2.6.1 Set Flip-Flops

Flip-flops that are set by a tune initiate pulse include U8B (Attenuator), U19A (Tune), U10A (L Home), and U10B (C Home).

5.12.2.6.2 Reset Flip-Flops

A tune initiate pulse resets U8A (Tune), U22A (Ready), U25A (Fault), U19B (Force), and U25B (Lockup/Retune).

5.12.2.6.3 Tune Initiate Pulse Logic

U18D, U24C, R28, and C23 comprise the Tune Pulse Logic. Initially, pin 8 of U24C is high and pin 9 is low, resulting in a logic 1 on pin 10. When a momentary ground is placed on U18D pin 9, pin 9 of U24C immediately goes high resulting in a logic on U24C pin 10. At the same time C23 begins to discharge through R28. As soon as the voltage across C23 has fallen to a logic 0, the output of U24C returns to its normally high state. This negative going pulse from the output of U24C lasts approximately 10 msec, as determined by the RC time constant of R28/C23. This pulse is gated so as to provide a positive pulse to set/reset the required flip-flops.

During the 10 msec that the time pulse is high, transistor Q3 is biased on and discharges the 30 second timer capacitor, C16, through R22. With U19A now set, U8A will be set as soon as its clock input receives a logic 1 from the RF Present line (TP2). When U8A is set, C16 starts recharging through R23. If the coupler tunes successfully within the 30 seconds allowed, the ready line going high will reset U19A, U8A and allow C16 to quickly discharge through CR8 to ground. Should no ready signal appear, C16 will eventually be charged enough to force the output of U18C low, signifying a time out fault.

Pin 8 of U14C will go low only if a VSWR fault occurs. Thus the output of U14C going high will indicate a fault condition for either a time out or VSWR fault. This high level on the output of U14C enables the free running oscillator, consisting of U15B, C, R27, C20, and C21, and causes the fault light to blink, indicating a fault condition.

At the same time U19A is set, both inputs of U28A are low causing its output to be high.

This biases on transistor pair Q6/Q7 to illuminate the Tune light. Should a fault occur, pin 1 of U28A goes high and the tune light will extinguish.

5.12.2.7 Lock Up/Retune

The purpose of the Lock Up/Retune circuitry is to re-initiate a tune cycle if the coupler elements have not reached their "home" positions or a ready condition has not occurred within the retune timer interval. This is necessary because the element home cycles are sometimes terminated by error signals from the detectors in order to shorten the tune cycle. However, certain antenna/frequency combinations may produce a "lock up" condition in which the element home cycles are terminated and insufficient/incorrect error signals will not allow the elements to complete tuning without going to their home positions first.

When tune flip-flop U8A is set by a tune initiate pulse, its Q output (pin 1) goes high and starts the 30 second timer and also the lock up retune timer consisting of U28B, R38, C28 and CR16. Approximately 7 seconds after U8A is set, C28 will charge to a logic 1 through R38 and will cause U28B pin 4 to go to a logic 0. This results in a logic 0 on U28C pin 9. If the force flip-flop U19B has not been set (indicating the elements have not reached home positions), U28C pin 8 will also be low. This causes U28C pin 10 to place a logic 1 on the set input of U25B. A logic 0 on U1 pin 3 will cause CR10 to force the output of U28C high and set U25B. R25 and C19 provide a time delay so that when U25B is set, both inputs to U28D are momentarily low resulting in a short positive pulse from U28D pin 11. This pulse clocks a logic 0 through the key enable flip flop U22B and also is gated into the tune initiate circuitry through U21D. This results in the transmitter being unkeyed and a tune cycle reinitiated resulting in the elements returning to their home positions before attempting to tune.

If a ready signal occurs before the lock up/retune timer times out, U8A is reset and causes C28 to quickly discharge through CR16 to ground.

Note that once the lock up/retune flip-flop U25B has been set, it can only be reset by a ready or power up/reset pulse. This prevents the coupler from cycling indefinitely if a successful tune does not follow a lock up/retune cycle.

The lock up/retune function is not required during a silent tune cycle. Consequently, a ground on the force/retune inhibit line (J2-9) pulls the output of U28D to a logic 0 through R26/CR9 to inhibit the lock up/retune pulse.

5.12.2.8 Elements Home Logic

Upon receiving a positive tune pulse, the C Home (U10B) and L Home (U10A) flip flops are set. Outputs from these flip flops are used by the servo control logic to steer the tuning elements towards their "home" positions. These cycles are sometimes interrupted in order to shorten the tune cycle time.

5.12.2.8.1 C Home

The C Home flip flop may be reset by four conditions: Power Up/Reset, VSWR $<$ 2:1, positive phase ( $+ \phi$ ), or by the C element reaching its "home" position (C max). At power up/reset, a pulse is gated through U21B/U14B and applied to the reset input of U10B. During a tune cycle if the VSWR falls below 2:1, a logic 1 will be gated through U1C/U21B/U14B to reset U10B. Also, a positive phase angle signal from the Phase Comparator will be gated through U3A to clock a log 0 through U10B to terminate the C Home cycle. If the C Home Cycle is not interrupted, it will be terminated when the Capacitor element engages its C Max (home) limit switch causing U14B to place a logic 1 on U10B's reset input.

5.12.2.8.2 L Home

The L Home flip flop (U10A) may be reset by four conditions: Power Up/Reset, VSWR < 2:1, magnitude less than 50 ohms (R < 50 ohm), or by the Inductor element reaching its "home" position (L Min). At Power Up/Reset, a pulse is gated through U21B/U7C and applied to the Reset input of U10A. During a tune cycle if the VSWR falls below 2:1, a logic 1 will be gated through U1C/U21B/U7C to reset U10A. Also a magnitude less than 50 ohms signal from the R Comparator will be gated through U1B to clock a logic 0 through U10A and terminate the L Home cycle. If the L Home cycle is not interrupted, it will be terminated when the Inductor element engages its L Min (home) limit switch causing U7C to place a logic 1 on U10A's reset input.

5.12.2.9 Force Logic

The conditions required to generate the force function will normally occur only during an initial tuning operation in the low frequency range. When the elements are at their home positions, the mismatch appears as such a high impedance load that very little line current is produced. Therefore, insufficient voltage is induced in the toroidal transformers of the discriminators and no output results. To correct this condition, the variable inductor is forced to run toward maximum inductance until the line impedance changes enough to provide an output from the phase discriminator. At this point, the capacitor and inductor will be actively driven from the discriminator outputs and normal tuning will be completed.

The actual circuit operation of the force function is as follows:

At the same time that U10A and B are reset by the elements at home signal, U19B is set, making its Q output on pin 13 high. Assuming that the output of the phase discriminator is not indicative of an inductive reactance, the force/retune inhibit line remains high, and the capacitor is at its home position, all inputs of U11A will be low. The output of U11A will be high and is inverted by U16A to result in a low level. This force instruction, which may be checked on TP5, is used in the servo control logic to force the variable inductor to run toward maximum inductance. As previously mentioned, when the capacitor moves off its limit switch the appropriate input of U10A goes high and the force instruction is terminated. Because there is a small time delay before the capacitor actually leaves is limit switch, an output from the capacitor drive-to-minimum control logic is also applied to the input of U11A to disrupt the forcing function. By gradually removing the forcing of the inductor as the phasing goes inductive, smoother, less violent movement is achieved. When the coupler has successfully tuned, U19B is reset by a low to high transition of the ready line applied to its clock input on pin 11.

The Force/Retune Inhibit function inhibits the force function during a silent tune cycle.

5.12.3 RF Power Status

This circuit monitors both the forward and reflected power levels, as sampled in the detector module, and provides four outputs: two metering outputs and two logic outputs. U13C and U13A buffer the forward and reflected power samples respectively for the metering lines.

The forward and reflected power levels are compared in U13B. The values of R9 and R10 have been chosen such that VSWR levels less than 2:1 will produce a high logic level at the output of U7B called VSWR < 2:1(+). This level may be checked at TP1.

The RF present (+) threshold is established by the reference voltage from divider R11 and R12 at the inverting input of comparator U13D. U13D compares the forward power output of U13A with the reference voltage to produce a high logic level at its output whenever the forward power sample exceeds this reference.

This logic level may be checked at TP2. This RF present signal is used to enable the servos when RF power is applied.

5.12.3.1 Ready/Fault Logic

To allow the coupler to achieve optimum matching, the elements are allowed to fine tune for approximately 2 seconds after the VSWR goes below 2:1.

After this delay, the ready light will light and the servos will be switched off.

The VSWR fault circuit also has a delay in order to reject minor VSWR excursions during the final phase of the tuning cycle. A VSWR fault will occur whenever the VSWR exceeds 2:1 for approximately 1 second. This short time delay allows the surveillance tuning action to operate over a wider range of mismatch than if no delay were present. During an actual tuning cycle, the VSWR is expected to exceed 2:1 and is not considered to represent a fault condition. If a matched, ready condition is not achieved within approximately 30 seconds after a tuning cycle has been initiated, a fault condition will be indicated and the servos disabled. Likewise, failure of the elements to reach their home positions will also cause a fault condition. A fault condition, for whatever reason, is indicated by a blinking of the fault light.

When DC power is initially applied, the tuned, ready/fault status of the coupler is unknown and retuning may or may not be necessary. This condition is indicated by a steady non-blinking illumination of the fault light. When RF is applied, the fault light will start blinking if the VSWR exceeds 2:1 or, if the coupler is already tuned, the ready light will light. The ready/fault detectors are always enabled and will display the coupler's tuned status as conditions dictate.

The actual circuit operation of the ready/fault logic is as follows:

U16E and U16D, CR2, R13, and C8 comprise the ready delay. When the VSWR goes below 2:1, pin 1 of U6A goes high. Pin 2 of U6A is also high whenever sufficient RF power is present. When the output of U6A goes low, C8 is allowed to discharge through R13. Eventually, as determined by the RC time constant of R13 and C8 the output of U16E goes high and clocks U22A. Assuming the data input of U22A is high, as is always the case except during homing, the Q output of U22A goes high, turns on transistor pairs Q10/Q11, and places the coupler in the ready mode. CR12 is used to quickly recharge C8 when the output from U6A returns high. During a silent tune cycle the ready delay is preempted and the attenuator delay is used instead in order to shorten the tune cycle.

U18F and U18E, CR4, R15, and C9 comprise the VSWR fault delay which operates identically to the ready delay circuit only when RF power is present. U6B inverts the VSWR line so that the output of U6C goes low when the VSWR exceeds 2:1.

Assuming a ready status already exists or the coupler has just been turned on, should the VSWR exceed 2:1, the output of U18F goes high and clocks U25A. If the data input of U25A is high, as is always the case except during a tuning cycle, the Q output of U25A will go high. The data input of U25A is held low during a tuning cycle to inhibit a false VSWR fault indication.

At the same time U25A is clocked, U22A is reset. This action will remove the ready signal, if present, and make Q high. With both inputs of U24B now high, its output will go low signifying a VSWR fault.

5.12.3.2 Attenuator Control Logic

During the tuning cycle, a 6 dB attenuator is switched in series with the RF input to the coupler. This provides protection for the transmitter/transceiver by limiting the impedance variations while tuning. The attenuator is switched out of the circuit just prior to the completion of the tune cycle.

The actual operation of the attenuator control logic is as follows:

U8B is set by the tune pulse and turns on transistor pairs Q4/Q5. This, in turn, activates the relay in the RF Module by completing a circuit-to-ground through Q5. Should the VSWR go below 2:1 for approximately 0.5 seconds, (as determined by the time delay consisting of U16F and U16B, CR5, R17 and C13) U8B will be reset and Q5 switched off. The time delay prevents the attenuator from being removed prematurely due to minor VSWR perturbations. Likewise, the data input of U8B is held high during homing for additional protection against premature attenuator removal.

During a silent tune cycle Q2 is biased off allowing the attenuator reset pulse to be clocked through R20/CR6 into U22A's clock input. This causes a ready status to be reached as soon as the attenuator is removed and shortens the tune cycle.

5.12.3.3 Key Enable

The Key Enable logic causes the exciter to produce a tune power RF signal for tuning purposes. The Key Enable line J2-19, 20 goes to the Interface Board where it is gated with other logic signals to control the exciter RF tune signal.

The Key Enable condition occurs after the Key Enable flip flop U22B has been set and a tune cycle is in progress. U22B is set when both inputs to U3B are low, signifying the elements have reached home positions. When this occurs U3B's output goes to logic 1 and sets U22B. U22B is reset by a Power Up/Reset pulse, Lockup/Retune function, or a fault condition. Therefore the Key Enable line will normally go to a logic 0 upon tune initiate unless one of these conditions has occurred.

When a Tune Cycle is in progress U28A's output will be high and U15A pin 1 will be high if U22B has been set. U15A's output turns on transistor pairs Q8/Q9. When U22B is reset by a Ready or U28A pin 1 goes to a logic 1 due to a cycle time out, the Key Enable line will return to a high state unkeying exciter.

5.12.3.4 Servo Enable Logic

The servo enable logic is used to turn the L and C servo systems on and off as required. The servo system is enabled during homing and tuning, and is disabled whenever power is initially applied, if a fault condition exists, or in the absence of sufficient RF power. The servo system is normally switched off after the coupler has tuned and the ready light lights. However, should the surveillance tuning feature be enabled, the servos will remain on.

The actual operation of the servo enable logic is as follows:

U3C produces a low level at its output whenever a fault condition exists or when the coupler is initially turned on. As a result, the output of U2C and pin 6 of U7B will be forced high.

During a homing condition, both inputs to U14A will be high; therefore, the output of U14 and pin 5 of U7B will be low. This forces the output of U7B high and the servo system is enabled to allow the elements to run toward their home positions. If the elements fail to home within the allotted time, pin 2 of U14A will go low and the output of U14A will go high. With both inputs of U7B now high, the output of U7B will go low and the servo system will be switched off.

At all times other than homing, pin 1 of U14A will be low, resulting in pin 5 of U7B being high. Consequently, the servo system will be controlled by the output status of U2C. A low on any input of U2C will turn the servos off.

As mentioned previously, pin 13 of U2C will be high in the absence of a fault or initial power on and pin 12 will be high whenever sufficient RF is present. The logic state of the remaining input of pin 13 is determined by the output status of U6D. If the Surveillance tuning feature is disabled, pin 12 of U6D will be pulled high through R43. When a tuning cycle is underway, the output of U6D will still be high since pin 3 of U6D will be low. However, after the coupler is tuned, pin 13 will go high with the Ready signal, the output of U6D will go low, and the servos will be switched off. Should Surveillance tuning feature be enabled, pin 12 of U6D will be pulled low and the output of U6D will be forced high.

5.12.3.5. Antenna Modification Logic

The Antenna Modification Logic provides a positive pulse on the Antenna Mod J1-3,4 line to the Interface Board causing the Antenna Modification solenoid to be activated on the Inductor Chassis Assembly.

During a tune cycle the Force function may occur and the network may not be able to achieve a positive phase angle. Consequently, the Capacitor will remain at its "home" position and the Inductor will be forced to its maximum limit (L Max). When this occurs, a logic 1 will occur on U27B pins 5 and 6. U27B/U27C/R93/C55 form a "one-shot" generator to plug a logic 0 pulse on U27C's output. This is gated through U27A and U27D to turn off Q31 momentarily, resulting in setting of the Antenna Modification flip-flop on the Interface Board.

The Capacitor element may also activate the Antenna Modification Logic. If, during a tune cycle, the Capacitor element receives a positive phase error signal causing it to leave its "home" limit switch and then returns - the Logic will be activated. The operation of the Capacitor "one-shot" logic is identical to that for the Inductor. Note that U27D pin 13 must be at a logic 1 to enable the Antenna Modification Logic to produce an output. U27D pin 13 will be high only if a Home cycle is not in progress; otherwise, the Antenna Modification Solenoid would be activated during a Home cycle whenever the capacitor reached its "home" position.

5.12.4 Input Specifications

| Connector/Pin No. | Signal Name/Function | Specification |
|---|---|---|
| J1-1,2,19,20 | −GND | Logic Ground, 0 Volts. |
| J1-5,6 | $\phi$ Signal | May vary from +5 VDC to −5 VDC. A positive voltage results in an output on J3-8 (C Run Max). A negative voltage results in an output on J3-9 (C Run Min). |
| J1-7,8 | $\phi$ REF | Signal ground for $\phi$ SIG. 0 volts. |
| J1-9,10 | R REF | Signal ground for R SIG. 0 volts. |
| J1-11,12 | R SIG | May vary from +5 VDC to −5 VDC. A positive voltage results in an output on J3-6 (L RUN Min). A negative voltage results in an output on J3-7 (L RUN Max). |
| J1-15,16 | Reflected Power | May vary from 0 to +5 VDC. A voltage 10 ±3% of the value of input voltage on J1-17, 18 (Forward Power) will result in a logic 0 on J2-15 (READY) after 2 ±.5 seconds and a logic 1 on TP1 (VSWR less than 2:1). This also results in an output on RFL Power Metering (J2-5,6). |
| J1-17,18 | Forward Power | May vary from 0 to ±5 VDC. 0.75 ±.25 volts is required to produce a logic 1 on TP2 (RF Present). This also results in an output on FWD Power Metering (J2-7,8). |
| J2-1,2,3,4 | GND | Logic Ground 0 volts. |
| J2-9 | Force/Return Inhibit | A Logic 1 will allow a Force Sequence or a Lock-Up/Retune sequence to occur. A logic 0 disables these sequences. In addition, a logic 0 causes the Ready sequence to occur after a 0.5 ±.25 sec delay after a logic 0 transistion of the Reflected Power input (J1-15,16). |
| J2-11,12 | Surveillance Tuning | Logic 0 will enable surveillance feature logic 1 on TP6 (Servo Enable +). |
| J3-3 | L-Min | A Logic 0 will inhibit an output from J3-6 (L RUN Min). A logic 0 also interrupts the L Home cycle and is required in conjunction with a logic 1 on J3-4 (C Max) to advance a tune cycle. |
| J3-4 | C Max | A logic 1 will inhibit an output from J3-8 (C RUN Max). A logic 1 also interrupts the C Home Cycle and is required in conjunction with a logic 0 on J3-3 (L Min) to advance a tune cycle. In addition, a logic 1 causes a logic 1 pulse on the Antenna Mod output (J1-3,4). |
| J3-C | L Max | A logic 0 will inhibit an output on J3-7 (L RUN Max). A logic 0 will also cause a logic 1 pulse on the Antenna Mod output (J1-3,4). |

5.12.4 Input Specifications (Con't)

| | | |
|---|---|---|
| J3-D | C Min | A logic 1 will inhibit an output from J3-9 (C RUN Min). A logic 1 will also force a C Min retune sequence. |
| J3-E,F,H,J,K,L,10 | GND | Servo motor ground, 0 volts. |
| J3-B | +15 volts Unreg. | Requires 15 ±4 volts DC at 100 mA maximum. |
| J2-23,24,25,26 | +28 volts | Requires 28 ±4 VDC at 6A maximum. |
| J2-21,22 | Tune Initiate | A logic 0 pulse (0.5 msec minimum) initiates Tune Cycle sequence. |

5.12.5 Output Specifications

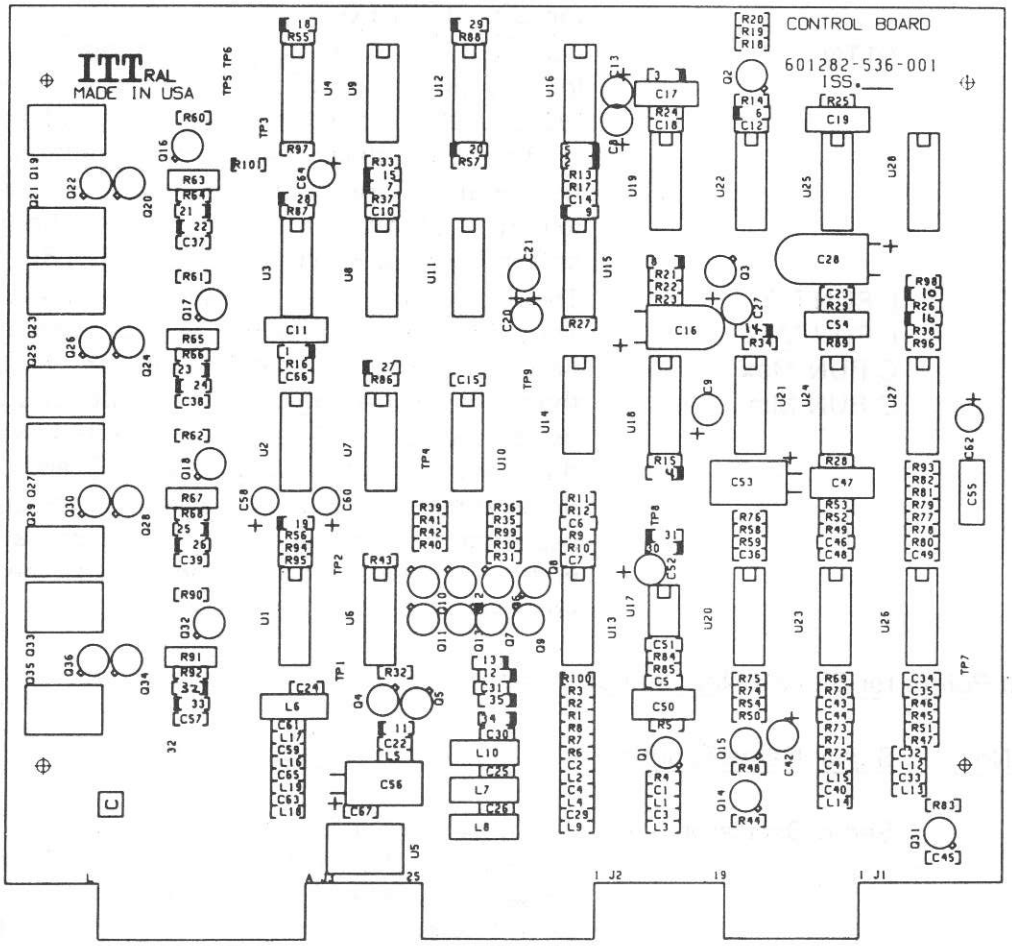
| Connector/Pin No. | Signal Name/Function | Specification |
|---|---|---|
| J2-5,6 | RFL Power Metering | Delivers an output voltage proportional (±10%) to the input voltage applied to J1-15, 16. |
| J1-17,18 | FWD Power Metering | Delivers an output voltage proportional (±10%) to the input voltage applied to J1-17, 18. |
| J1-3,4 | Antenna Mod | Open collector output; delivers a logic 1 pulse 10 ±5 mSec during an Antenna Modification sequence. |
| J2-13,14 | STANDBY/FAULT | Open collector output; goes to logic 0 at initial power on and goes to logic 1 during a Tune Cycle. Goes to a logic 0 following a Tune Cycle Time-out (Fault) condition and goes to an alternating logic 1/logic 0 state (frequency = ±1 +.25 Hz) following a VSWR or a 30 second Tune Cycle time out fault condition. |
| J2-15,16 | Ready | Open collector output; goes to a logic 0 after a 2 ±.25 second delay whenever the input voltage on the reflected power line (J-15, 16) is less than 10 ±3% of the voltage on the Forward Power line (J1-17, 18). This delay is shortened to 0.5 ±.25 seconds if the Force/Retune Inhibit input (J2-9) is at logic 0. This output will go to a logic 1 during a Fault sequence whenever the Reflected Power input voltage is greater than 10 ±3% of the Forward Power input voltage J1-17, 18 for more than 0.5 ±.25 seconds. |
| J2-17,18 | Tune | Open collector output; goes to a logic 0 whenever a logic 0 pulse occurs at the Tune Initiate input J2-21 and returns to a logic 1 after a Ready or Fault condition occurs. |

5.12.5 Output Specifications (Con't)

| | | |
|---|---|---|
| J2-19,20 | Key Enable | Open collector output; goes to logic 0 after C Max (J3-4) and L Min (J3-3) inputs go to logic 0 concurrently. Returns to a logic 1 after a Ready, Fault, or Lock-Up/Retune sequence occurs. This output also remains at logic 0 during a Lock-Up/Retune sequence if the Force/Retune Inhibit input (J2-9) remains at logic 0. |
| J3-5 | ATTN | Open collector output; goes to a logic 0 when a logic 0 pulse occurs at the Tune Initiate input (J2-21, 22) and returns to a logic 1 after a 0.5 ±.25 second delay following a condition where the input voltage on the Reflected Power input (J1-15, 16) is less than 10 ±3% of the voltage on the Forward Power Input (J1-17, 18). |
| J3-6<br>J3-7<br>J3-8<br>J3-9 | L RUN Min<br>L RUN Max<br>C RUN Max<br>C RUN Min | These outputs remain at logic 0 except during a Tune Cycle or during a Surveillance Tuning condition. At logic 0, the output voltages will be less than 1.5 VDC. At logic 1, the output voltages will rise to a value not less than 1.5 volts lower than the input voltage at J2-23, 24, 25 and 26. At times other than during a Home cycle or Force sequence, the logic 1 voltages may be pulse-width modulated proportionally to the input voltages at J1-11, 12 and J1-5, 6. |

5.12.6 Test Points for Signals Not Defined in Input/Output Specifications

| Connector/Pin No. | Signal Name/Function | Specification |
|---|---|---|
| TP7 | Servo Oscillator | Triangular waveform; frequency = 300 Hz ±10% Low Point is less than 0.5 VDC, Signal is present only when the voltage at J1-17, 18 (Forward Power) is greater than 0.75 VDC ±10%. |
| TP8 | −5V | −5 VDC ±5%, present only when the voltage J1-17, 18 (Forward Power) is greater than 0.75 VDC ±10%. |
| TP9 | +8V | +8 VDC +5%. |



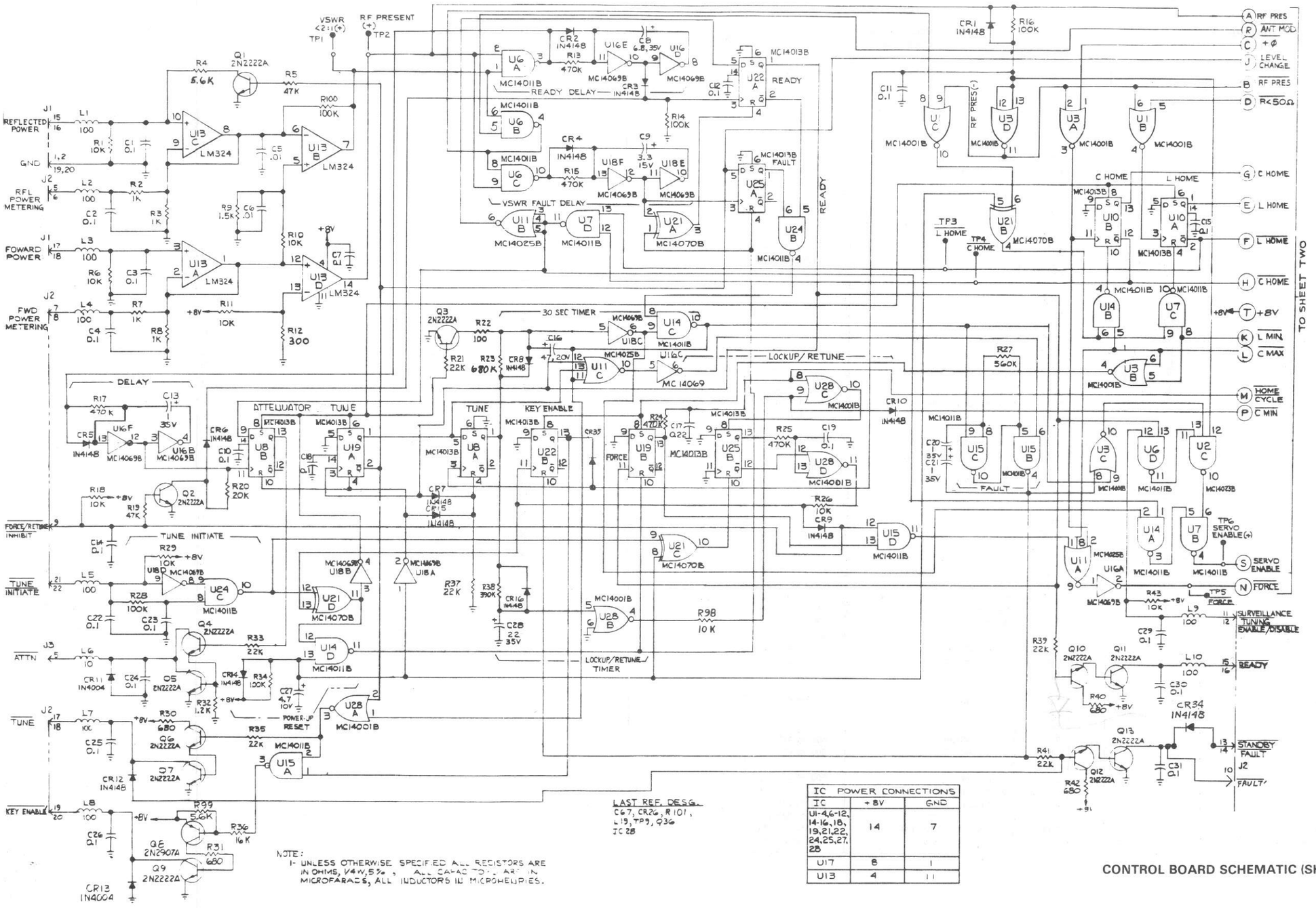

**CONTROL BOARD**

## CONTROL BOARD (601282-536)

| Symbol | Description | Part Number |
|---|---|---|
| C1-4,7, 10 15, 22-26, 29-33, 35, 37 41,45, 48,49, 57,59, 61,63, 65-67 | Capacitor, .1 uF, 50V | 600272-314-001 |
| C5,6,34, 43,44, 46,51 | Capacitor, .01 uF, 50V | 600272-314-002 |
| C8 | Capacitor, 6.8 uF, 35V | 600202-314-017 |
| C9 | Capacitor, 3.3 uF, 15V | 600202-314-012 |
| C11,17, 19,54,55 | Capacitor, .1 uF | 600204-314-020 |
| C13,20, 21,42,52 | Capacitor, 1 uF, 35V | 600202-314-007 |
| C16 | Capacitor, 47 uF, 20V | 600202-314-044 |
| C27 | Capacitor, 4.7 uF, 10V | 600202-314-014 |
| C28 | Capacitor, 22 uF, 35V | 600202-314-041 |
| C47 | Capacitor, 15 uF | 600204-314-027 |
| C50 | Capacitor, 470 pF | 647003-306-501 |
| C53-56 | Capacitor, 47 uF, 50V | 600297-314-026 |
| C58,60, 62,64 | Capacitor, 10 uF, 50V | 600297-313-013 |
| CR1-10, 12, 14-16, 18, 20 27-31, 35 | Diode 1N4148 | 600109-410-001 |
| CR11, 13, 21-26, 32, 33, 34 | Diode 1N4004 | 600011-416-002 |
| L1-5,9, 12-19 | Coil, 100 uH | 600125-376-002 |
| L6 | Coil, 10 uH | 600072-376-025 |
| L7,8,10 | Coil, 100 uH | 600072-376-037 |
| Q1-7, 9-18,20, 24,28, 31,32,34 | Transistor 2N2222A | 600080-413-001 |
| Q19,23, 27,33 | Transistor 2N5494 | 600196-413-001 |
| Q21,25, 29,35 | Transistor 2N6109 | 600215-413-001 |
| Q8,22, 26,30,36 | Transistor 2N2907A | 600154-413-001 |
| R1,6,10, 11,18, 25,26, 29,43, 45,47, 49,58, 59,70, 72,76, 79,81, 85,97,98 | Resistor, 10K, 1/4W, 5% | 610024-341-075 |

## CONTROL BOARD (601282-536)

| Symbol | Description | Part Number |
|---|---|---|
| R2,3,7, 8,64, 66,68, 84,92, | Resistor, 1K, 1/4W, 5% | 610014-341-075 |
| R5,19, 50,54 | Resistor, 47K, 1/4W, 5% | 647024-341-075 |
| R80 | Resistor, 15K, 1/4W, 5% | 615024-341-075 |
| R12 | Resistor, 300, 1/4W, 5% | 630004-341-075 |
| R13,15, 17,24, 25 | Resistor, 470K, 1/4W, 5% | 647034-341-075 |
| R14,16, 28,34, 100 | Resistor, 100K, 1/4W, 5% | 610034-341-075 |
| R20,46, 69 | Resistor, 20K, 1/4W, 5% | 620024-341-075 |
| R21,33, 35,37, 39,41, 52,53, 60-62, 74,75, 83,90 | Resistor, 22K, 1/4W, 5% | 622024-341-075 |
| R22 | Resistor, 100K, 1/4W, 5% | 610004-341-075 |
| R23 | Resistor, 680K, 1/4W, 5% | 668034-341-075 |
| R27 | Resistor, 560K, 1/4W, 5% | 656034-341-075 |
| R30,31, 40,42 | Resistor, 680K, 1/4W, 5% | 668004-341-075 |
| R32 | Resistor, 1.2K, 1/4W, 5% | 612014-341-075 |
| R38 | Resistor, 390K, 1/4W, 5% | 639034-341-075 |
| R44,48,82 | Resistor, 3.3K, 1/4W, 5% | 633014-341-075 |
| R78 | Resistor, 2.2K, 1/4W, 5% | 622014-341-075 |
| R51 | Resistor, 75K, 1/4W, 5% | 675034-341-075 |
| R55-57, 71, 86-88 | Resistor, 3.9K, 1/4W, 5% | 639014-341-075 |
| R63,65, 67,91 | Resistor, 2.2K, 1/2W, 5% | 622014-341-205 |
| R73,89, 93 | Resistor, 200K, 1/4W, 5% | 620034-341-075 |
| R77 | Resistor, 7.5K, 1/4W, 5% | 675014-341-075 |
| R101 | Resistor, 0K, 1/4W | 600000-341-075 |
| U1,3,28 | I.C. LM324 | 600078-415-101 |
| U2,4 | I.C. MC14023B | 600081-415-101 |
| U5 | I.C. A78M08UC | 600399-415-001 |
| U6,7, 14,15, 24,17 | I.C. MC14011B | 600079-415-101 |
| U8,10, 19,22, 25 | I.C. MC14013B | 600080-415-101 |
| U9,21 | I.C. MC14070B | 600188-415-101 |
| U13,20, 23,26 | I.C. LM324 | 600171-415-001 |
| U16,18 | I.C. MC14069UB | 600211-415-101 |
| U17 | I.C. NE555 | 600074-415-001 |
| R9 | Resistor, 1.5K, 1/4W, 5% | 615014-341-075 |
| R99,4 | Resistor, 5.6K, 1/4W, 5% | 656014-341-075 |
| R36 | Resistor, 16K, 1/4W, 5% | 616024-341-075 |

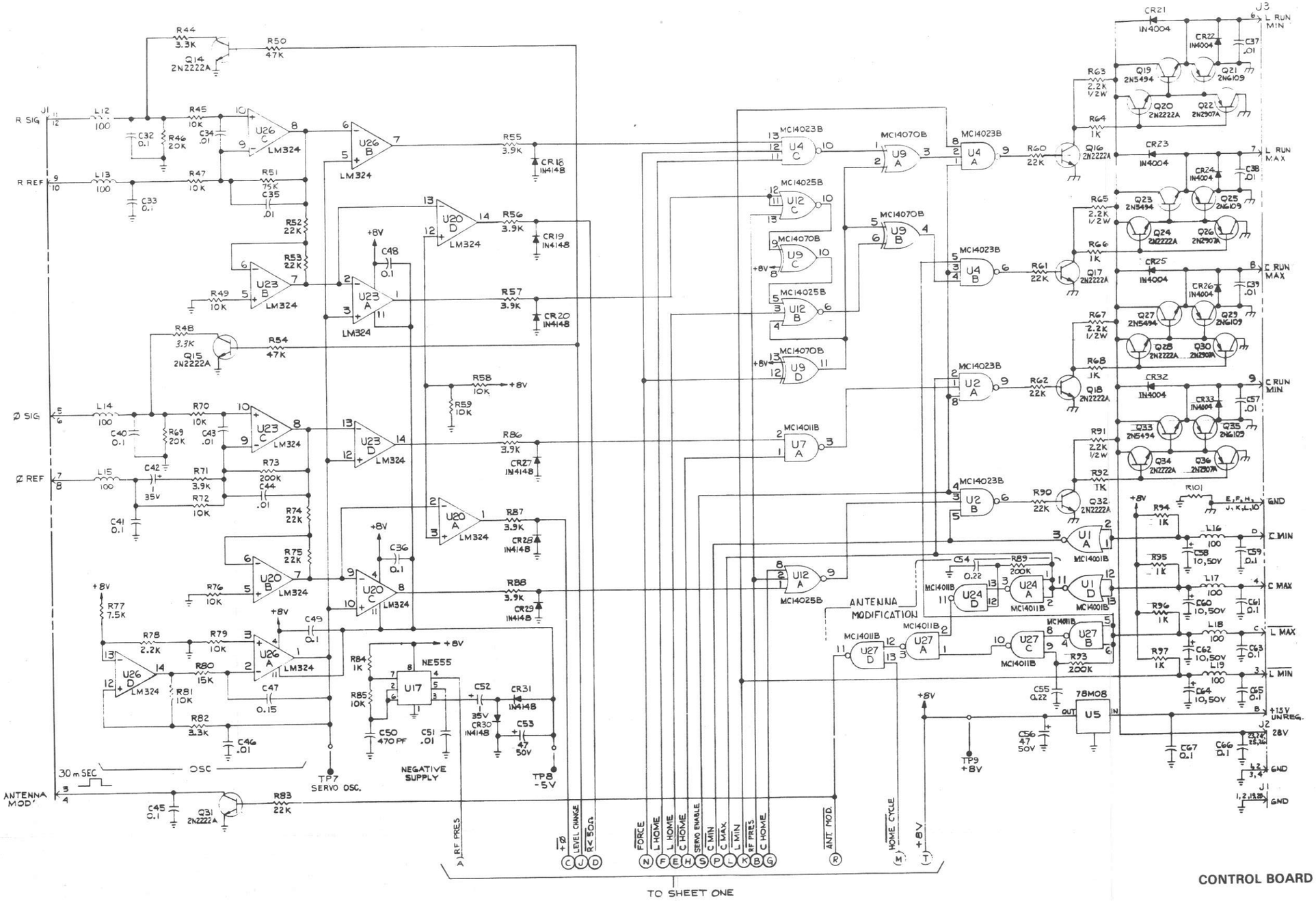



LAST REF. DES.
C67, CR26, R101, L19, TP9, Q36 IC 28

| IC POWER CONNECTIONS | | |
|---|---|---|
| IC | +8V | GND |
| U1-4,6-12, 14-16,18, 19,21,22, 24,25,27, 28 | 14 | 7 |
| U17 | 8 | 1 |
| U13 | 4 | 11 |

NOTE:
1- UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS, 1/4W, 5%, ALL CAPACITORS ARE IN MICROFARADS, ALL INDUCTORS IN MICROHENRIES.

CONTROL BOARD SCHEMATIC (SHEET 1 OF 2)




CONTROL BOARD SCHEMATIC (SHEET 2 OF 2)

## 5.13 CONNECTOR BOARD

### 5.13.1 General

The connector board provides AC power and control line interconnections between the external control cable and the coupler circuitry. The control line connector is mounted on the PC board and is secured to the case by 6-32 threaded studs. The connector board is connected to the mother board by a plug-on 40-conductor ribbon cable. All lines are bypassed by either axial-lead capacitors or a buffered inverter circuit on the connector board. The connector board also provides on board features to operate the coupler and determine its status locally. Additionally, it incorporates an AC switch and a 115/230 VAC option plug.

### 5.13.2 Filtering

Primarily, the connector board provides an interconnection for the control lines between the external control circuits and the logic in the MSR-4030. However, a secondary purpose is to provide additional filtering to protect these control lines from transients and RF interference. Some of the control lines from J11 are filtered by .1 mf capacitors. The other control lines are filtered by a buffer/inverter circuit used to suppress noise and to insure correct logic levels. All of these lines operate the same, to J11, pin "a" will be used for the example circuit. If a logic 1 comes into pin "a," it will be filtered by L15 and C15. CR15 is used to block the DC voltage into the anode of CR35, where the 1 k pullup resistor in Z3 provides 5 VDC through Pin 6. CR35 is a Zener diode that keeps the voltage at 3.3. VDC. R15 provides the Zener current as the voltage on U3 Pin 12 forward biases the NPN transistor which pulls the 5 VDC low through R22. Therefore, a high or no connection at Pin "a" will cause a low at the output of J15, Pin 36. If Pin "a" is low or sinking a current, then this will be felt through CR15, pulling the voltage at the anode of CR35 low. This, in turn, will cause a low to be applied to Pin 12 of U3, shutting OFF the NPN transistor. Because R22 provides a 5 VDC pullup to line 36 of J15, then the output will now be high.

### 5.13.3 On Board Functions

In addition to supplying an interconnection interface, the connector board provides on board features to control the MSR-4030 locally from this board. These were provided to increase the safety of repair and ease of maintenance for the coupler from its remoted location.

"Push to Tune" pushbutton - this momentary switch (S2) shorts J11, Pin "j" to ground causing the "tune" line to go on and the coupler to tune.

"Silent Tune" pushbutton - this momentary switch (S1) shorts J11, Pin "h" to ground causing the "Silent Tune" line to go low. This causes the coupler to tune from the information stored in one of the preset 95 memory channels.

"Tx Inhibit" switch - this slide switch (DPDT) is ordinarily in the "Normal" mode, which allows normal coupler tuning. It can be switched to "Tx Inhibit" so that the "Tx Interlock (n/o)" line is grounded. This causes an LED indicator to light and prevents the remote keying of the transmitter to protect the safety of the person servicing the coupler. CR38 pulls the Tx Interlock line (N/C) to a logic 0 when the Coupler power is off to allow the transmitter to be keyed.

### 5.13.4 Status Indicators

In addition to controlling the coupler from the connector board, there are three LED indicators that show coupler status. They are located on top of the board near the tune switches so they can be easily seen. DS1 is a red LED indicator that shows a coupler fault condition. DS2 is a yellow LED indicator that shows the coupler in a

tune mode. DS3 is a green LED indicator that lights when the coupler tunes and goes to "Ready."

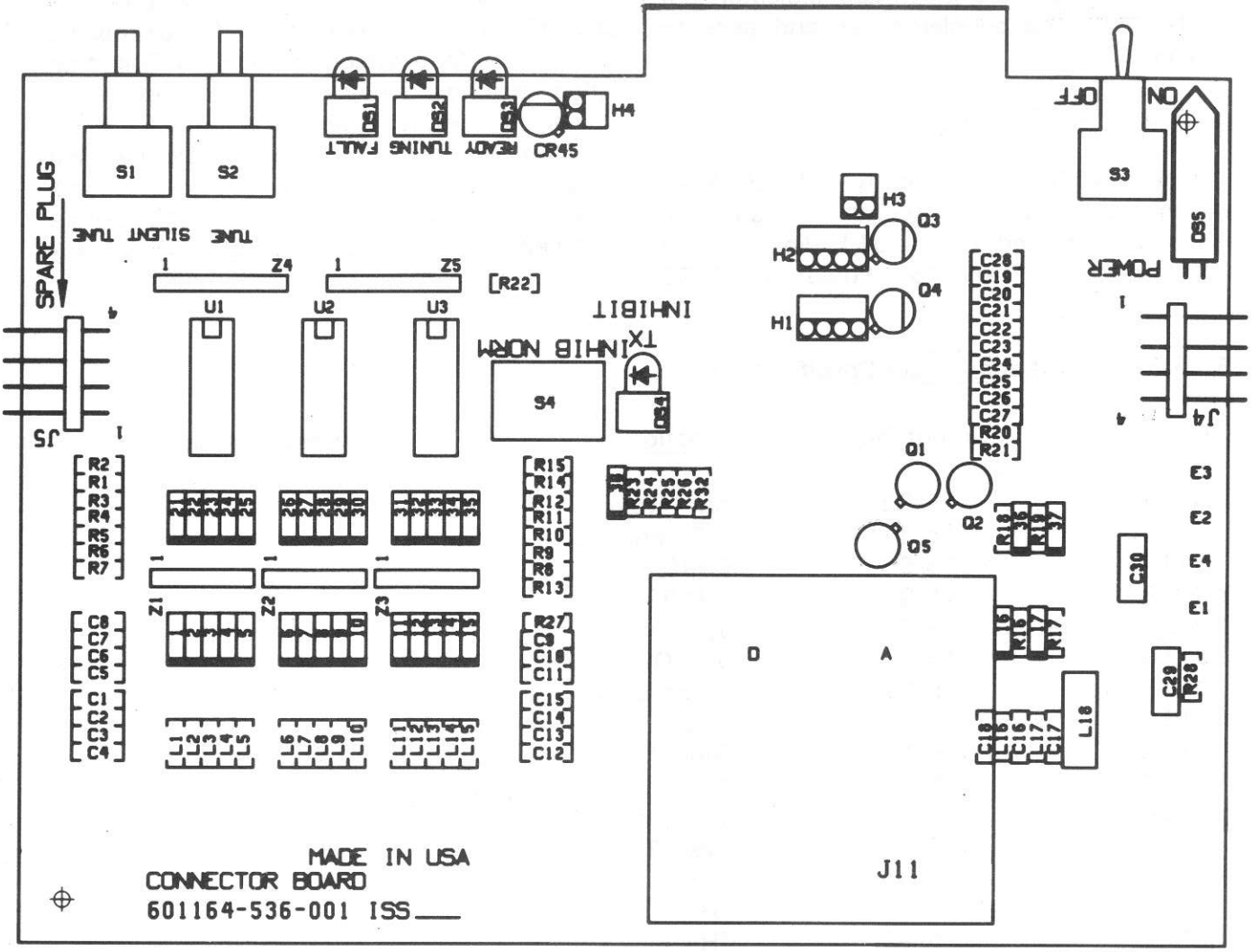
5.13.5 AC Section

The MSR-4030 is powered by 115/230 VAC which goes through the connector board. The AC power is routed through J11, Pins "g" and "n" and Pins "h" and "p." Power switch S3 allows a local position to turn the coupler ON and OFF for ease of servicing. R28 is a dropping resistor for DS5 which is a NEON Bulb that lights to indicate power is turned on to the coupler. The AC is routed out through E1-E4 on a molex plug to the power transformer and coupler power supply. J4 provides a jack whereby a 115 VAC or 230 VAC plug can be installed to select either AC voltage. J5 is a jack provided to store the unused AC plug.

5.13.6 Input and Output Specifications

| Input Pin | Output Pin | Function | Specification |
|---|---|---|---|
| J11-d | J15-32 | Auto-Home | * |
| J11-S | J15-39 | O.T. Inhibit/BDC Invert | * |
| J11-j | J15-6 | CH40 | * |
| J11-s | J15-8 | CH10 | * |
| J11-m | J15-10 | Bypass Sw | * |
| J11-e | J15-1 | O.T. Override P.B. | * |
| J11-f | J15-12 | Group Select | * |
| J11-Z | J15-3 | CH2 | * |
| J11-J | J15-11 | Tune P.B. | * |
| J11-P | J15-13 | Program/Tune P.B. | * |
| J11-D | J15-15 | Surveillance | * |
| J11-H | J15-17 | Silent Tune P.B. | * |
| J11-N | J15-21 | CH8 | * |
| J11-E | J15-31 | CH1 | * |
| J11-L | J15-37 | CH4 | * |
| J11-T | J15-34 | CH20 | * |
| J11-a | J15-36 | CH80 | * |

*An Input of less than 2.5 VDC (Low) will result in an Output of 5 ±.3 VDC (high). An Input voltage greater than 3 VDC (high) will result in an output of less than 0.5 VDC (low).

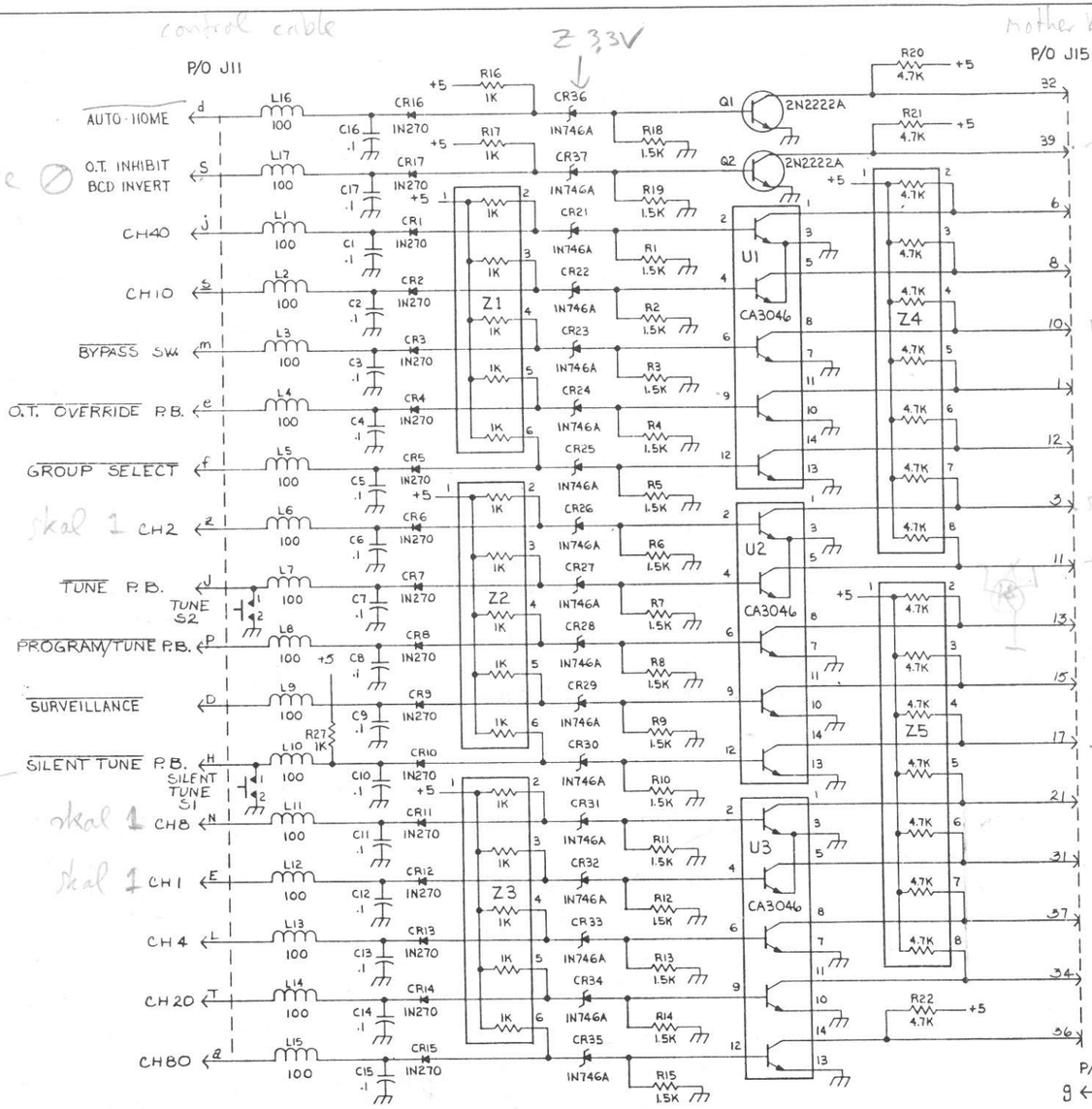



**CONNECTOR BOARD (601164-536)**

| Symbol | Description | Part Number |
|---|---|---|
| C1-28,31-38 | Capacitor, .1 UF, 50V | 600272-314-001 |
| C29,30 | Capacitor, .001 uF, 1KV | 600189-314-014 |
| CR1-17,38, 39,41 | Diode, 1N270 | 600052-410-001 |
| CR21-37 | Diode, 1N746A | 600002-411-001 |
| CR40,42-44 | Diode, 1N4148 | 600109-410-001 |
| — | Led Mount | 600005-635-001 |
| — | Protective Shield | 600841-609-001 |
| CR45 | Diode, LM335Z | 600598-415-001 |
| DS1, 4 | Led, Red | 600036-390-001 |
| DS2 | Led, Yellow | 600043-390-002 |
| DS3 | Led, Green | 600043-390-001 |
| DS5 | Neon Lmp | 600076-390-001 |
| H1, 2 | Component Mtg. | 600064-419-001 |
| H3,4 | Component Mtg. | 600064-419-004 |
| J4,5 | Header | 600078-608-028 |
| L1-17 | Coil, 10 uH | 600125-376-002 |
| L18 | Coil, 10 uH | 600072-376-025 |

**CONNECTOR BOARD (601164-536)**

| Symbol | Description | Part Number |
|---|---|---|
| P4 | Plug, 115 VAC | 600138-611-001 |
| P5 | Plug, 230 VAC | 600138-611-002 |
| P16 | Plug, 6P | 600264-606-003 |
| — | Pins, Plug (P16) | 600265-230-001 |
| Q1,2,3,4,5 | Transistor, 2N2222A | 600080-413-001 |
| R1-15, 18, 19 | Resistor, 1.5K, 1/4W, 5% | 615014-341-075 |
| R16,17,27,32 | Resistor, 1.0K, 1/4W, 5% | 610014-341-075 |
| R20-22,29 | Resistor, 4.7K, 1/4W, 5% | 647014-341-075 |
| R23-26 | Resistor, 160, 1/4W, 5% | 616004-341-075 |
| R28 | Resistor, 100K, 1/4W, 5% | 610034-341-075 |
| R30 | Resistor, 470 ohm, 1/4W, 5% | 647004-341-075 |
| S1, 2 | Mom. Switch, SPDT | 600204-616-001 |
| S3 | Switch, DPDT | 600250-616-002 |
| S4 | Slide Switch, DPDT | 600130-616-001 |
| U1,2,3 | IC CA3045 | 600038-415-002 |
| Z1,2,3 | Res. Net 1.0K | 600201-537-002 |
| Z4,5 | Res. Net 4.7K | 600201-537-001 |
| — | Pad, Transistor | 600025-419-001 |

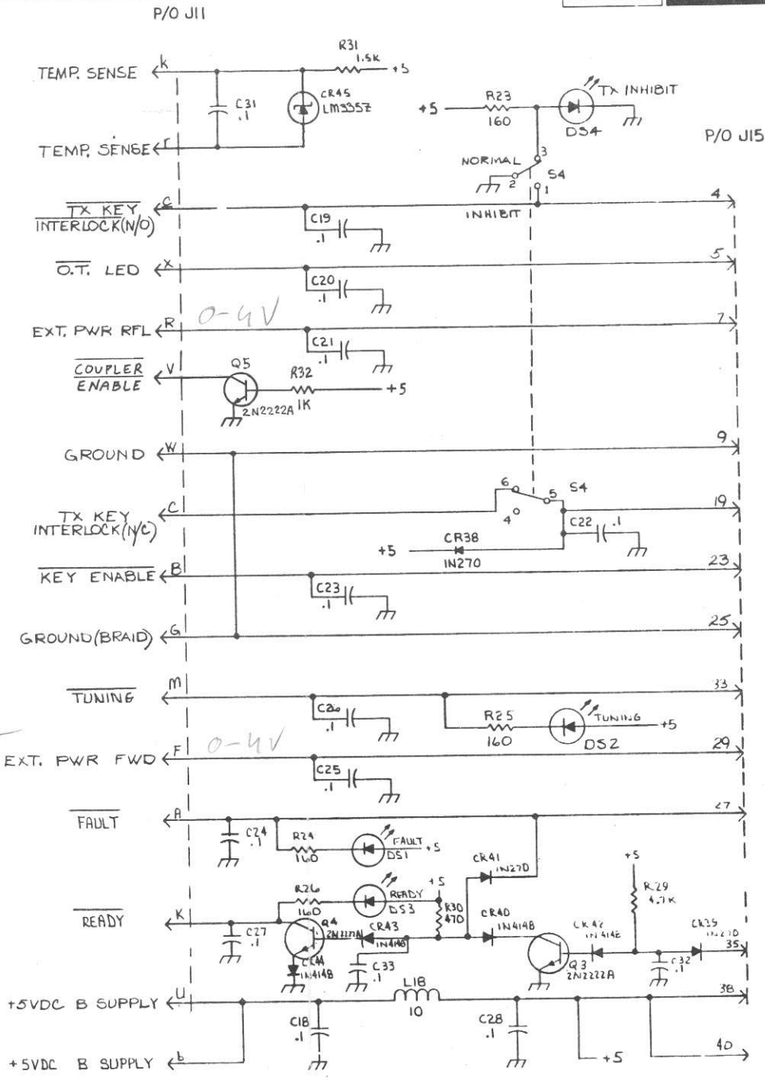


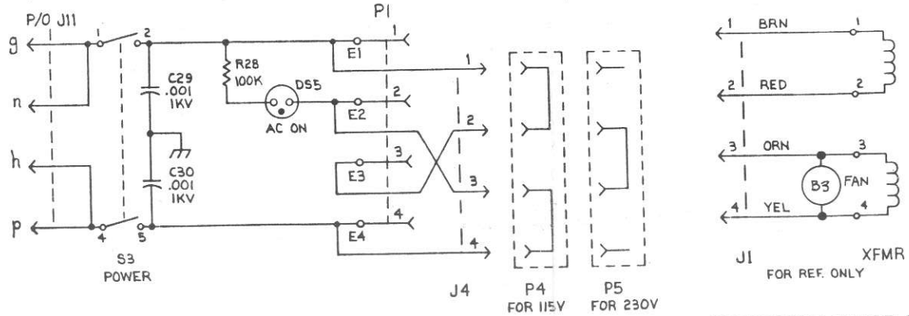

NOTES

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS RATED IN OHMS, 1/4 W, 5%
   ALL CAPACITORS RATED IN MFD.
   ALL INDUCTORS RATED IN MICROHENRIES.
   ALL ZENERS RATED 3.3V

| LAST REF. DESIG. USED | |
|---|---|
| C33 | R32 |
| CR45 | S4 |
| DS5 | U3 |
| J15 | Z5 |
| P5 | |
| Q5 | |

CR18-CR20 UNASSIGNED




CONNECTOR BOARD SCHEMATIC

5.13.6.1 Interconnection Specification

The connector board provides an interface connection between the control cable at J11 and the mother board (601168-536-001) through J15. There will be continuity on this board between the following Pins:

| Pin | Pin | Function |
|---|---|---|
| J15-4 | J11-c | Tx key interlock (n/o) |
| J15-5 | J11-x | O.T. LED |
| J15-7 | J11-R | Ext. Power RFL |
| J15-9 | J11-V | Coupler Enable |
| J11-W | J15-9 | Ground |
| J15-19 | J11-C | Tx Key Interlock (n/c) |
| J15-23 | J11-B | Key Enable |
| J11-G | J15-25 | Ground (Braid) |
| J15-27 | J11-A | Fault LED |
| J15-29 | J11-F | Ext. Power FWD |
| J15-33 | J11-M | Tuning LED |
| J15-35 | J11-K | Ready LED |
| J15-38 | J11-U | +5 VDC B Supply |
| J15-40 | J11-b | +5 VDC B Supply |

5.13.6.2 Switch Specifications

(S1) Enabled — applies ground to J11, H Disabled open circuit
(S2) Enabled — applies ground to J11
(S3) On — applies AC from J11, g and n to E1 and AC from J11, h and p to E4
Off — open circuit
(S4) Normal — ground +5 VDC through R23 at DS1 and shorts J15, 19 to J2, C
Enable — grounds J11, c, allows DS4 to light, and opens J15, 19 and J11, C

5.13.6.3 Status Indicator Specifications

(DS1) — lights when enabled (ground on J15-27)
(DS2) — lights when enabled (ground on J15-33)
(DS3) — lights when enabled (ground on J15-35)
(DS4) — lights when S4 is in the "Tx Inhibit" mode
(DS5) — lights when S3 is switched ON

5.13.6.4 115/230 VAC Plug Option

115 VAC operation - whenever P4 is plugged on J4, E1 is connected to E3 and E2 is connected to E4.

230 VAC operation - whenever P5 is plugged on J4, E2 is connected to E3.

## 5.14 OPTICOUPLER BOARD

5.14.1 General

The purpose of the Opticoupler PC board is to provide logic level pulses to the up-down counters located on the memory board. These pulses are counted and the information is stored in the memory board. In this way, location data can be used and stored electronically for the mechanical operation of the variable capacitor or inductor.

The Opticoupler board contains two groups of boards -601170-536-001 is used on the inductor chassis assembly and the 601170-576-002 board is used on the capacitor chassis assembly. The only difference between these groups of boards is the spacing of phototransistors Q1 and Q2. They are spaced further apart in the 601170-536-001 board due to the larger decoder disk used by the inductor.

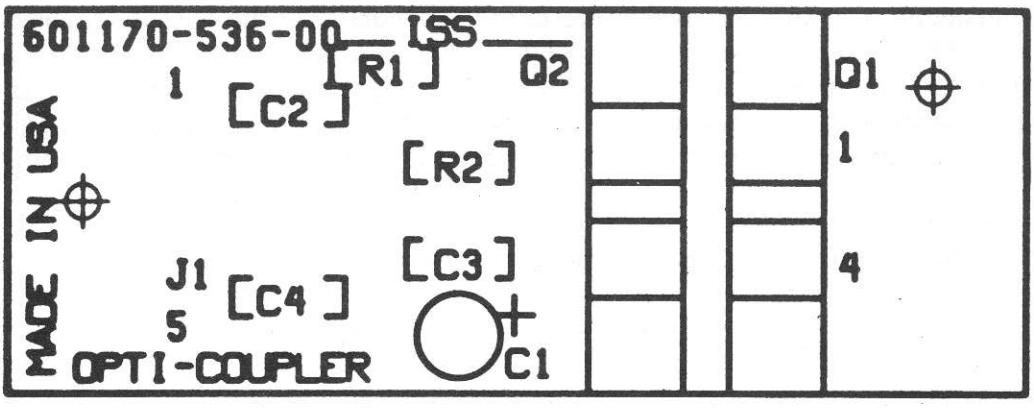
### 5.14.2 Description

The Opticoupler PC board contains two phototransistors, Q1 and Q2, which are gated ON and OFF by the encoder disk which is located on the capacitor shaft. Source current for the transistors is provided by R1 and R2. C1-C4 remove unwanted noise from the lines.

As the encoder disk rotates through the slots in Q1 and Q2, each transistor is alternately turned ON and OFF. The spacing between Q1 and Q2 is such that the output signals on J1 pins 2 and 3 will be leading or lagging by 90 degrees, depending on the element's rotational direction. The output of J1-2 will be lagging the output at J1-3 when the element is homing.

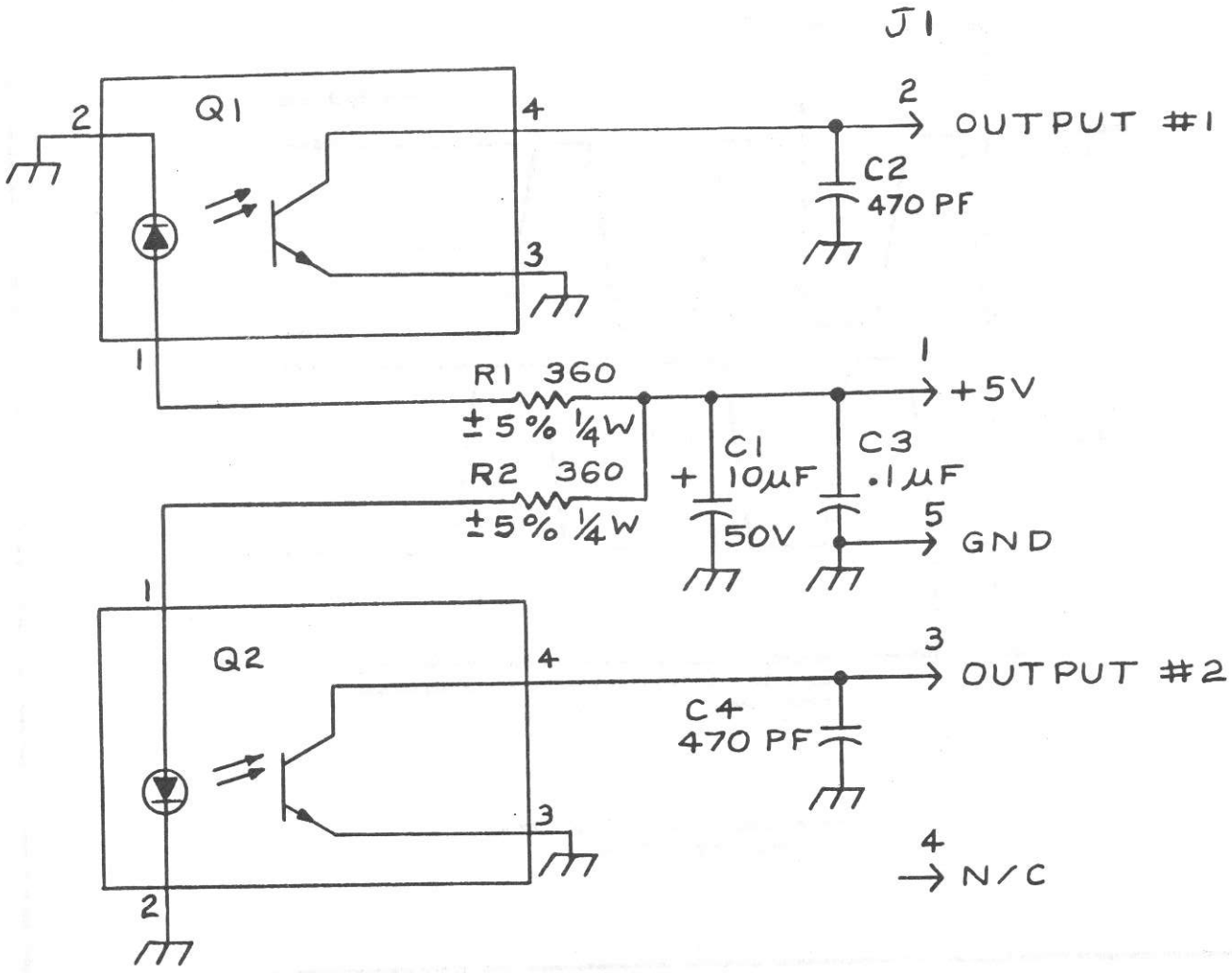
### 5.14.3 Input and Output Specifications

| Pin | Input/Output | Function | Specification |
|---|---|---|---|
| J1-3 | Output | Output No. 2 | Opticoupler Board pulsed waveform (see Figure 5.9) |
| J1-2 | Output | Output No. 1 | Opticoupler Board pulsed waveform (see Figure 5.9) |
| J1-5 | — | Ground | GND for Opticoupler Board |
| | — | No Connection | |
| J1-1 | Input | +5 VDC | +5 VDC ±.3V to Opticoupler Board |




**OPTICOUPLER PCB**
**(601170-536)**

| Symbol | Description | Part Number |
|---|---|---|
| C1 | Capacitor, 10 uF, 50V | 600297-314-013 |
| C2,4 | Capacitor, 470 pF | 600272-314-005 |
| C3 | Capacitor, 0.1 uF | 600272-314-001 |
| Q1,2 | Phototransistor | 600011-373-001 |
| R1,2 | Resistor, 200K, 1/4W | 620004-341-075 |




**OPTICOUPLER BOARD SCHEMATIC**

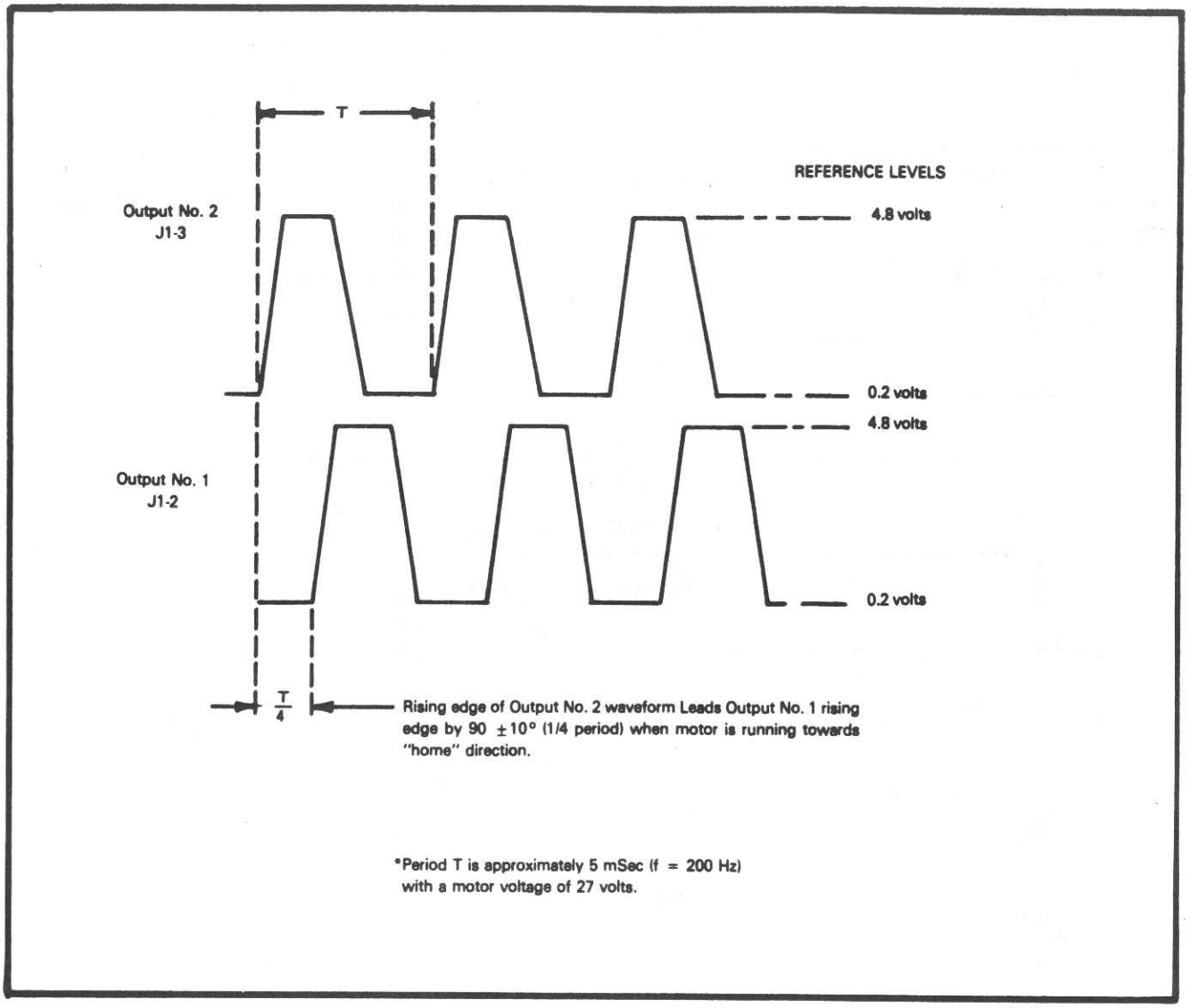



**Figure 5.9 Opticoupler Waveform**

## 5.15 MEMORY BOARD

### 5.15.1 General

The Memory Board contains the majority of circuitry required for the MSR-4030 "Silent Tune" feature.

### 5.15.2 Description

The function of the Memory Board is to provide a means for storing the positions of the Coupler's tuning elements into memory upon completion of a normal tuning cycle with RF power. Then it can generate the necessary control signals to allow the element servomotors to reposition the elements to their previously tuned positions during a "Silent Tune" cycle. The memory has capacity for 96 channels or previous tunes. The Memory Board structure is such that two nearly identical circuits exist: one for the Inductor element and one for the Capacitor element. The circuits share the same memory, address, and read/write functions. For this reason, only the Inductor circuitry is discussed.

#### 5.15.2.1 L Counter Encoder

The L Counter Encoder receives two square-wave signals from the Inductor Opticoupler PCB/Encoder Disk Assembly. These logic-level signals are in quadrature phase such that one signal leads or lags the other by 90 degrees, depending on the direction the Inductor is rotating. These signals are amplified, buffered, and processed by an edge detector circuit. This results in a clock signal 0 L, and an up-down signal, U/D. When the inductor is homing, the up-down signal will be low during the positive going transitions of the clock signal. This will cause the L counter to count down. Conversely, the clock signal transitions will occur when the up-down signal is high for a count-up sequence.

The two L Opticoupler outputs enter the Memory Board on Pins 23 and 30 of P4. L3 and C1 filter the L input 1 signal and L4-C2 filter the L input 2 signal. R1 and R3 are pull-up resistors for the open-collector opticoupler outputs. Each signal is applied to an inverting input of OP AMP U36, sections A and B. Resistors R16 And R17 form a voltage divider to reference the non-inverting inputs of U36 to 2.5 volts. Whenever a signal at the inverting input of U36 exceeds 2.5 volts, the output will go to a logic 0. Resistors R2 and R4 insure that the outputs of U36 will pull down to a logic 0.

The output of U36, Pin 1, is processed by R18-C84, U9, and U1. This circuitry forms an edge detector and produces a clock signal $\phi$ L that is twice the frequency of the L input 1 signal. An up-down signal is derived by feeding the output of U36A and B (buffered by U9A and C) into exclusive OR gate U1-B. This results in a signal that toggles at twice the frequency of each L input. When observed with the positive transitions of the $\phi$ L signal, this U/D signal represents the direction of rotation.

### 5.15.2.2 L Counter

The L (Inductor) Counter is a 12-bit binary up/down counter consisting of three 4-bit counters cascaded. The counter resets when the Inductor L-Min. limit switch is actuated. This sets the counter output to "0." As the Inductor runs toward L-Max. the count-up signals from the L Counter Encoder will cause the counter output count to increase until L-Max. is reached. Then the count will be close to the counter's maximum count of 4096. The Counter count is increased or decreased as the Inductor rotates in a maximum/minimum inductance direction. The L Counter output is connected to the L Comparator and a Tri-State Driver.

The L Counter Reset function requires a ground on the load input. However, the counter is synchronous and resetting does not occur until the $\phi$ L input receives a clock pulse. U8A + B, R20, and C86 form a pulse generator to toggle the $\phi$ L line through CR8 whenever L Counter Reset goes low.

### 5.15.2.3 L Comparator

The L Comparator is a 12-bit digital comparator consisting of three 4-bit comparators cascaded. The L Comparator has two comparing inputs. One is connected to the L Counter output and the other to the L Read Latch output. The L Read Latch holds the count of a previously-stored L Counter output that has been read from memory. The L Comparator compares these two inputs and provides an output that indicates whether the L Counter count is less than, greater than, or equal to the count read from memory. These signals are fed to the Interface PC Board, conditioned, and fed to the Control PC Board where they appear as error signals on the Magnitude comparator inputs for controlling the L Servo-Motor. In this way, the Inductor is positioned until the L Counter count is the same as the count read from memory during a "Silent Tune" cycle.

The Comparator has three outputs: $A < B$, $A = B$, and $A > B$. The "A" input is the L Counter output while the "B" input is the L Read Latch output. The following truth table defines the Comparator Outputs:

| Condition | Output Logic Levels | | |
|---|---|---|---|
| | A > B,L | A = B,L | A < B,L |
| L Counter greater than L Read Latch | 1 | 0 | 0 |
| L Counter equal to L Read Latch | 0 | 1 | 0 |
| L Counter less than L Read Latch | 0 | 0 | 1 |

### 5.15.2.4 Tri-State Driver

The Tri-State Driver consists of U18, U20, and U25. Both sections of U18 and one section of U20 are used for storing the L Counter output into memory. The remaining section of U20 and U25 are for C Counter storage. The L Counter outputs are connected to the inputs of U18A and B and U20A. All outputs are connected to the 4-bit write bus of the memory. Normally, the outputs of the Drivers present a high impedance to the Memory Write Bus. When the Driver receives a negative-going enable from the Chip Enable Decoder, the data at the Driver input is transferred to the Memory Write Bus.

### 5.15.2.5 L Read Latch

The L Read Latch consists of three D-type latches with all data inputs parallel-connected to the Memory Read Bus. The $\overline{Q}$ outputs are connected to the L Comparator "B" inputs. Whenever latches U17, U3, or U6 are clocked by a positive-going pulse on their respective clock inputs, the data present on the Memory Read Bus will be latched at the $\overline{Q}$ outputs and

held for comparison by the L Comparator. The outputs of NOR gates U19A and B, and U21A provide the clock signals to each latch. Each NOR gate input is connected to a Chip Enable Decoder output and to the L "Read Latch Enable" line. This line must be at a logic "0" and a negative-going pulse must appear at the NOR gate inputs in order for a positive-going clock pulse to occur at the Latch clock inputs. The Read Latch Enable line is connected to the Q output of the Silent Tune Flip-Flop on the Interface Board. A Silent Tune Cycle must be in progress to result in clocking of the L Read Latch.

5.15.2.6 Chip Enable Decoder

The Chip Enable Decoder is a 3 to 8 decoder whose inputs are connected to the output of the Address Generator. During a Read or Write operation, the Chip Decoder output lines enable the Tri-State Drivers and Read Latches as required to serially store or recall counter bytes to/from the memory. It also stops the Six Cycle Clock.

5.15.2.7 Address Generator

The Address Generator consists of a 4-bit binary counter that receives clock signals from the Six Cycle Clock. Its function is to generate a different address for each 4-bit byte that is stored/recalled from memory. Its output is connected to the three least significant bits of the Memory address bus and also to the input of the Chip Enable Decoder. The Address Generator is responsible for starting the Six Cycle Clock whenever it is reset by a start clock signal from the Interface Board.

5.15.2.8 Six Cycle Clock

The Six Cycle Clock provides a 1 kHz clock signal to control all Read/Write operations on the Memory Board. Only six clock cycles are required because for a given channel, a memory operation involves storing/recalling six 4-bit bytes: three for the C position and three for the L position. The Six Cycle Clock is started by the Address Generator and stopped by the Chip Enable Decoder. A start Clock pulse from the Interface Board starts the clock by resetting the Address Generator counter U28. This causes all of U28's outputs to go to a logic 0. This in turn causes all outputs of the Chip Enable Decoder U27 to go to a logic 1. Output Y7 is connected to the Reset input of Clock timer U29. When the Reset goes high, the clock starts to run. It will continue to run until six cycles have occurred. After six cycles, the input count of U27 will be binary 6. The Y7 output will go to a logic 0 and will cause the Reset line of U29 to go low, stopping the clock. The Y7 output is gated through U14B and U21B to prevent the clock from running while U28 is being reset.

5.15.2.9 Memory

The Memory consists of three 4 X 256 bit CMOS static RAMs U33, U34, and U35. U33 stores data for channels 0-31; U34 channels 32-63; and U35 channels 64-95.

The Chip Select line $\overline{E2}$ (Pin 17) on each RAM must be at a logic 0 for that RAM to be active. A decoder on the Interface Board selects the proper RAM depending on the Channel Switch position. It also provides a BCD to Binary Conversion to allow the BCD channel switch to provide a correct address on lines A3-A7 on each RAM. The address on these lines ranges from binary 0 (Channel Switch positions 0, 32, 64) to binary 31 (Channel Switch positions 31, 63, 95). RAM address lines A0-A2 are connected to the Address Generator. This address ranges from binary 1 to binary 6 during each Read or Write Cycle. This allows Reading/Writing the six counter bytes to/from memory in the required six address locations. The address at A3-A7 remains fixed according to the Channel Switch position.

$\overline{E1}$ and $\overline{W}$ signals remain at a logic 1 when no memory operations are occurring. For a Read

operation, $\overline{E1}$ must go to a logic 0 for each byte read from memory. $\overline{W}$ remains high. U7 and associated components provide the necessary delay between $\overline{E1}$ and the Six Cycle Clock output to insure that the address is present on lines A0-A2 before the Read cycle begins.

During a write operation, $\overline{E1}$ occurs as in the Read operation but $\overline{W}$ also goes to logic 0. $\overline{W}$ is gated with the Write Enable line through NAND gate U13D so that $\overline{W}$ only goes low during a Write Cycle. The Write Enable line is connected to the Q output of the Write Enable Flip-Flop on the Interface Board and is set by a Tune/Store signal at the Coupler control point.

5.15.2.10 Capacitor Element Memory Circuitry

The Capacitor Element Memory Circuitry is identical to that for the Inductor Element with the following exceptions.

C Counter

The C Counter is 11-bits instead of 12 as in the Inductor Counter. The 12th bit is reserved for the Antenna Modification Feature.

Antenna Modification Feature

This feature allows the Coupler to switch in additional series capacitance for tuning some antennas. The 12th bit of the Capacitor Memory Circuitry is used to store the status of the Antenna Modification Capacitor Relay located on the Inductor Chassis Assembly.

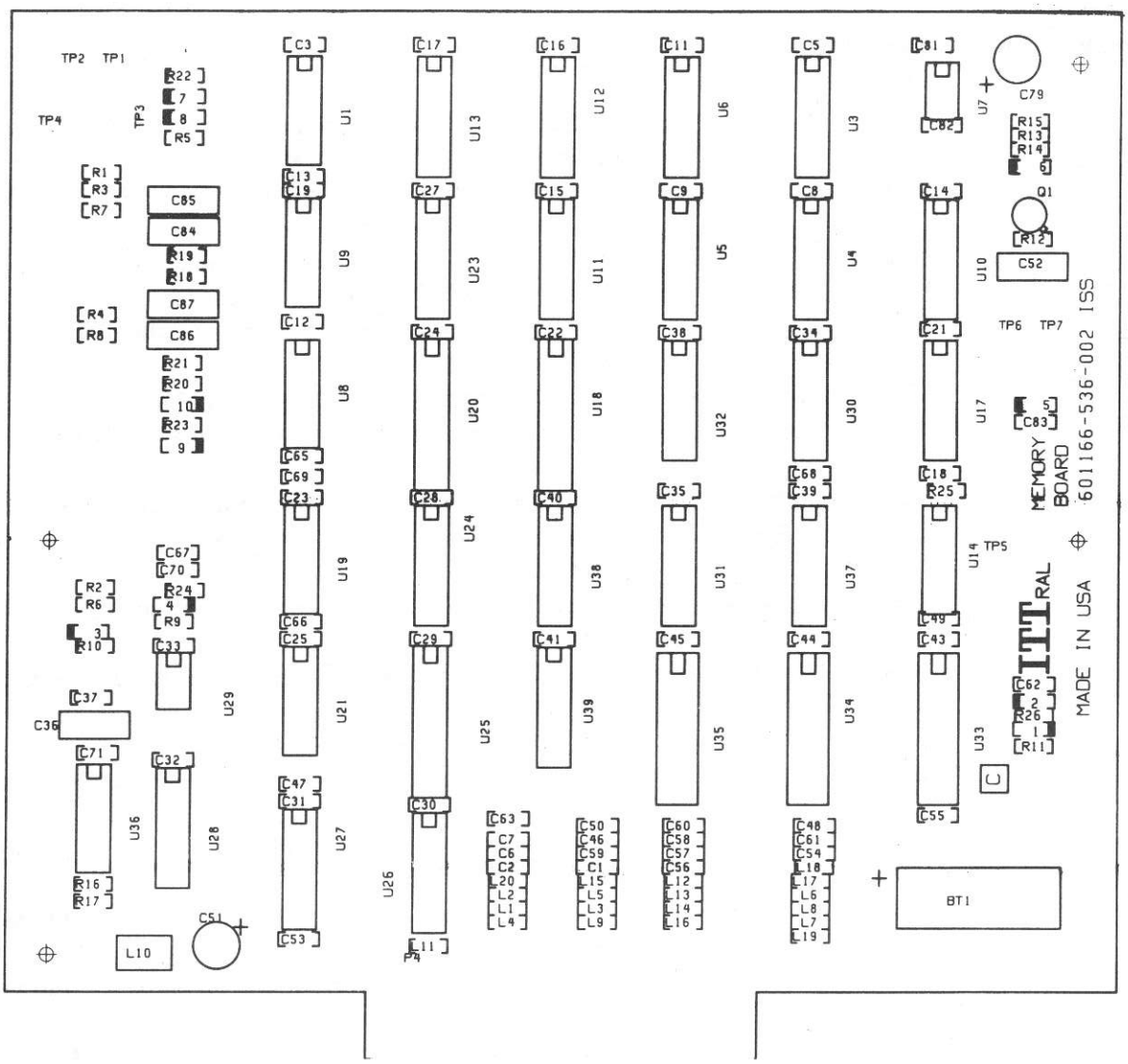
5.15.2.11 Standby Memory Power

A lithium battery keeps the Vcc of U32-35 at approximately 2.8 volts during power off intervals. Diode CR1 is normally reverse-biased when the Memory is operating at 5 volts Vcc since the anode of CR1 is at 3 volts and the cathode at 5 volts. When the operating Vcc goes to zero volts, CR1 is forward-biased and 3 volt battery B1 is switched onto the Memory Vcc bus. Diode CR2 isolates the power supply bus from the Memory Vcc bus during power-off intervals to prevent B1 from discharging.

### 5.15.3 Input and Output Specifications

#### 5.15.3.1 Inputs

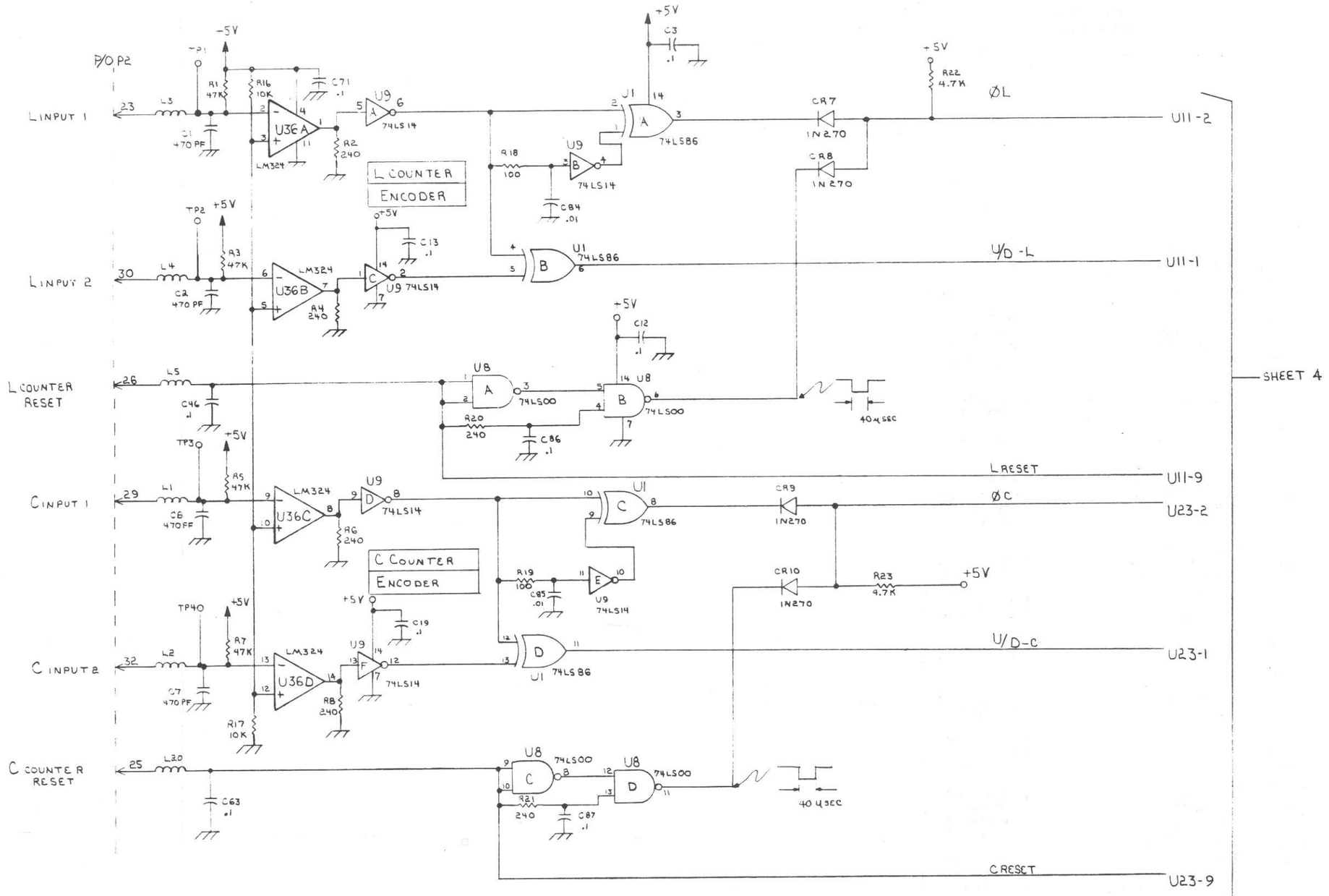
| Connector J4 Pin Number | Signal Name/Function | Specification |
|---|---|---|
| 23 | L input 1 | Logic 0 min value; Logic 1 max value sine or square wave 200 Hz max frequency |
| 30 | L input 2 | Same as L input 1 but quadrature shifted +90° ±5° and −90° ±5° |
| 29 | C input 1 | Logic 0 min value, Logic 1 max value sine or square wave 200 Hz max frequency |
| 32 | C input 2 | Same as C input 1 but quadrature shifted +90° ±5° and −90° ±5° |
| 14 | $\overline{\text{Read Latch Enable}}$ | Logic 0 during Read Cycle; Logic 1 otherwise |
| 12 | Start 6 Cycle Clock | Logic 1 pulse 0.5 ±.1 msec to start clock, Logic 0 otherwise |
| 11 | Write Enable | Logic 1 during write cycle, Logic 0 otherwise |
| 26 | L Counter Reset | Logic 1 pulse during L Counter Reset 0.5 ±.1 msec |
| 25 | C Counter Reset | Logic 1 pulse during C Counter Reset 0.5 ±.1 msec |
| 36 | Ant. MOD Write | Logic 1 if Ant. Mod. Capacitor utilized, Logic 0 otherwise |
| 37-40 | +5V | +5 VDC ±0.25V 600 mA max. |
| 19 | A3 | Logic 0 or Logic 1, depending on Binary Channel Address |
| 21 | A4 | Logic 0 or Logic 1, depending on Binary Channel Address |
| 20 | A5 | Logic 0 or Logic 1, depending on Binary Channel Address |
| 17 | A6 | Logic 0 or Logic 1, depending on Binary Channel Address |
| 18 | A7 | Logic 0 or Logic 1, depending on Binary Channel Address |
| 16 | $\overline{\text{CS1}}$ | Logic 0 to enable U32, Logic 1 otherwise |
| 17 | $\overline{\text{CS2}}$ | Logic 0 to enable U33, Logic 1 otherwise |
| 9 | $\overline{\text{CS3}}$ | Logic 0 to enable U34, Logic 1 otherwise |




**MEMORY BOARD**

## MEMORY BOARD
## (601166-536-002)

| Symbol | Description | Part Number |
|---|---|---|
| BT1 | Battery, L1, 3V | 600027-392-001 |
| C3-5,8, 9,11-19, 21-25, 27-35, 38-41, 43-50, 53-63, 71,81 | CAP., .1 uF | 600272-314-001 |
| C1-2, 6,7 | CAP., 470 pF | 600272-314-005 |
| C37, 65-70, 82,83 | CAP., .01 uF | 600272-314-002 |
| C51,79 | CAP., 47 uF, 50V | 600297-314-026 |
| C36,86, 87 C52 | CAP., .1 uF | 600204-314-020 |
| C84,85 | CAP., .01 uF | 600204-314-001 |
| CR1,2 | Diode, 1N6263 | 600145-410-001 |
| CR3,4-6 | Diode, 1N4148 | 600109-410-001 |
| CR7-10 | Diode, 1N270 | 600052-410-001 |
| Q1 | XSTR, 2N2907A | 600154-413-001 |
| L1-9, 11-20 | Inductor, 100 uH | 600125-376-002 |
| L10 | Inductor, 4.7 uH | 600091-376-001 |
| R1,3, 5,7 | RES., 47K, 1/4W, 5% | 647024-341-075 |
| R2,4,6, 8,14, 20,21 | RES., 240Ω, 1/4W, 5% | 624004-341-075 |
| R12 | RES., 22K, 1/4W, 5% | 622024-341-075 |
| R13 | RES., 750Ω, 1/4W, 5% | 675004-341-075 |
| R15 | RES., 3K, 1/4W, 5% | 630014-341-075 |
| R16, 17,11 | RES., 10K, 1/4W, 5% | 610024-341-075 |
| R9,10 | RES., 5.1K, 1/4W, 5% | 651014-341-075 |
| R24-26 | RES., 4.7K, 1/4W, 5% | 647014-341-075 |
| U1 | IC, 74LS86 | 600222-415-001 |
| U9 | IC, 74LS14 | 600272-415-001 |
| U8 | IC, 74LS00 | 600114-415-001 |
| U4,5, 10,30, 31,39 | IC, 74LS85 | 600432-415-001 |
| U11-13, 23,24, 26 | IC, 74LS169 | 600418-415-001 |
| U14 | IC, 74LS03 | 600239-415-001 |
| U18,20, 25 | IC, 74LS244 | 600282-415-002 |
| U19,21 | IC, 74LS02 | 600118-415-001 |
| U3,6, 17,32, 37,38 | IC, 74LS75 | 600259-415-001 |
| U29,7 | IC, NE555 | 600074-415-001 |
| U28 | IC, 74LS161 | 600176-415-001 |
| U27 | IC, 74LS138 | 600309-415-001 |
| U33,34, 35 | IC, 6551 | 600531-415-101 |
| U36 | IC, LM 324 | 600171-415-001 |
| — | Battery Tie Down Strap | 600008-116-001 |

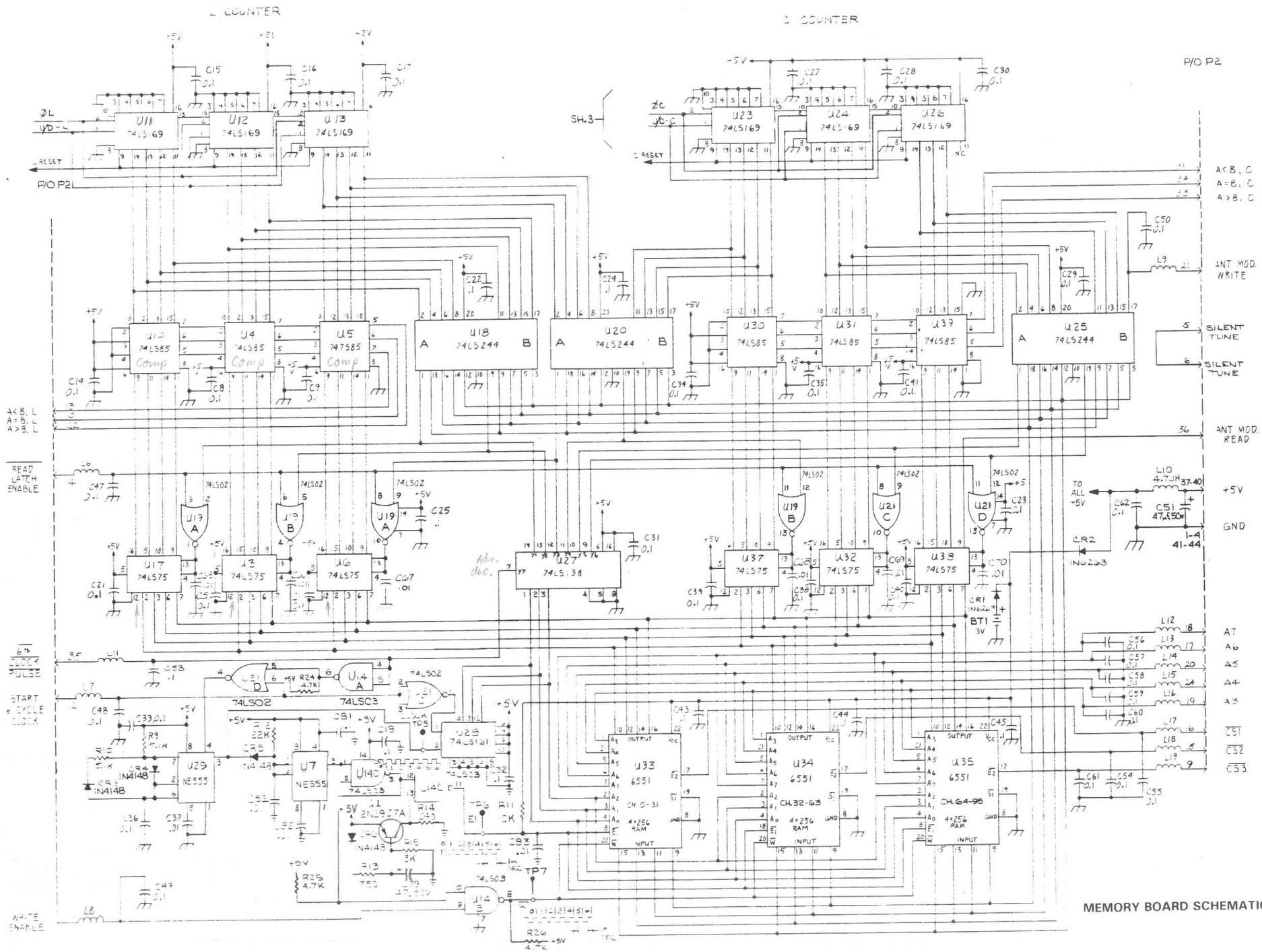



NOTES:

1. UNLESS OTHERWISE SPECIFIED: ALL CAPACITORS ARE IN MICRO-FARADS; ALL RESISTORS ARE IN OHMS, 1/4 W, ± 5%; ALL INDUCTORS ARE 100 MICRO-HENRYS.



MEMORY BOARD SCHEMATIC (SHEET 1 OF 2)




MEMORY BOARD SCHEMATIC (SHEET 2 OF 2)

5.15.3.2 Outputs

| Connector J4 Pin Number | Signal Name/Function | Specification |
|---|---|---|
| 35 | 6th Clock Pulse | Logic 1 or Logic 0 |
| 13 | A < B, L | Logic 1 or Logic 0 |
| 10 | A = B, L | Logic 1 or Logic 0 |
| 22 | A > B, L | Logic 1 or Logic 0 |
| 31 | A < B, C | Logic 1 or Logic 0 |
| 34 | A = B, C | Logic 1 or Logic 0 |
| 33 | A > B, C | Logic 1 or Logic 0 |
| 1-4,41-44 | Ground | 0V |

## 5.16 GENERAL TROUBLESHOOTING CHART

| SYMPTOM | PROBABLE CAUSE(S) |
|---|---|
| Coupler Power Breaker trips on MSR-6212 Power Supply or fuse on MSR-6408 blows. | 1. Wrong voltage selection plug installed on J4 on connector board or plug not properly installed.<br>2. Defective Power Supply Board. |
| No steady fault light at initial power turn on. | 1. Coupler not properly connected to Amplifier Control Unit.<br>2. Fault LED defective.<br>3. Power Up/Reset circuits not working - Faulty Control Board and/or Interface Board(s).<br>4. Power Switch on Connector Board inside coupler has not been switched on.<br>5. Fuse blown on Power Supply Board inside coupler (16 VDC).<br>6. P4 not installed on Connector Board. |
| No Tuning light when tune cycle is initiated. | 1. Tuning LED defective.<br>2. Power Switch on Connector Board inside coupler has not been switched on.<br>3. Fuse blown on Power Supply Board inside coupler (16 VDC).<br>4. Faulty Control and/or Interface Board(s). |
| Tuning light comes on when a tune cycle is initiated but tuning elements do not run. | 1. Fuse blown on Power Supply Board inside coupler (28 VDC).<br>2. RF power from Amplifier is not present or is too low (see next symptom).<br>3. Defective Control Board.<br>4. Defective Inductor/Capacitor Motor. |

## 5.16 GENERAL TROUBLESHOOTING CHART (CON'T)

| SYMPTOM | PROBABLE CAUSE(S) |
|---|---|
| Coupler elements do not move after they have homed. | 1. Key enable signal from coupler not present to cause exciter/amplifier to put out RF Tune Power - defective Control and/or Interface Board(s).<br>2. RF power from amplifier too low - should be at least 100 watts for tuning.<br>3. Excessive RF present on power or control lines causing key enable circuitry to be reset prematurely - better grounding of system may be required.<br>4. Defective Inductor/Capacitor Motor.<br>5. Defective limit switches L Max or C Max. |
| Tuning element (Inductor or Capacitor) runs past its limit switch and jams. | 1. Defective limit switch or broken wire from switch.<br>2. Defective Control Board. |
| Coupler will not tune below 4 MHz | 1. Inductor Force function not operating - defective Control Board.<br>2. Inductor not moving because it has jammed -see symptom above.<br>3. Improperly adjusted or defective RF Module. |
| Coupler tunes to a low VSWR but Ready light does not occur | 1. Excessive RF on Control or power lines - better grounding of system may be required.<br>2. Improperly adjusted RF Module.<br>3. Tune Power RF signal from exciter/amplifier has high harmonic content or other spectral impurities. |
| Coupler goes Ready but Faults on SSB or CW | 1. Antenna or lead-in arcing.<br>2. Arcing occurring in coupler tuning network.<br>3. Excessive RF on Control or power lines - better ground may be required.<br>4. Inductor back turn shorting assembly defective. |
| Excessive Reflected Power on all frequencies | 1. Improperly adjusted or defective RF Module.<br>2. RF signal from amplifier has high harmonic content or other spectral impurities. |

## 5.16 GENERAL TROUBLESHOOTING CHART (CON'T)

| SYMPTOM | PROBABLE CAUSE(S) |
|---|---|
| Tuning element (Inductor or Capacitor) runs only in one direction or runs very slowly or erratically | 1. Defective Control Board. |
| Vacuum capacitor goes to home and shaft begins to unscrew | 1. C Maximum limit switch defective.<br>2. Switch actuator screw improperly adjusted.<br>3. Broken wire to switch.<br>4. U6 defective. |
| Coupler will not tune some frequencies. | 1. Internal arcing occurring in tuning network.<br>2. Inductor back turns shorting assembly defective.<br>3. Misadjusted or defective RF Module. |
| Arcing occurs in tuning network | 1. Ball gap improperly adjusted.<br>2. Defective back turns shorting assembly.<br>3. Damaged tuning elements or other network components.<br>4. Antenna used is too short for frequency of operation at 1 kW level. See 2.4.1.6. |
| Coupler will not tune to a Ready condition in Silent Tune mode | 1. Defective Memory, Interface, or Opticoupler PC Board. |
| Coupler tunes to a Ready in Silent Tune mode but Faults when RF applied | 1. Defective Memory, Interface, or Opticoupler PC Board.<br>2. Surveillance switch not enabled. |
| Coupler will not start a Silent Tune Cycle when "Check Tx" Button on MSR-8000 is depressed | 1. Channel switch on MSR-8000 is in "FREQ" or Manual position. |

# SECTION 6
# ACCESSORIES AND ADDENDUMS

## 6.1 GENERAL

This section contains information and instructions required for the proper operation of the MSR-4030 with the following optional equipment:

1. MSR-6408 Control Unit
2. Antenna Bypass Kit
3. Shock Mount Kit

Section 1.5 in this manual contains all of the stock numbers for these options as well as a complete list of all of the other optional equipment available for the MSR-4030. Also included are the recommended antennas, cables, maintenance accessories, and a kit of spare parts.

The Spare PC Board Kit (1.5.5) contains one complete set of boards used in the MSR-4030. The PC Board Extender Kit (1.5.13) contains a set of extenders that allows the main boards to be plugged in above the card cage for easy troubleshooting. A Depot Spares Kit (1.5.4) is available for maintenance facilities to provide the most commonly used parts to maintain 3-5 antenna couplers for 2 to 4 years.

## 6.2 MSR-6408 CONTROL UNIT

### 6.2.1 General

The MSR-6408 is required if the MSR-4030 antenna coupler is to be used with a transmitter other than the MSR-6700 or MSR-8000. This control unit interfaces the antenna coupler with non-Mackay transmitters, either to replace an existing coupler or as original equipment. It contains all of the necessary interfacing and control line connections to operate the antenna coupler and all of its functions. In addition, a separate connector (J1) is provided to interface the transmitter connections such as power, key line, and interlocks directly to the control unit.

### 6.2.2 Equipment Supplied

6.2.2.1 MSR-6408 control unit - Part Number 699016-000-001 (Grey), 699016-000-002 (Olive Drab), or 699016-000-003 (Light Grey).

6.2.2.2 MSR-6408 accessory kit - Part Number 699016-017-001 consisting of:

a) 2 fuses, 2 amp, SLO-BLO - Part Number 600004-396-014
b) Connector, MS3106A28-21P - Part Number 600375-606-004
c) Clamp, MS3057-16A - Part Number 600376-606-003
d) Connector, MS3106A20 - Part Number 600375-606-010
e) Clamp, MS3057-12A - Part Number 600376-606-002
f) Bushing, Rubber - Part Number 600035-643-006
g) Bushing, Rubber - Part Number 600035-643-007

### 6.2.3 Installation

The MSR-6408 is designed for use in a standard 19 inch rack mounting bay. It has interface connections from a 14-pin connector at J1 to connect all internal bay wiring. A 37-pin connector at J2 is used for the control cable connection to the MSR-4030. See Figure 6.1 for the outline dimensions of the control unit.

#### 6.2.3.1 Cable Fabrication

Use accessory kit items b, c, d, and e to fabricate the connections at J1 and J2. An 18 AWG, 8-conductor stranded wire cable that is shielded or a shielded cable bundle of 8 wires can be used at J1. An 18 AWG, 37-conductor stranded wire cable that is shielded or a shielded cable bundle of 36 wires can be used at J2. The cable that is used at J2 is available from ITT Mackay using the part number

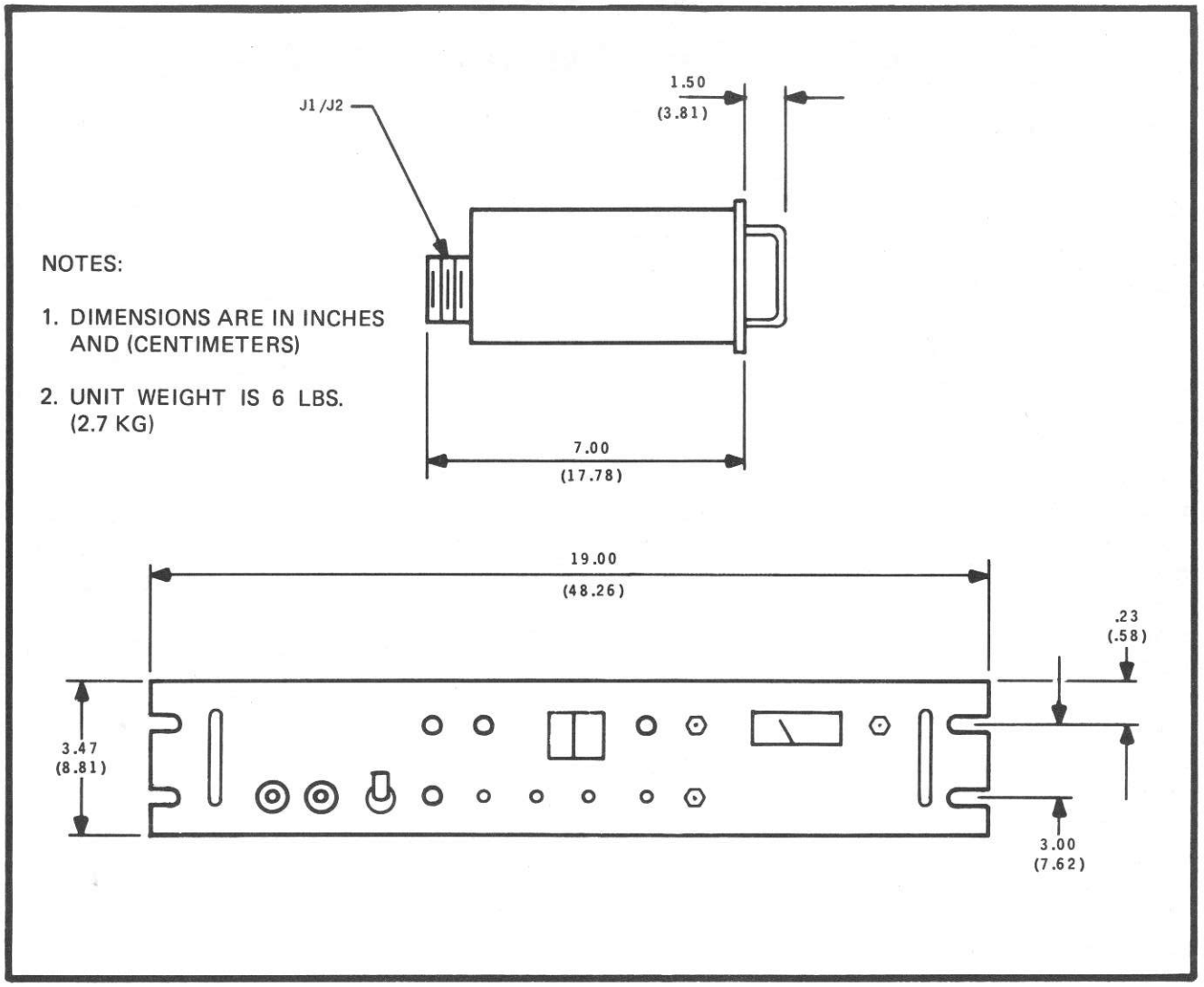



**Figure 6.1 MSR-6408 Control Unit Outline**

600069-102-010 (specify length). Prefabricated cables are also available using the part number 600530-540-XXX in 20, 50, 100, 150 and 250 ft. lengths.

Use Figure 6.2 and Tables 6.1 and 6.2 as guides for the following steps in fabricating both control cables:

1. Slide the clamp, connector back, and connector collar back onto the control cable.
2. Cut the PVC sleeving back 1.5 inches if using control cable.
3. Cut the braid off of the end of the control cable, leaving .20 inches exposed.
4. Strip and tin .20 inches off of all of the wires.
5. Prepare the wire as shown in detail "A" and solder the long stripped end completely around the braid.
6. Solder each wire into the solder sockets in each plug. Use table 2.1 in this manual as a guide for the control cable at J2.
7. After all wires are soldered, push the collar over the plug and screw the back piece securely onto the collar.
8. Loosen the screws on the cable clamp and securely screw it onto the back piece. Tighten both screws securely against the rubber sleeving and the cable.

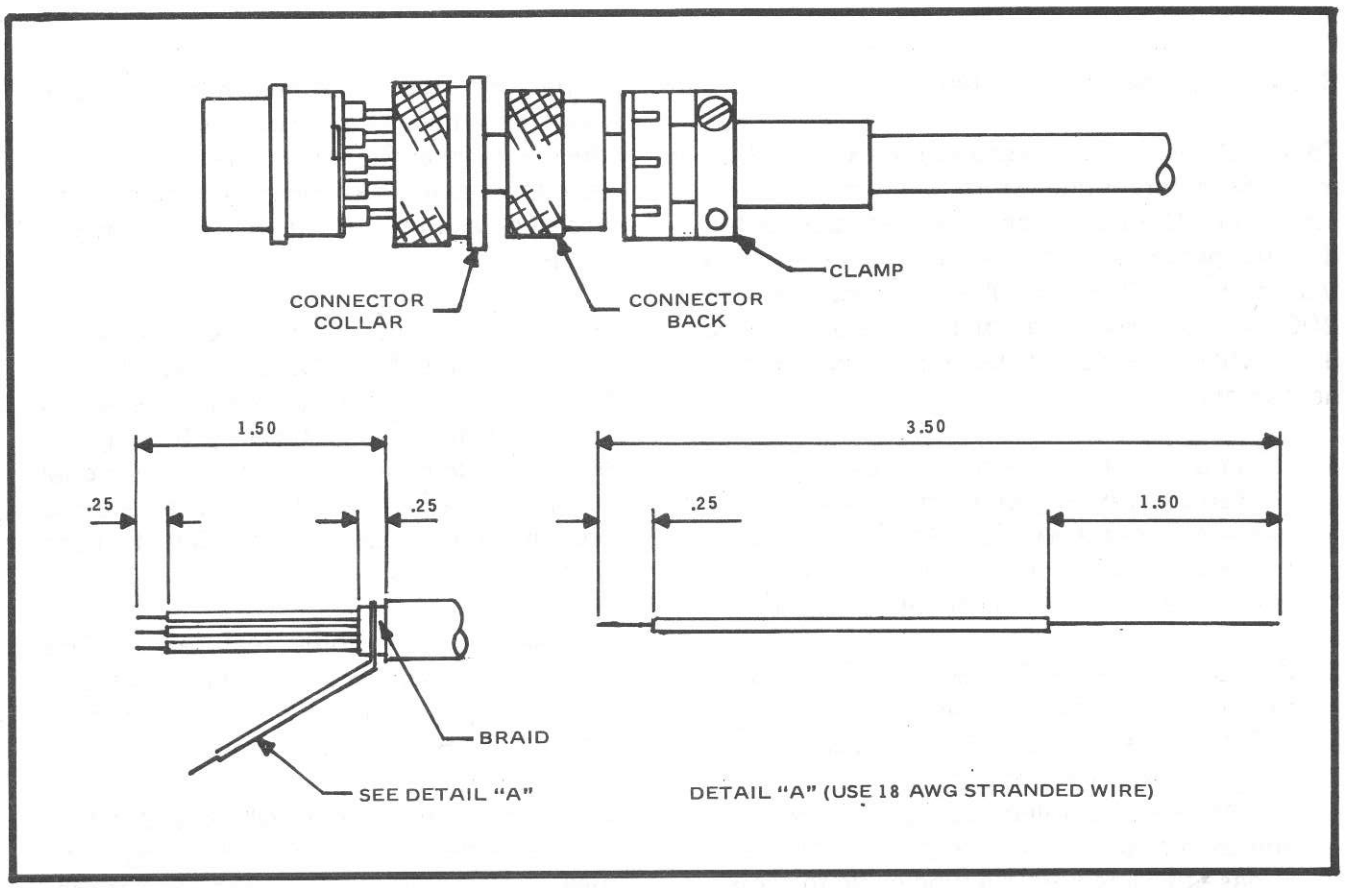



**Figure 6.2 Control Cable Assembly**

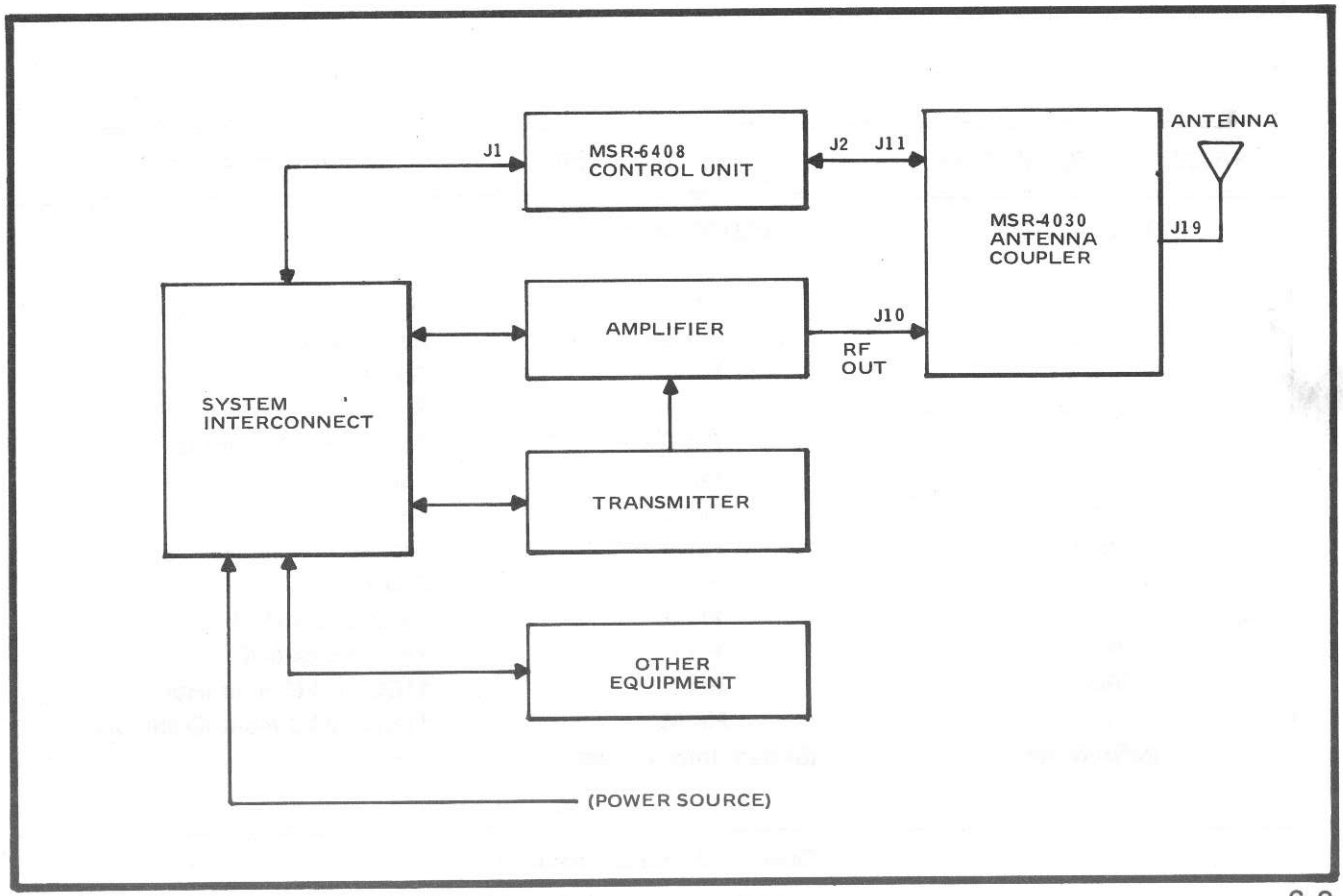



**Figure 6.3 System Block Diagram**

### 6.2.4 System Interconnect

Table 6.1 indicates power and control lines that must be interconnected to equipment at installation. Control lines may be connected directly provided voltages do not exceed 40 VDC and current sink requirements are less than 200 mA. Otherwise, a small DC relay may be used where required. Lines that must be connected are:

1. Ground (Pin A). This line should be connected to system ground. In addition a #8 or larger ground wire should be connected to the terminal post at the rear of the control unit and connected to system ground.

2. Key Enable (Pin B). This line should be connected to the exciter transmit or keyline (PTT) in systems where the coupler has control of the exciter during a tune cycle. The MSR-4030 will place a ground on this line as a request for tune power and may release this line during a tune cycle to allow switching the Antenna Modification Capacitor. This line should not be used in systems where release of this line signals the exciter that the tune cycle is completed (exciters having a keyhold latching circuit). For this case the tuning line (Pin F) should be used.

3. Auto-Home (Pin E). Use of the Auto-Home feature in the MSR-4030 is not recommended for normal applications since it lengthens the tuning time by forcing the elements home. Also, an Auto-Home signal readies the MSR-4030 for an RF tune cycle and excludes use of the Silent Tune feature.

   To use the Auto-Home feature, this line must be connected to the exciter so that a momentary ground on this line occurs when Auto Homing is desired.

   The exciter must be manually keyed to provide tune power after Auto-Homing. Normally, a latching circuit in the exciter provides this function.

| FROM CONNECTOR TYPE | TO CONNECTOR TYPE | DESCRIPTION |
|---|---|---|
| MS3102A20-27P | MS3106A20-27S | |
| Pin A | Pin A | Ground |
| Pin B | Pin B | Key Enable |
| Pin C | Pin C | Spare |
| Pin D | Pin D | Spare |
| Pin E | Pin E | Auto-Home Gnd Pulse |
| Pin F | Pin F | Tuning |
| Pin G | Pin G | Spare |
| Pin H | Pin H | Ground |
| Pin I | Pin I | Spare |
| Pin J | Pin J | TX Interlock (N/O) |
| Pin K | Pin K | TX Interlock (N/C) |
| Pin L | Pin L | 115/230VAC Input (Hot) |
| Pin M | Pin M | 115/230VAC Input (Common) |
| (MSR-6408) | (System Interconnect) | |

**Table 6.1 J1 Pin Connections**

| FROM CONNECTOR TYPE | TO CONNECTOR TYPE | DESCRIPTION |
|---|---|---|
| MS3102A28-21S | MS3106A28-21P | |
| Pin A | Pin A | Fault |
| Pin B | Pin B | Key Enable |
| Pin C | Pin C | TX Interlock (N/C) |
| Pin D | Pin D | Surveillance |
| Pin E | Pin E | CH 1 |
| Pin F | Pin F | PWR FWD |
| Pin G | Pin G | Ground (Braid) |
| Pin H | Pin H | Silent Tune P.B. |
| Pin J | Pin J | Tune P.B. |
| Pin K | Pin K | Ready Led |
| Pin L | Pin L | CH 4 |
| Pin M | Pin M | Tuning Led |
| Pin N | Pin N | CH 8 |
| Pin P | Pin P | Program/Tune P.B. |
| Pin R | Pin R | PWR RFL |
| Pin S | Pin S | O.T. Inhibit/BCD Invert |
| Pin T | Pin T | CH 20 |
| Pin U | Pin U | +5 VDC B Supply |
| Pin V | Pin V | Coupler Enable |
| Pin W | Pin W | Ground |
| Pin X | Pin X | O.T. Led |
| Pin Z | Pin Z | CH 2 |
| Pin a | Pin a | CH 80 |
| Pin b | Pin b | +5 VAC B Supply |
| Pin c | Pin c | TX Interlock (N/O) |
| Pin d | Pin d | Auto Home |
| Pin e | Pin e | O.T. Override P.B. |
| Pin f | Pin f | Group Select |
| Pin g | Pin g | 115/230 VAC (Hot) |
| Pin h | Pin h | 115/230 VAC (Common) |
| Pin j | Pin j | CH 40 |
| Pin k | Pin k | Temp Sense |
| Pin m | Pin m | Bypass Sw |
| Pin n | Pin n | 115/230 VAC (Hot) |
| Pin p | Pin p | 115/230 VAC (Common) |
| Pin r | Pin r | Temp Sense |
| Pin s | Pin s | CH 10 |
| (AT6211) | (MSR-4030) | |

**Table 6.2 J2 Pin Connections**

Σ = 26

4. Tuning (Pin F). This line should be connected to the exciter transmit or keyline (PTT) in systems where the exciter has a keyhold latching circuit. The MSR-4030 will place a ground on this line as a request for tune power and this line will remain at ground until tuning is complete.

5. Tx Interlock N/O (Pin I). This line should be connected to the Transmit Interlock input of the exciter and allows the MSR-4030 to interlock the exciter by placing a ground on this line. Normally this line presents a high impedance (open circuit) to the exciter. If the exciter requires a ground for normal operation and an open circuit to cause interlocking, the Tx Interlock (N/C) line (Pin K) should be used instead.

6. Tx Interlock N/C (Pin K). This line is provided for exciters that require a ground for normal operation and an open circuit to cause interlocking.

7. 115/230 VAC (Pins L + M). AC Power for the MSR-4030 must be supplied to these inputs. A 200 VA circuit rating is required. Care should be taken to insure that the voltage supplied to these pins is the proper voltage as indicated on the MSR-4030 voltage nameplate.

### 6.2.5 Operation and Checkout

Referring to Figure 6.3, make sure that J1 and J2 are securely connected and that all system wiring and transmitter connections are complete. Turn on all of the equipment and note that the MSR-6408 "FAULT" LED is on. This indicates that the antenna coupler has power and is in the correct standby condition. Terminate the RF output from the amplifier into a 2 kW 50 ohm load with a 1000 watt wattmeter in series for measurement purposes. With all of the switches in the positions as indicated by Figure 6.4, push the "TUNE" button and the "FAULT" LED should go out and the "TUNING" LED should come on. Note that there is 150-300 watts output during tuning on the wattmeter. If not, the transmitter should be adjusted for this output during the tuning mode. Turn off the AC power switch on the control unit. Remove the load and reconnect the RF line back to the MSR-4030. Turn the MSR-6408 power on and a steady "FAULT" LED should be indicating. Select a low operating frequency and push the "TUNE" button again. After a short delay, the antenna coupler should tune the antenna and the green "READY" LED should come on. Place the transmitter in the CW mode and depress the key. Check the relative power meter on the control unit in the "FWD" position and it should indicate forward power output. Put the meter in the "RFL" position and there should be very little reflected power, indicating a good antenna coupler tune.

The following operating controls, indicators, and functions are located on the front panel of the MSR-6408:

1. The control unit has two fuses that protect both the "HOT" and the "COMMON" side of the AC power source.
2. The power on and off switch is located beside these fuses.
3. The "SILENT TUNE" pushbutton, "NORMAL/STORE" switch, "CHANNEL" switches, and the "STORE" LED indicator are part of the optional "SILENT TUNE" feature of the MSR-4030 and are covered in Section 6.2.6.
4. The "TUNE" pushbutton is depressed to initiate a coupler tuning cycle. A momentary depression of this button is the only action required.
5. The "READY" LED is illuminated after a tuning cycle has been completed and the coupler has tuned to an acceptable VSWR.

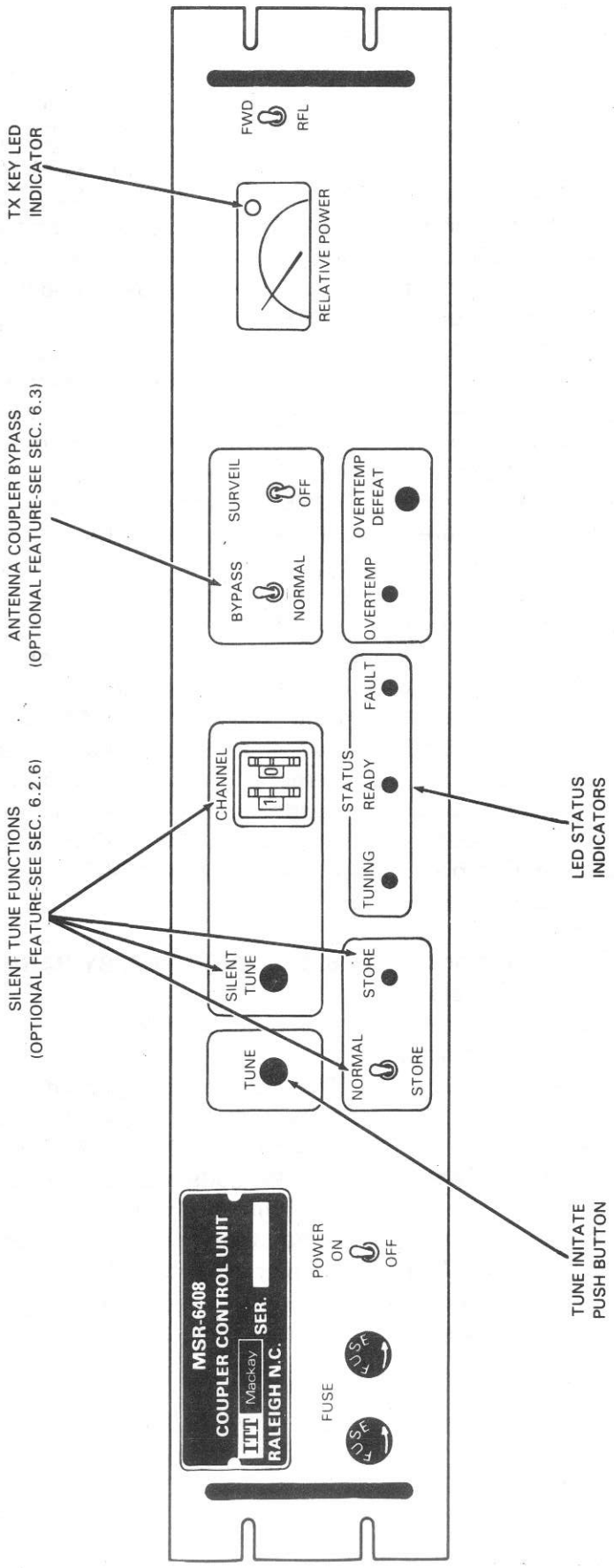



Figure 6.4 MSR-6408 Operational Functions

6. The "FAULT" LED is illuminated for the following conditions:
   a) When the antenna coupler power is initially turned on, it illuminates with a steady light.
   b) If the tuning time delay runs out (approximately 30-40 seconds after a tune command) the light will blink.
   c) Anytime the VSWR exceeds 2:1 for more than one second, except during a tuning cycle, the light will blink on and off.
7. The "OVERTEMP" LED comes on whenever the antenna coupler case has reached an unacceptably high temperature level. At this time, the transmitter key line is locked out and the only way to defeat this interlock is to depress the "OVERTEMP DEFEAT" pushbutton.
8. The "SURVEIL" on/off switch is turned on whenever the operator desires the "Surveillance" feature of the antenna coupler. This feature allows the coupler to automatically retune itself for small VSWR changes by sampling the RF carrier.
9. The "NORMAL/BYPASS" switch is an antenna coupler bypass in receive feature that is an option covered in Section 6.4.
10. The meter contains a red LED that is illuminated whenever the transmitter key line is used during a transmit condition.
11. The "RELATIVE POWER" meter along with the "FWD/RFL" switch indicates the relative forward and reflected power from the transmitter.

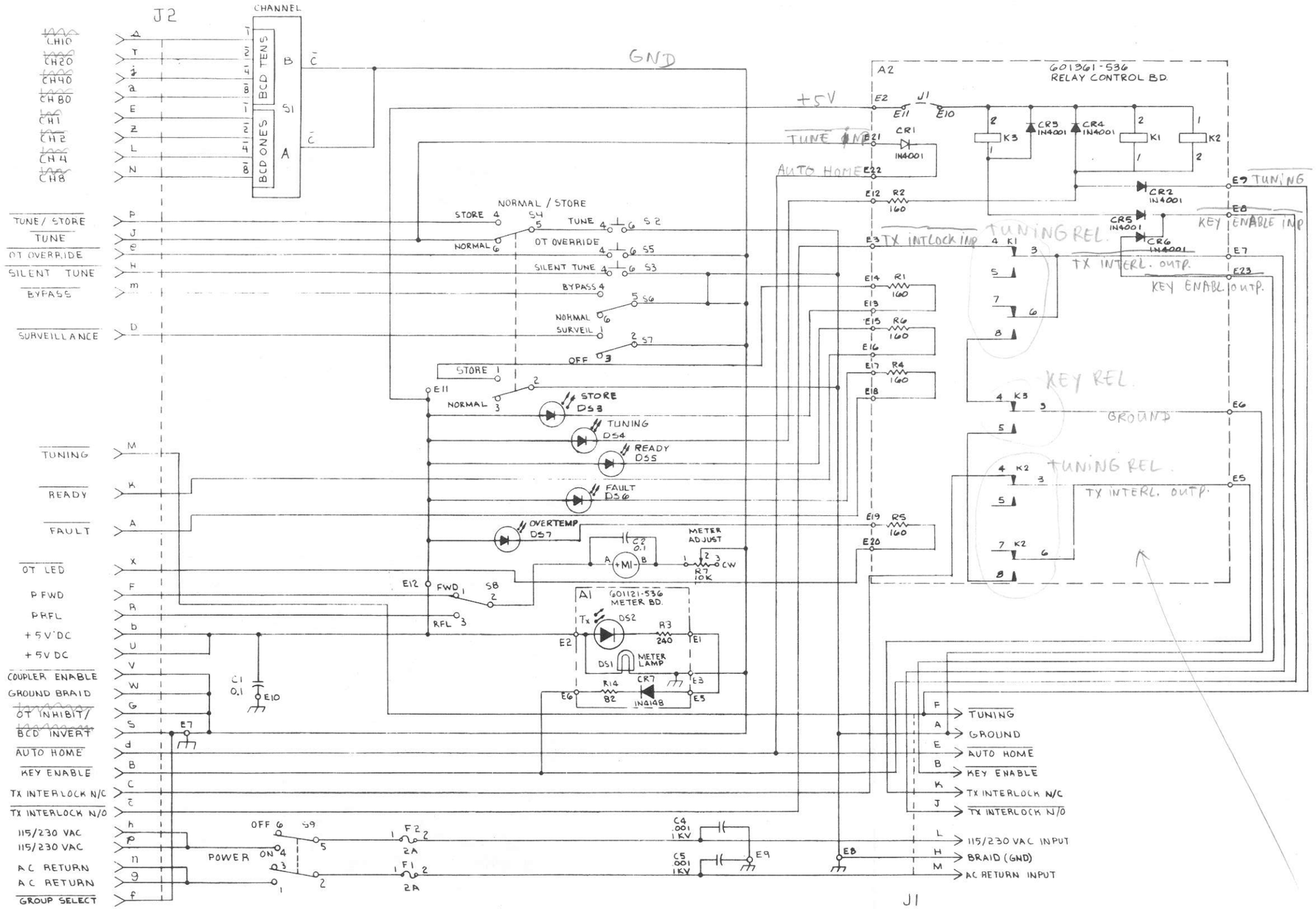
### 6.2.6 Operation and Checkout of MSR-6408 Silent Tune Feature

If the optional MSR-6408 control unit is being used, the "SILENT TUNE" pushbutton, "NORMAL/STORE" switch, "STORE" status indicator, and the "CHANNEL" switch are used in the silent tune mode. To initiate a programmed channel, select a channel on the "CHANNEL" switch (00-95). Place the "NORMAL/STORE" switch in the "STORE" position and the "STORE" LED should light. Select an operating frequency and push the "TUNE" pushbutton. The coupler should go through a normal tune with an RF carrier, except that the tuning information will now be stored in the selected channel. Select another frequency and channel and depress the "TUNE" pushbutton again. Now there will be two programmed channels stored in the coupler memory. Place the switch back to "NORMAL," select the first programmed channel and frequency, and push the "SILENT TUNE" pushbutton. The logic in the antenna coupler will cause the meter to give an indication, however, the transmitter key LED will not come on and there will be no RF carrier. After the "READY" LED on the control unit comes on, transmit a CW carrier and check the forward and reflected power indications on the meter. A good VSWR (low reflected power) indicates that the coupler has tuned properly from memory in the silent tune mode. It is recommended that the surveillance switch be in the ON position when using the Silent Tune feature to ensure a low VSWR.

## 6.3 ANTENNA BY-PASS KIT

### 6.3.1 General

The antenna by-pass kit contains a pre-wired relay and all of the wiring to install this optional feature into the MSR-4030 antenna coupler. This kit adds a by-pass relay that provides the user with a convenient method of receiving out-of-band signals. It is designed to by-pass the coupler network during receive so that the tuned circuits will not degrade out-of-band received signals.



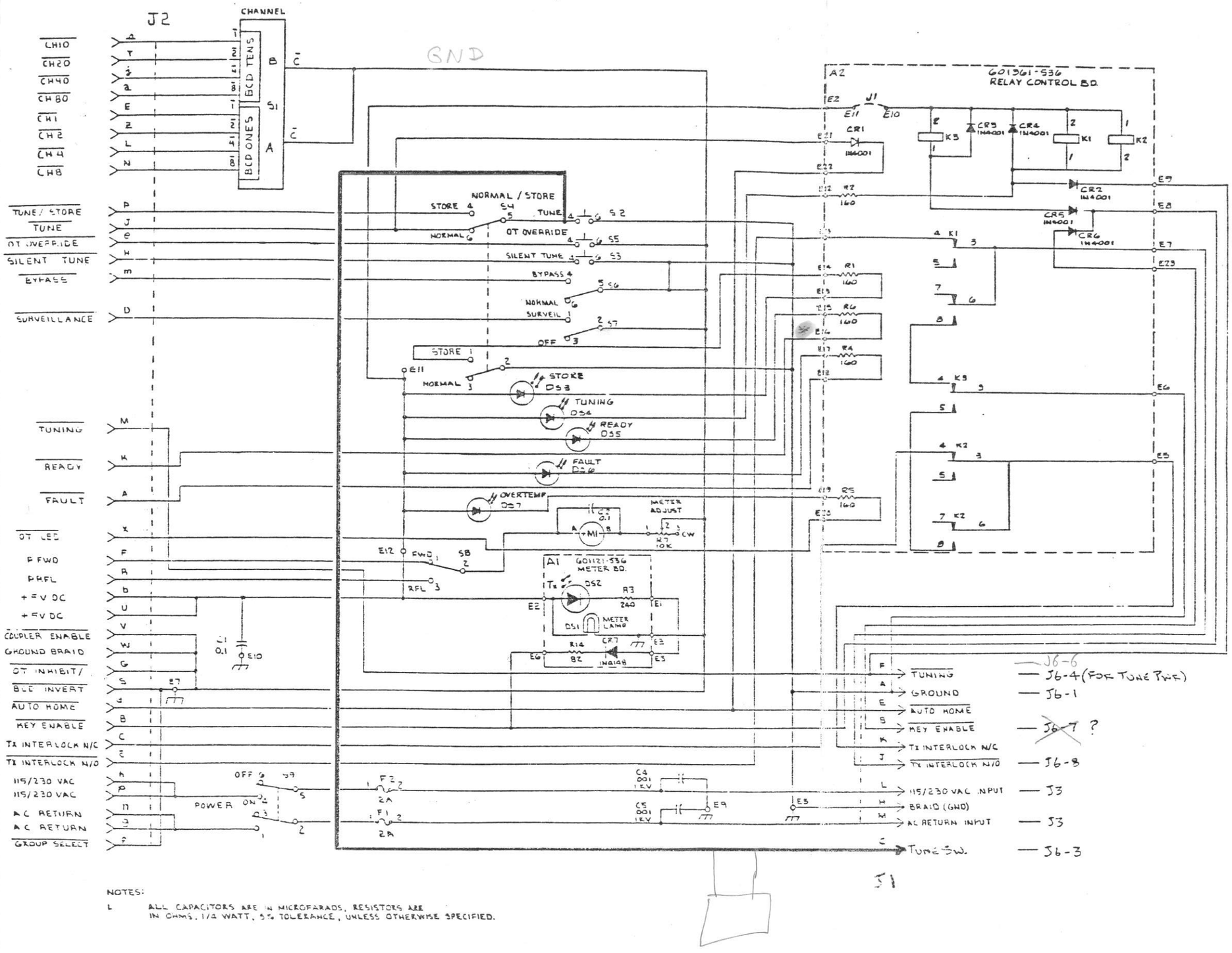

NOTES:

1. ALL CAPACITORS ARE IN MICROFARADS; RESISTORS ARE IN OHMS, 1/4 WATT, 5% TOLERANCE; UNLESS OTHERWISE SPECIFIED.

**CONTROL UNIT, MSR 6408**

| Symbol | Description | Part Number |
|---|---|---|
| A1 | Meter Mount Board | 601121-536-001 |
| A2 | Relay Control Board | 601361-536-001 |
| C1,2 | Cap., .1uF, 50V | 600272-314-001 |
| C3,4 | Cap., .001 uF, 1KV | 600189-314-014 |
| CR2-6 | Diode, 1N4001 | 600011-416-005 |
| DS3,6,7 | Led, Red | 600073-390-001 |
| DS5 | Led, Green | 600073-390-002 |
| DS4 | Led, Yellow | 600073-390-003 |
| F1,2 | Fuse, 2A | 600004-396-013 |
| J1 | Connector, 14 Position | 600374-606-011 |
| J2 | Connector, 37 Position | 600374-606-004 |
| K1-3 | Relay, DPDT, 5 VDC | 600052-403-004 |
| M1 | Meter | 600034-368-002 |
| R1,2,4-6 | Res. 160 ohm, 1/4W, 5% | 616004-341-075 |
| R7 | POT., 10K | 600064-360-003 |
| S1 | Thumbwheel Switch | 600180-616-003 |
| S2,3,5 | Switch, Pushbutton | 600170-616-001 |
| S4,6-9 | Switch, DPDT | 600287-616-002 |

referenes funktion: normall kører TX interlock direkte over, men during TUNING bliver TX interlock styret af KEY ENABLE




NOTES:

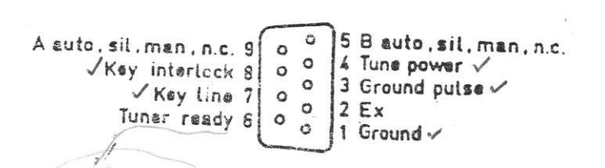
1. ALL CAPACITORS ARE IN MICROFARADS, RESISTORS ARE IN OHMS, 1/2 WATT, 5% TOLERANCE, UNLESS OTHERWISE SPECIFIED.

**CONTROL UNIT, MSR 6408**

| Symbol | Description | Part Number |
|---|---|---|
| A1 | Meter Mount Board | 601121-536-001 |
| A2 | Relay Control Board | 601361-536-001 |
| C1.2 | Cap., .1uF, 50V | 600272-314-001 |
| C3.4 | Cap., .001 uF, 1KV | 600189-314-014 |
| CR2-6 | Diode, 1N4001 | 600011-416-005 |
| DS3.6.7 | Led, Red | 600073-390-001 |
| DS5 | Led, Green | 600073-390-002 |
| DS4 | Led, Yellow | 600073-390-003 |
| F1.2 | Fuse, 2A | 600004-396-013 |
| J1 | Connector, 14 Position | 600374-606-011 |
| J2 | Connector, 37 Position | 600374-606-004 |
| K1-3 | Relay, DPDT, 5 VDC | 600052-403-004 |
| M1 | Meter | 600034-368-002 |
| R1.2.4-6 | Res. 160 ohm, 1/4W, 5% | 616004-341-075 |
| R7 | POT., 10K | 600064-360-003 |
| S1 | Thumbwheel Switch | 600180-616-003 |
| S2.3.5 | Switch, Pushbutton | 600170-616-001 |
| S4.6-9 | Switch, DPDT | 600287-616-002 |

DANSK

J6 (Ant. Tuner control)




MSR-6408 SCHEMATIC

MODIFIED

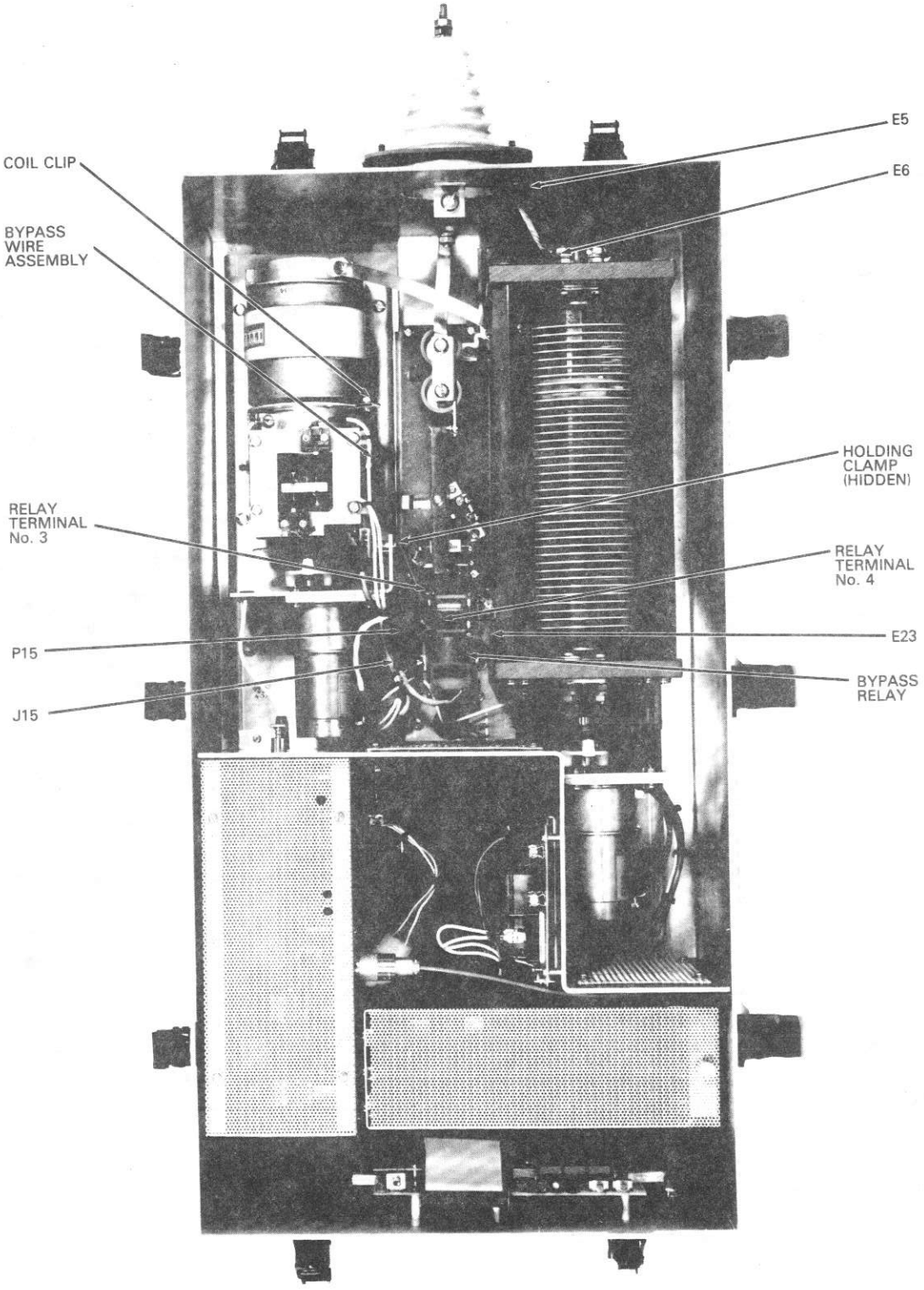



**Figure 6.5 Bypass Relay Features**

### 6.3.2 Equipment Supplied

MSR-4030 antenna by-pass kit - part number 600067-700-001 consisting of:

a) Assembly, relay - Part No. 600310-537-001
b) Assembly, cable - Part No. 600055-540-001
c) Screw, 8-32 - Part No. 690632-203-085
d) Washer, No. 8 flat - Part No. 612008-217-005
e) Washer, No. 8 split - Part No. 642008-217-005
f) Coil Clip - Part No. 600153-233-001
g) Instructions - Part No. 600067-700-001 (Page 1 of 2)

### 6.3.3 Installation

The antenna by-pass kit can be installed inside the MSR-4030 without removing any modules or the main chassis. Refer to Figure 6.6 for all of the by-pass relay features and connection points. Start by removing the coil grounding strap between E5 and E6. Remove the screw and other hardware from the tie down clamp that is holding plug P-15 in position. Position the by-pass as shown in Figure 6.5 and secure the relay, ground strap coming from relay terminal No. 3, and the tie down clamp with the hardware that was previously removed. Make sure that the ground strap is securely grounded to the chassis. Use the kit hardware (items c, d, and e) and secure the other side of the relay to the chassis. Take the other ground strap from the relay and connect it to E23 on the coil mount. Take the plug (J15) on the relay and connect it to P15 from the chassis. Route the cable assembly through the unused holding clamp on the capacitor assembly mount and push the quick connect terminal onto relay terminal No. 4. Loosely attach the coil clip on the lip of the capacitor bracket, slide the other terminal lug from the cable assembly into this clip, and tighten the clip hardware to secure both the clip and the lug.

### 6.3.4 Operation and Checkout

The antenna by-pass kit is used as a receive only function when the operator wants to listen to out-of-band signals. In the antenna by-pass mode, the transmitter key line is locked out and the transmitter cannot key. The MSR-6408 control unit and the MSR-6700 exciter can be used with the MSR-4030 in the antenna by-pass mode.

#### 6.3.4.1 MSR-6408

The MSR-6408 control unit has "NORMAL/BY-PASS" switch on the front panel that is used for the antenna by-pass. Make sure this switch is in "NORMAL" and tune the MSR-4030 at a high operating frequency. When the "READY" LED is on, change the receiver until a signal on a low frequency is heard. Switch to "BYPASS" and the signal strength should increase noticeably. Check and make sure that the transmitter cannot be keyed in the by-pass mode. To return to normal coupler operation, place the switch back into the "NORMAL" position.

#### 6.3.4.2 MSR-6700

The MSR-6700 exciter can also switch the MSR-4030 into the antenna by-pass mode. For specific operating details regarding the antenna by-pass feature with this exciter, refer to MSR-6700 manual.

## 6.4 SHOCK MOUNT KIT

### 6.4.1 General

Although the MSR-4030 is designed to withstand severe shock and vibration conditions, an optional shock mount kit is available for additional protection. With this kit, the coupler can withstand the shock and vibration environment as defined by MIL-STD-810C.

### 6.4.2 Equipment Supplied

MSR-4030 shock mount kit - Part No. 600095-700-001 consisting of:

a) 4 mounts, shock - Part No. 600001-649-001
b) 4 screws, 3/8 x 16 x 1 - Part No. 693716-203-165
c) 4 washers, 3/8 split - Part No. 612375-217-005
d) 4 washers, 3/8 flat - Part No. 642375-217-005
e) Instructions - Part No. 600095-700-001 (Page 1 of 2)

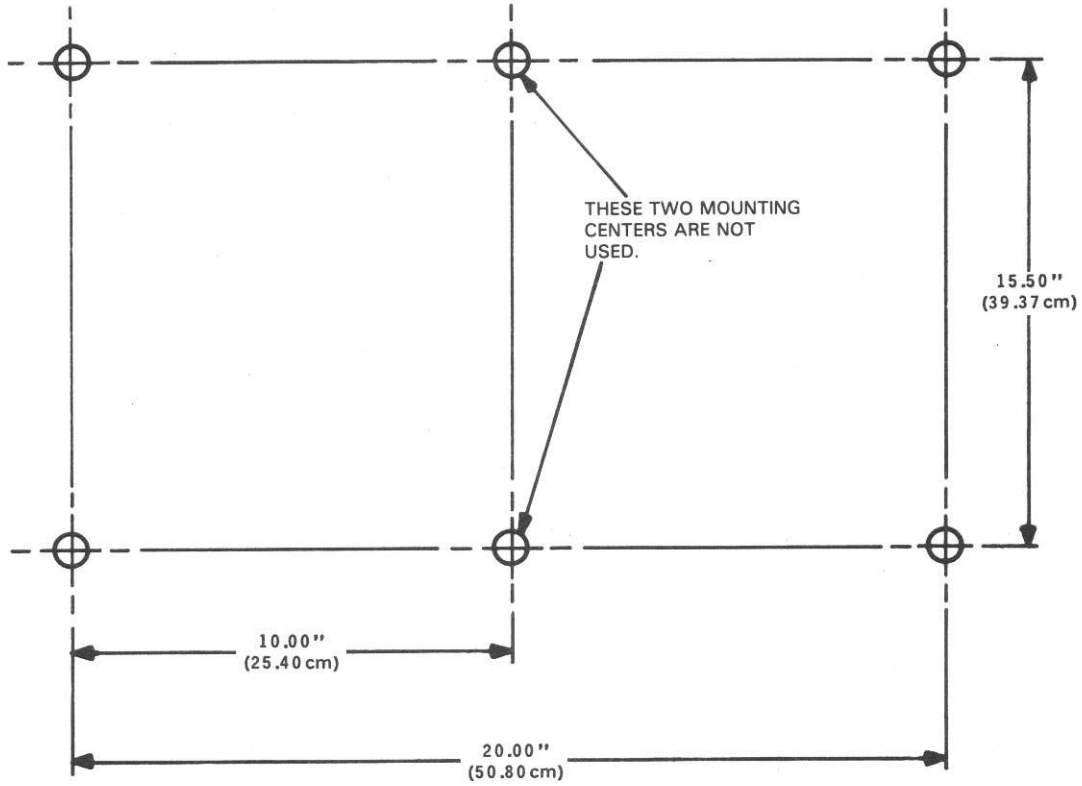
### 6.4.3 Installation

With the shock mount kit, the MSR-4030 can only be mounted in a horizontal place, right side up. Make sure that the mounting surface is flat and that there is adequate room for the coupler to move on its shock mounts. A metal surface is preferred for the mounting of the coupler, but a non-metallic surface can be used if adequate ground is made. Refer to Figure 6.6 for the installation of the four shock mounts. Each one will be mounted over a center hole location as diagrammed. Using this center hole as a reference, drill a pattern of four holes as dimensioned in the shock mounting diagram. Using 1/4-20 hardware (not supplied), secure all four shock mounts to the mounting surface. Make sure that the mounting strap is secured under each shock mount with the surface mounting hardware.

Place the MSR-4030 case on the mounts and secure each one to each coupler mounting foot with a 3/8-16 screw, split washer, and flat washer, Since these shock mounts will not provide adequate ground to the mounting surface, the ground lug on the case must be well grounded. The ground must be the equivalent of a copper strap (1 " wide per foot of length) connected to the case grounding lug and the antenna ground.

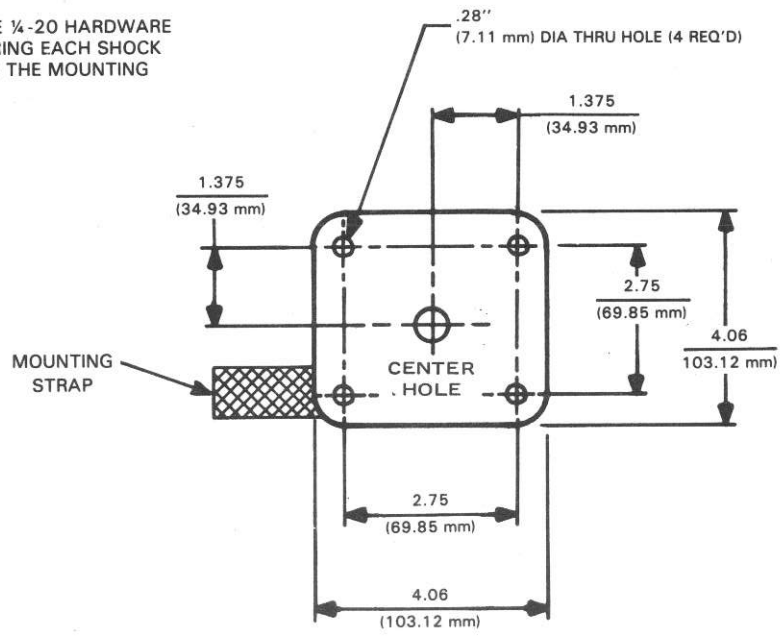
### 6.4.4 Installation Checkout

Check all four of the shock mounts and make sure that they are well secured to the coupler mounting surface. Check, and tighten as necessary, the hardware that attaches the mounts to the coupler case. Rock the coupler on the shock mounts to make sure the case does not hit any obstruction. Check the ground connections and make sure that they are adequate and secure.




SHOCK MOUNTING CENTER
HOLE LOCATIONS

NOTE: USE ¼-20 HARDWARE FOR SECURING EACH SHOCK MOUNT TO THE MOUNTING SURFACE.




TYPICAL SHOCK MOUNTING
DIMENSIONS

**Figure 6.6 Shock Mounting Hole Pattern Dimensions**

ITT Mackay

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