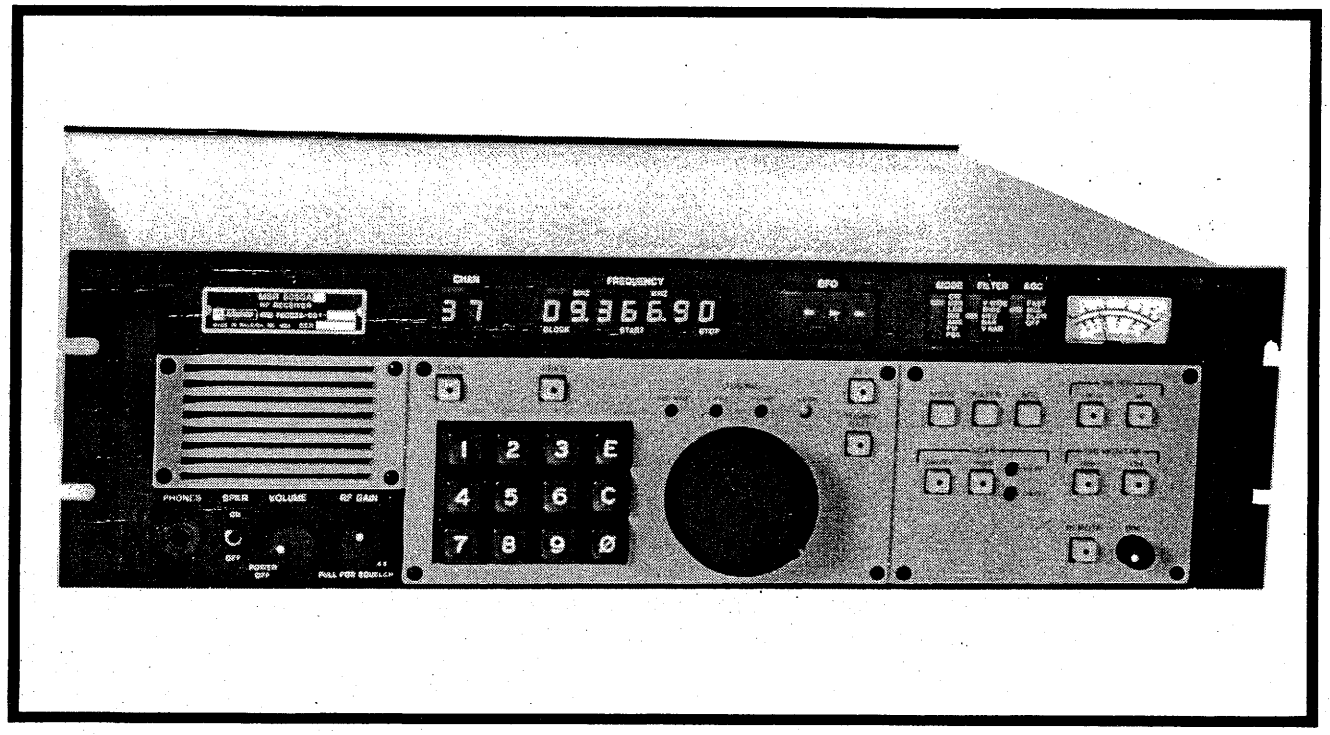
Mackay
COMMUNICATIONS

Operation and Maintenance Manual

HF Receiver
MSR 5050A



MSR 5050A RECEIVER

Issue 1

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NOTICE

MACKAY COMMUNICATIONS INC. reserves the right to make changes to the equipment without notice.

PROPRIETARY STATEMENT

SAFETY NOTICE

This equipment has dangerous RF voltages which can cause BURNS and INJURY. Do not touch the antenna connector, long wire antenna or metal portion of whip antennas when transmitting. When practicable, maintenance should be performed with the equipment de-energized. If power-on maintenance is required, use caution. Do not touch high voltage or RF components.

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GLOSSARY

A	Ampere(s)
A/D	Analog-to-Digital (Converter)
AFSK	Audio frequency shift keying; a baseband modulation scheme in which two audio frequencies are used to represent binary coded data; the frequency is shifted to one frequency to represent a 1 (mark) and to the other to represent a 0 (space).
AGC	Automatic gain control
ALC	Automatic level control
ALE	Address latch enable
AM	Amplitude modulation; a modulation scheme in which the carrier is made to vary in amplitude in accordance with the modulating signal.
AMPL	Amplifier
AME	Amplitude modulation equivalent
ANTIVOX	Prevents false VOX operation; see VOX
BNC	Baby "N" connector
BCD	Binary-coded decimal
BFO	Beat Frequency Oscillator, used in SSB detection circuits
BITE	Built-in Test Equipment
BPF	Bandpass filter
BW	Bandwidth
CPU	Central processing unit
CW	Continuous wave; a wave that does not vary in amplitude or frequency and is turned on and off to carry intelligence, e.g., Morse Code
CCW	Counterclockwise
CMOS	Complementary metal oxide semiconductor
D/A	Digital-to-Analog (Converter)
DAGC	Delayed AGC
dB	Decibel(s)
dBm	Decibel(s) relative to one milliwatt
EMI	Electromagnetic interference
EPROM	Erasable programmable read-only memory
FSK	Frequency shift keying
HF	High frequency; a radio frequency band extending from about 3 MHz to 30 MHz; in this manual, HF includes 1.6 to 30 MHz.
HV	High voltage
IF	Intermediate frequency
IP2	Second order intermodulation intercept point
IP3	Third order intermodulation intercept point
ISB	Independent sideband
IMD	Intermodulation (distortion)
I/O	Input/Output
LED	Light emitting diode

LIST OF ILLUSTRATIONS (Cont.)

LIST OF ILLUSTRATIONS

GLOSSARY (Cont.)

LO	Local oscillator
LPA	Linear power amplifier
LPF	Low pass filter
LSB	Lower sideband; a modulation scheme in which the intelligence is carried on the first sideband below the carrier frequency; see SSB
MIC	Microphone
mA	Milliampere(s)
mS	Millisecond(s)
mV	Millivolt(s)
NBFM	Narrow band frequency modulation
OCXO	Oven-controlled crystal oscillator
PEP	Peak envelope power
PCB	Printed circuit board
RAM	Random access memory
RF	Radio frequency
RMS	Root mean square
RX	Receive
RTTY	Radio teletypewriter
SPKR	Speaker
SSB	Single sideband; a modulation scheme in which the intelligence is carried by one of the carrier sidebands, the other sideband and the carrier center frequency being suppressed
TCXO	Temperature-compensated crystal oscillator
TGC	Transmitter gain control
TTL	Transistor/transistor logic
TX	Transmit
uA	Microampere(s)
uP	Microprocessor
uS	Microsecond(s)
USB	Upper sideband; a modulation scheme in which the intelligence is carried on the first sideband above the carrier frequency; see SSB
uV	Microvolt(s)
Vac	Volts, alternating current
VCO	Voltage controlled oscillator
Vdc	Volts, direct current
VSWR	Voltage standing wave ratio; the ratio of the maximum to the minimum voltage of a standing wave on a radio frequency transmission line
W	Watt(s)
XTAL	Crystal element

SECTION 1

INTRODUCTION

1.1 SCOPE

This manual contains information necessary for the installation, operation, and maintenance of the receiver.

1.2 DESCRIPTION

1.2.1 GENERAL

The MSR 5050A is an all solid state, remote-controllable, synthesized HF receiver designed to operate from 10 Hz to 30 MHz in 10 Hz steps. It is primarily designed as a 19 inch rack-mounted unit operating from 115/230 VAC. The plug-in replacable modules, most of which are common with the companion MSR 6700A Exciter and MSR 8050A Transceiver, enhance maintainability. The front panel layout is logically arranged so that control keys are located adjacent to their resulting indicators.

The MSR 5050A HF Receiver is a microprocessor controlled unit which was designed with a wide range of standard and optional features which allow it to be tailored to almost any receiver application. Applications for the MSR 5050A range from simple monitoring tasks to complex HF systems where groups of receivers are computer controlled in a high density signal environment where selecting that unique desired signal is paramount. This cost-effective receiver will do the job not only in a communications system, but also for surveillance and signal aquisition requirements where high performance characteristics are needed.

The standard and optional remote interfaces for the receiver allow it to be used in a flexible array of remote control systems. Full serial remote control using an RS-232C/422/423 or MIL-STD-188C interface is standard, while an optional internal Tone Key /Modem board provides two-tone FSK remote control through the MSR 6420 Remote Control Unit. A remoted system may contain up to 99 addressable equipments in any combination and be controlled by multiple remote control units or computers.

The MSR 5050A with optional data filters becomes a High Speed Data receiver. The ISB Option along with these filters allows the receiver to operate in full duplex Tactical Data Information Link (TADIL) systems. Depending on the options specified, the MSR 5050A has the following capabilities:

- Frequency range 10 kHz to 29.99999 MHz with 10 Hz resolution.
- Tuning incrementally in 3 selectable rates or by direct keypad entry.
- Automatic scan of up to 100 sequential easily programmed channels in any of 10 programmable groups.
- Automatic sequential frequency scan with programmable start/stop frequency in 3 selectable frequency steps.
- Frequency stability of 1 part in 10^6 standard (1 part in 10^8 optional).
- All normal reception modes including J3E (USB, LSB), B9W (2ISB optional), A1A, J1A (CW), H5E, R3E (AM), and F1B (FSK with external modem).
- ISB (optional) with both audio outputs (USB, LSB) simultaneously available at the rear panel.
- Front panel selection of optional bandwidth filters.
- Provision for external automatic preselector.
- Computer control via RS-232C/422/423 or MIL-STD-188C interface as standard.

• Remote control via optional two- tone FSK from the MSR 6420 Remote Control Unit.

• Optional synthesized BFO ±7.99 kHz in 10 Hz steps.

• IF gain control, front panel operated.

• Syllabic squelch, front panel selected.

• Selectable AGC decay rates.

• Antenna protection to 100 VRMS.

• Self-contained speaker with three watts output.

1.2.2 MECHANICAL DESCRIPTION

The receiver is composed of three major separable mechanical assemblies: a front panel assembly, a rear panel assembly and a chassis/ Mother board assembly.

The front panel assembly is 3/16 inch aluminum subpanel 5 1/4 inch x 19 inch with cast polyurethane overlays which contain all operator accessable controls and displays. The display board, which mounts to the panel, contains the LED displays, meter and function keys. The speaker, numeric keypad assembly and other controls are mounted directly to the panel. After the top cover is removed (2 DZus quarter-turn fasteners), the front panel is removable from the receiver by nine screws and four ribbon cable connectors.

The rear panel assembly contains the power supply assembly and all external interface connectors. It attaches to the receiver by 11 screws (two to the bottom cover). Electrical connection is by three molex connectors, ribbon cable assemblies and three coax connectors. The power supply assembly (with heat sink) may be removed from the rear panel with four screws. It may be separated from the receiver without removing the rear panel by two molex connectors in addition to the four screws.

The chassis/Mother board consists of an aluminum card cage and three chassis support panels all of which mount to the Mother board. The Mother board contains all PCB edge card connectors and interconnect wiring. A card cage and top shield mount to the Mother board to provide shielding and support for the PCBs. All except coax connectors are mechanically keyed to prevent insertion into the wrong position. The three support panels connect the rear and front panels. The bottom and top covers complete the receiver assembly.

1.2.3 ELECTRICAL DESCRIPTION (Figure 1.1)

The receiver may be divided into four major electrical functions: power supply, synthesizer, signal path and control circuitry.

1.2.3.1 Power Supply

The power supply is a linear type operating from 115 or 230 VAC at 47 to 400 Hz. A power transformer and two rectifiers supply pre-regulated voltage to the rear panel power supply assembly. The power supply assembly consists of a PCB with voltage regulators mounted to a heat sink containing associated pass transistors supplying +13, +9 and +5 VDC to the receiver.

1.2.3.2 Synthesizer

The synthesizer consists of four PC boards: 1) Major Loop, 2) Translator Loop, 3) Minor Loop, and 4) Reference board. With the BFO option, a BFO board is added which is similar to the Minor Loop board. The synthesizer is a three loop design, which provides the receiver with the first LO from the Major Loop, the second LO from the Translator Loop and the third LO from the Reference board (or from the BFO board when installed). All frequencies are derived from a 5 MHz TCXO mounted on the Reference board.

With the High Stability option, an OCXO is mounted on the card cage and electrically replaces the TCXO. A rear panel buffered output from either the TCXO or OCXO is available at TTL levels to allow other radios to operate synchronously from the same reference frequency. A rear panel REF in/out switch electrically disconnects the internal TCXO/OCXO allowing an ex-

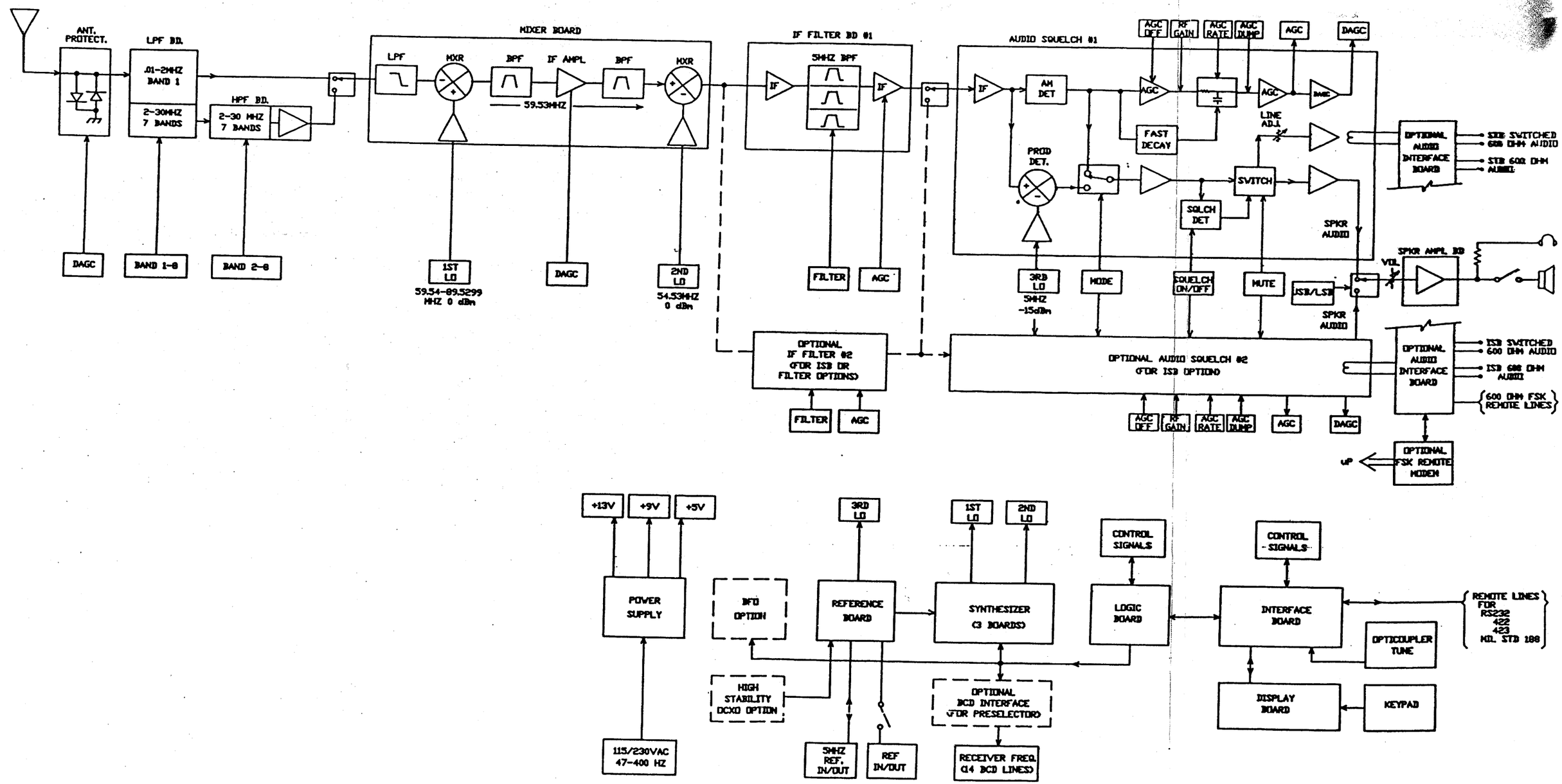


Figure 1.1

Block Diagram, MSR 5050A
790025-028

ternal 5 MHz TTL level to operate the radio through the same BNC connector. A fault causing any of the "loop" boards to lose "lock" will cause the loss-of-lock LED on that board to light (visible through the top shield). Any loss-of-lock will mute the receiver audio signal and a front panel BITE display will indicate "E1".

1.2.3.3 Signal Path

The signal path is primarily contained on six PCBs: 1) Low Pass Filter, 2) High Pass Filter, 3) Mixer, 4) IF Filter, 5) Audio/Squelch and 6) Speaker Amplifier. With various options a second Audio/Squelch and /or IF Filter board or an Audio Interface board are added.

The 10 kHz to 30 MHz antenna signals are converted to a 5 MHz IF using a double conversion process which minimizes low order spurious responses. The first inversion results in a 59.53 MHz IF which is filtered by two crystal bandpass filters to remove undesired images and spurious responses. The second conversion produces a 5 MHz IF which is filtered by selectable crystal bandpass filters to determine the information bandwidth of the receiver. The ultimate selectivity of the radio is primarily determined by the product of the first and second conversion crystal filters with the tracking half-octave bandpass response of the Low Pass Filter and High Pass Filter boards.

The 5 MHz IF signal is demodulated by an AM detector (in AM mode) or a product detector (CW, SSB or FSK modes) to produce the final audio output signal.

1.2.3.4 Control Circuitry

The microprocessor (except for local function of speaker ON/OFF, volume, RF gain, dimming and squelch ON/OFF) directs all receiver control functions. The majority of the control logic and channel memory circuitry is on the Logic board using an 8035 8-bit microprocessor and a "zero-power" RAM with 10 year memory. Front panel keys and indicators are controlled by a keypad I.C. in the interface board. Microprocessor responses are decoded in circuits on the logic board and Interface board to provide band, filter, mode, AGC and miscellaneous outputs to the receiver modules. Decoders on the Mother board supply frequency control inputs to the synthesizer.

1.3 TECHNICAL SPECIFICATIONS

The equipment specifications are listed in Table 1.1. Additional specifications may be detailed with various options in Section 6.

1.4 EQUIPMENT SUPPLIED

This equipment is listed in Table 1.2.

1.5 OPTIONAL EQUIPMENT - NOT SUPPLIED

Optional equipment is listed in Table 1.3. Descriptions and specifications are found in Section 6.

Table 1.1 EQUIPMENT SPECIFICATIONS

All specifications at 115 VAC, 60 Hz operation at 25°C, 2 to 30 MHz unless otherwise specified.

CHARACTERISTIC	SPECIFICATION
Frequency Range	10 kHz to 30 MHz in 10 Hz increments
Tuning Controls	Keypad entry or continuous tune by TUNE knob in 3 rates of 10 Hz, 1 kHz, and 100 kHz
Frequency Scan	Automatic scan of frequency in 3 front panel selectable steps
Frequency Stability	± 1 PPM (standard) ±.01 PPM (option)
BFO Tuning Range	±7.99 kHz (10 Hz steps)
BFO Tuning Control	Continuous tune by TUNE knob in 2 rates of 10 Hz or 1 kHz.
Channel Operation	
Channel Storage	Up to 99 channels programmable for frequency, BFO, AGC decay rate, mode and IF bandwidth by keypad
Channel Scan	Automatic scan of channels in memory in any of 10 programmable blocks
Sensitivity	SSB: -113 dBm for 10 dB (S+N)/N AM (6 kHz bandwidth): -97 dBm for 10 dB (S+N)/N at 30% modulation CW (2.70 kHz bandwidth): -113 dBm for 10 dB (S+N)/N (Sensitivity degraded 6 dB below 2 MHz in addition to 6 dB per octave below 0.5 MHz)
Operating Modes	Standard: AM (H3E, R3E), CW (A1A, J1A), LSB, USB (J3E upper and lower), and FSK (F1B) with optional external modem.

Table 1.1 EQUIPMENT SPECIFICATIONS (Cont.)

Selectivity (Fc = 5.000 MHz)

BANDWIDTH	MODE	6dB BANDWIDTH	60dB BANDWIDTH
*VWide	AM, CW, FSK	12 kHz Min (3dB)	40 kHz Max
Wide	AM, CW, FSK	5 kHz Min	18 kHz Max
Med	AM, CW, FSK	2.7 kHz Min	6 kHz
*Narrow	Am, CW, FSK	1 kHz Min (3 dB)	6 kHz Max
*VNar	AM, CW, FSK	400 Hz Max 3 dB)	4 kHz Max
Med	USB	300 & 3000Hz	-1.5 & 4.5 kHz
Med	LSB	-300 & -3000 Hz	1.5 & -4.5 kHz
Med	ISB	Same as USB & LSB	Same as USB & LSB
+Med	USB	450 & 3050 Hz (2dB)	-0.4 & 4.4 kHz
+Med	LSB	-450 & -3050 Hz (2dB)	+0.4 & -4.4 kHz

*Optional Equipment with Filter option
+Optional Equipment with Data Filter Option has controlled differential delay of 500 Usec 815 to 3050 Hz (-815 to -3050 Hz)

CHARACTERISTIC	SPECIFICATION
IF and Image Rejection	80 dB minimum
External Spurious Rejection	70 dB minimum
Internal Spurious Rejection	99.5% below 0.2 μV
Intermodulation Distortion (In Band)	For two equal 0.1 volt input signals that produce tones of 1100 and 1700 kHz, the IM products shall be at least 35 dB below the audio tones.
Intermodulation Distortion (Out-of Band)	Two 0 dBM signals at +30 and +60 kHz removed from the receiver frequency shall produce an IM product less than -30 dBm at the receiver frequency (IP_3 15 dBm min, +20 typical)
Crossmodulation	With a desired signal of 1 mV unmodulated, the level of an interfering 30% modulated signal at 100 kHz from the desired signal shall be at least 0 dBm to cause an audio output 20 dB below the reference (when desired signal 30% modulated)

Table 1.1 EQUIPMENT SPECIFICATIONS (Cont.)

CHARACTERISTIC	SPECIFICATION
Blocking	With a desired signal of 200 µV, the level of an undesired signal removed ±60 kHz shall be at least +3dBm to reduce the audio output by 3dB.
Oscillator Reradiation	Signals at the antenna connector due to internal oscillators (59.54 - 89.53 MHz first L.O.; 54.53 MHz second L.O.; 5.0 MHz third L.O.) shall be less than -73 dBm (2 to 30 MHz)
Unwanted Sideband Rejection	The response of a signal 1 kHz below/above tuned receiver frequency shall be down 50 dB in USB/LSB mode with respect to the response in LSB/USB mode.
Audio Output	
Speaker	Not less than 3 watts at 5% maximum distortion into 3 ohms load (or 1W into 8Ω load).
Phones	Not less than 10 mW at 5% distortion into 600 ohms (10% AM).
Standard and Optional ISB 600 ohm line	Internally adjustable (Audio Squelch Board) from less than -10 to not less than +10 dBm at not more than 5% distortion into 600 ohms. (10% AM). Not more than 1% distortion(5% in AM) at 0 dBm output.
Mute	Speaker and phone audio reduced 50 dB by external TTL signal (rear panel).
Squelch (syllabic)	Mutes speaker and phone audio (and 600 ohm audio with internal jumper) by front panel ON/OFF control. Recognizes voice characteristics to unsquelch on signals > -113 dBm.
Diversity Outputs	In ISB both audio outputs (USB, LSB) are simultaneously available at rear panel. Individual IF AGC voltage available in rear panel.

Table 1.1 EQUIPMENT SPECIFICATIONS (Cont.)

CHARACTERISTIC	SPECIFICATION
AGC	
Range	-97 to +13 dBm with less than 10 dB change in audio output (measured in SSB)
Attack-Time	Less than 10 milliseconds
Decay Time	(For 60 dB change in signal) AGC FAST - not greater than 50 mSec.; 30 mSec. typical. AGC Medium - 200 milliseconds nominal. AGC Slow - 3 Sec. nominal
Antenna Input Protection	Protection up to 100 volts at 50 ohms.
Dimensions	Height 5.25 inches; width 19 inches; depth 17 5/8 inches (Exclusive of controls, connectors and handles).
Weight	30 pounds Max.
Power	115/230 VAC (± 10% to specification, ±15% operational; 47 to 400 Hz, 75 watts typical.
Temperature	
Operating	-10°C to +55°C
Storage	-40°C to +70°C
Humidity	95% at +50°C for 24 hours
Shock	MIL-STD-810C Method 516.2, Procedure I, Figure 516.2-2 (with shock mount).
Vibration	MIL-STD-810C Method 514.2, Procedure VIII, Figure 514.2-6, Curve V (15 to 200 Hz) (with shock mounts).
Remote Control	
Formats	RS232C, RS422, RS423, MIL-STD-188C or optional FSK
Functions	Channel select, channel scan, frequency select, frequency tune, frequency scan, BFO tune, mode select, AGC decay, RF gain.
Protocol	See Appendix I.

Table 1.2 EQUIPMENT AND ACCESSORIES SUPPLIED

QTY	ITEM	MACKAY PART NO.	DESCRIPTION/USE
1	Accessory Kit	795025-017-001	Kit of following parts:
1	Connector DB25P	600290-606-005	External connect to J42
1	Connector DB25S	600290-606-005	External connect to J43
2	Connector, shell	600225-233-003	For DB25 connectors
1	Connector, coax	600244-606-001	External connector for J46
2	Screw set	600116-606-002	For DB25 connectors
1	Connector, shorting	700009-606-002	Used to replace J43 to bypass radio in a daisy chain remote control network
1	Card extractor	600268-616-001	To remove plug-in PCB modules
1	Power cable	600078-102-001	For 115/230 volt line power
4	Fuse,1A SLO-BLO	600006-396-019	For 115 VAC operation
4	Fuse, 1/2A SLO-BLO	600006-396-014	For 230 VAC operation

Table 1.3 OPTIONAL EQUIPMENT - NOT SUPPLIED

ITEM	MACKAY PART NO.	DESCRIPTION/USE
IF Filter	Future Release	Provides the following bandwidths: USB/LSB 2.7 kHz, CW/AM (v. wide) 12 kHz, CW/AM (wide) 6 kHz, CW/AM (narrow) 1 kHz, CW/AM (v. narrow) 400 Hz, CW/AM (medium) 2.7 kHz
BFO **Note** - BFO option must be specified for reception of CW, RTTY, or Data using 1 kHz or 400 Hz filters.	600107-700-001	Synthesized BFO tunable from 0 to ±7.99 kHz in 10 Hz steps. Recommended when Filter Option is specified.
Independent Sideband: ISB Option "A"	700014-700-001	Reconfigures radio for ISB operation by adding a second simultaneous IF and audio signal path. Operates within the same bandwidths as the standard radio without the IF Filter Option.
ISB Option "B"	700014-700-002	Reconfigures radio for ISB operation by adding a second simultaneous IF and audio signal path. Operates within the same bandwidths as provided when the IF Filter Option is supplied.
High Stability	700402-700-001	Oven controlled crystal oscillator provides stability of 1 part in 10^8.
Remote FSK Modem Option	700015-700-001	Uses Tone Key/Modem Board (602025-536-002) to communicate with MSR 6420 Remote Control Unit by 300 Baud FSK over a standard 2 wire telephone circuit.
Addressable Audio I/O Option	700015-700-002	Uses Audio Interface board (700014-536-001) to provide an additional 600 ohm standard and ISB switchable output to operate on a multi-radio parallel audio bus. Also provides capability of multi-radio daisy chain operation on the 600 ohm FSK remote control line.

Table 1.3 OPTIONAL EQUIPMENT - NOT SUPPLIED (Cont.)

ITEM	MACKAY PART NO.	DESCRIPTION/USE
MSR 6420 Remote Control Unit	799042-000-xxx	Separate stand alone remote control unit capable of multi-radio control via RS232C, RS422, RS423, MIL-STD-188C or 300 Baud FSK. Refer to the MSR 6420 manual for associated optional equipment.
Miscellaneous: Desk Top Cabinet (Black)	600257-704-001	Allows MSR 5050A to be installed as a freestanding desk-top system. Overall dimensions of the MSR 5050A installed in cabinet: 19 3/4"W x 19 1/4"D x 6 3/4"H
Rackmount Kit	600078-700-001	Rack slides and hardware allow MSR 5050A to be installed in standard 19 inch rack.
Spare PCB Kit	700011-700-001	Contains one each of all plug-in PCB assemblies. Allows on-site servicing by substitution of modules.
Comprehensive Spares Kit (CSK)	700013-700-001	Intended for on-site or depot repair of MSR 5050A with minimum downtime. Contains PCB assemblies, other assemblies and some piece parts. One CSK should support up to five MSR 5050A receivers for 2-4 years.
Depot Spares Kit (DSK)	700012-700-001	Includes individual components required to repair defective MSR 5050A assemblies, and other parts not included in the CSK. DSK is intended for use at Depot level by trained technicians and, with the CSK, should support up to 5 receivers for 2-4 years.
Extender Board Kit	600081-700-001	Maintenance aid provides means to extend any plug-in PCB in MSR 5050A. (Particularly applicable for Depot level maintenance in conjunction with DSK(s).

Table 1.3 OPTIONAL EQUIPMENT - NOT SUPPLIED (Cont.)

ITEM	MACKAY PART NO.	DESCRIPTION/USE
Preselector	700007-700-001	Provides narrow bandpass front end selectivity automatically tuned by the receiver from 1.6 to 29.9 MHz. Includes BCD interface, MSR 6300 interface cable, MSR 6300 preselector, and 12 volt power supply.
Cable Assembly	700028-540-xxx	For 2 wire audio and FSK remote control between MSR 6420 and single MSR 5050A.
Cable Assembly	700029-540-xxx	For 2 wire audio and remote control via RS-232C, RS-422, RS-423 or MIL-STD-188C between MSR 6420 and single MSR 5050A.
Cable Assembly	700038-540-xxx	For 2 wire audio and FSK remote control between MSR 6420 and multiple MSR 5050A's.
Cable Assembly	700039-540-xxx	For 2 wire audio and remote control via RS-232C, RS-422, RS-423, or MIL-STD-188C between MSR 6420 and multiple MSR 5050A's.
CSW 1000 Control Software	89001-000-001(English) 89001-000-002(Spanish)	The CSW 1000 is computer software which allows an IBM PC compatible computer to control a system of MSR 6700A Exciters and MSR 5050A Receivers. As many as 99 Exciters and 99 Receivers may be connected in a system and controlled by this software.
Data Filter Option	700418-700-001	This option substitutes controlled group delay filters (per TADIL A specs) for the USB, LSB filters in the standard radio.
	700418-700-002	Same as -001 but is applied to a radio with ISB option A where USB and LSB filters are on separate IF filter boards.

SECTION 2

INSTALLATION

2.1 GENERAL

This section describes the installation procedure for the receiver. Installation of the receiver is quick and simple as the unit is completely wired, calibrated and tested before shipment from the factory. Included within this section are procedures for unpacking, inspection and, if necessary, reshipping.

2.2 UNPACKING AND INSPECTION

Unpack the receiver and make certain that all equipment outlined in Table 1.2 is present. Retain the carton and packing materials until the contents have been inspected. If there is evidence of damage, do not attempt to use the equipment. Contact the shipper and file a shipment claim.

2.3 RESHIPPING

If return of the receiver should become necessary, a Returned Material (RM) number must first be obtained. This number must be clearly marked on the outside of the shipping carton.

2.4 INSTALLATION

Thoroughly plan the receiver/antenna locations and carefully follow the installation considerations given below. Satisfactory system performance depends upon the care and attention taken prior to and during installation.

The protection connector covers installed on the receiver for shipping should remain over unused connectors.

2.4.1 REAR PANEL

All external connections are made to the receiver's rear panel. Mounted on the rear panel are the following connectors.

WARNING

Before connecting power, check voltage selector card and fuse located under power cord.

• AC POWER - Standard AC Power connector. To change AC input voltage, the line cord is unplugged from the assembly. Then the plastic cover is slid down exposing the fuse/selector card chamber. The operating voltage is indicated by the exposed numbers on the card. By top-to-bottom, the operating voltage may be changed from 115 volts (marked 120), to 230 volts (marked 240), to 100 volts (marked 100), to 220 volts (marked 220). Operation at 400 Hz at 115 or 230 VAC ±15% is possible by selecting the 100V or 220 VAC position. The appropriate fuse must be installed when the operating voltage is changed. (See Fuses in Section 3.3.2.)

• ANTENNA (J46) - An SO-239 type connector.

• GND - A 1/4-20 chassis ground stud.

• FUSE - 1A for 115V or 0.5 for 230V.

• SIGNAL IN/OUT (J42) - A 25-pin miniature "D" connector containing the audio line outputs, optional two-wire FSK remote control lines, miscellaneous signals, and spare lines for future use. See Table 2.1.

• RS-232 (J43) - A 25 pin miniature "D" connector containing FSK remote control lines duplicated from the signal IN/OUT connector; remote control lines for RS-232C, RS-422, RS-423, MIL-STD-188C; and remotely switched audio lines (with option). See Table 2.2.

• BCD (J44) - An optional-25 pin miniature "D" connector installed as part of the BCD Interface kit to control the MSR 6300 Preselector. Fourteen BCD encoded frequency control lines and a TX/RX line are included (TTL high >/= +3.5 VDC, TTL low </= +0.8 VDC). See Table 2.3.

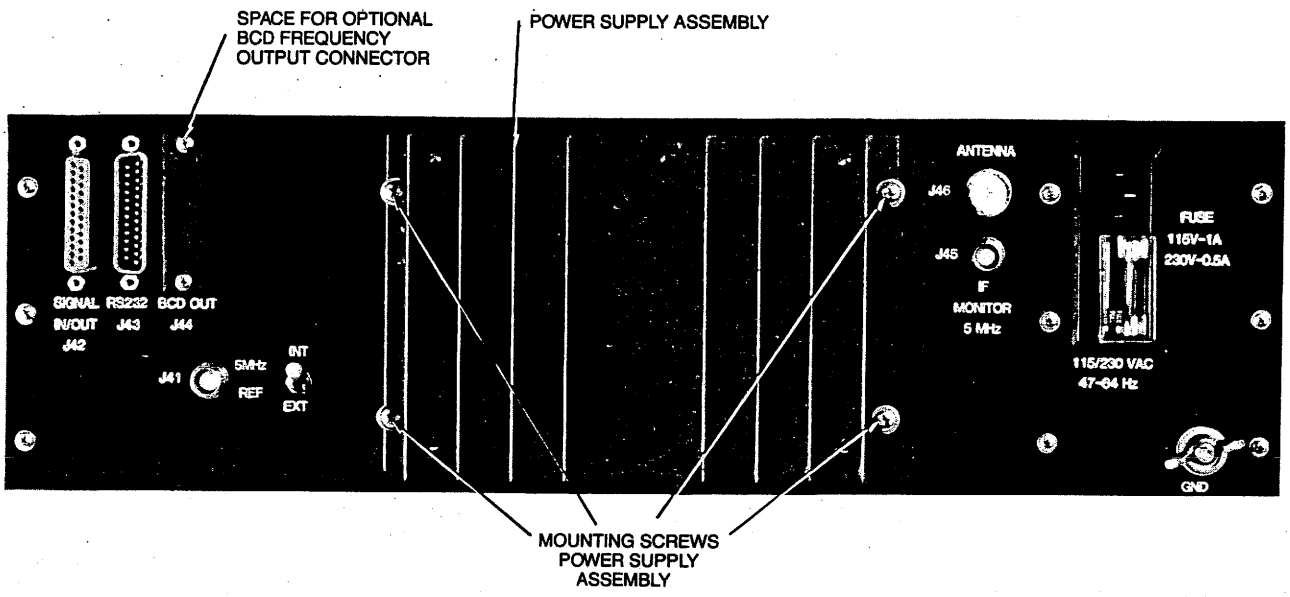


Figure 2.1

MSR 5050A Rear Panel

• REF IN/OUT (J41) - A BNC for the 5 MHz reference. Rear panel switch determines whether this is an input or output. Output loading is limited to 20pf.

• IF MONITOR (J45) - A BNC which provides a 5 MHZ filtered IF output signal at 50 ohms. Nominal level is -40 dBm.

2.4.2 INSTALLATION CONSIDERATIONS

2.4.2.1 Antenna Site Location

For optimum characteristics and safety, the antenna should be mounted high enough to clear any surrounding obstructions. The antenna should also be located as far as possible from nearby objects such as power lines, buildings, etc.

2.4.2.2 Adequate Ground

Provide the best possible RF ground for the receiver and the antenna. Use a flat copper strap, 25 mm wide or number 6 guage or larger wire and connect it to the ground terminal at the rear of the receiver and on the antenna. Leads to the ground system should be as short as possible.

2.4.3 BASE STATION INSTALLATION

The receiver can be installed in its own (optional) cabinet for the table-top mounting or can be installed in a communications console.

It is important to provide adequate ventilation for the heat-sink. Clearances on the order of 25 mm on the sides and 50 mm at the top and rear should be provided.

2.4.3.1 Rack Mount Installation

The receiver may be conveniently mounted in a standard 19 inch rack, by using the rack mount kit (P/N 600078-700-001). This kit includes a pair of rack slides, and associated hardware. The receiver in the rack mounted configuration requires a standard panel space of 13.21 cm (5.2 inches).

The front panel is not designed to support the receiver when the unit is installed in an equipment rack.

CAUTION

Do not support the receiver by the chassis bottom in such a way that the air flow will be restricted.

If installation assistance is required, consult the Mackay Communications Service Department.

2.4.4 MARINE INSTALLATION

The receiver is not weather, splash and corrosion resistant, and should not be installed where it is exposed to salt spray. It should be installed in a well ventilated area away from heat sources such as heating vents, etc. The location should be as close as possible to the power source and grounding point.

IT IS RECOMMENDED THAT THE RECEIVER BE SECURELY GROUNDED, as poor grounding can degrade performance. With a metal hull, the receiver can be grounded directly to the vessel's structure. With a wood or fiberglass hull, a grounded/counterpoise system must be constructed. The counterpoise should have as much surface area as possible. About 9.5 square meters (100 square feet) should be provided for 2 MHz operation. A reasonably good ground can be achieved by bonding together large metal objects. Bonded to this ground should be two or three wide copper straps running as far as possible fore and aft, together with three or four cross members (ground plates may be effective on lower frequencies but are subject to fouling; therefore, they are not recommended). Figure 2.1 shows a typical ground/counterpoise system.

2.5 ANTENNA AND GROUND SYSTEMS

The receiver is designed to operate from a 50 ohm resistive antenna system. VSWR should be low to ensure optimum performance.

Some general antenna system guidelines are:

• Mount the antenna as high as possible.

• Where possible, use antennas over 1/8 wavelength long at the lowest operating frequency.

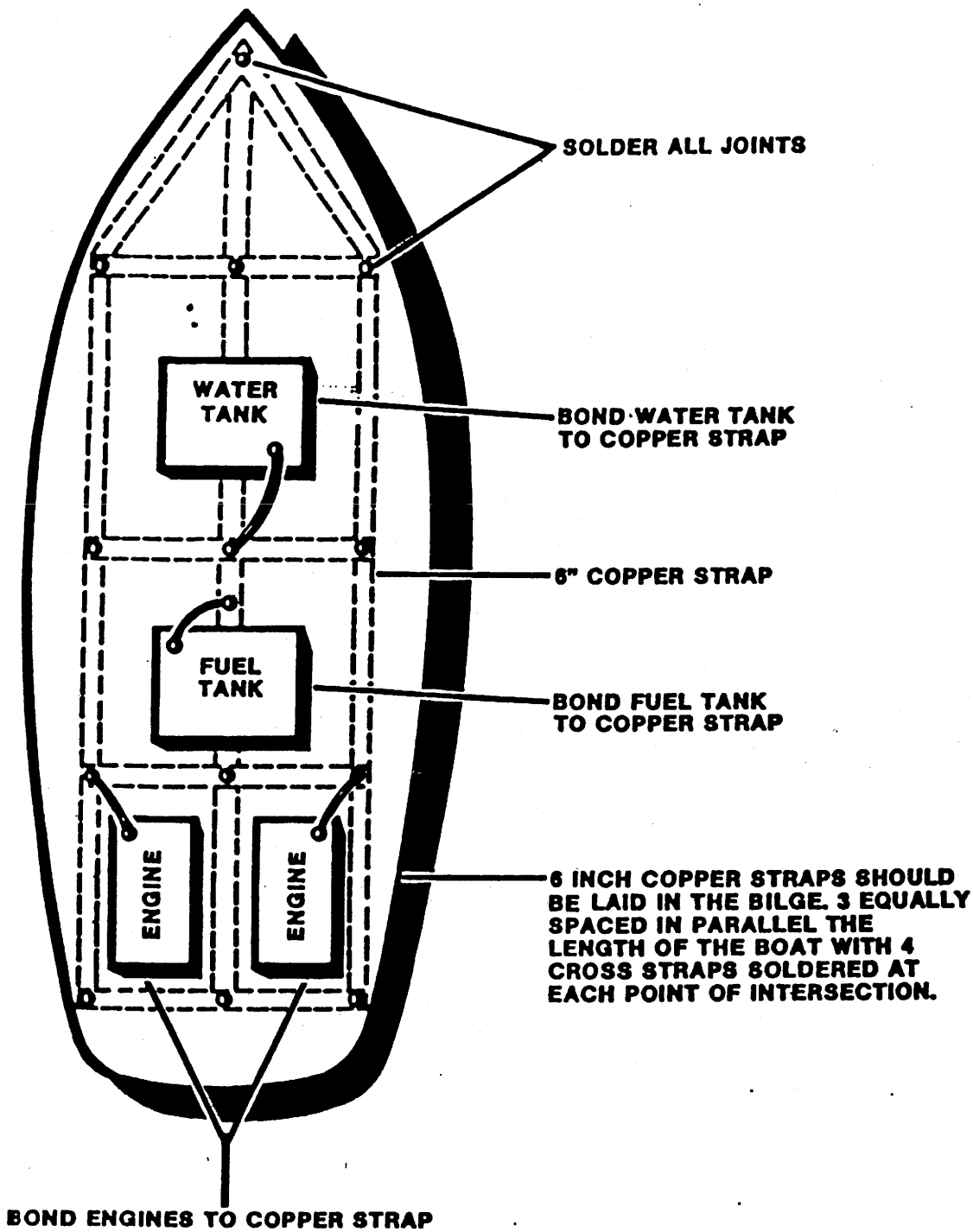


Figure 2.2 Typical Ground/Counterpoise Installation

• Short antennas are most sensitive to ground loss. When a short antenna is used, the best possible ground system should be obtained.

• On ships with non-metallic hulls, make the ground/counterpoise system cover as large an area as possible. Make maximum use of large metal objects, copper screen, the propellor shaft and properly bonded copper straps.

When used with a MSR 6700A Exciter or MSR 8050A Transceiver sharing the same antenna, an external T/R relay is required - - operated from the TX line from the transmitter (refer to options to the MSR 6700A or MSR 8050A). The T/R relay is built into the MSR 1020 1kW LPA. In these cases efficient matching to short or long wire antennas is accomplished with associated An-tenna Couplers MSR 4020 (125 watt), MSR 4040 (125 watt) or MSR 4030 (1 kW). The frequency of efficient matching is determined by the transmitter frequency.

Table 2.1

SIGNAL IN/OUT CONNECTOR (J42) PIN ASSIGNMENTS

PIN	LINE NAME	DESCRIPTION
1	+13 VDC	Utility output 100 mA max.
2	CNTL STAT C	600 Ohm FSK remote port 2
3	CNTL STAT D	Return line for pin 2
4	NC	
5	/PWR ON	TTL low input turns unit on
6	+5 VDC	Utility output 100 mA max.
7	GND	
8	GND	
9	GND	
10	SIDETONE	External 0 dBm, 600 Ohm audio input produces speaker output.
11	AGC B	AGC voltage output (0 to 6 VDC) from optional ISB IF channel
12	NC	
13	/STOPSCAN	TTL low input stops channel scanning
14	NC	
15	CNTL STAT A	Remote FSK 600 Ohm port 1
16	CNTL STAT B	Return line for pin 15
17	SPKR RET	Return line for pin 18
18	SPKR	Output for external speaker (2 Watts at 3.2 Ohms/ 1 Watt at 8 Ohms)
19	/SCAN DET	TTL low (open collector) output when receiver stops on channel (in scan mode) with signal > scan threshold
20	/MUTE	TTL low input mutes receiver and reduces IF gain
21	ISB B2	Return line for pin 22
22	ISB A2	600 Ohm audio line output from optional ISB channel
23	STD A2	600 Ohm audio line output from standard receiver IF channel
24	STD B2	Return line for pin 23
25	AGC A	AGC voltage output (0 to 6 VDC) from standard receiver IF channel

Table 2.2

RS-232 CONNECTOR (J43) PIN ASSIGNMENTS

PIN	LINE NAME	DESCRIPTION
1	NC	
2	GND	
3	RXB BAL	Return line for pin 18; RS-422 only
4	TXB	Remote control output line
5	NC	(internal locating pin)
6	TXB BAL	Return line for pin 4; RS-422 only
7	RXA BAL	Return line for pin 9; RS-422 only
8	TXA BAL	Return line for pin 10; RS-422 only
9	RXA	Remote control input port 1 *
10	TXA	Remote control output port 1 *
11	NC	
12	NC	
13	NC	
14	SW ISB B	Return for pin 15
15	SW ISB A	Remotely addressed - switched 600 Ohm audio from ISB channel
16	SW STD B	Return for pin 17
17	SW STD A	Remotely addressed - switched 600 Ohm audio from standard channel
18	RXB	Remote control input port 2 *
19	NC	Reserved
20	CNTL STAT C	600 Ohm IN/OUT port 2 for FSK remote control
21	CNTL STAT D	Return for pin 20
22	DNTL STAT A	600 Ohm IN/OUT port 1 for FSK remote control
23	CNTL STAT B	Return for pin 22
24	NC	
25	NC	

* Used for RS-232, RS-422, RS-423, or MIL-STD-188C format.

Table 2.3

BCD CONNECTOR (J44) PIN ASSIGNMENTS

PIN	LINE NAME	DESCRIPTION
1	1M4	TTL high output for 4 MHz bit
2	GND	
3	NC	
4	NC	
5	1M8	TTL high output for 8 MHz bit
6	NC	
7	NC	Internal key pin
8	NC	
9	NC	
10	NC	
11	100K1	TTL high output for 100 kHz bit
12	10K1	TTL high output for 10 kHz bit
13	100K2	TTL high output for 200 kHz bit
14	1M2	TTL high output for 2 MHz bit
15	1M1	TTL high output for 1 MHz bit
16	10M2	TTL high output for 20 MHz bit
17	10M1	TTL high output for 10 MHz bit
18	NC	Internal key pin
19	+12 VDC	Future output for Preselector 700 ma.
20	/TX2	TTL low output (internally bussed from /MUTE input on J42 pin 20). Used to control TX/RX state of MSR 6300 Preselector.
21	10K8	TTL high output for 80 kHz bit
22	100K8	TTL high output for 800 kHz bit
23	10K4	TTL high output for 40 kHz bit
24	100K4	TTL high output for 400 kHz bit

SECTION 3

OPERATION

3.1 GENERAL

This section describes the control and connector functions and gives complete operating instructions for the receiver.

3.2 FRONT PANEL CONTROLS AND CONNECTORS

Refer to Figure 3.1 for control locations.

NOTE

Most front panel functions switches contain LEDs (Light Emitting Diodes) to indicate when a particular function is active. Mode, filter and AGC switches have associated bar-graph LED indicators.

3.2.1 HEADPHONE JACK

The headphone jack accepts a standard 1/4" two circuit plug from the headphones. Using the headphone jack does not cut off the speaker. Headphone impedance of 600 ohms or more is recommended.

3.2.2 SPEAKER SWITCH

This switch turns the internal speaker on and off.

3.2.3 VOLUME/POWER

Controls the received signal level at the speaker and PHONES jack. Click-off CCW position turns off the receiver primary power. VOLUME setting does not affect 600 ohm receive audio output.

3.2.4 SQUELCH/RF GAIN

This is a dual function control which reduces RF/IF gain by CCW rotation from its normal full clockwise position. Pulling the knob engages the syllabic squelch circuit which mutes the audio for all but signals with voice characteristics.

3.2.5 KEYPAD

The keypad is a 3 x 4 array of momentary switches electrically connected in a row/column matrix to interface with the microprocessor data bus. These keys are used for numeric entries such as frequency, channel, etc. The E (enter) key is normally used to execute a program function.

3.2.6 CHANNEL

Pressing the "CHAN" key will put the radio into "Channel Mode". Channel mode is used to select a new channel or program the current channel. There are 100 channels available (00-99). Channel 00 is reserved for use by the radio and is sometimes referred to as the "scratchpad" channel. It is not intended to be used by the operator as permanent channel storage. When the radio is placed into channel mode the CHAN key LED will light and the channel display window will display "---". This indicates that the radio is waiting for a channel number to be entered.

To change channels, press the CHAN key to put the radio into channel mode, and then enter the desired channel number. When both digits of the channel number are entered, the radio will recall, display, and output the new channel. The radio will stay in channel mode until a channel number has been entered and the ENTER key pressed. This allows successive channels to be recalled without having to press the CHAN key each time. Pressing ENTER will cause the radio to select the channel and leave channel mode. Pressing the CLEAR key will cause the last channel (before entering channel mode) to be restored (this also causes the radio to leave channel mode).

To program a channel, first enter channel mode and select the channel number to be programmed. Press the FREQ key to enter the desired frequency. Press the BFO key to enter the desired BFO (if the BFO option is not installed

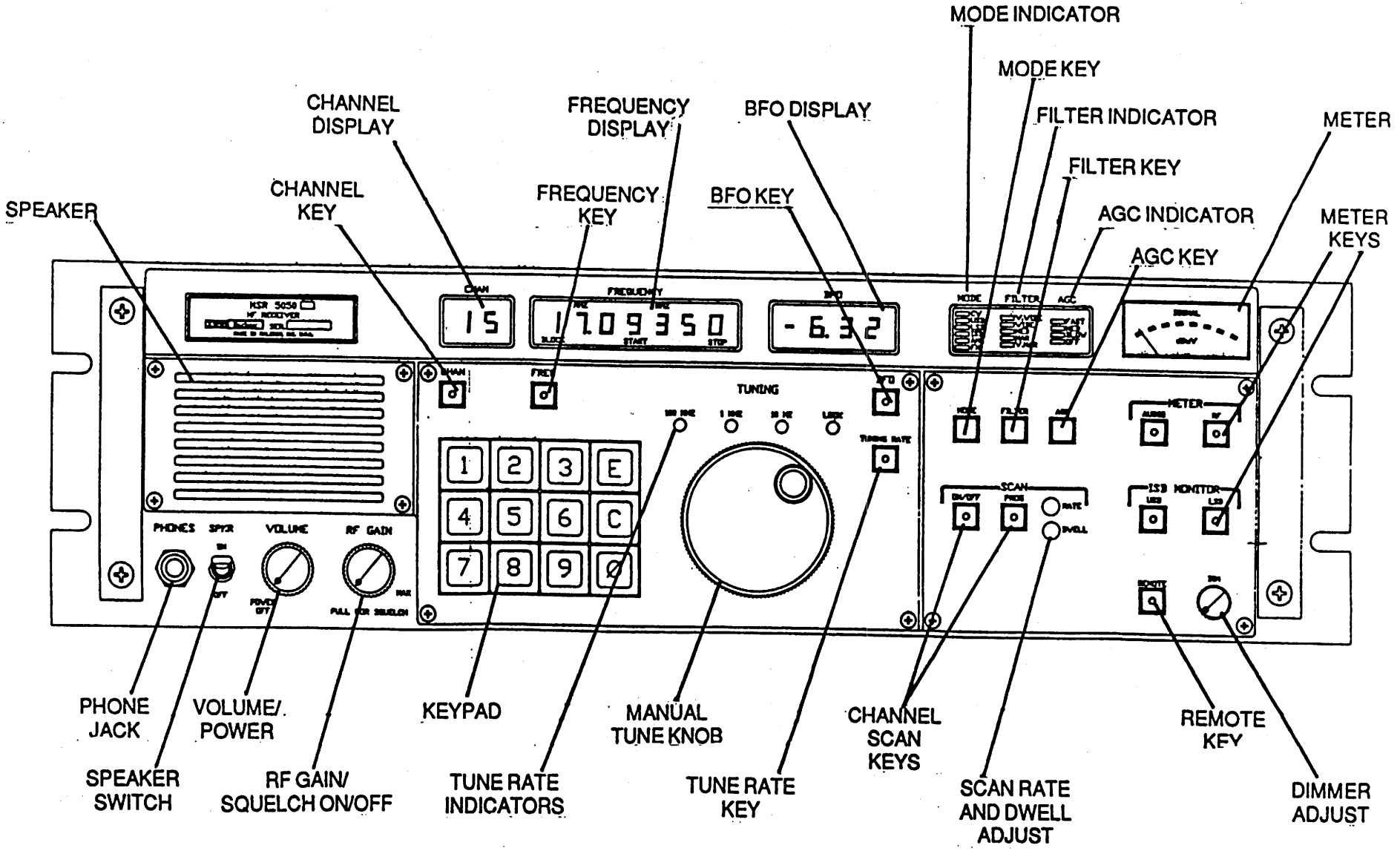


Figure 3.1

Front Panel Controls and Connectors

in the radio then the BFO key is ignored). Enter the desired Mode, Filter and AGC speed. Pressing the ENTER key will cause this data to be stored in the permanent channel memory. Pressing the CLEAR key will cause the previous channel to be restored, and no data is saved. If a new channel number is entered then the previously selected channel is left intact (no data is stored).

3.2.7 FREQUENCY

The frequency of the radio (indicated by seven LED displays) is changed by numeric keypad entry or by rotation of the tuning knob. The keypad entry is enabled by pressing the "FREQ" key. The tuning knob, normally locked, can change the frequency in incremental steps of 10 Hz, 1 kHz or 100 kHz as selected by the TUNING RATE key and indicated by the LEDs above the knob.

To enter a new frequency, press the FREQ key. This will cause the radio to enter frequency mode (the FREQ key LED will light). As the frequency is entered, the display will update to show the next digit to be entered. Pressing the CLEAR key will allow the operator to backspace to correct mistakes. If the CLEAR key is pressed in the first digit (it can not backspace) then the radio will restore the frequency for the currently selected channel and it will leave frequency mode. When all seven digits of frequency have been entered, the radio will attempt to change to the new frequency. If the desired frequency is too high, the maximum frequency available for that radio will be substituted. Likewise, if the desired frequency is too low, the minimum frequency for that radio will be substituted. The radio will stay in frequency mode to allow another frequency to be entered. Pressing the ENTER key will cause the radio to select the new frequency. If the frequency has only partially been entered then pressing ENTER will cause the remaining digits to be filled in as 0, and the radio will leave frequency mode.

Entering frequency mode will cause the radio to select channel 00 unless the radio is in channel mode at that time. The selected frequency is stored in channel 00. If the frequency is to be stored permanently, it must be saved in a channel other than channel 00.

3.2.8 BFO (Optional)

Pressing the BFO (Beat Frequency Oscillator) key on the front panel will cause the radio to go into BFO mode. If the BFO option is not installed in the radio the BFO key is locked out, and the BFO window will display "---".

To enter a BFO value, press the BFO key to enter BFO mode. Assuming the BFO option is installed, the BFO window will display the current setting. The tune rate indicator will preset to 10 Hz rate, and the TUNE knob will be enabled to control the BFO offset frequency from +7.99 kHz (the "+" sign being suppressed) to -7.99 kHz. When the desired BFO offset is indicated, pressing E (enter) will store the BFO in the indicated channel and exit the BFO mode. Pressing C (clear) will return the BFO offset to the previously stored entry for the indicated channel and exit the BFO mode. In both cases the BFO key LED will turn off, returning the TUNE knob to frequency. The tune rate will preset to 10 Hz when entering BFO mode with only 1 kHz or 10 Hz rates being available with the TUNE RATE key. The TUNE rate will revert to the previous position when exiting the BFO mode.

The BFO is used to modify the detected audio signal frequency. It is active in USB, LSB, ISB, CW and FSK modes although normally used only in CW or FSK modes. The standard radio (without filter option or BFO) receives J2A CW signals which are offset from the assigned channel center frequency (by 1 kHz for normal communication systems) and produces an audio output frequency equal to the offset. FSK signals (also offset) are reproduced the same way. Adding the BFO option produces an output frequency equal to SIGNAL FREQ - RCVR FREQ - BFO OFFSET. For a signal offset + 1 kHz from a 11.000 MHz assigned channel frequency, a receiver tuned to 11.000 MHz in CW (or FSK or USB) would produce a 1 kHz output with BFO offset 0.00 kHz. A BFO offset of +0.10 kHz would produce 0.9 kHz output, and an offset of -0.10 kHz would produce 1.1 kHz output.

An MSR 5050A with Filter Option electrically centers all CW and FSK filters on the receiver frequency. Operation is the same as before except for NAR (1 kHz bandwidth) and VNAR (400 Hz bandwidth) filters. A 1 kHz offset signal would be out of the passband for these filters so the receiver must tune to 1 kHz (11.001 MHz) to center the signal in the IF passband. The resulting audio frequency would then be zero. Offsetting the BFO by + or - 1 kHz would then produce the 1 kHz intended output.

3.2.9 MODE

To change the radio detector mode, press the MODE key on the front panel. This will cause the radio to switch to the next available mode. The current mode is displayed in the window above the MODE key. The new mode is not stored in channel memory unless the channel is being programmed through channel mode. ISB and FM positions are options and will be skipped in the toggle sequence unless activated by internal switches on the logic board.

3.2.10 FILTER

To change the filter, press the FILTER key on the front panel. This will cause the radio to switch to the next available filter. The current filter is displayed in the window above the FILTER key. The new filter is not stored in channel memory unless the channel is being programmed through channel mode.

When operating in USB, LSB or ISB, dedicated SSB filters are used. The "MED" filter position is lit with all other positions locked out.

When AM mode is selected, the "WIDE" filter (5 kHz bandwidth) is automatically selected. In the standard radio, the "MED" filter (3 kHz bandwidth) may also be selected with all other filters locked out. With the FILTER option installed, the V WIDE (12 kHz bandwidth), NAR (1 kHz bandwidth) and VNAR (400 Hz bandwidth) may also be selected.

When CW mode is selected, the MED filter is automatically selected, with the WIDE filter available as a second choice. In the standard radio, the MED filter is a USB filter with passband from +300 to +3000 Hz. The WIDE filter has a ±2.5 kHz bandwidth. All other filters are locked out. In the MED position the receiver then is tuned to the channel assigned frequency to receive a CW signal 1 kHz above frequency. In the WIDE position CW signals above or below channel frequency can be received; and CW signals right on channel frequency could also be received with the BFO option (which would produce an audio frequency output with an appropriate BFO offset).

With the Filter option, the same filters available for AM are available for CW, and all filters are electrically centered on the tuned frequency (the MED filter bandwidth of +300 to +3000 Hz then is 0±1300 Hz). For J2A emissions where the signal is 1 kHz offset from the channel frequency, operation could be the same as the standard radio; producing 1 kHz audio without a BFO offset. For NAR and VNAR filters however, the signal would be outside the filter passband. In this case the receiver must be tuned to the signal frequency, not channel frequency (i.e. for a zero beat or maximum RF meter indication), and then modified by BFO offset to produce the desired audio.

3.2.11 AGC

To change the AGC decay rate, press the AGC key on the front panel. This will cause the radio to switch to the next available AGC rate. The current AGC rate is displayed in the window above the AGC key. The new AGC rate is not stored in channel memory unless the channel is being programmed through channel mode.

The AGC rate relates to the time AGC circuits adjust from a high level to a low level antenna signal. The attack time or reaction time from low level to high level signals is less than 10 milliseconds in all positions. The decay time in FAST is < 50 milliseconds, in MED 200 milliseconds, and in SLOW 3 seconds. The AGC OFF position disables the AGC detector, transferring IF/RF gain control from antenna signal to the manual RF gain control. In frequency scan and channel scan, the AGC is forced to FAST rate. If the scan is manually stopped (with the "C" key), the AGC

rate returns to the AGC rate programmed for the channel indicated. In remote status (remote key LED lit) the front panel RF gain control is disabled and a remotely addressed gain control is enabled.

3.2.12 METER

The meter indicates either received RF signal strength (in dB above 1 U volt) or detected audio signal level deliverable from the rear panel 600 ohm line output (in dBm). The desired meter response is selected by the AUDIO/RF keys below the meter (the active key being lit). The audio output level is internally adjustable by R64 on the audio squelch board (accessable by removing the top cover). If the ISB option is installed, the ISB 600 ohm line level (LSB) is independently adjustable by R64 of its associated audio squelch board. The audio level indicated on the meter depends on the load impedance on that line and reads accurately only with a proper 600 ohm load. (The output reads 6 dB high with no load.) If the Addressable Audio I/O option is installed, both a switched and non-switched 600 ohm audio output is provided for standard and ISB outputs. In this case the meter reads available power independent of loading. The normal output level is 0 dBm for all outputs and is adjustable from -10 to +10 dBm. The keys revert to "AUDIO" position on power-up or when pressing "C" (reset).

3.2.13 ISB MONITOR

The ISB MONITOR keys select either USB or LSB signal inputs to the meter and to the speaker. These keys are only activated when the receiver is in ISB mode which, in turn, is only possible with the ISB option installed. In the ISB mode two independent signal paths are enabled producing simultaneous audio outputs from USB signals on one channel and LSB on the other. The USB audio output is on the standard 600 ohm line output (which also produces the audio from all other detection modes). The LSB audio is on the ISB 600 ohm line output in ISB mode but on the standard 600 ohm line in LSB mode. The keys only affect local meter and speaker monitoring and do not interrupt or change the rear panel line outputs. The RF meter position indicates the larger signal level of the USB/LSB channels when in ISB mode, but indicates individual audio levels in AUDIO position. In ISB mode, the monitor keys revert to USB position on power-up or when pressing "C" (reset). In all other modes the USB monitor key is locked on indicating only the standard 600 ohm line is active.

3.2.14 DIMMER

The DIMMER control adjusts the brightness of the displays and the status LEDs.

3.2.15 REMOTE KEY/REMOTE OPERATION

Selecting the REMOTE key locks all front panel controls except the DIMMER, VOLUME/POWER OFF, SPEAKER ON/OFF, and SQUELCH ON/OFF controls. In REMOTE the radio may be controlled from a computer or from the MSR 6420 univeral remote control unit via two wire FSK or RS-232, RS-422, RS-423, MIL-STD-188 formats. The radio is selected for control by a two digit address code (00 to 99). This code is operator-programmed into the radio memory by pressing E5, then the two digit number and then E. (This is done in the Local mode.) After E5 is pressed, the frequency display will indicate the presently stored code by "Addr XX". If the number is acceptable, either C or E may be pressed to return to previous radio conditions. To change the address, two numbers are then entered. When the second number is entered, the address is stored and the radio returns to previous conditions. Refer to the MSR 6420 manual or CSW 1000 software manual (as applicable) and Section 6 for details on interconnects and operation via remote control. See Table 3.1 for setting internal switches.

3.2.16 CHANNEL SCAN CONTROLS

The MSR 5050A is designed to scan an unbroken sequence (block) of up to 99 channels. Up to10 blocks may be memorized and recalled for scan by block number. The SCAN-PROG key enables scan block programming. The SCAN-ON/OFF key starts the scanning of the block number entered. SCAN-RATE is a screwdriver adjustment which varies the rate of scanning from 0.2 to 5 channels per second (5 to 0.2 seconds pause on each channel). SCAN-DWELL is a screw-

driver adjustment which varies the delay time on channel when a scanned signal exceeds a threshold response. An internal adjustment (R36 on the interface board) sets the threshold to as low as 1 µVolt equivalent antenna input.

To program a channel block, first press the SCAN PROG key. The key will light and the frequency display will blank except for a "---" over the block digit. This cues the operator to enter the desired block number. (If either the C or E key are pressed, the frequency display will return to normal and the scan program mode will be aborted with no change in data.) Pressing the block number (0 to 9) recalls and displays the START channel and STOP channel previously stored in that block. Next enter a two digit START channel (00 to 99). After the first digit is entered, the second digit position is displaced by "---" to cue the operator to enter the second digit. The two-digit stop channel is next entered (with a "---" cueing each digit entry). The stop channel entry completes and stores the program for that block. The frequency display will blank except for a "--" in the block digit position, cueing the entry of another block program following the same sequence. If no other entry is desired, pressing "C" or "E" will exit the SCAN PROG mode returning the radio to previous settings.

To scan a block of channels, press the SCAN ON/OFF key. This will cause the frequency display to blank except for a "---" over the block digit. Enter the desired scan block (0-9). After the scan block has been entered, the start and stop for that block are displayed. If another number is entered, that scan block is displayed. This allows the operator to review the contents of each scan block. If the CLEAR key is pressed, the radio will restore the frequency display and will leave scan mode. After selecting a scan block, press the ENTER key to begin scanning. The radio will select the start channel, and will increment through the channels until it reaches the stop channel. After the stop channel is scanned, the start channel is selected and the process begins again. If during scanning a signal is detected on a channel, the radio will pause on that channel before going on to the next channel. The rate and dwell controls are used to control the scanning speeds. Both of these controls are adjusted by means of a small screwdriver. The RATE control determines the time the radio pauses on a channel before going to the next channel. The DWELL control determines the amount of time the radio will pause on a channel if a signal is detected. The operator can use the RF GAIN control (lower left corner), to control the signal strength needed to cause the radio to pause during scanning. This will keep the radio from pausing due to static or very weak signals. Pressing either the ENTER or CLEAR key will cause the radio to pause on the current channel. This allows the operator to listen to the channel as long as he likes. Pressing any key will allow the radio to resume scanning. To stop scanning press the SCAN ON/OFF key.

By moving an internal jumper (JP1 on the interface board) to the left, the scan mode may be altered to HOLD on a channel where a signal exceeds the scan detector threshold. As long as the signal exceeds the threshold, the scan DWELL time will be extended. Scan will not resume until the signal remains below threshold for a period longer than the dwell time. Scan may be manually continued even while stopped on a signal by pressing E or C, or by turning the RF GAIN control CCW. Enabling the SQUELCH control will prevent the scan from being locked on a large CW signal. The squelch will momentarily open but will mute the radio after approximately two seconds.

3.2.17 FREQUENCY SCAN

Frequency scan is similar to channel scan, except that the frequency changes while the Mode, Filter and the AGC decay rate remain the same. The frequency is incremented in 10 Hz, 1 kHz or 100 kHz steps. Frequency sweeping is similar to using the manual tuning knob except that the radio continually sweeps a frequency range, pausing when a signal is detected.

To Frequency Scan, first select the scan increment by pressing the TUNING RATE key. This determines which frequency digit is incremented during scanning. Key in the E6 sequence to enter frequency sweeping mode. The radio automatically switches to channel 00, and the channel win-

dow displays "St". Enter the starting frequency. (Pressing ENTER will select the current frequency as the starting frequency. Pressing CLEAR terminates frequency sweeping mode.)

After the starting frequency has been entered, the channel window will display "SP". Enter the stopping frequency. (Pressing ENTER will select the current frequency as the stopping frequency. Pressing CLEAR terminates frequency sweeping mode.) After the stop frequency has been entered, the radio will begin frequency sweeping. The frequency will increment, pausing momentarily when a signal is detected. The RATE and DWELL controls are used to control the sweeping speeds. Both of these controls are adjusted by means of a small screwdriver. The RATE control determines the time the radio pauses on a frequency before going to the next frequency. The DWELL control determines the amount of time the radio will pause on a frequency if a signal is detected. The operator can use the RF GAIN control (lower left corner) to control the signal strength needed to cause the radio to pause during sweeping. This will keep the radio from pausing due to static or very weak signals. The operator can make the radio pause during sweeping by pressing the CLEAR key. The channel window will display "PS". Pressing any key (other than the CLEAR key) will allow the radio to resume scanning. Pressing the CLEAR key when the radio is paused will terminate frequency scan. While the radio is in frequency scan, the TUNING RATE key can be pressed to change the digit incremented.

In order for frequency sweeping to operate correctly, the starting frequency should be lower than the stopping frequency. Frequency sweeping with the TUNING RATE in the LOCK position does not do any harm, but it does not allow for sweeping to occur. The Mode, Filter and AGC decay rate should all be selected before frequency sweeping begins.

3.2.18 MANUAL TUNING CONTROLS

The radio frequency or BFO can be changed manually by use of the tuning knob (located in the middle of the front panel) and the tuning rate selector (located to the right of the tuning knob).

The tuning knob is used to manually scan for a signal.

To use the tuning knob, first select a tuning rate by pressing the Tuning Rate key. The tuning rate determines which frequency digit will change when the tuning knob is rotated. When the tuning rate is in the "LOCK" position, the tuning knob is ignored. Rotating the tuning knob clockwise will cause the frequency to increase, likewise, rotating the knob counterclockwise will cause the frequency to decrease. When the desired frequency is found the tuning rate should be placed in the LOCK position to keep the frequency from changing should the tuning knob accidentally be moved.

The tuning knob is used to temporarily change the frequency. The new frequency is not stored in channel memory. Use channel mode to store the new frequency in channel memory.

3.3 REAR PANEL CONTROLS AND CONNECTORS

3.3.1 POWER CONNECTOR

Accepts standard AC input of 115V or 230 VAC ±15% 47 to 400 Hz.

Operating voltage is selected by a printed circuit card plugged into the connector assembly.

3.3.2 FUSES (Inserted in power connector)

Fuses are slo-blo type. 1A 115 VAC or 0.5A 230 VAC.

3.3.3 EXTERNAL REFERENCE INPUT (J41)

A BNC jack accepts an external reference frequency input or outputs the internal 5 MHz reference depending on the adjacent switch position.

3.3.4 EXT/INT REFERENCE SWITCH

EXT/INT reference switch selects an externally applied reference signal, or the internal reference. The switch is located on the rear panel by J41.

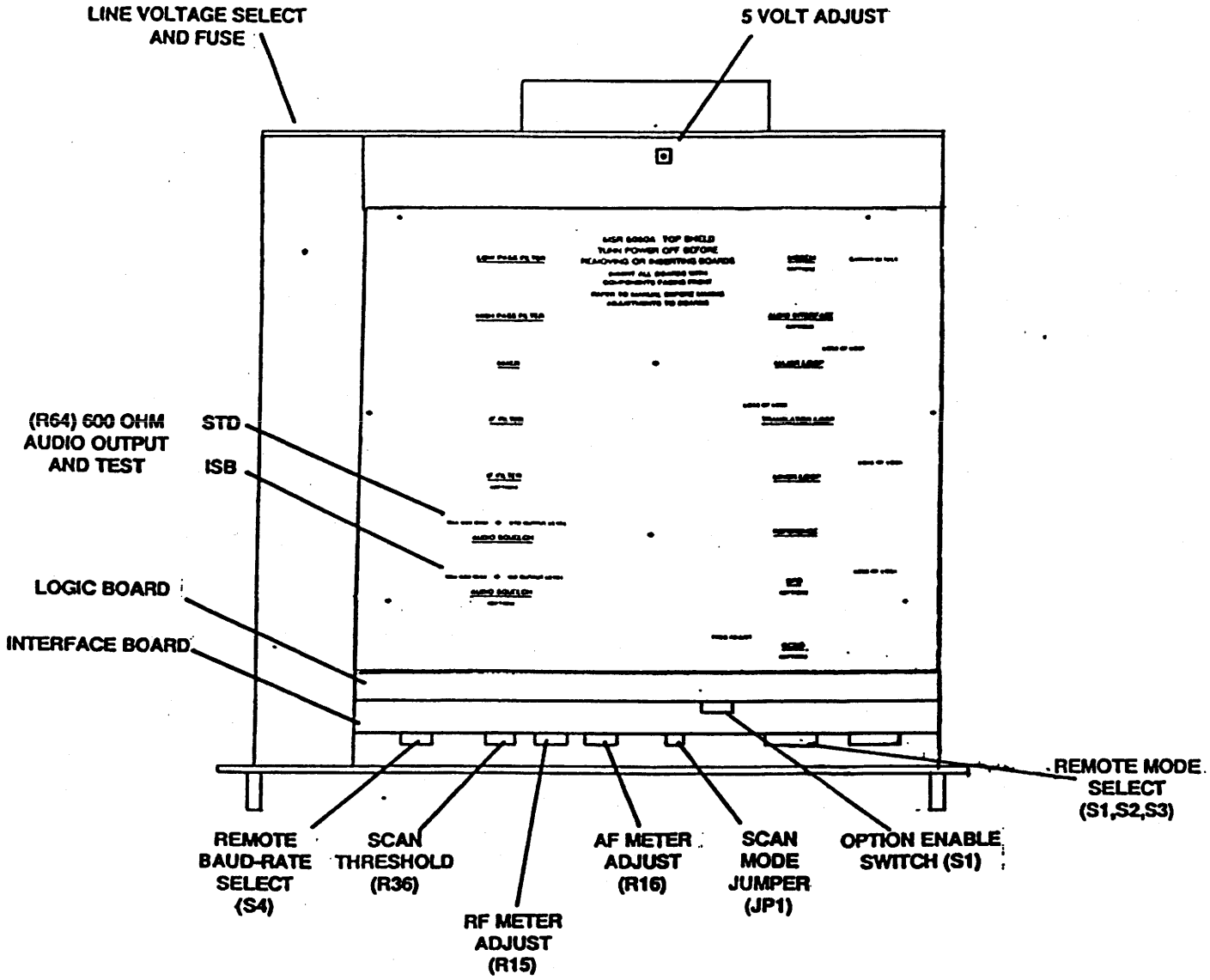


Figure 3.2

Internal Control Locations

3.3.5 IF MONITOR (J45)

A BNC jack outputs a 5 MHz IF signal for external monitor.

3.3.6 ANTENNA CONNECTOR (J46)

Connects RF input to the receiver. Mates with standard PL-259 connector.

3.3.7 GROUND STUD

Used for making good RF ground to receiver.

3.3.8 SIGNAL IN/OUT (J42)

Connects 600 ohms balanced audio lines and miscellaneous control and monitor lines. (See Table 2.1.)

3.3.9 RS-232 CONNECTOR (J43)

For remote control via RS-232, RS-422, RS-423, MIL-STD-188C. (See Table 2.2.)

3.4 OPERATOR INTERNAL CONTROLS

Refer to Figure 3.2 for locations.

3.4.1 LINE VOLTAGE

Selects line voltage input of 115 VAC or 230 VAC.

3.4.2 600 OHM RECEIVE OUTPUT LEVEL

This control (R64) adjusts the level of 600 ohm receiver audio that can be supplied from the receiver to the remote source or optional equipment. Nominal output is 0 dBm, adjustable to +10 dBm.

3.4.3 SCAN THRESHOLD (Interface board R36)

Varies the signal level required to stop scan in either channel or frequency scan. Factory set at approximately 2μ volts.

3.4.4 METER ADJUST (Interface board R15, R16)

Adjusts full scale meter deflection for 100 mvolts RF signal (R15) and +10 dBm audio output (R16).

3.4.5 SCAN HOLD JUMPER (Interface board JP1/E1)

JP1 to the left causes Channel or Frequency Scan to stop as long as signal is above threshold; to the right causes scan to stop for a "dwell" time and then continue.

3.4.6 OPTION SWITCH (Logic board S1)

Four switch position (down-engaged) selects ISB, Filter, BFO and FM options, enabling microprocessor programming and displays for those options.

3.4.7 REMOTE MODE SELECT (Interface board S1, S2, S3)

Conditions the radio for either RS-232, RS-422 or internal FSK modem remote control formats. See Table 3.1.

3.4.8 BAUD-RATE (Interface board S4)

Sets rate of data transfer in remote control operation from 300 to 9600. See Table 3.1.

3.4.9 5 VOLT ADJUST (Power Supply board R18)

Fine adjusts +5 volt supply in radio.

3.4.10 INDICATORS (See Figure 3.4.)

Amber LEDs indicate presence of power supply voltages +13V, +9V and +5V; and presence of a remote control FSK carrier when the optional Modem board is installed.

Red LEDs indicate failure in one of the synthesizer boards by detecting a loss of lock. The front panel frequency display will indicate a failure of any one of the power supply voltages by "bite 01" or failure of any of the synthesizer loop boards by "bite 02".

3.4.11 OPTION JUMPERS

Various two-pin shorting jumpers (JPXX) are used to alter circuitry to accommodate optional

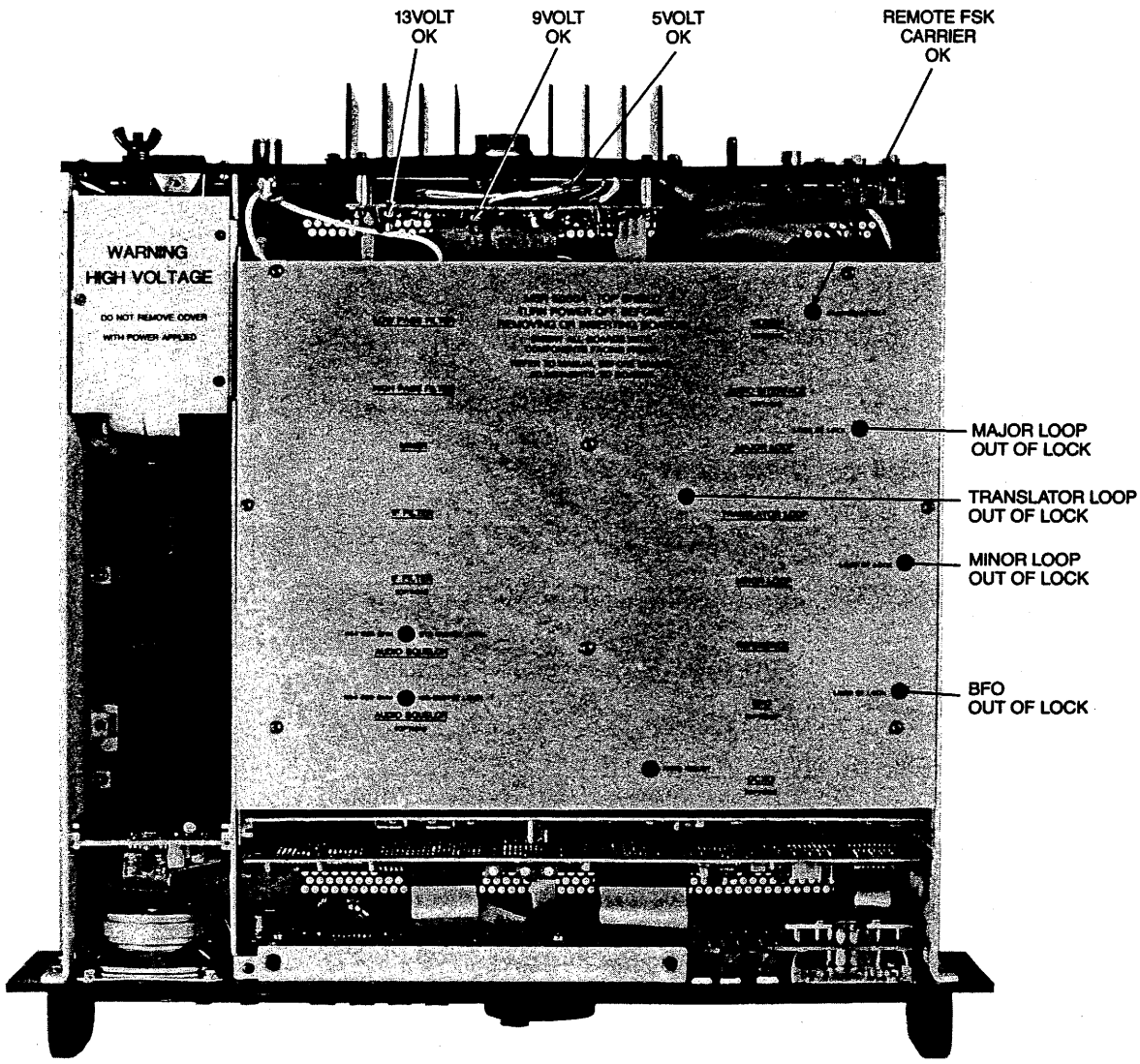


Figure 3.3
MSR 5050A Internal Fault/Status Indicators

Table 3.1

Baud Rate and Remote Mode Switches (Interface Board MSR 5050A, MSR 6700A)

S4	BAUD RATE SWITCH					
	300	600	1200	2400	4800	9600
1	0	X	0	X	X	X
2	X	0	0	0	X	0
3	0	0	0	X	0	0
4	X	X	X	0	0	0

1) Turn off AC power when setting switches.
2) All switches must be set to one of the configurations listed.
3) S2, S3, Baud Rate Switch:
X=Closed=On 0=Open=Off

* FSK-To-Digital Transitional Radio

	RX B, TX B PORTS				RX A, TX A PORTS				C/S PORTS			
	RS-232C RS-423	RS-422	MIL-188C	NO CONN	RS-232C RS-423	RS-422	MIL-188C	NO CONN	C/S USED, NO DIGITAL	NO C/S CONN	*C/S C,C/S D RX A, TX A	*C/S A,C/S B RX B, TX B
S1 - 1	—	—	—	—	UP	DN	UP	UP	—	—	—	—
2	—	—	—	—	DN	UP	DN	DN	—	—	—	—
3	—	—	—	—	UP	DN	DN	DN	—	—	—	—
4	UP	DN	UP	UP	—	—	—	—	—	—	—	—
5	UP	DN	UP	UP	—	—	—	—	—	—	—	—
S2 - 1	—	—	—	—	—	—	—	—	X	0	X	0
2	—	—	—	—	—	—	—	—	0	0	0	X
3	—	—	—	—	X	X	0	X	—	—	—	—
4	—	—	—	—	0	0	X	0	—	—	—	—
5	—	—	—	—	X	X	0	X	—	—	—	—
6	—	—	—	—	0	0	X	0	—	—	—	—
7	X	X	0	X	—	—	—	—	—	—	—	—
8	0	0	X	0	—	—	—	—	—	—	—	—
9	X	X	0	X	—	—	—	—	—	—	—	—
10	0	0	X	0	—	—	—	—	—	—	—	—
S3 - 1	—	—	—	—	X	X	X	0	—	—	—	—
2	—	—	—	—	0	0	0	0	—	—	—	—
3	—	—	—	—	X	X	X	0	—	—	—	—
4	—	—	—	—	0	0	0	0	—	—	—	—
5	0	0	0	0	—	—	—	—	—	—	—	—
6	X	X	X	0	—	—	—	—	—	—	—	—
7	X	X	X	0	—	—	—	—	—	—	—	—
8	0	0	0	0	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—	X	0	0	X
10	—	—	—	—	—	—	—	—	0	0	X	0

equipment by their position on three-pin headers (with corresponding EXX marked on the Mother board). Refer to Figure 3.3 for locations.

JP37, located between J10 and J12, should be positioned to the left (pin 2 to 3) for standard operation. If a second IF Filter board is installed, the jumper should be to the right.

JP9 and JP10 (between J7 and J9) should be positioned left (pins 1 to 2). If the BFO board is installed, both jumpers should be moved to the right.

JP11, 12, 33 and 34 (between J15 and J17) should be positioned toward the rear (pins 1 to 2). If the Audio Interface board is installed in J17, the jumpers should be positioned forward.

JP35 and JP36 (between J15 and J17) should be positioned to the left (pins 1 to 2). If the Modem board is installed in J19 without the Audio Interface board in J17, the jumpers should be moved right.

When the High Stability Reference option is installed, JP1 is moved to the lower position on E1 of the Reference board (see Section 5 or 6).

If muting of the 600 ohm audio as well as the speaker audio is desired, JP1 is moved down on E1 of the Audio Squelch board (on both boards when ISB is installed). See Section 5 Audio Squelch board.

If the Audio Interface board is installed, all sections of S1 and S2 should be positioned down.

3.5 OPERATION

The receiver may be operated in manual mode or channel program mode. Automatic scan of frequency or of preprogrammed channels is possible. Remote control operation of nearly all front panel functions is also possible. See Table 3.2 for operating steps.

3.5.1 REMOTE CONTROL OPERATION

There is a wide variety of remote control configurations available with the MSR 5050A. The receiver can be controlled by the MSR 6420 Remote Control Unit (RCU) or by a computer. Allowable system configurations include multi-radio, single RCU, single radio, multi-RCU and also multi-radio, multi-RCU. Available communication modes are RS-232C, RS-423, RS-422, MIL-STD-188 (all standard) and 300 BAUD FSK Modem (optional). Optional "switched-audio" circuitry allows the audio lines of exciters, receivers and transceivers in a system to be all connected together on a single audio bus; RCU software then controls the audio link between any RCU-radio pair.

Each RCU or radio in a system is identified by its own address code. The address is used by the RCU operator to control or extract status information from one particular radio. The RCU operator selects an address and sends a command signal; the command reaches all radios in the system but is ignored by all except the radio with the selected address.

To verify or change receiver address:

a) Press E5 on receiver keypad. The present address will appear in the FREQ display.

b) If no change is required, press C to clear out of address entry mode.

c) To change address simply enter new address desired (single digit address must be preceded by a zero, as in 06).

d) Press E to enter the new address into receiver memory.

To put the receiver in the remote control mode, simply press the REM key on the front panel. While the receiver is controlled by the RCU, the front panel controls are non-functional. If the MSR 5050A is turned off or if AC power is momentarily lost, the receiver will return to the remote mode when power is restored. To return the receiver to local control, press the REM key a second time. The MSR 5050A may also be put into, or removed from, the remote mode by the RCU.

Please refer to the following sources for complete information regarding the various remote control

configurations available, as well as instructions for setting up the MSR 5050A for each configuration.

Table 1.3 - Basic explanation for available MSR 5050A remote control options and features.

Section 5 - Detailed explanation of remote control options and operation.

Table 3.1 -Baud Rate & Remote Mode Switches

MSR 6420 Technical Manual - Detailed description of MSR 6420 remote control unit. Interconnect wiring instructions included.

CSW 1000 Technical Manual - Detailed description of CSW 1000 software to allow control of radios with IBM compatible computer. Interconnect wiring instruction included.

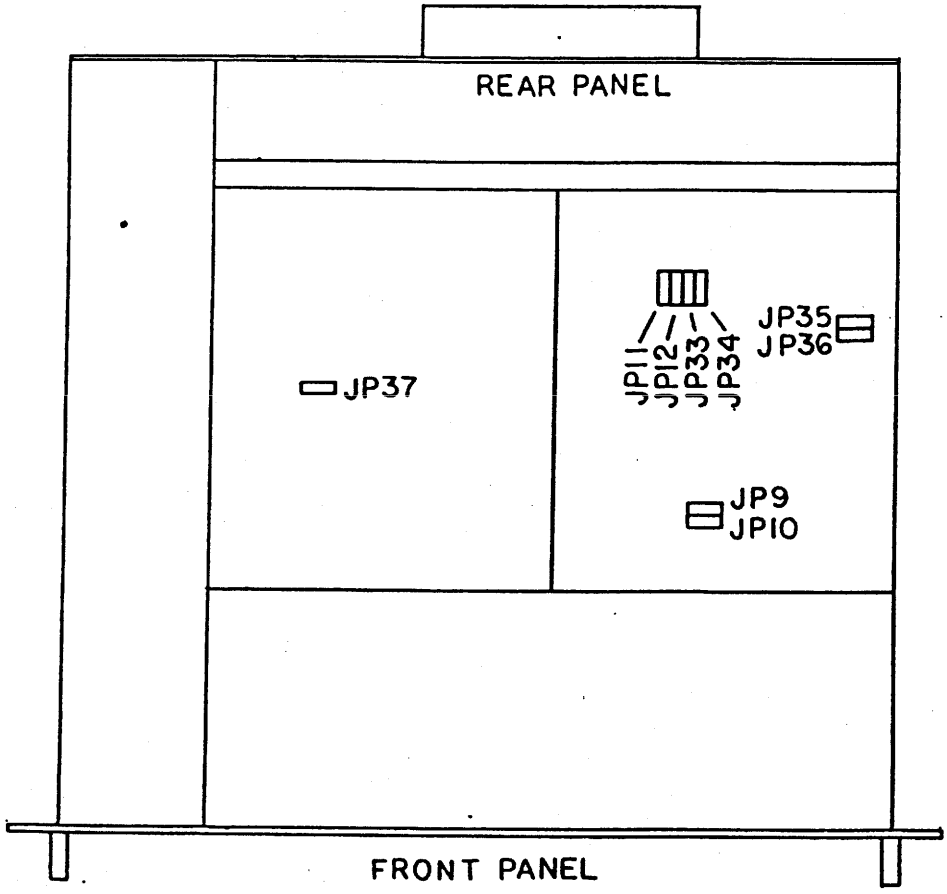


Figure 3.4

Mother Board Jumper Locations

Table 3.2 OPERATION PROCEDURES

TYPE OF OPERATION	STEPS
Manual Mode - used primarily to search for signals or to modify receiver characteristics to optimize reception. Controls may be operated freely without fear of affecting stored data. The only way to modify stored channel data is to press CHAN, XX and then E (enter).	1) Connect a 50Ω antenna to the ANTENNA connector. 2) Connect the headphones or switch speaker ON. Turn power switch to ON and advance VOLUME control approximately 1/3 rotation. 3) Turn RF GAIN control fully CW and push SQUELCH knob in. 4) Verify that the REMOTE key is off, dimmer control adjusted for desired brightness. **NOTE: If the REMOTE switch is pressed, the front panel keypad and control function will be "locked out" and in the remote control operating mode.** 5) Press the desired METER switch to display RF or audio signal level. 6) Press the TUNE RATE key to indicate the desired tuning steps. 7) Tune the receiver to the desired frequency by turning the TUNE knob, either clockwise or counterclockwise until the desired frequency is displayed on the front panel of the receiver. 8) Select the desired operating MODE, AGC decay rate, and Filter by pushing their respective switches. The bar-graph LED indicators will light as each switch is made. 9) The unit should now receive. The volume may be adjusted to a comfortable level. 10) The SQUELCH control may now be pulled out to mute the audio output from all signals except voice.

Table 3.2 OPERATION PROCEDURES (Cont.)

TYPE OF OPERATION	STEPS
Channel Program Mode	1) Press "CHAN". CHAN key lights. Display reads "---". 2) Enter channel (00 to 99). 3) Displays show data stored in that channel: Frequency, BFO, MODE, FILTER, AGC; and Receiver tunes to these conditions. 4) Succeeding channels may be recalled by successive channel number entries. **<OR>** 5) Press E to exit Channel Mode with the control settings of the last recalled channel. **<OR>** 6) Press C to exit Channel Mode with control settings of the last stored channel. **<OR>** 7) Program new data in the channel number recalled: in any order, modify any or all tuning settings, i.e.: a) Press "FREQ", FREQ key lights. b) Enter frequency numbers from keypad, starting with 10 x MHz, 1 x MHz, 100 x kHz, etc. up to the full 7 digits. Press E to complete frequency entry (FREQ key LED goes out). Less than 7 digit entry will fill in trailing zeros. First number entry will cause remaining frequency display to show "---"etc. Each succeeding number entry will displace a "---". **<OR>** Pressing "C" will "erase" the last entered number leaving a "---" in its place. Successive "C" presses will displace numbers; and the last erasure (10 x MHz) will exit the frequency entry mode, recalling the previous frequency. c) Press BFO key. Key lights, tune rate indicates 10 Hz. •Turn knob CW or CCW (+7.99 to -7.99 kHz) to desired offset (tune rate may be changed to 1 kHz to expedite). •Press "C" to exit BFO mode with last stored BFO offset. **<OR>** •Press "E" to exit BFO mode with new setting. d) Press Mode key until LED indicates desired Mode (some Modes are locked out if option not installed). e) Press Filter key until LED indicates desired filter (USB, LSB, ISB only allows MED filter; some filters locked out if options not installed). f) Press AGC key until LED indicates desired rate. g) Press "E" after all changes made. CHAN key light goes off. Changed data is stored in the indicated channel.

Table 3.2 OPERATION PROCEDURES (Cont.)

TYPE OF OPERATION	STEPS
Channel Scan Program (to change program)	1) Press SCAN PROG key. Key lights. Frequency display blanks except first digit "---". 2) Press block number. Display indicates last stored program for that block: block number (0-9), start channel (00-99), stop channel (00-99). 3) Press new start channel then new stop channel--display indicates selections. As last digit of stop channel is entered, the display blanks except for a "——" at the block number position and the block just entered is stored. 4) Successive blocks may be programmed in the same sequence. **<OR>** 5) Press E to exit scan program mode. Key light goes out. Displays return to previous condition.

Table 3.2 OPERATION PROCEDURES (Cont.)

TYPE OF OPERATION	STEPS
Channel Scan (If desired, select SIGNAL HOLD feature by moving JP1 on Interface board to left position.)	1) Press SCAN ON/OFF key. Key lights. Frequency display blanks except "———" in block number position. 2) Press desired block number (0-9). Display indicates block number, start channel, and stop channel. 3) Press successive block numbers to review programs in each block. **<OR>** 4) Press C to exit mode. **<OR>** 5) Press E to start scanning. 6) Press C to stop on a channel. 7) Press C to continue scan (unless held on channel by signal presence in the SIGNAL HOLD mode). 8) Press E to step to next channel (even if held by a signal) and continue scanning. 9) Engage SQUELCH (pull knob) to prevent SIGNAL HOLD caused by non-syllabic signals (i.e. CW). 10) Press SCAN ON/OFF any time after scan is started to exit mode.

Table 3.2 OPERATION PROCEDURES (Cont.)

TYPE OF OPERATION	STEPS
Frequency Scan (Interface board JP1 moved to left if SIGNAL HOLD function desired)	1) Press E, then 6. Channel display indicates "S -". SCAN ON/OFF key lights. 2) Press numbers on keypad for desired start frequency. 3) Press E. Trailing zeros will be added and indicated in frequency display. Channel display will indicate "SP". 4) Press numbers on keypad for desired stop frequency. 5) Press E. Trailing zeros will be added. Channel display will indicate "FS". Frequency display will indicate start frequency and radio will start scanning. 6) Press TUNING RATE key for desired frequency step size. Frequency display will scan in step sizes indicated. 7) SCAN RATE and SCAN DWELL adjustments are the same as for channel scan. 8) SCAN will stop on frequencies where signal is above threshold (approximately 2 UV). 9) SCAN will continue after scan DWELL time (unless in SCAN HOLD mode). 10) Pressing C will stop scanning. Channel display will indicate "PS". 11) Pressing C again will restart scan unless being held by a signal. 12) Pressing E will step frequency one tuning rate increment (even if held by a signal) and continue scanning. Frequency will revert to start frequency if the next frequency step exceeds the stop frequency. 13) Press SCAN ON/OFF to exit frequency scan mode.

SECTION 4

MAINTENANCE

4.1 GENERAL

This section provides information for routine maintenance, repair and evaluation of the overall performance of the receiver. Modular construction of the receiver lends itself to a logical and straightforward troubleshooting procedure. By referring to the overall and individual block diagrams, and using related level and frequency information, a trouble can be quickly localized to a particular assembly. Voltage and signal levels to all assemblies, except the rear panel A3, and front panel, A1, may be measured on the Mother board, A2, at the appropriate connector or signal point.

After establishing the existance of a trouble in a particular asembly, refer to the servicing information for that assembly located elsewhere in this section of the manual.

Figure 4.4-1 locates the component assemblies in the receiver. Pin outs are located in Sections 4.8 through 4.19 for each assembly.

4.2 PC BOARD REPAIRS

4.2.1 REMOVAL AND REINSTALLATION

Care should be used when removing PC boards from the receiver. The card extractor, P/N 600268-618-001, should be used if possible. If no card extractor is available, a temporary substitute can be made from a length of solid heavy gauge wire (#10-#12). Form a hook at each end of the wire, and then insert each hook into the holes provided at the top outer edge of each PC board. Apply gentle upward pressure near each hook to free the board(s) from their edge connectors.

NOTE: Do not use pliers or screwdrivers to remove the boards.

When replacing boards into the PC sockets, insure that the board is in its proper position in the card guides at each board edge. Apply light downward pressure to the top edge of the board until it is fully seated into the edge connector.

4.2.2 SOLDERING

To avoid damaging the PC boards during the replacement of components, extreme care should be used in soldering and component removal. A low wattage soldering iron (25-50 watts) with a narrow tip should be used.

A low wattage iron is necessary to prevent the application of excesssive heat to the copper foil of the PC board. Excessive heat may cause the foil to separate from the board, rendering the board unrepairable. Only a high quality electronic grade rosin solder should be used in making repairs.

CAUTION

Do not use an acid core solder.

Due to the circuit density on the boards, solder "bridges" or short circuits between adjacent foil runs are possible, if care is not used during soldering operations. After soldering is completed, the area around the connection should be closely inspected for excess solder or "bridges" between adjacent runs or connections. Any "bridges" or excess solder between connections must be removed before reinstalling the board. Because of the double sided construction used on the PC boards, a component lead may be soldered to printed circuit areas on top and bottom of the board. Consequently, when a component lead is removed, the replacement component should be resoldered top and bottom as applicable.

4.2.3 CMOS DEVICE HANDLING PRECAUTIONS

CMOS devices may be damaged by static voltages, and therefore the following is recommended:

- All MOS devices should be placed on a grounded work bench surface, and the repair operator should be grounded prior to handling MOS devices, since a person can be statically charged with respect to the work bench surface.

- Nylon clothing should not be worn while handling MOS circuit or devices.

- Do not insert or remove MOS devices from the sockets while power is applied.

- When soldering MOS devices, be sure the soldering iron used is a grounded type.

4.3 LOGIC INTERPRETATION

Several types of digital devices are used in the receiver. The following descriptions are presented to explain their basic operation and symbolic notation. The digital devices used (gates, flip-flops, inverters, etc.) are binary in nature; that is, the output voltage of each can only be in two permissible states. The two possible states are called logic "1" and logic "0". The assignment of voltage levels to these states is arbitrary. However, in this manual positive logic is standardized, which means we define the logic states as shown in Table 4.3-1.

Table 4.3-1 LOGIC STATES

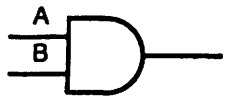
	TTL	CMOS
Logic 1: Normally greater than Logic 0: Normally less than	2.0 Volts 0.8 Volts	3.5 Volts 1.5 Volts

4.3.1 GATES

A gate is a circuit element whose output level depends upon the levels of all of its inputs in a particular pattern.

The AND gate can have two or more inputs, the level of its output is dependent on the state of all input levels. It can be seen from the truth table for the AND gate if any input is 0, the output will be 0. For the output to be 1, all inputs must be 1.

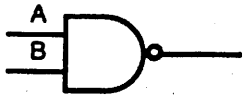
AND GATE



INPUTS A	B	OUTPUTS
0	0	0
1	0	0
0	1	0
1	1	1

The outputs of the NAND gate are the opposite of the AND gate. If any input is 0, the output will be 1.

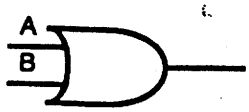
NAND GATE



INPUTS A	B	OUTPUTS
0	0	1
1	0	1
0	1	1
1	1	0

The output of the OR gate is 1 if any input is 1.

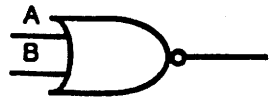
OR GATE



INPUTS A	B	OUTPUTS
0	0	0
1	0	1
0	1	1
1	1	1

The output of the NOR gate is the opposite of the OR gate. The output is 0 if any input is 1.

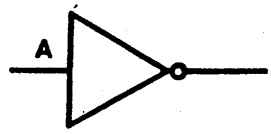
NOR GATE



INPUTS A	B	OUTPUTS
0	0	1
1	0	0
0	1	0
1	1	0

4.3.2 INVERTER

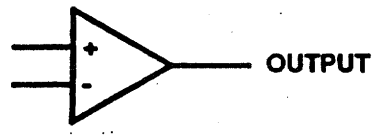
The inverter has a single input. The output level is the opposite of the input level.



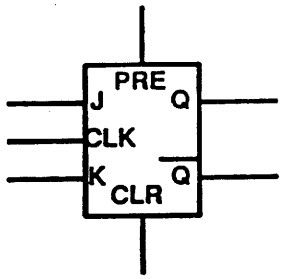
INPUT	OUTPUT
0	1
1	0

4.3.3 VOLTAGE COMPARATOR

The voltage comparator has two inputs, V + and V -. The V + input is normally connected to a fixed or reference voltage. As the V - input becomes more positive and exceeds the V + input level, the output switches low. If the V - input voltage becomes less positive than the V+ reference input, the output switches to a high level once again.



4.3.4 J-K FLIP-FLOP



The flip-flop is a memory device that stores a logic state. The above symbol is that of a J-K flip-flop. The state of which is referred to by the level of the Q output. If, for example, the Q output is high, the FF (flip-flop) contains a 1. The $\overline{Q}$ (Q NOT) output is always the opposite of the Q output. The state of the FF can be changed in two ways. It can be changed by means of the clock input, or by the PRESET and CLEAR inputs. The effect of an applied clock pulse on the state of a FF depends upon the J and K inputs. The J input must be high for a clock pulse to cause a 1 output. The K input must be high for a clock pulse to cause a 0 output. If both J and K inputs are high, the FF toggles (changes state) on each applied clock pulse.

The PRESET and CLEAR inputs operate independently of the clock. A high level input to the PRESET line drives the FF to a level 1, while a high input to the CLEAR line drives the FF to a level 0. Some circuits PRESET or CLEAR with a low level input instead of a high level. This is indicated by a "circle" at the appropriate input terminal.

4.3.5 MICROPROCESSOR

The microprocessor is basically a small computer contained within an integrated circuit. This is a device that can store, retrieve, and process data. They are manufactured in many different configurations. The microprocessor used in this receiver contains an 8 bit central processor unit, a 64 byte on chip RAM, 27 input/output lines, and an internal clock. It is configured in a 40 pin dual in line package.

4.3.6 INPUT/OUTPUT PORT (8 BIT LATCH)

The input/output port is an interface device for use with a microprocessor. It contains, within one package, a large number of gates, buffers, and flip-flops. They are manufactured in many different configurations. The in/out port used in this receiver is configured in a 24 pin dual in line package.

4.3.7 RAM

Random access memories are logic elements that can be reprogrammed over again many times, and the information stored, can be retrieved by utilizing read/write, and address inputs. A 2k bit CMOS zero power RAM is used in the receiver memory system. It is configured in a 24 pin dual in line package.

4.3.8 INPUT/OUTPUT EXPANDER

The input/output expander is an interface device for use with a microprocessor. The function of which is to increase the permissible number of inputs and outputs to the microprocessor. It contains, within one package, a large number of buffers, latches, decoders, and other logic circuitry. I/O expanders are used in the Logic board and Mother board. They are configured in 24 pin dual in line packages.

4.3.9 EPROM

Eproms are electrically programmable, ultraviolet light erasable data storage devices which control the microprocessor. Two 24-pin 8k bit devices are used in the receiver Logic board.

4.3.10 PRIORITY INTERRUPT

This 24-pin device assigns priority to eight interrupt inputs to control the interrupt to the microprocessor.

4.3.11 TRISTATE BUFFER

A tristate buffer has the normal TTL high and low states plus a controllable off (or open circuit) state which allows bidirectional operation.

4.3.12 PROGRAMMABLE KEYBOARD/ DISPLAY INTERFACE

This 40-pin IC operates with the microprocessor to interface keyboard inputs (up to 8 x 8 matrix) and 16 7-segment displays.

4.4 ASSEMBLY AND SUBASSEMBLY IDENTIFICATION

Table 4.4-1 and Figure 4.4-1 lists and identifies the assemblies and modules used in the receiver. Figure 4.7-1 is an interconnection/wiring diagram for the receiver. Schematics for each assembly and module, parts lists and circuit descriptions are contained in this section of the manual.

Most signal path and synthesizer boards described here are also in the MSR 8000 and MSR 8050 transceiver and MSR 6700 exciter and are fully interchangeable. In addition, the MSR 5050A minor loop (with 10 Hz resolution) is interchangeable with the MSR 8000 minor loop (100 Hz resolution). The resulting resolution is limited by the type board used or the unit's controls.

The MSR 5050A Reference board has the added capability of either outputting the 5 MHz reference signal or accepting an external signal as determined by a TTL control signal.

4.5 COVER REMOVAL

The top cover is removed by two quarter turn fasteners. The top inner cover can be removed by removing the eight mounting screws that secure the inner cover to the chassis. See Figure 4.5-1.

The bottom cover is held by 10 screws to the chassis, rear panel and front panel.

4.6 RECEIVER ALIGNMENT AND ADJUSTMENT

All modules and assemblies of the receiver are of high reliability, solid state design. Adjustments and alignments are seldom, if ever, required. If a module or component replacement or performance indicates the need for adjustment or alignment, the following tables and procedures are provided.

4.6.1 PRELIMINARY ADJUSTMENTS

Before performing adjustments on the receiver:

a) Check proper line voltage and fuse. Check desired internal jumper/control settings per section 3.4.

b) Connect an RF signal generator (HP 8640B or equal) to the antenna connector of the receiver, A3J46.

c) Set the generator frequency and output as listed in Table 4.6-2. See Figure 4.6-1 for the locations of the modules and adjustments.

d) Audio output may be measured by an audio voltmeter (HP 400LR or equal) connected to the rear panel 600 ohm receiver output A3J42, pins 24 and 23. See Figure 2.1.

e) To make some of the adjustments on the assemblies, it is necessary to use an extender card (optional equipment, P/N 601198-536-001).

Table 4.4-1 RECEIVER ASSEMBLIES

DESIGNATOR ASSEMBLY/SUBASSEMBLY	DESCRIPTION	PART NUMBER
MSR 5050A	Receiver, Grey	790025-000-001
	Receiver, O.D.	790025-000-002
A1	Front Panel Assembly	700002-539-001
A1A1	Keypad/Display Board	700001-536-001
A2	Mother Board Assembly	700006-536-001
A3	Rear Panel Assembly	700201-539-001
A3A1	Power Supply Assembly	600423-705-001
A3A1A1	Power Supply Board	601213-536-001
A4	Interface Board	700002-536-001
A5	Logic Board	700003-536-002
A5U4	Programmed IC	700001-412-001
A5U15	Programmed IC	700001-412-002
A6	Low Pass Filter Board	601217-536-001
A7	High Pass Filter Board	601086-536-003
A8	High Level Mixer Board	601258-536-002
A9 (STD)	IF Filter Board #1	601076-536-010
A9 (FILT. OPT)	IF Filter Board #1 (Part of Filter Option 700411-700-001)	601076-536-013
A10 (ISB OPT A)	IF Filter Board #2 (Part of ISB Option A 700014-700-001)	601076-536-011
A10 (FILT. OPT)	IF Filter Board #2 (Part of Filter Option 700411-700-001)	601076-536-019
A11 (STD)	Audio Squelch Board #1	601077-536-005
A12 (ISB OPT A, B)	Audio Squelch Board #2 (Part of ISB Option A or B 700014-700-001, 002)	601077-536-005
A13	Speaker Amplifier Board	601311-536-001
A14 (OPT)	Tone Key/Modem Board (Part of Remote FSK Option 700015-700-001)	602025-536-002
A15 (OPT)	Audio Interface Board (Part of Addressable Audio I/O Option 700015-700-002)	700014-536-001
A16	Major Loop Board	601081-536-001
A17	Translator Loop Board	601083-536-001
A18	Minor Loop Board	601214-536-001
A19	Reference Board	601080-536-003
A20 (OPT)	BFO Board (Part of BFO Option 600107-700-001)	601215-536-001
A21 (OPT)	OCXO Assembly (Part of High Stability Reference Option 700402-700-001)	600173-378-001
A22 (OPT)	BCD Interface Board (Part of BCD Interface Kit 700022-700-001)	602021-536-002

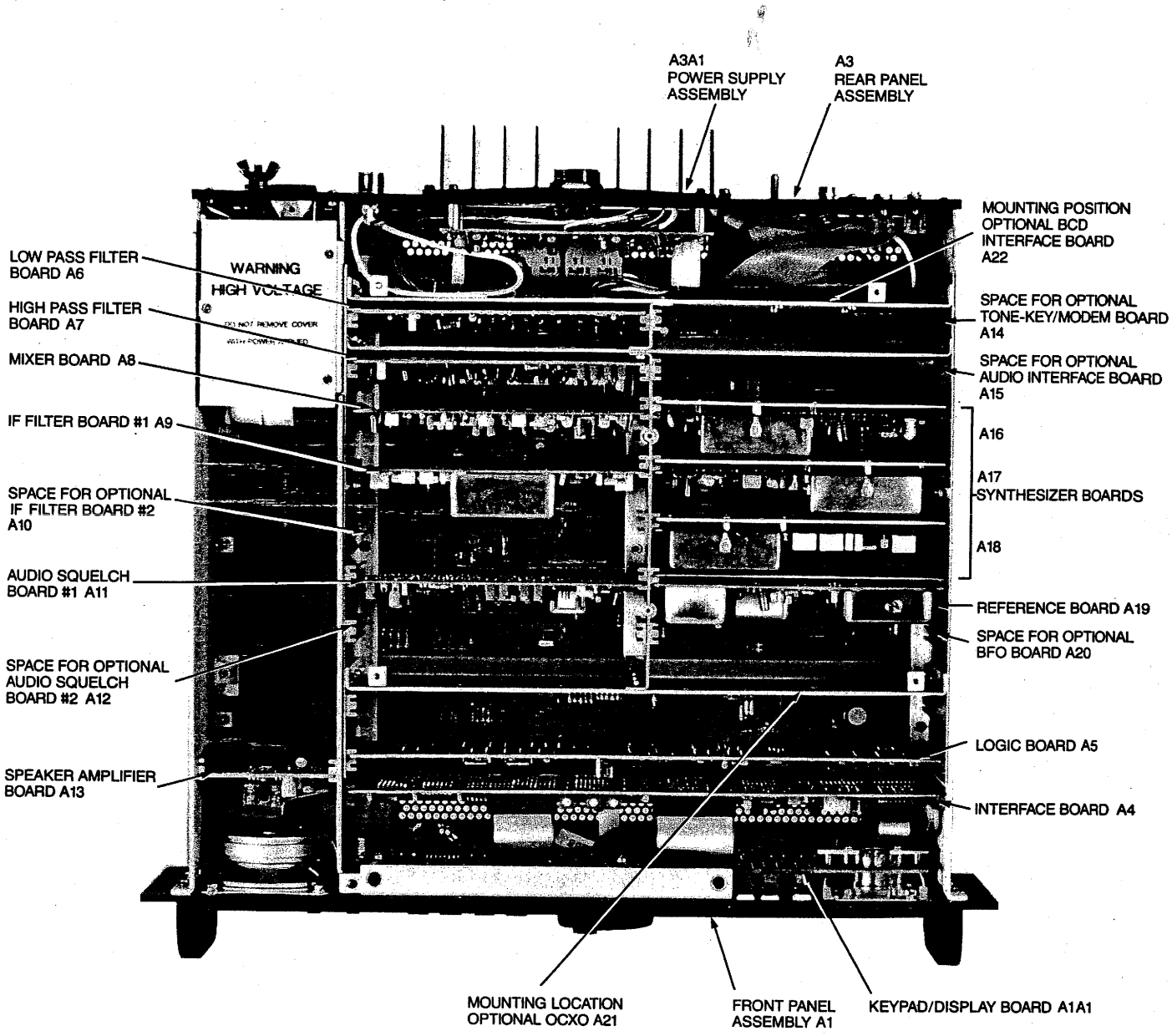


Figure 4.4-1

Major Assemblies

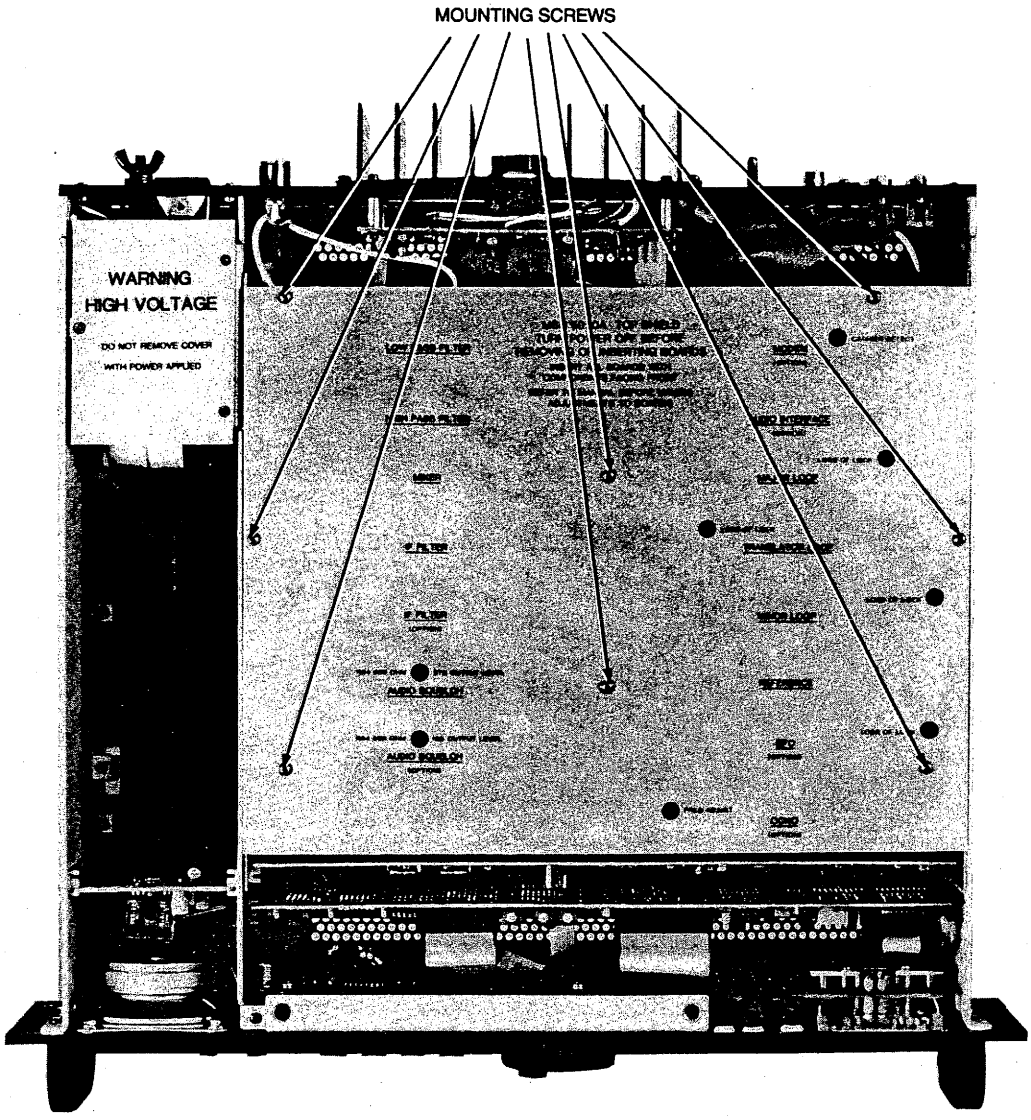


Figure 4.5-1

Top Shield Mounting

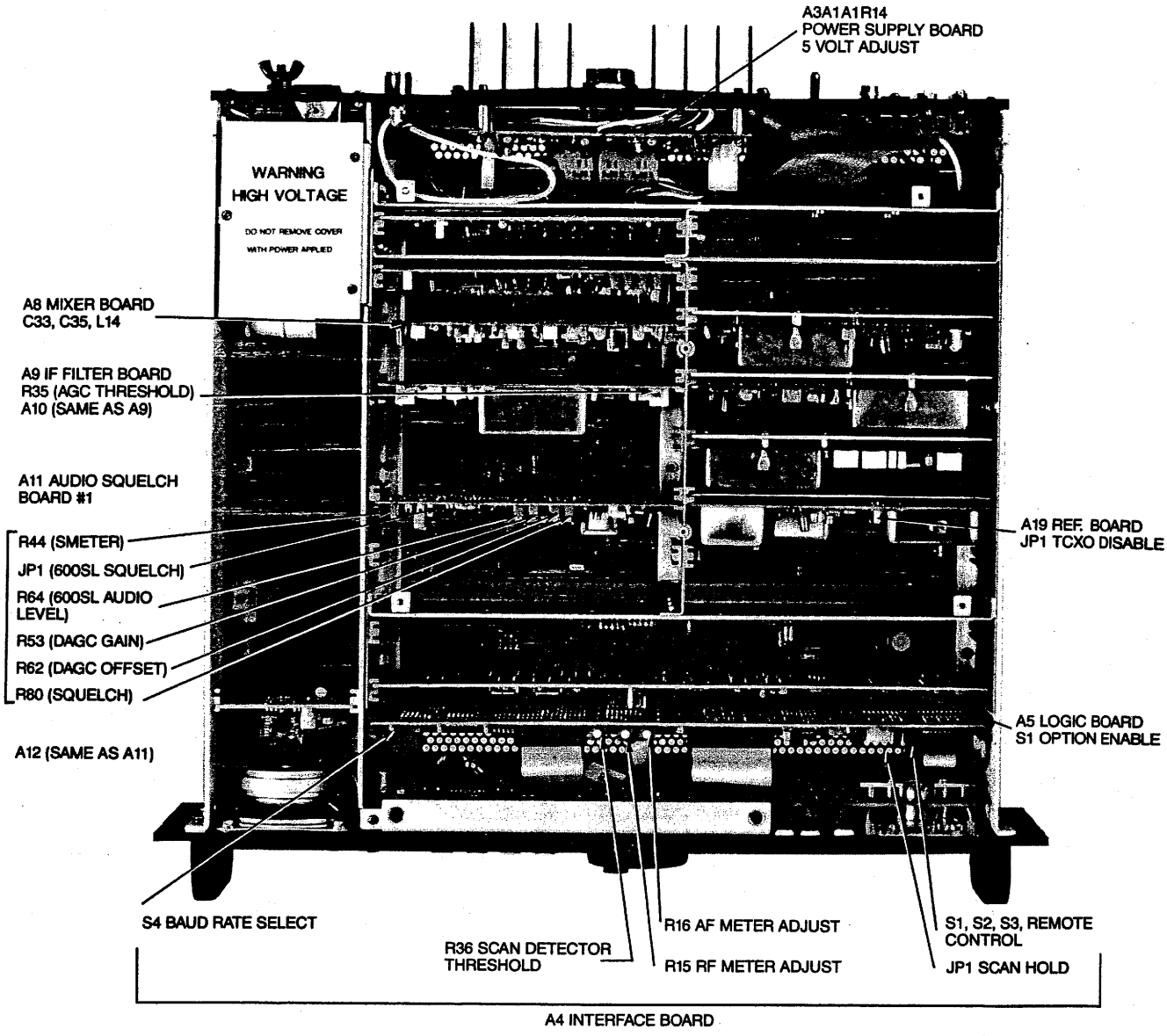


Figure 4.6-1

Adjustment Locations

Table 4.6-1 RECOMMENDED TEST EQUIPMENT

ITEM	REPRESENTATIVE TYPE
2 each, Signal Generators	HP 8640B or equal
Audio Meter and Distortion Analyzer	HP 334A or equal
Frequency Counter	Accurate to 0.1 PPM at 30 MHz
Audio Generators	HP 200CD or equal
Digital Voltmeter	HP 3466A or equal
Spectrum Analyzer	HP 141T with 8553 B and 8556A RF sections
RF Voltmeter	Model 92C Voltmeter with 50 ohm adaptor
RF Combiner	Merrimac PD-20-10-M2
Power Meter and Load	GR1840 or equal
Oscilloscope	Tektronix 475 or equal
Extender Cards	6.5" wide, 2 each (P/N 601198-536-001)
Signal Input/Output Monitor Fixture	Connections to A3J42

Table 4.6-2 RECEIVER ADJUSTMENTS

ASSEMBLY	ADJUSTMENTS AND PERFORMANCE
A3A1 Power Supply Assembly	1) R18 (5 Volt Adj.): Measure dc voltage at rear panel J42-6. Adjust for 5.1 VDC.
A8 Mixer Board (Put on extender for adjustment)	1) C35, C33, L14 (VHF IF Adj.): Frequency to 11.6 MHz, mode to USB. Apply 0.5 µV RF, adjust for maximum audio output (Adjustments only required after board repair. All adjustments preset at board test.)
A9 IF Filter Board	1) JP2, JP3 (IF Gain): Position on E2-1,2 and E3-1,2 (away from board edge). 2) JP1 (TX ISB): Positioned down (on terminal 2 and 3) - transmit function only. 3) L20 (IF Bandpass tuning): Frequency to 11.6 MHz, USB. Apply 0.5 µV RF; adjust for maximum audio output. 4) R35 (IF Gain): Increase RF input to 7µV (-90 dBm). Adjust for 1.0 ±.2 v dBc at Audio Squelch board TP2 (or for a barely perceptable RF meter movement). 5) R7 (TX Gain): TX function only; no effect on receive.
A11 Audio Squelch Board	POWER OFF. 1) R44 (S Meter): Adjust for 2k ohms from TP2 to R44 terminal 3 (top terminal). 2) R80 (squelch): Adjust for 2.7k ohms from E3 to ground. 3) R53 (DAGC Gain): Adjust for 100 ohms from R53 pin 3 (top terminal) to ground. POWER ON. 4) R52 (DAGC Offset): Adjust for 4.0 VDC at R52 pin 2 (center terminal). Radio to 11.6 MHz, USB. Generator to 11.6 MHz and 13 dBm. 5) Vary generator frequency ±5 kHz monitoring speaker audio for oscillation. If oscillation is present, adjust R53 CCW until stable.

Table 4.6-2 RECEIVER ADJUSTMENTS (Cont.)

ASSEMBLY	ADJUSTMENTS AND PERFORMANCE
	6) Generator frequency to produce 1 kHz audio. Vary generator level from +13 dBm to -90 dBm. Audio level should change less than 3 dB. Adjust R53 CW if necessary. 7) R64 (600 ohm audio): Generator to 50 µV (-73 dBm). Adjust R64 for 0 dBm audio out into 600 ohms (J42 pin 23, 24). 8) JP1 (600 ohm MUTE): Normal position on E1 pin 1, 2 (top of board) does not allow muting or squelch of 600 ohm audio. Move to pins 2, 3 if desired.
A4 Interface Board	1) R16 (AF Meter): Generator still 50 µV (-73 dBm) 11.6 MHz, 600 ohm audio still 0 dBm. Front panel meter switched to audio. Adjust Interface board R16 for 0 dBm on front panel meter. 2) R15 (RF Meter): Generator level to -7 dBm (100 µV). Front panel meter switch to RF. Adjust R15 for full scale meter indication. 3) R36 (Scan Threshold): Front panel squelch knob pushed in (squelch off). Generator to 2 µV. Monitor scan detect output at rear panel J42-19 for DC TTL levels. Press front panel keys E, 6 (frequency scan). Press E (start frequency 11.6 MHz). Press E (stop frequency 11.6 MHz). Adjust R36 to point where scan detect output just goes low.

4.7 TROUBLESHOOTING

Troubleshooting the radio is accomplished by associating the symptom to one or more modules. Since the majority of the radio consists of easily replaced plug-in modules, the trouble may be narrowed to a single module by substitution of good modules.

Table 4.7-1 lists suspected modules with symptoms of malfunctions. Figure 4.7-1 shows the module interconnections.

Troubleshooting within the module may be attempted with the aid of schematics, pinouts, assembly layouts and circuit descriptions in the following sections of the manual for each module.

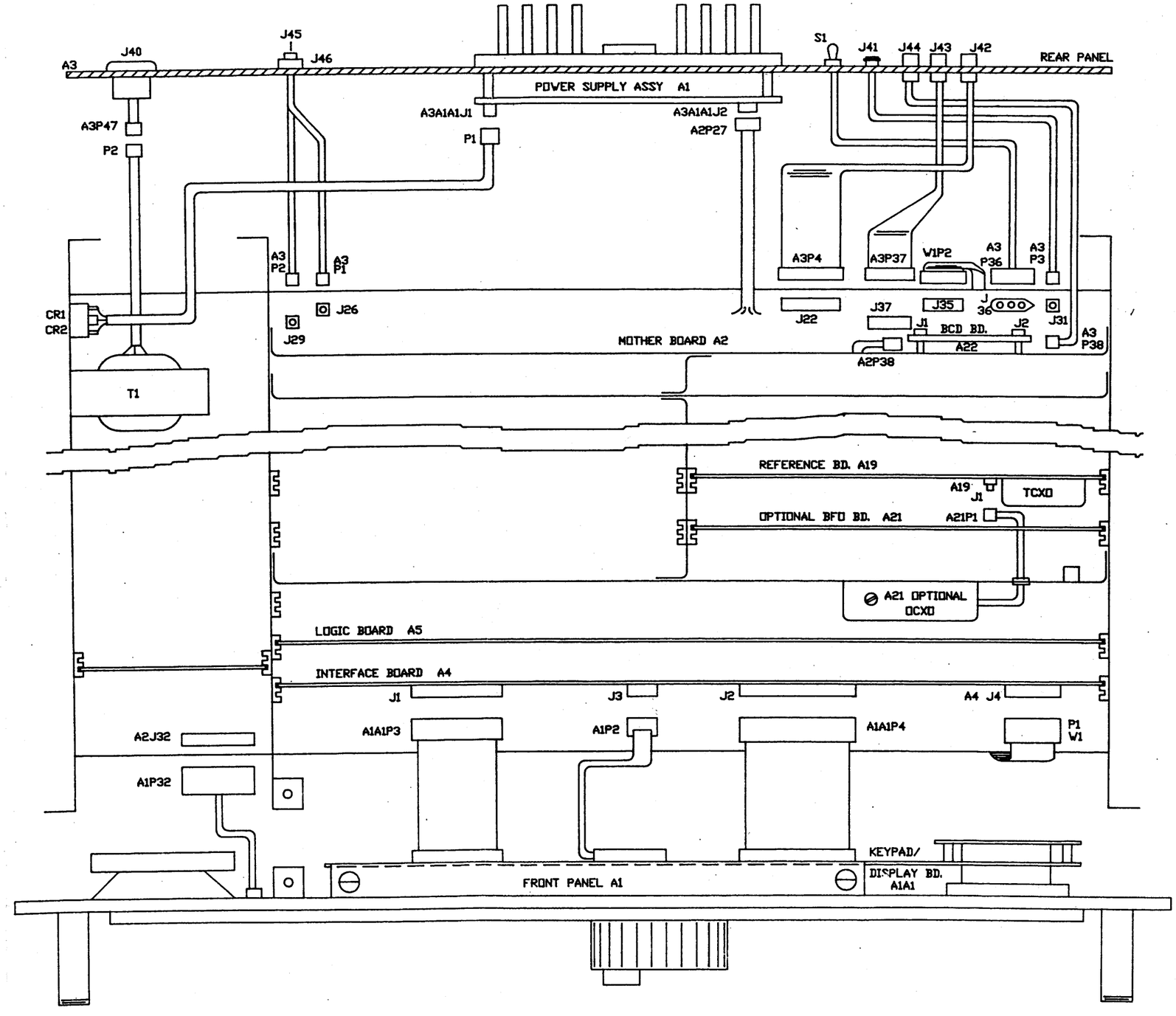


Figure 4.7-1

Receiver Interconnection Diagram

Table 4.7-1 TROUBLESHOOTING CHART

	SYMPTOM	CAUSES
1	Receiver inoperative, Display and Key Lights not lit. Power Supply LED's not lit.	1) AC line cord defective or not connected. 2) Fuse blown. 3) Transformer T1 or Rectifiers CR1 and CR2 defective. 4) Connectors A2P27 or P1 not plugged into Power Supply A3A1A1. 5) Front Panel Cable Connector A1P32 not plugged into mother board. 6) Defective Front Panel Volume Control Power Switch A1S2. 7) Defective Power Supply Assembly A3A1.
2	No Audio or Background Noise at Speaker or Phone Jack. Meter indicates RF Signal present.	1) Speaker switch off or defective. 2) Volume control at "Min" position or defective. 3) Squelch control pulled out. 4) Defective Cable A1P32. 5) Defective Speaker Amplifier board A13. 6) Defective Audio Squelch board A11, A12. 7) Defective Interface board A4. 8) Ground on Mother board "LL" trace or $\overline{\text{Mute}}$ Line or Rear Panel Connection A3J42, pin 20.
3	Same but Meter may or may not indicate. One of the Synthesizer "Loss of Lock" lights indicating.	1) Defective Synthesizer board A16, A17, A18, A19 or optional A20. (Remove top cover and locate defective board by illuminated loss-lock LED.)
4	AM Mode normal; other Modes inoperative. (Check AM-Wide and AM-Medium.)	1) 3rd LO injection absent at Audio Squelch board. a. Mother board jumpers JP9 or 10 incorrectly placed. b. Defective Reference board A19 (or option BFO board A20). 2) Defective Logic board. 3) Defective Interface board. 4) Defective Q8 circuit on Mother board.
5	Distorted Audio at Speaker.	1) Defective Speaker Amplifier board A13. 2) Defective Audio Squelch board A11, A12. 3) Defective Interface board A4. 4) Incorrect setting of RF gain.
6	Receiver signals weak in all Modes. "S" Meter indicates low.	1) Defective High Pass Filter board. 2) Defective Low Pass Filter board. 3) Defective Mixer board. 4) Defective IF Filter board. 5) Defective Rear Panel Cable A3P4 to Mother board. 6) Defective Mother board buffer amplifier A2Q4, A2Q5. 7) Defective Audio Squelch board.

Table 4.7-1 TROUBLESHOOTING CHART (Cont.)

	SYMPTOM	CAUSES
		8) Defective Logic board (band A, B, C code incorrect). 9) Defective Interface board (band 1 - 8 signals incorrect). 10) RF Gain pot incorrectly adjusted.
7	Received signals weak in some but not all Bands.	1) Defective Low Pass Filter board. 2) Defective High Pass Filter board. 3) Defective Logic board. 4) Defective Interface board.
8	"Bite 02" appears in Frequency Display.	1) Press "C". If displays return to normal, fault was a momentary loss of 9 volts or 13 volts. 2) If "bite 02" reappears: a. Defective Power Supply A3A1. (Amber LEDs indicate status of 5, 9 and 13 volt regulators.) b. Short circuit or excessive load on 9 or 13 volt bus. c. Short circuit on "PS BITE" line on Mother board to Logic board A5, J4 pin 13.
9	"Bite 01" appears in Frequency Display.	1) Same as Symptom 3.
10	Front Panel Displays and Switch LEDs dim or not lit.	1) Keypad/Display board defective (5 volt DIM circuit).
11	Inoperative Meter/Switches.	1) Keypad/Display board defective. 2) Interface board defective.
12	Operation of Displays and Switches not correct.	1) Keypad/Display board. 2) Interface board. 3) Logic board.
13	No response from Front Panel Switches. (Check that Remote Switch is not lit.)	1) Keypad/Display board. 2) Interface board. 3) Logic board. (Check for /INT signal at U1-6.)

4.8 FRONT PANEL ASSEMBLY, 1A1

The front panel assembly contains the controls and indicators for operating the receiver. Mounted to the front panel are the Keypad/Display board (A1A1), Keypad assembly (S4), speaker (LS1), speaker switch (S1), phone jack (J1), volume control (R2), RF gain control (R3), dimmer control (R5) and opticoupler tuning assembly (A1A2). Power on/off is controlled by a switch (S2) on the volume control activated at the CCW detent. Squelch is activated by a push-pull switch (S3) on R3. Clearance holes in the panel allow screwdriver adjustment of R14 (scan rate) and R15 (scan dwell) on the Keypad/Display board.

The front panel is detached from the receiver by seven screws (two each at left, right and bottom; and one at the top side) and four ribbon cable connectors. Three cables connect to the Interface board (A1A1P3, A1A1P4, A1P2) and one to the Mother board (A1P32). Refer to Figure 4.8-1 front panel schematic for electrical interconnections.

4.8.1 DISPLAY/KEYPAD BOARD, A1A1

4.8.1.1 General Description

This board contains a 4 x 4 keypad and 14 push-button switches for data and command entering. There are four 4-digit, 7-segment display chips to display channel, frequency and BFO; and three 10-segment bar graphs for MODE, FILTER and AGC indication. In addition, a dimmer circuit, scan delay pot, scan rate pot and a meter are included.

4.8.1.2 Keypad Scanning

A 3-bit encoded scan signal, SL0, SL1 and SL2 on J1-24, 26 and 25 are applied to the three to eight decoder U1. Lower four bits of U1 are used as four scan lines for the key matrix. Eight return lines of the matrix, RL0 through RL7, are connected to J1-20, 18, 16, 14, 11, 9, 7 and 5. When a key is pressed, one of the return lines will go low and the keypad chip on the Interface board will convert it into a key code and transfer to the microprocessor chip.

4.8.1.3 Input/Output Expander

U9 is a 8243 I/O expander chip directly tied to the microprocessor through J2-18, 20, 22, 24 and 28. Port 5 of this chip (U9-1, 23, 22 and 21) is used for 7-segment display control. P50 and P51 (U9-1, and 23) are connected to the input of U2, a 2- to 4-decoder 74LS139, to select one of four displays U5, U6, U7 and U8 while P52 is used as clock input and P53 for data input to these chips in parallel. Port 4 (U9-2, 3, 4 and 5) is used to drive the tune rate indicator DS4, DS3, DS2 and DS1 respectively. Port 6 (U9-20, 19, 18 and 17) and Port 7 (U9-13, 14, 15 and 16) are used to control lights in CHAN, FREQ, SCAN ON/OFF, SCPG, AF2, AF1, RF and AF pushbutton switches respectively.

4.8.1.4 7-Segment Display Chip

U5-U8 are 4-digit serial controlled, 7-segment displays chip with built-in driver. Display information is applied to the data input pin (pin 4 of the chip) in serial and is latched by the clock signal in pin 5 when /en pin (pin 3) is low. Data received is latched and shown in the display until chip is selected and data is clocked in again.

4.8.1.5 Bar Graph Display

AGC signal is applied to the bar graph display chip U3-16, 17, 18 and 19 through J2-27, 25, 23 and 29. When the signal goes low, the corresponding bar will be turned on. BG1 and BG2 are connected to the output of decoder chip U3 and U4 (74LS145). Input of U3 (U3-15, 14 and 13) is tied to J1-15, 14 and 13 which is a 3-bit encoded MODE input signal (MODE A, B and C) while input of U4 is connected to J1-23, 21 and 19, which is a 3-bit encoded FILTER input (FL A, B and C). Mode and filter codes are defined in the following table.

Mode and Filter Codes

A	0	1	0	1	0	1	0
B	0	0	1	1	0	0	1
C	0	0	0	0	1	1	1
MODE	CW	USB	LSB	ISB	AM	N/A	FSK
FILTER	VWIDE	WIDE	MED	NAR	VNAR	N/A	N/A

4.8.1.6 Dimmer and Others

Q1 is used to control the DIM +5V supply which is connected to all displays and LEDs. Control voltage is obtained from the dimmer pot in the front panel. The wiper of this pot is tied to J6-2 which goes through a current limiting resistor, R16, to the base of Q1. The GND side of this pot is tied to J6-4 which connects to GND through a 470 ohm resistor R23.

DC voltage on J1-12 is connected to the meter M for AF and RF meter indication. DS0 and DS9 will light the meter as long as main power is on.

Pots R14 and R15 are connected to the Scan Oscillator and the Delay Oscillator on the Interface board through J2-28 and J2-26, respectively, to control the rate of these oscillators.

Front Panel (700002-539-001)

PART NUMBER	DESCRIPTION	SYMBOL
700001-536-001	KEYPAD BD, 5050A	A1
700003-360-001	POT. 500, DIMMER	A2
600079-611-002	PHONE JACK	J1
600008-370-001	SPEAKER	LS1
647004-341-075	RES. 470, 1/4W, 5%	R1
600109-360-002	POT/SWITCH, 10K, AUDIO TAPER	R2/S2
600110-360-001	POT/SWITCH, 10K, LINEAR TAPER	R3/S3
610014-341-075	RES. 1K, 1/4W, 5%	R4
600111-360-001	POT. 500, DIMMER	R5
600213-616-001	SWITCH,SPKR	S1
700001-616-001	KEYPAD	S4

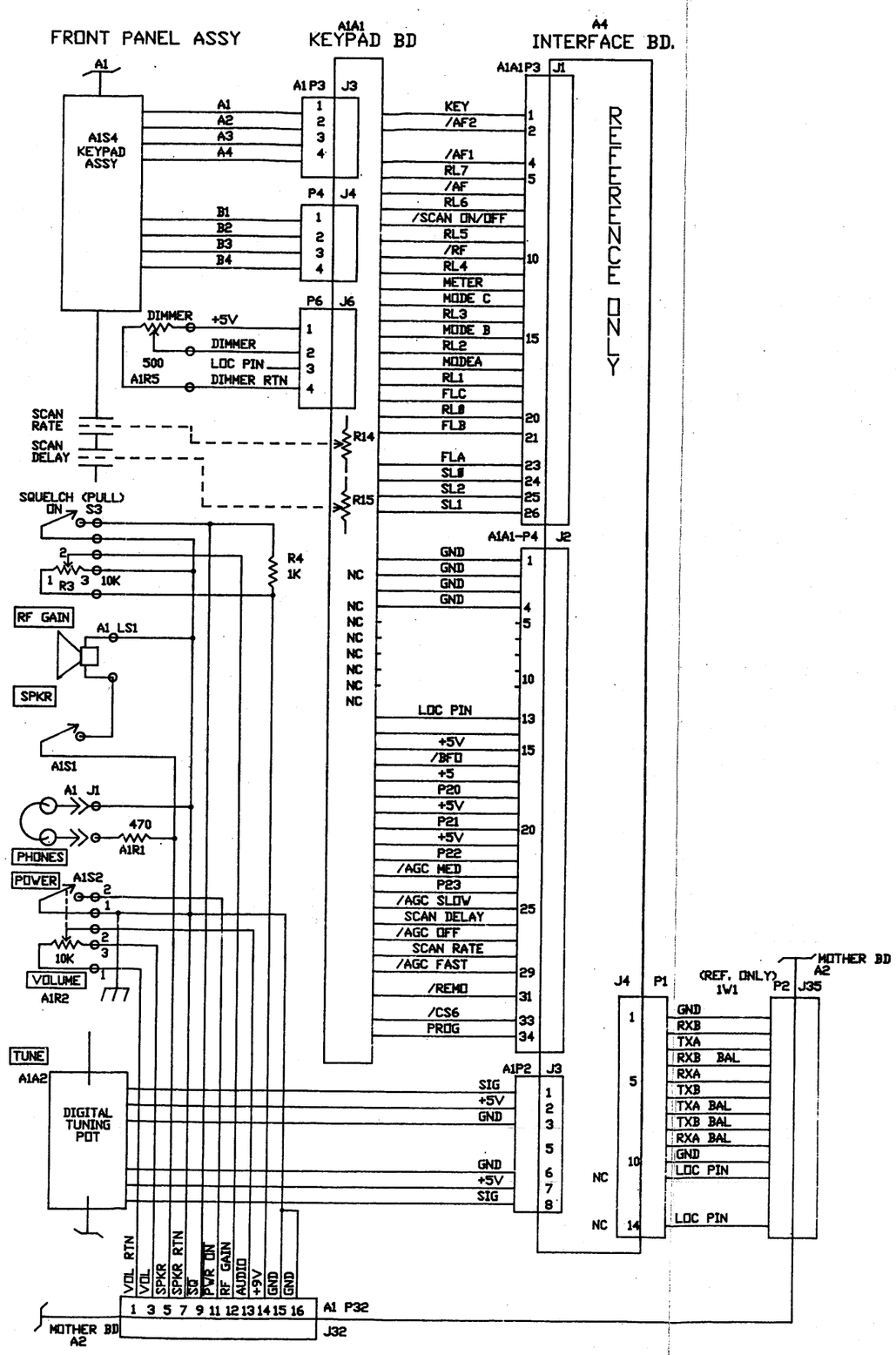


Figure 4.8-1

Front Panel Schematic

Keypad (700001-536-001)

PART NUMBER	DESCRIPTION	SYMBOL
700009-390-001	DIFFUSER LAMP	BG1-3
700001-390-001	BAR GRAPH, HDSP4830	C1-4,11,
600302-314-013	CAP. .1UF, MYLAR, 50V	13,15
600297-314-040	CAP. 2200UF, ALUM, 16V	C10
600297-314-025	CAP. 47UF, ALUM, 25V	C12,14
600302-314-001	CAP. .001UF, MYLAR, 63V	C5-8
600259-314-108	CAP. 1000UF, ALUM, 16V	C9
700010-390-001	LED, RED	DS0,9
700007-390-001	LED, 1.00 LG	DS1-4
600423-608-106	CONN. RT/AN HEADER, 6 PIN	J3,4
600423-608-104	CONN. RT/AN HEADER, 4 PIN	J6
600034-368-003	METER 0-1 MA	M1
600220-413-001	TRANSISTOR MJE520	Q1
647014-341-075	RES. 4.7K, 1/4W, 5%	R1-4
620004-341-075	RES. 200, 1/4W, 5%	R11-13
612004-341-075	RES. 120, 1/4W, 5%	R16
615084-341-325	RES. 1.5, 1W, 5%	R17
647004-341-075	RES. 470, 1/4W, 5%	R23
600072-360-014	POT. 100K, 1/2W, CERMET, TOP	R5-10,12 14,15
613004-341-075	RES. 130, 1/4W, 5%	R5-10,18, 19,22
600365-616-002	SWITCH, PUSH-BUTTON, LIT	S04,05, 34,15-16, 35
600366-616-002	SWITCH, PUSH-BUTTON, NON-LIT	S06,07, 14,17
600365-616-002	SWITCH, PUSH-BUTTON, LIT	S24-27
600309-415-001	IC 74LS138, 3 TO 8 LN DEC/MUX	U1
600397-415-001	IC 74LS139, 1 OF 4 DCDR	U2
600528-415-001	IC 74LS145, BCD TO DECI DEC	U3,4
700116-415-001	DISPLAY, 4 DIGIT, NSM4700A	U5-8
600217-415-101	IC 8243, I/O EXP	U9
600206-419-024	IC SOCKET, 24 PIN	XU9

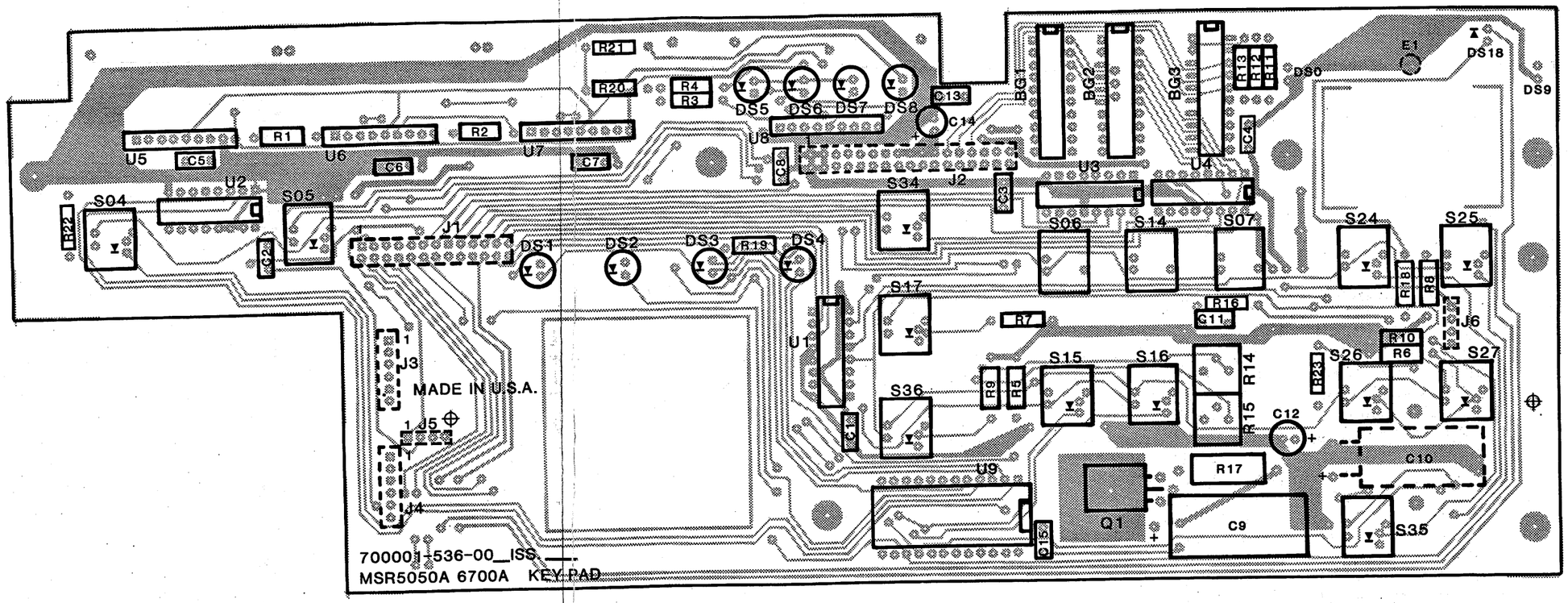
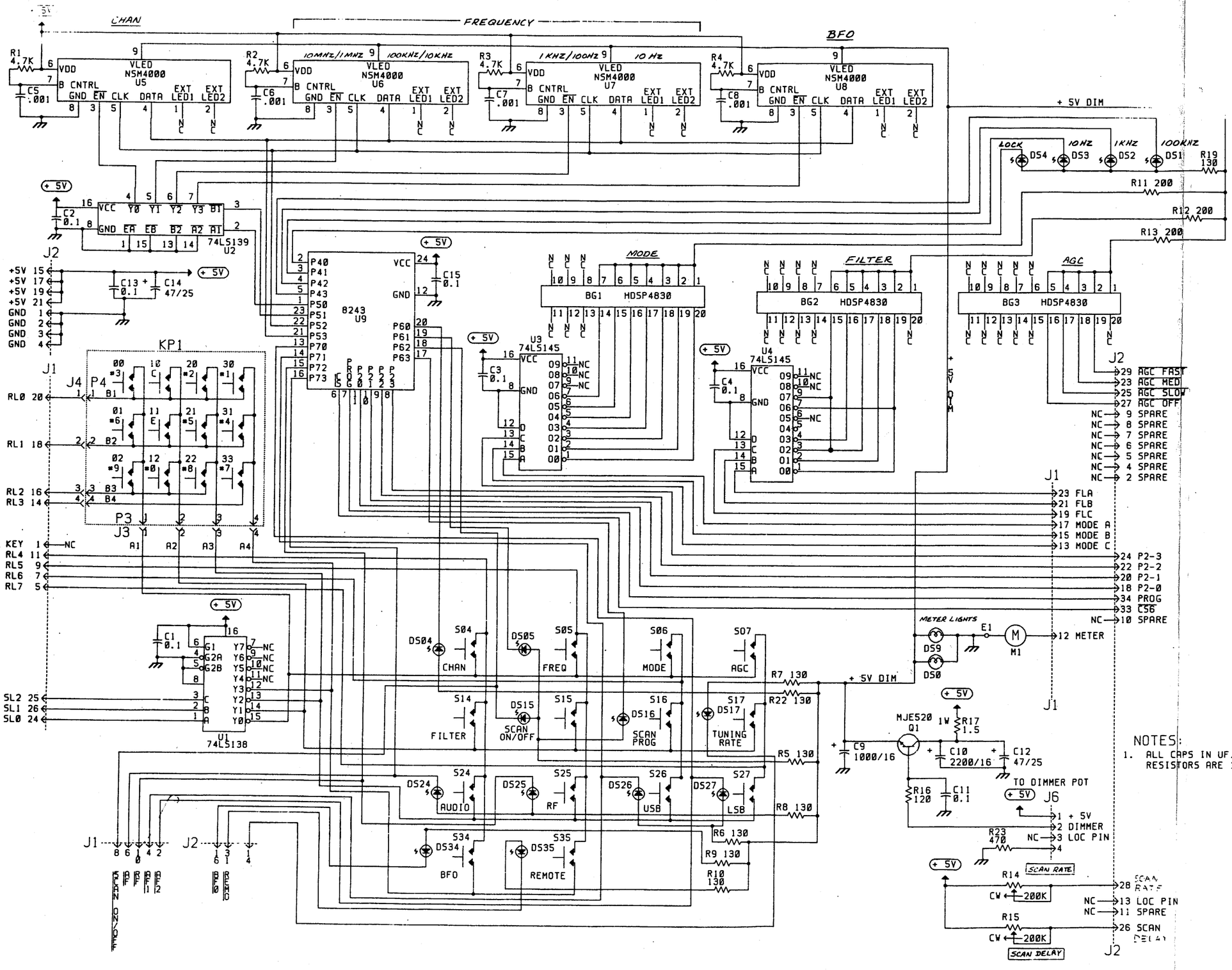


Figure 4.8-2

Keypad Assembly



NOTES:

1. ALL CAPS IN UF, ALL RESISTORS ARE 1/4W, 5%.

Figure 4.8-3

Keypad Board Schematic

MSR 5050A KEYPAD BOARD A1A1

PIN CONNECTIONS AND VOLTAGE READINGS

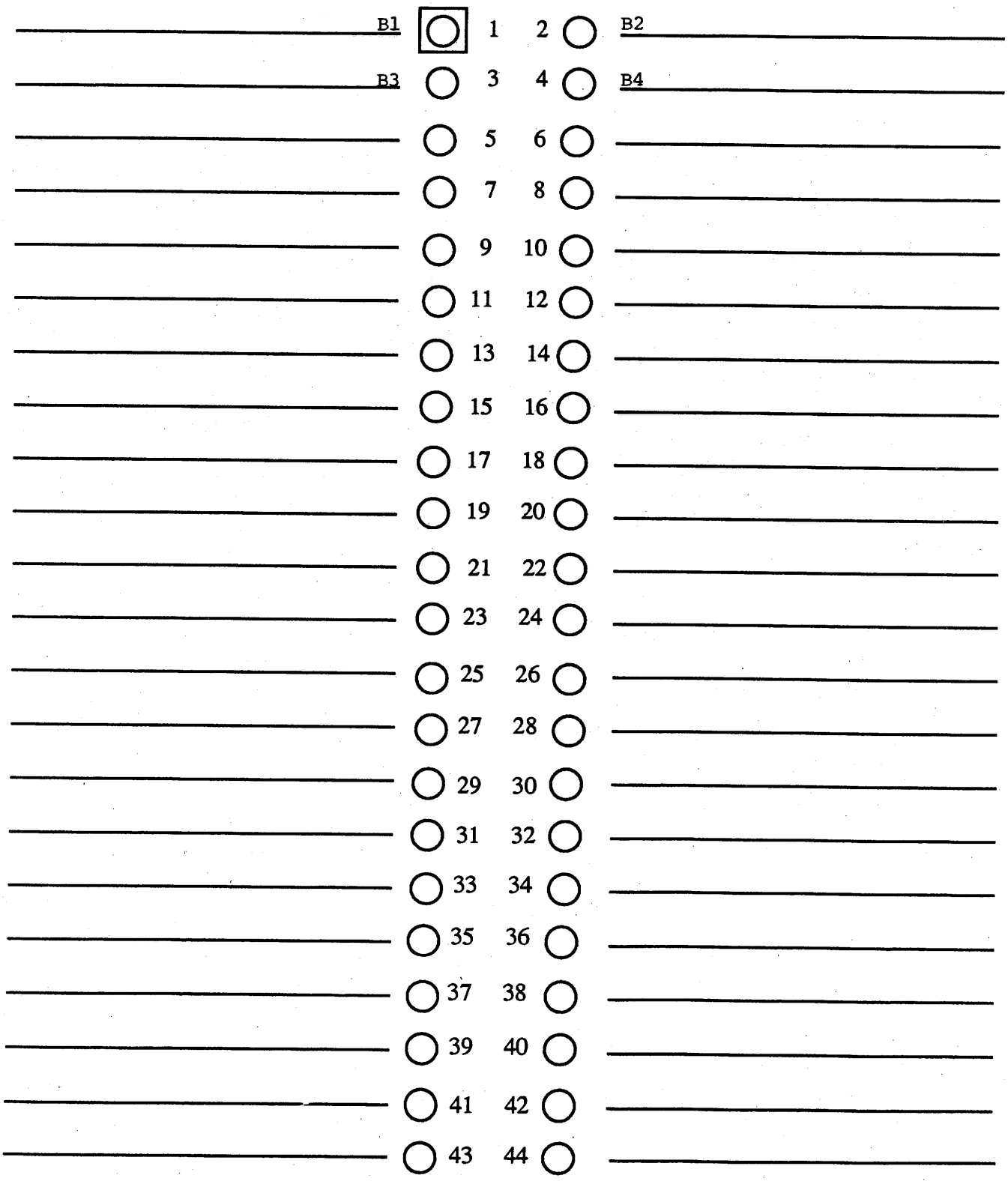
A1A1 J6 (FROM FRONT PANEL DIM CONTROL A1P6)

+5 VDC	1	2	DIMMER
NC - LOC PIN	3	4	DIMMER RETURN
	5	6	
	7	8	
	9	10	
	11	12	
	13	14	
	15	16	
	17	18	
	19	20	
	21	22	
	23	24	
	25	26	
	27	28	
	29	30	
	31	32	
	33	34	
	35	36	
	37	38	
	39	40	
	41	42	
	43	44	

MSR5050A KEYPAD BOARD A1A1

PIN CONNECTIONS AND VOLTAGE READINGS

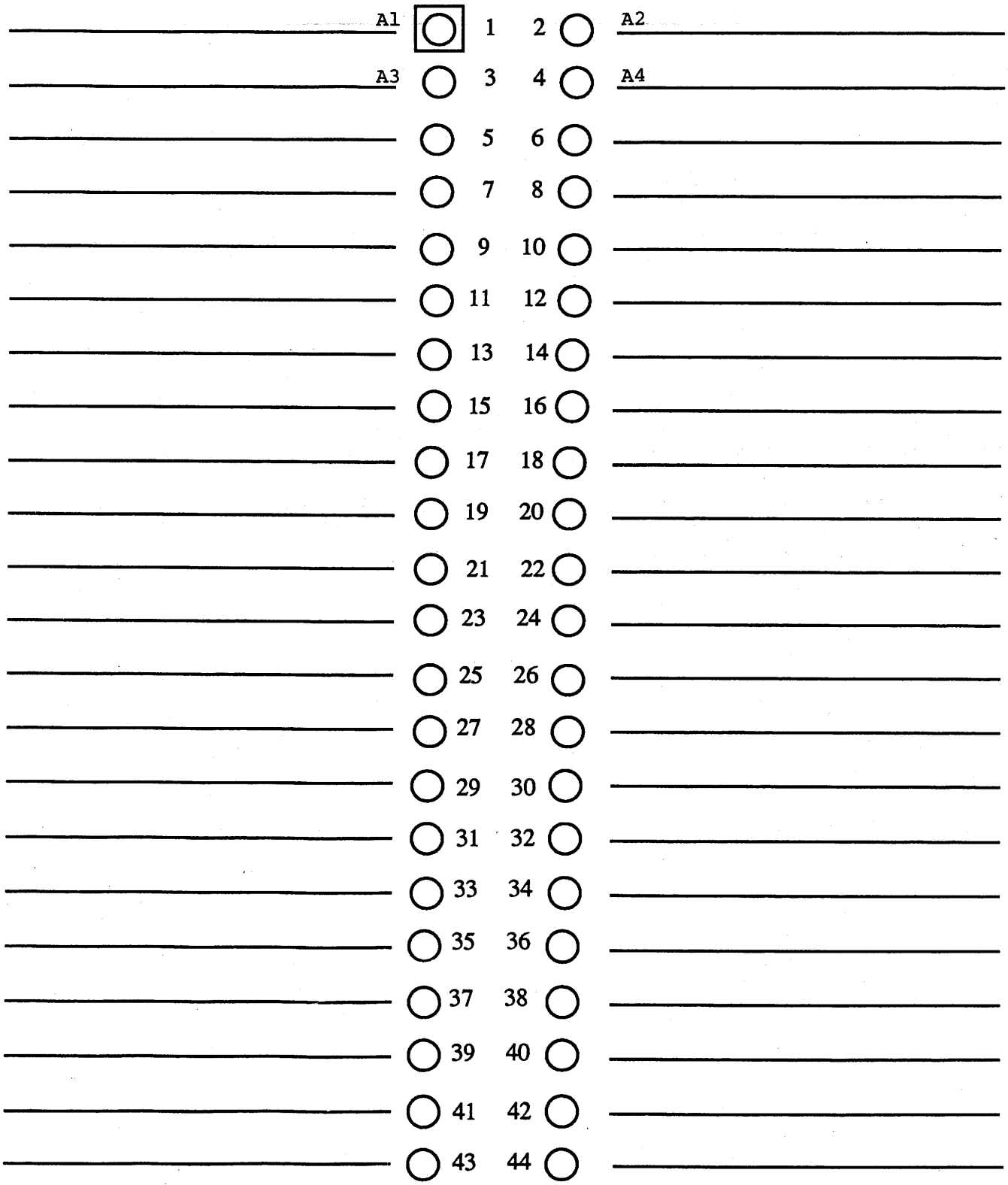
A1A1J4 (FROM FRONT PANEL KEYPAD ASSY A1P4)



MSR 5050A KEYPAD BOARD A1A1

PIN CONNECTIONS AND VOLTAGE READINGS

A1A1J3 (FROM FRONT PANEL KEYPAD ASSY A1P3)



MSR 5050A KEYPAD BOARD A1A1

PIN CONNECTIONS AND VOLTAGE READINGS

A1A1J2(P4) (TO INTERFACE BD A4 J2)

GND	1	2	GND
GND	3	4	GND
NC - SPARE	5	6	NC - SPARE
NC - SPARE	7	8	NC - SPARE
NC - SPARE	9	10	NC - SPARE
NC - SPARE	11	12	NC - SPARE
NC - LOC PIN	13	14	NC
+5 VDC	15	16	$\overline{\text{BFO}}$ LOGIC "Ø" OR "1"
+5 VDC	17	18	P2Ø
+5 VDC	19	20	P21
+5 VDC	21	22	P22
LOGIC "Ø" OR "1" $\overline{\text{AGC MED}}$	23	24	P23
LOGIC "Ø" OR "1" $\overline{\text{AGC SLOW}}$	25	26	SCAN DELAY Ø to +5 VDC
LOGIC "Ø" OR "1" $\overline{\text{AGC OFF}}$	27	28	SCAN RATE Ø to +5 VDC
LOGIC "Ø" OR "1" $\overline{\text{AGC FAST}}$	29	30	
LOGIC "Ø" OR "1" $\overline{\text{REMO}}$	31	32	
LOGIC "Ø" OR "1" $\overline{\text{CS6}}$	33	34	PROG
	35	36	
	37	38	
	39	40	
	41	42	
	43	44	

MSR 5050A KEYPAD BOARD A1A1

PIN CONNECTIONS AND VOLTAGE READINGS

A1A1J1(P3) TO (INTERFACE BOARD A4 J1)

LOC PIN	1	2	$\overline{AF2}$ LOGIC "Ø" OR "1"
	3	4	$\overline{AF1}$ LOGIC "Ø" OR "1"
RL7	5	6	$\overline{AF}$ LOGIC "Ø" OR "1"
RL6	7	8	$\overline{SCAN\ ON/OFF}$ LOGIC "Ø" OR "1"
RL5	9	10	$\overline{RF}$ LOGIC "Ø" OR "1"
RL4	11	12	METER
LOGIC "Ø" OR "1" MODE C	13	14	RL 3
LOGIC "Ø" OR "1" MODE B	15	16	RL 2
LOGIC "Ø" OR "1" MODE A	17	18	RL 1
LOGIC "Ø" OR "1" FLC	19	20	RL Ø
LOGIC "Ø" OR "1" FLB	21	22	
LOGIC "Ø" OR "1" FLA	23	24	SL Ø
SL 2	25	26	SL 1
	27	28	
	29	30	
	31	32	
	33	34	
	35	36	
	37	38	
	39	40	
	41	42	
	43	44	

4.9 REAR PANEL ASSEMBLY, A3

The rear panel contains the power supply and connectors for external interface. It is detachable from the main receiver by 11 screws. Electrical disconnect is by seven connectors from the Mother board and by two molex connectors to the left side support assembly which contains the power transformer and low-voltage rectifiers for the pre-regulator circuits.

The AC power is brought in through J40 which contains the fuse, line filter and a voltage selector card, which interconnects transformer windings to adapt to various line voltages. J46, J45 and J41 are coax connectors for antenna, 5 MHz IF monitor and 5 MHz reference signals. S1 provides a signal to the reference board A19, to allow synthesizer operation from an external reference or internal reference using J41. J42 contains line audio outputs and miscellaneous inputs and outputs. J43 contains remote control lines (via RS-232, FSK, MIL-STD-188, RS-422 or RS-423). The power supply A3A1 is detachable by four screws. It supplies the DC requirements of the radio.

See Section 2.4 for signal descriptions on all connectors. Figure 4.9-4 is a rear panel schematic showing internal interconnections.

With the BCD Interface option, a cable assembly is added providing outputs through J44.

4.9.1 POWER SUPPLY ASSEMBLY, A3A1

The power supply consists of a printed circuit board (containing regulators and associated circuitry) mounted to a heatsink to which the pass transistors for the series regulator circuits are attached. U1 supplies the 13 VDC output by controlling the pass transistor Q1 via U1-11 to maintain 7.15 VDC at U1-4. The ratio of resistors R6 and R7 determines the ratio of the output voltage to U1-4. The 9-volt supply is provided by U2 and Q2 in the same manner, with a different ratio of resistors (R13 and R14) determining the ratio of 7.15 VDC to 9 VDC.

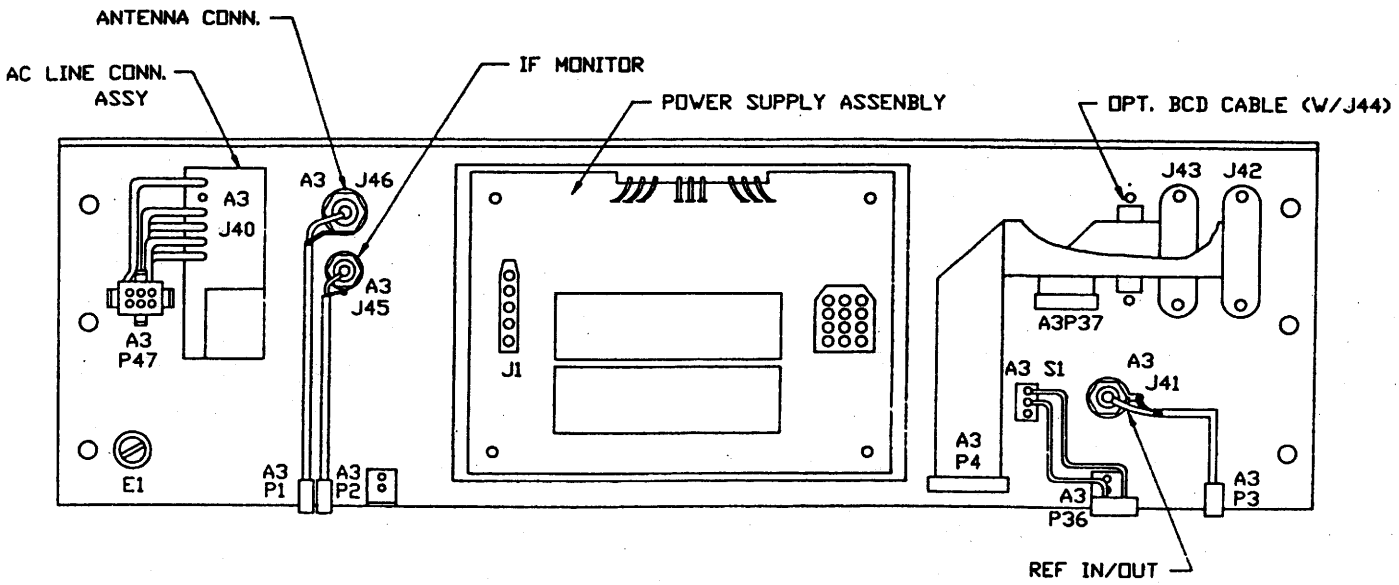
R5 and R12 are the current limiting resistors for U1 and U2 which limit the 13 volts to two amps and the nine volts to 1.4 amps. The input supply for the 13 and 9-volt regulators is a full wave rectified output from a 16.5 VRMS transformer. C3 smooths the ripple to about one volt RMS. To increase the low line operating range, the 16.5 VRMS AC signal (J1-3) is doubled and clamped to the normal pre-regulated input (J1-5) so that U1 always has a high supply voltage. CR3 limits the maximum voltage to U1-12.

U3 supplies an adjustable 5-volt output by varying the reference input to U3-5 via R18. The output current is limited to 3.2 amps by R21. The power input (J1-1) is obtained by full wave rectifying a 10 VRMS AC transformer output. C10 reduces the ripple to one VRMS. The supply voltage for U3 (pin 12) is obtained from the 13-volt pre-regulated input (20 VAC nominal) to allow low line operation.

An on-board BITE indication is produced by DS1, DS2, DS3 and associated current-limiting resistors and zeners to indicate the presence of the 13, 9 and 5-volt outputs. An additional off-board BITE signal is produced by U4 and associated circuitry which detects a drop of 10 percent in the 9 or 13-volt supply to produce a logic 0 output on J2-1.

The power supply outputs are enabled by a logic 0 on J2-3 which removes the grounds on U1, 2 and 3 (pin 13) via Q4.

A frequency reference oven supply voltage is provided at J2-10 which maintains a nominal 12.6 VDC output any time pre-regulated power is provided to the board. When the outputs are disabled, the pre-regulated voltage at J1-5 increases to 24 volts because of the reduced loading. CR13 and CR14 drop the voltage by 11.2V to 12.8 VDC. When the outputs are enabled, the voltage reduces to 8.8 VDC from CR13 and CR14 but the 13-volt output overrides this through CR12 providing 12.4 VDC to J2-10.



Rear Panel (700201-539-001)

PART NUMBER	DESCRIPTION	SYMBOL
600440-540-009	COAX CABLE ASSY	(J41)
600476-540-008	RIBBON CABLE	(J42)
600866-540-038	RIBBON CABLE	(J43)
600440-540-004	COAX CABLE ASSY	(J46,J45)
600559-540-001	CABLE ASSY	(J47)
600567-540-001	CABLE ASSY	(S1)
600423-705-001	POWER SUPPLY ASSY	A1
600070-529-001	FILTER, AC/FUSE BLOCK	J40
600052-606-001	BNC CONNECTOR	J41,J45
600373-606-001	CONN. UHF, PANEL MOUNT	J46
600289-616-006	TOGGLE SWITCH	S1

Figure 4.9-1

Rear Panel Assembly

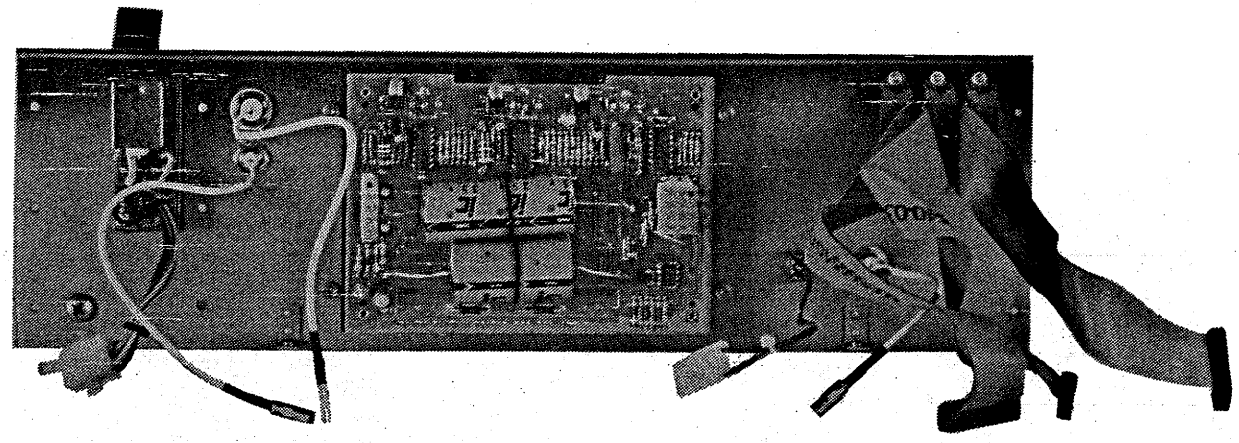


Figure 4.9-2 Rear Panel Assembly, Interior

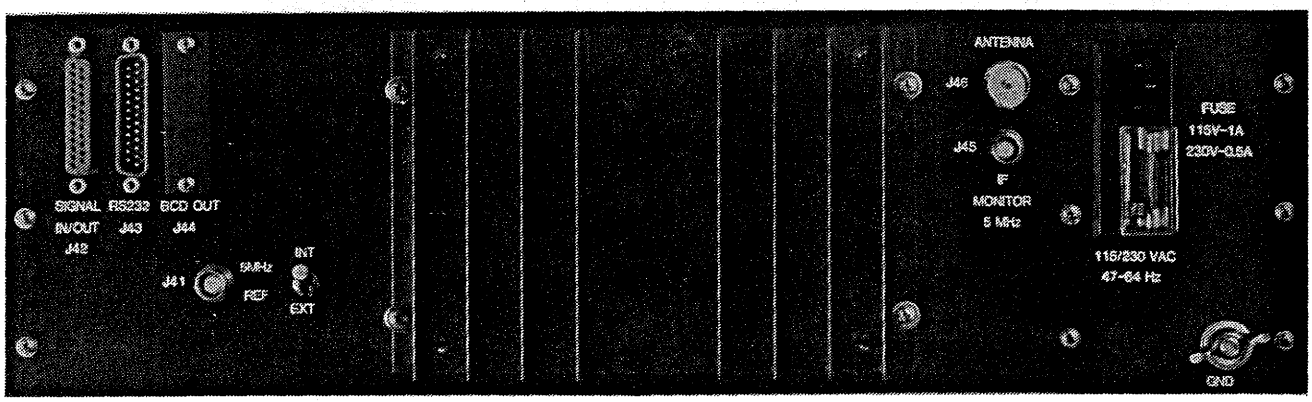


Figure 4.9-3 Rear Panel, Exterior

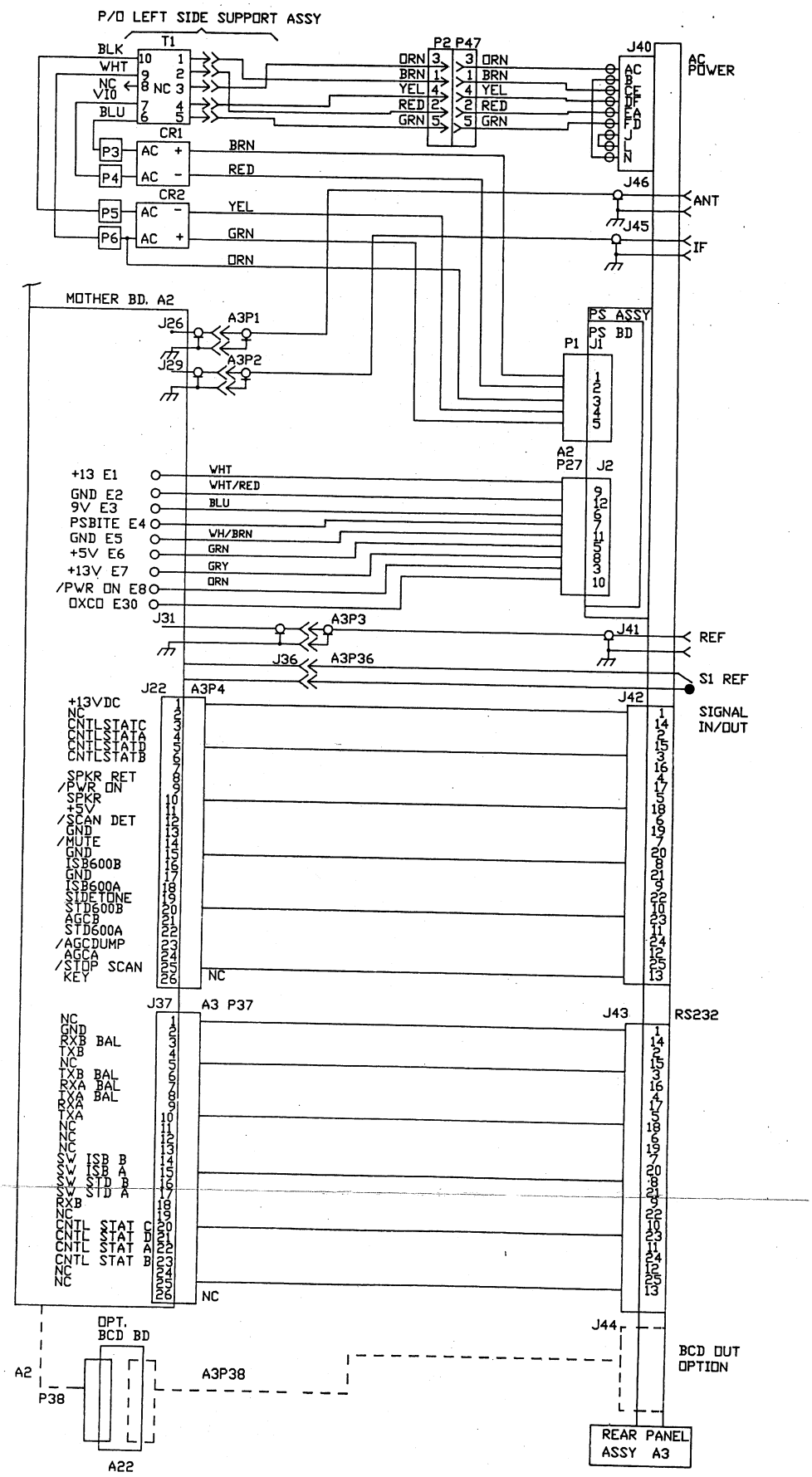
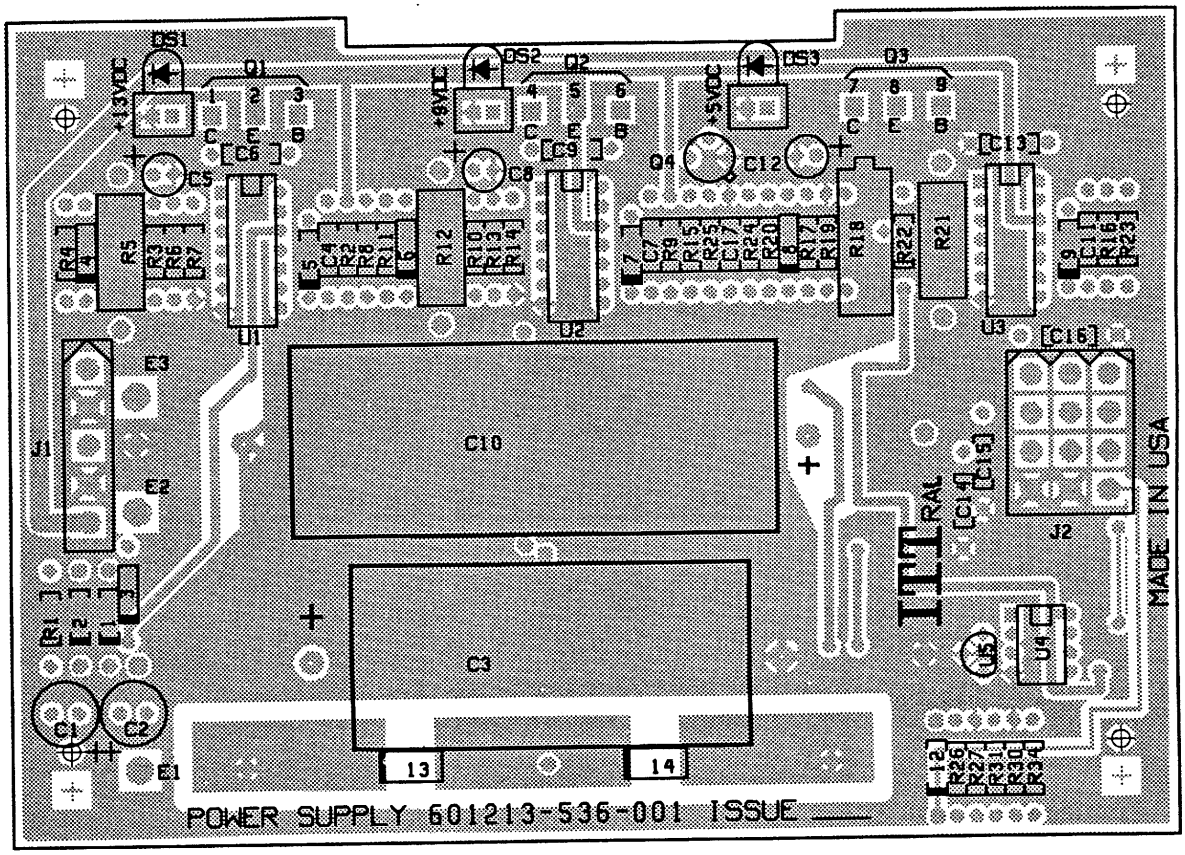


Figure 4.9-4
Rear Panel Schematic

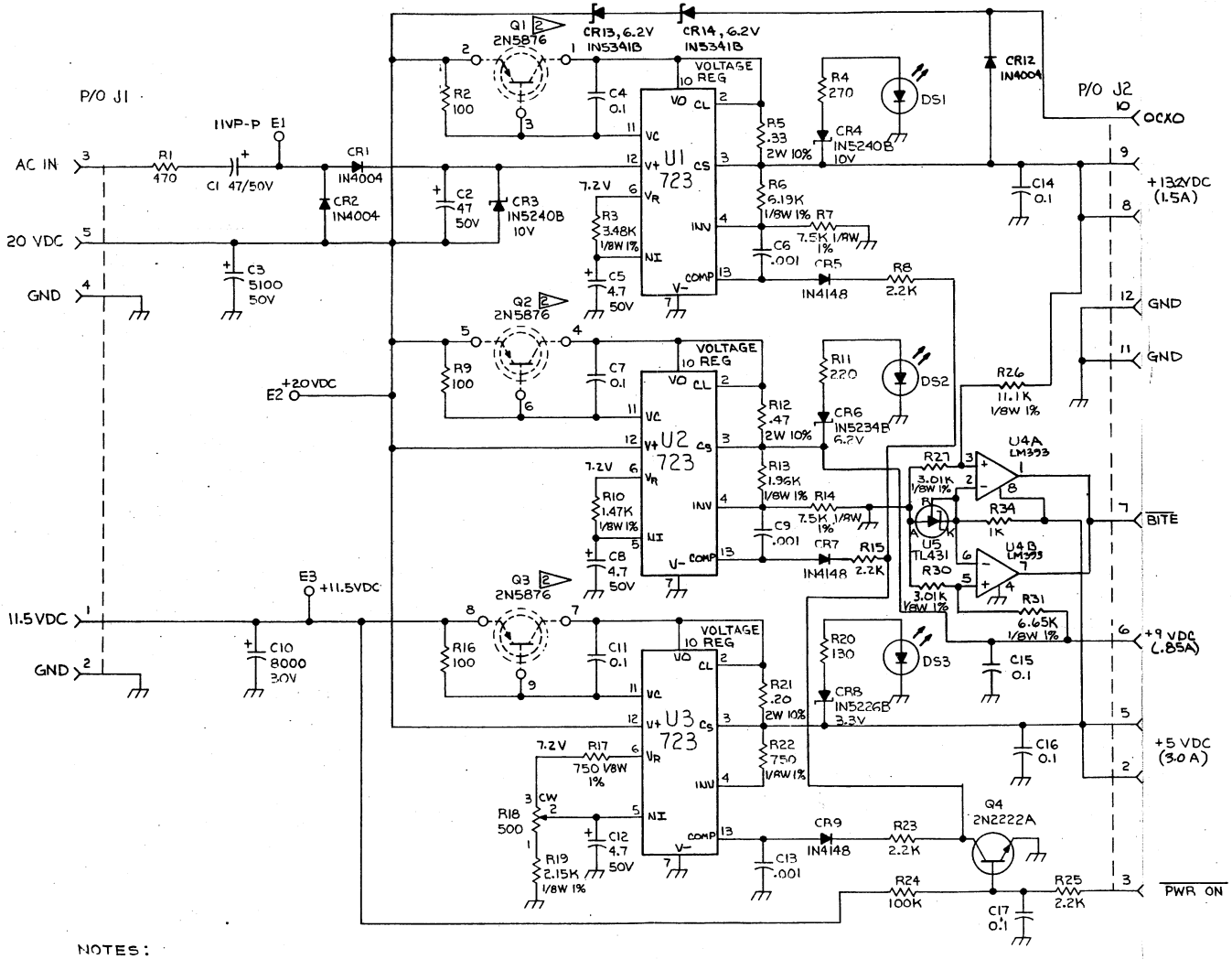


Power Supply (601213-536-001)

PART NUMBER	DESCRIPTION	SYMBOL
603263-602-001	HEATSINK	
600005-635-001	LED MOUNT	
600214-413-001	TRANS	(Q1-3)
600297-314-026	CAP. 47UF, ALUM, 50V	C1,2
600309-314-002	CAP. 8000UF, ALUM, 30V	C10
600309-314-001	CAP. 5100UF, ALUM, 50V	C3
600272-314-001	CAP. .1UF, CERAMIC, 50V	C4,7,11, 14-17
600297-314-010	CAP. 4.7UF, ALUM, 50V	C5,8,12
600272-314-004	CAP. .001UF, CERAMIC, 50V	C6,9,13
600011-416-002	DIODE IN4004	CR1,2,12
600026-411-009	DIODE, ZENER, IN5341A 6.2V	CR13,14
600033-411-020	DIODE, ZENER, IN5240B, 10V	CR3,4
600109-410-001	DIODE IN4148	CR5,7,9
600033-411-014	DIODE, ZENER, IN5234B, 6.2V	CR6
600033-411-006	DIODE, ZENER, IN5226A, 3.3V	CR8
600043-390-002	LED, YEL	DS1,2,3
600261-230-001	TERMINAL	E1,2,3
600237-608-003	CONN. MOLEX, 5 PIN, PC MOUNT	J1
600237-608-001	CONN. MOLEX, 12 PIN, PC MOUNT	J2

PART NUMBER	DESCRIPTION	SYMBOL
600080-413-001	TRANSISTOR 2N2222A	Q4
647004-341-075	RES. 470, 1/4W, 5%	R1
614711-342-059	RES. 1.47K, 1/8W, 1%	R10
622004-341-075	RES. 220, 1/4W, 5%	R11
600057-340-004	RES .47 2W	R12
619611-342-059	RES. 1.96K, 1/8W, 1%	R13
675001-342-059	RES. 750, 1/8W,1%	R17,22
600063-360-006	POT. 500, 15 TURN	R18
621511-342-059	RES. 2.15K, 1/8W, 1%	R19
610004-341-075	RES. 100, 1/4W, 5%	R2,9,16
613004-341-075	RES. 130, 1/4W, 5%	R20
600005-340-138	RES. .2, 3W	R21
610034-341-075	RES. 100K, 1/4W, 5%	R24
611121-342-059	RES. 11.1K, 1/8W, 1%	R26
630111-342-059	RES. 3.01K 1/8W, 1%	R27,30
634811-342-059	RES. 3.48K, 1/8W, 1%	R3
666511-342-059	RES. 6.65K, 1/8W, 1%	R31
610014-341-075	RES. 1K, 1/4W, 5%	R34
627004-341-075	RES. 270, 1/4W, 5%	R4
600057-340-002	RES. .33, 2 WATT, 10%	R5
661911-342-059	RES. 6.19K, 1/8W, 1%	R6
675001-342-059	RES. 750, 1/8W,1%	R7,14
622014-341-075	RES. 2.2K, 1/4W, 5%	R8,15, 23,25
600040-415-101	IC, UA 723, VOL REG	U1,2,3
600486-415-001	IC LM393, DUAL VOL COMP	U4
600632-415-001	IC TL431ILP, SHUNT REG	U5

Figure 4.9-5 Power Supply Assembly



NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL CAPACITORS RATED IN MICROFARADS AND ALL RESISTORS ARE RATED IN OHMS, 1/4 WATT, 5%.

2. FUTURE CONNECTIONS SHOWN FOR REFERENCE ONLY. COMPONTS NOT PART OF THIS UNIT.

LAST USED

C17
E3
Q4
R34
U5
CR14

Figure 4.9-6

Power Supply Schematic

4.10 MOTHER BOARD, A2

The Mother board is a .125 inch PC board, 13 x 16 1/2 inches, which serves mainly as a signal interconnection between 17 plug-in PC boards (via 44-pin edge card connectors), a rear panel assembly and a front panel assembly. The board is also used to enforce the mechanical stability of the chassis and to complete the shielding integrity of the metal "card cage" around the signal path and synthesizer boards. Refer to schematic Figure 4.10-3 for electrical description.

4.10.1 FILTER SWITCH LOGIC

Outputs of either IF Filter board #1 or #2 are connected to Audio Squelch board #1 via analog switches Q1 or Q2, respectively, in response to TTL logic high signals from U4 (pin 4 or 3). The standard radio has only one IF Filter board and thus, Q1 is always "ON" routing all signals to Audio Squelch board #1. The only time Q2 is "ON" and Q1 is "OFF", is with the ISB option or IF Filter option and when an LSB, VNAR or NAR filter is selected. In these cases, the filter activated is in IF Filter board #2 and signals are routed to Audio Squelch board #1, producing audio signals on the standard 600 ohm line.

4.10.2 AGC CONTROL

In most cases the AGC voltage is developed in Audio Squelch board #1 to control both IF Filter board #1 and #2. The IF Filter AGC inputs (AGC A and AGC B) are connected by opticoupler U1, biased on by Q6 in response to a logic high on the ISB line. In ISB mode, Q6 is off - thus U1 is off, disconnecting AGC A and B and allowing Audio Squelch board #2 to control IF Filter board #2, independent of Audio/Squelch board #1/IF Filter board #1.

4.10.3 IF BUFFER AMPLIFIERS

Q4 and Q5 are 5 MHz JFET buffer amplifiers to provide two IF outputs from the Mixer board. The input impedance of the two FETs in parallel, present a near 50 ohm load to the Mixer board output from pin 36. Each FET is tuned and matched at the output (L26, C40, R16 and L27, C41, R17) to present a 50 ohm source impedance to IF Filter #1 (pin 36) and IF Filter #2 (pin 36) with a net 0 dB gain.

4.10.4 I/0 EXPANDERS

U2, U3 and U4 are I/O Expanders operated from microprocessor outputs from the Logic board to control the BCD frequency control inputs of the Minor Loop, Major Loop and BFO boards. U4 also has IF switch outputs and U2 has outputs used in remote operation.

4.10.5 OPTION JUMPERS

Various 2-pin shorting jumpers (JPXX) are used to alter circuitry to accommodate optional equipment by their position on 3-pin headers (with corresponding EXX marked on the Mother board). Refer to Figure 4.10-2 for locations.

JP37, located between J10 and J12, should be positioned to the left (pin 2 to 3) for standard operation. If a second IF Filter board is installed, the jumper should be to the right.

JP9 and JP10 (between J7 and J9) should be positioned left (pins 1 to 2). If the BFO board is installed, both jumpers should be moved to the right.

JP11, 12, 33 and 34 (between J15 and J17) should be positioned toward the rear (pins 1 to 2). If the Audio Interface board is installed in J17, the jumpers should be positioned forward.

JP35 and JP36 (between J15 and J17) should be positioned to the left (pins 1 to 2). If the Modem board is installed in J19 without the Audio Interface board in J17, the jumpers should be moved right.

4.10.6 MISCELLANEOUS

The AGC decay time is controlled by TTL low signals at CR4, CR5 for fast AGC decay or at R9, R20 for medium decay. A logic high signal at both inputs (> 5 VDC) causes a slow AGC decay.

The audio and IF stages are both desensitized by a TTL low from the rear panel via J22, pin 14 MUTE line. The TTL low signal mutes the audio through L7, CR7 and CR9 to the Audio Squelch boards. The IF is desensitized by Q7, which pulls up CR14 and CR15 to +9 VDC and causes maximum AGC attenuation in the IF Filter boards.

The receiver circuits are protected against large antenna signals to 100V RMS by pin diodes CR20 and CR21. The diodes are also used as a DAGC controlled attenuator for very large signals.

Mother Board (700006-536-001)

PART NUMBER	DESCRIPTION	SYMBOL
600521-540-001	PWR SUPP CABLE ASSY	(P27)
600272-314-002	CAP. .01UF, CERAMIC, 50V	C1-5, 12-18, 27,33,39 39,42
600302-314-007	CAP. .01UF, MYLAR, 63V	C34,43, 44,52,53
600272-314-001	CAP. .1UF, CERAMIC, 50V	C38,8-11, 19-26, 28-32, 48-51
620003-306-501	CAP. 200PF, 3%, MICA, 500V	C40,41
600226-314-014	CAP. 1UF, CERAMIC, 50V	C45,59
600302-314-013	CAP. .1UF, MYLAR, 50V	C54-56, 62-64
600297-314-025	CAP. 47UF, ALUM, 25V	C57
600297-314-040	CAP. 2200UF, ALUM, 16V	C58
600269-314-005	CAP. 4.7PF, CERAMIC, 500V	C60
600269-314-022	CAP. 47PF, CERAMIC, 100V	C61
600173-410-001	DIODE, UM4001C	CR20
600173-410-002	DIODE, PIN, UM4001CR	CR21
600109-410-001	DIODE IN4148	CR3-7, 9-12, 27,14,15
600109-410-001	DIODE IN4148	CR22
600052-410-001	DIODE IN270	CR8,13, 18,19
600279-608-002	CONN. HEADER, 4 PIN, PC MOUNT	E9-12, 33-37
600147-605-001	CONN. CARD EDGE, 44 PIN	J1-4, 7-20,34
600174-608-022	CONN. HEADER, 26 PIN, ST.	J22,37
600198-606-002	CONN. MALE MIN. RF, PC MOUNT	J26,29, 31
600174-608-025	CONN. HEADER, 16 PIN, ST.	J32
600174-608-021	CONN. HEADER, 14 PIN, ST.	J35
600237-608-002	CONN. MOLEX, 3 PIN, PC MOUNT	J36
600190-608-001	CONN, JUMPER, 2 POS.	JP9-12, 33-37
600125-376-007	CHOKE 33UH	L1-24, 28-30
600125-376-022	CHOKE 180UH	L25
600125-376-043	CHOKE 5.6UH	L26,27
600091-376-001	CHOKE 4.7UH	L31
600125-376-040	CHOKE 1.0UH	L32
600125-376-030	CHOKE 4.7UH	L33
600125-376-015	CHOKE 470UH	L34
600034-376-001	CHOKE 1000UH	L35
700001-413-001	TRANSISTOR, 2N4393	Q1,2
600259-413-001	TRANSISTOR J310	Q3-5
600229-413-003	TRANSISTOR 2N3904 TO-92	Q6,8,9
600116-413-002	TRANS, 2N3906	Q7,10
610004-341-075	RES. 100, 1/4W, 5%	R15,32
668004-341-075	RES. 680, 1/4W, 5%	R16,17
651094-341-075	RES. 51, 1/4W, 5%	R19
620024-341-075	RES. 20K, 1/4W, 5%	R2,12
612024-341-075	RES. 12K, 1/4W, 5%	R21
647014-341-075	RES. 4.7K, 1/4W, 5%	R22,27, 28,11,37
612014-341-075	RES. 1.2K, 1/4W, 5%	R25
610024-341-075	RES. 10K, 1/4W, 5%	R3,6,18, 23,24, 29,30
662014-341-075	RES. 6.2K, 1/4W, 5%	R36
610014-341-075	RES. 1K, 1/4W, 5%	R4,5, 33,34
610034-341-075	RES. 100K, 1/4W, 5%	R7,31
647004-341-075	RES. 470, 1/4W, 5%	R8,35
651024-341-075	RES. 51K, 1/4W, 5%	R9,10
600005-373-001	ISOLATOR	U1
600217-415-001	IC 8243, I/O EXP	U2-4
600206-419-024	IC SOCKET, 24 PIN	XU2-4

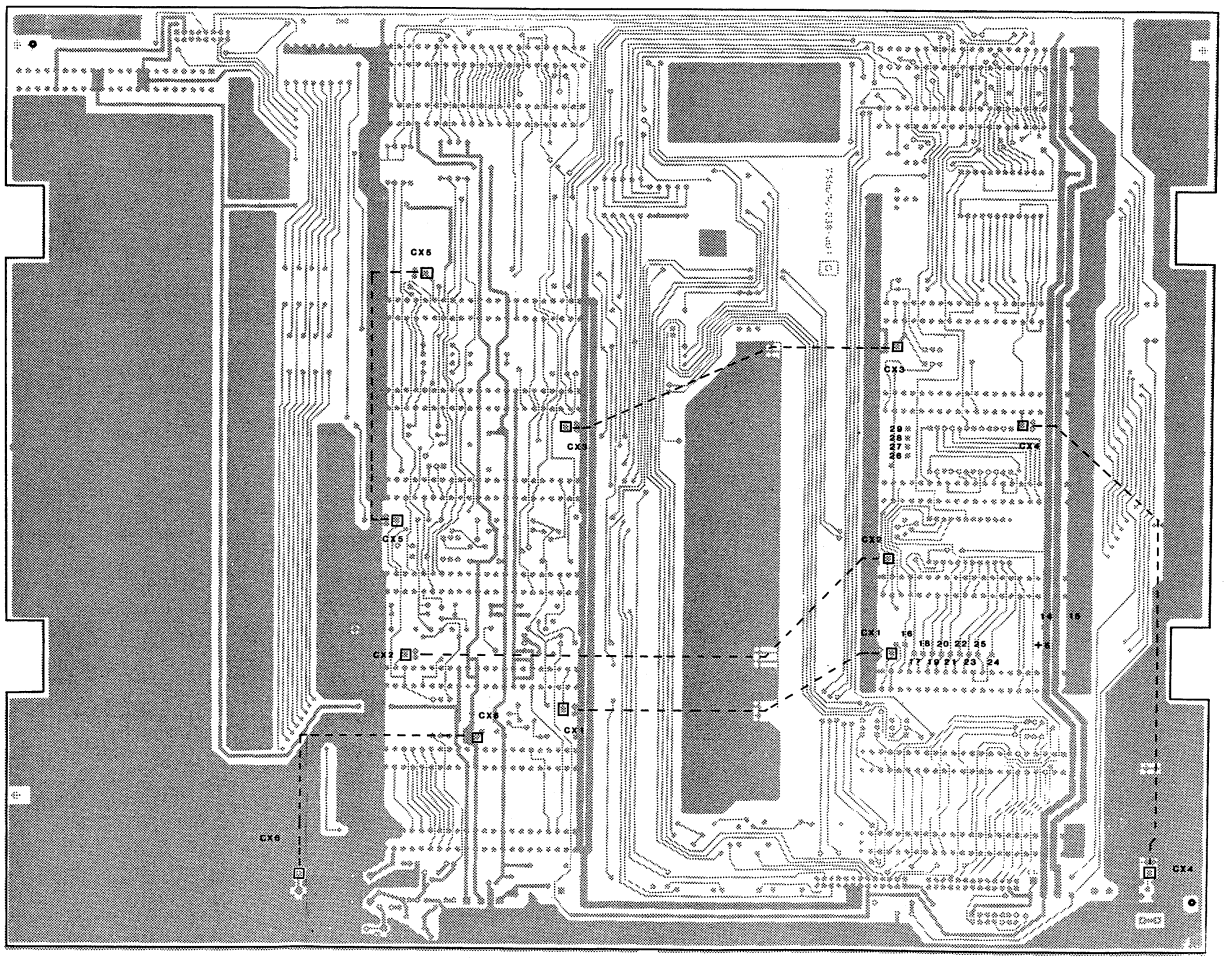


Figure 4.10-1 (Sheet 1 of 2)

Mother Board Assembly

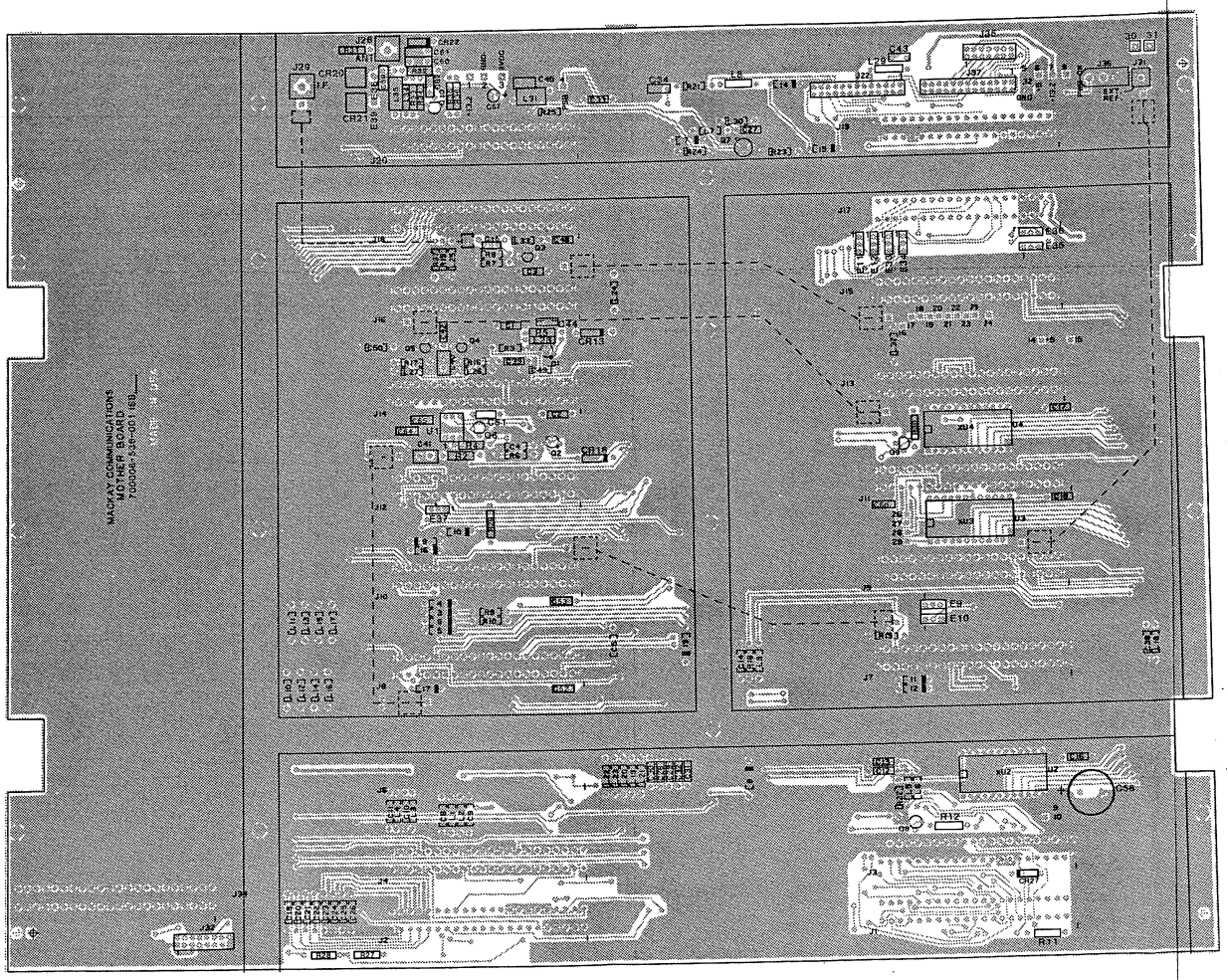


Figure 4.10-1 (Sheet 2 of 2)

Mother Board Assembly

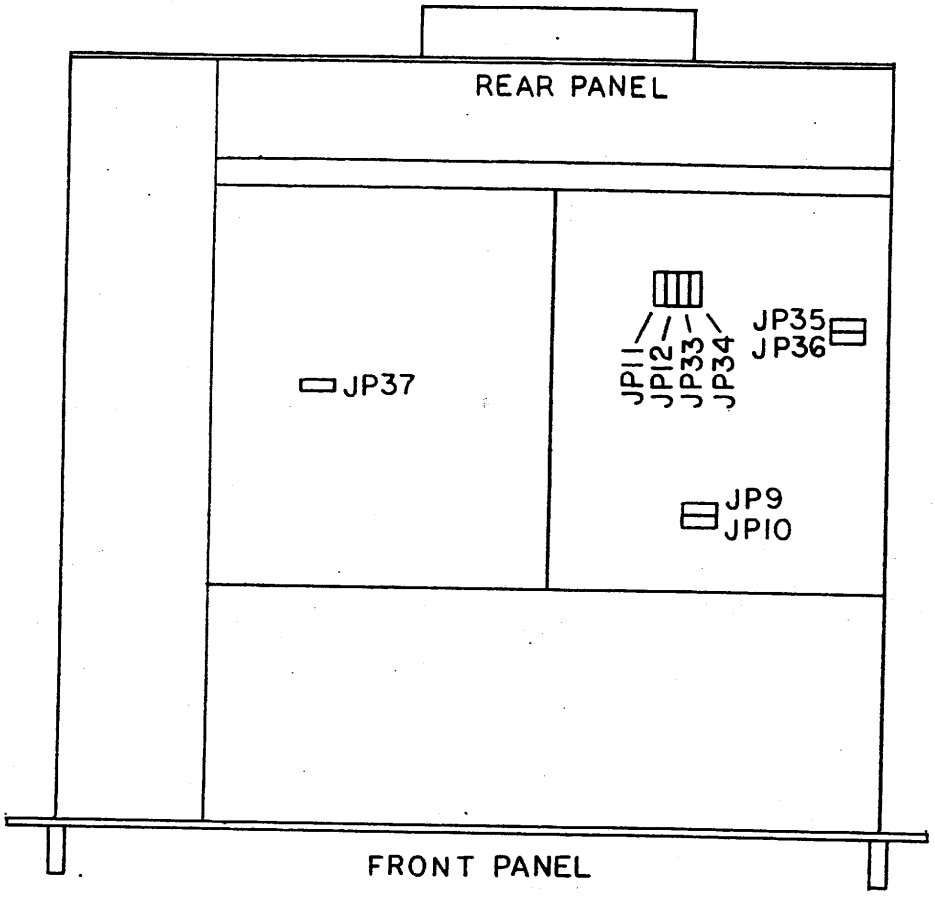


Figure 4.10-2

Mother Board Jumper Locations

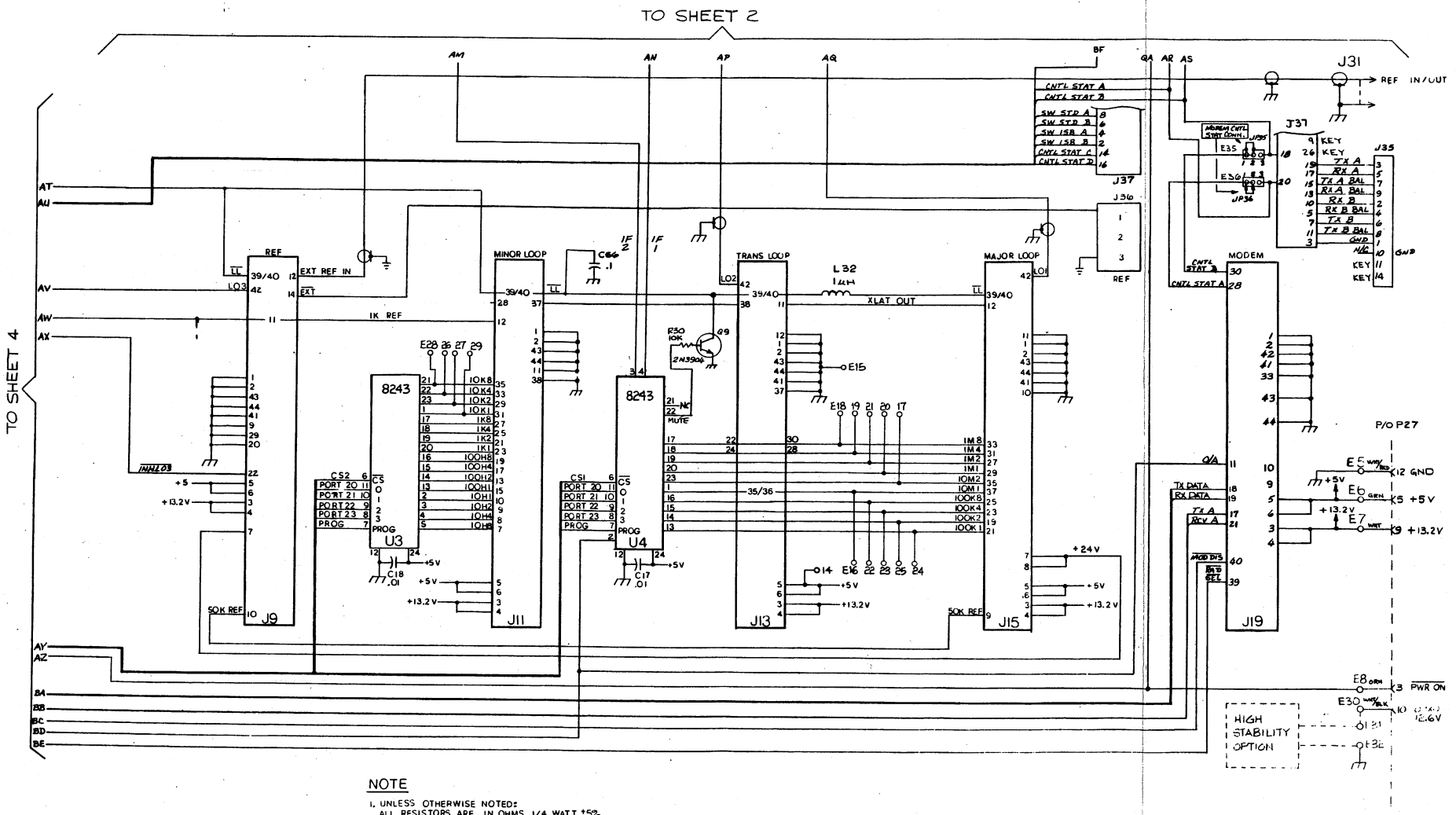


Figure 4.10-3 (Sheet 1 or 4)

Mother Board Schematic

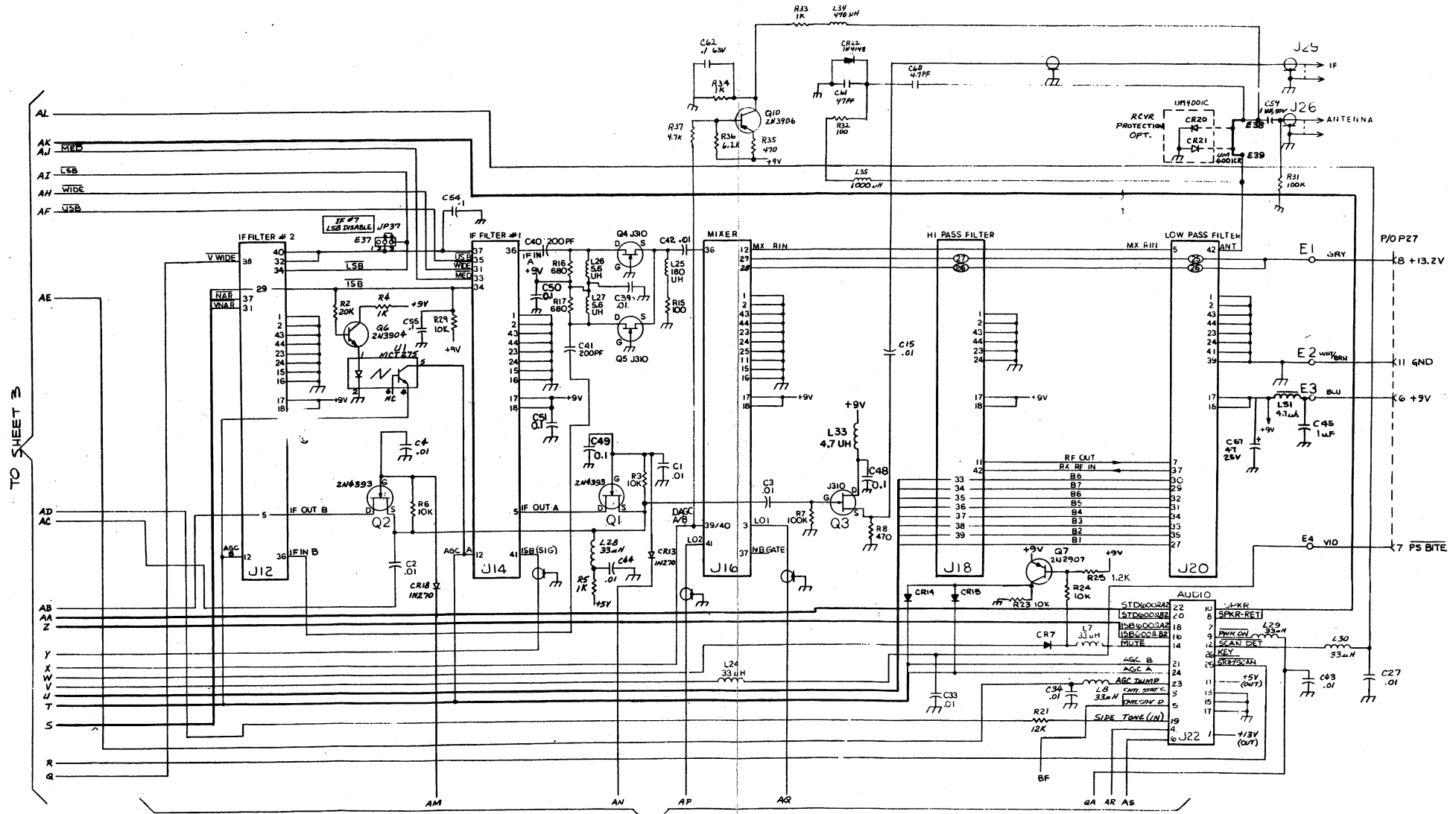


Figure 4.10-3 (Sheet 2 or 4)

Mother Board Schematic

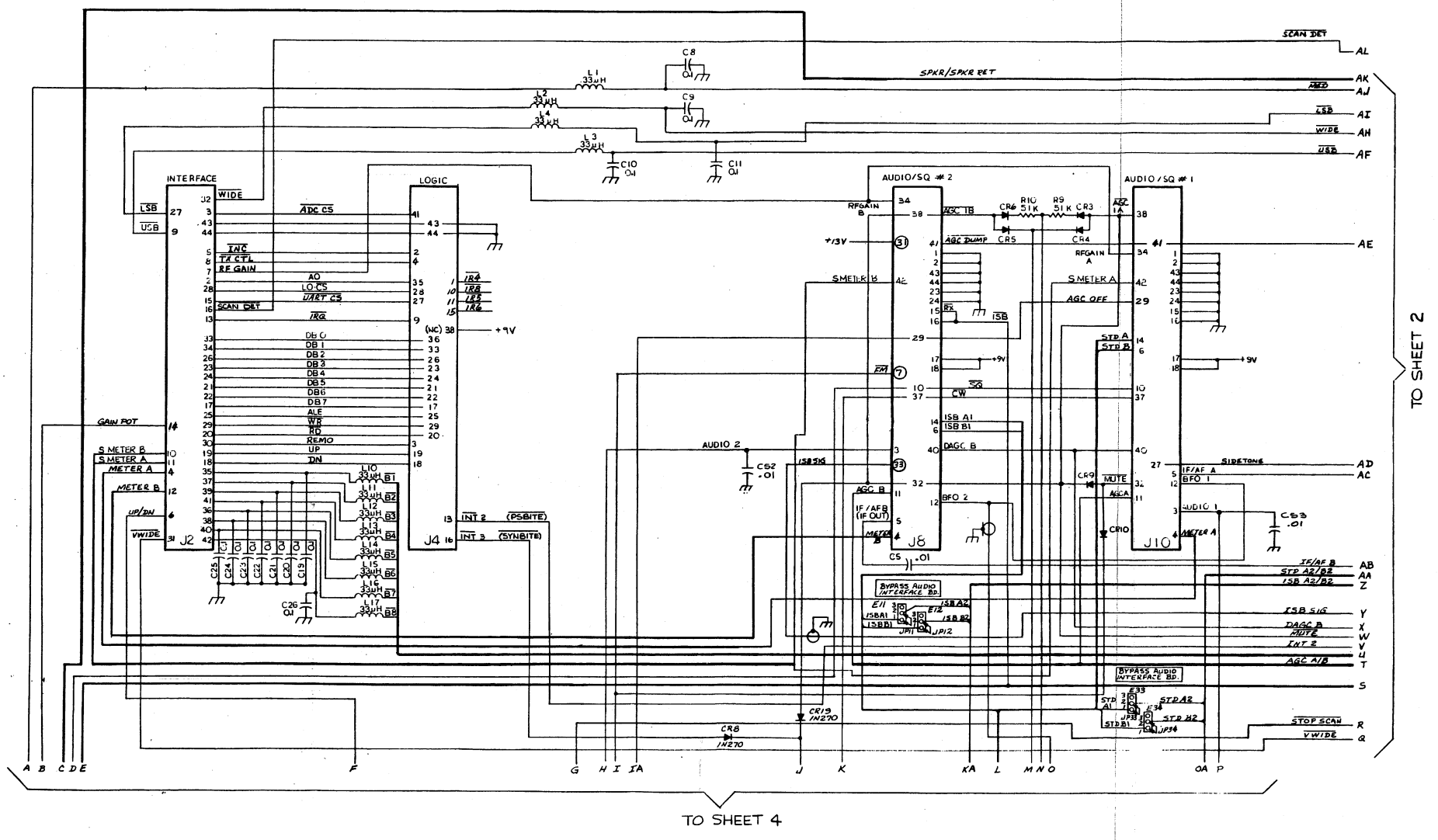


Figure 4.10-3 (Sheet 3 of 4)

Mother Board Schematic

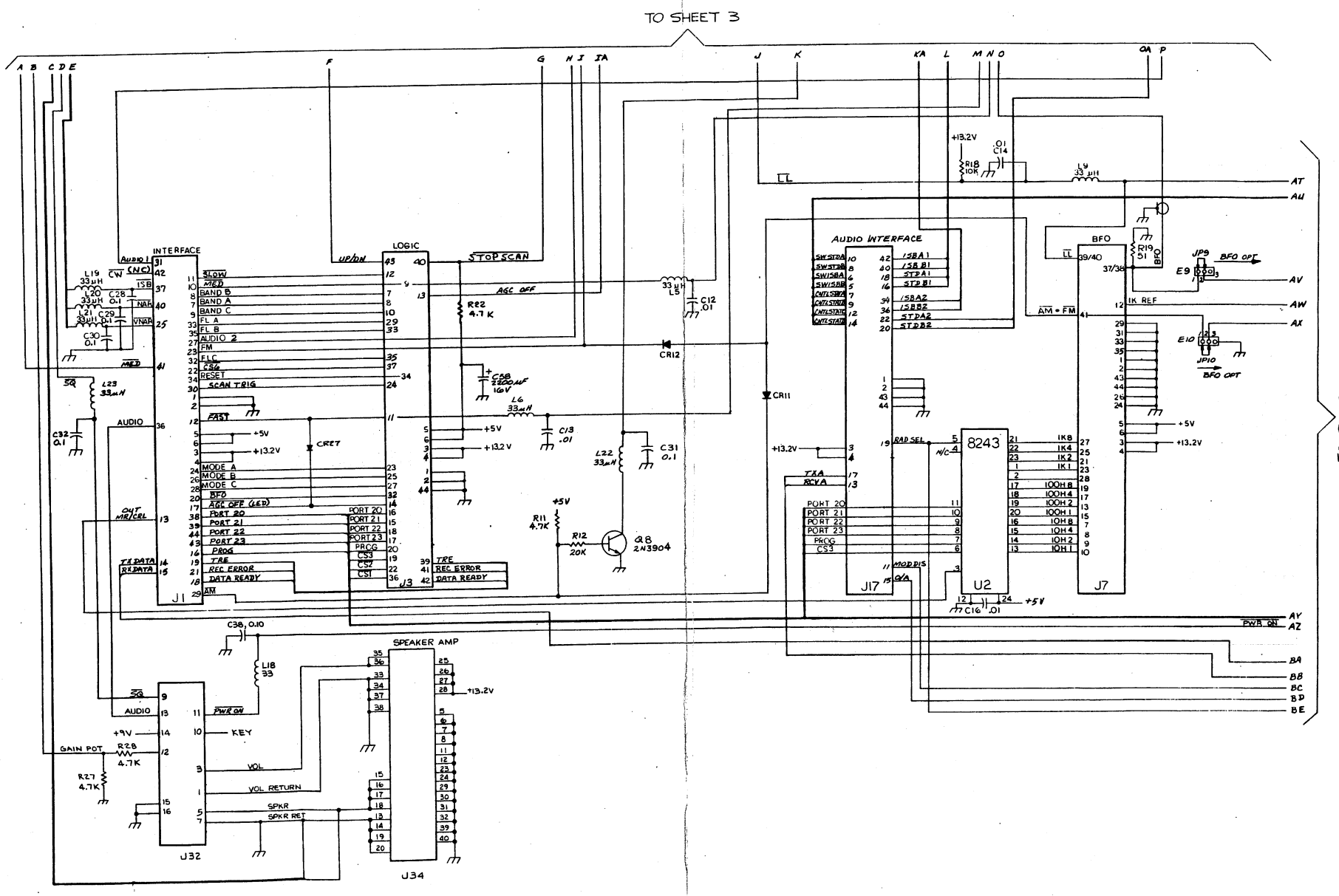


Figure 4.10-3 (Sheet 4 of 4)

Mother Board Schematic

4.11 INTERFACE BOARD, A4

The Interface board plugs into the Mother board by two 44-pin edge card connectors. Connection to the Front Panel assembly is made by three ribbon cable assemblies; two to the Keypad/ Display board and one to the opticoupler tune assembly. A fourth ribbon cable assembly, routed under the Mother board, connects at the rear of the Mother board. (Refer to Figure 4.11-2 for schematic.)

The Interface board must be unplugged from the Mother board for access to switches S1 to S4 (for remote control variations) and jumper JP1 (to change scan function from scan hold to scan delay). To remove, first disconnect J1, J2 and J4 at the top of the board. If complete removal is desired, J3 at the center of the board must also be disconnected.

Three adjustments are required, all accessable at the top of the board without removal: 1) R36 SCAN THRESHOLD, 2) R15 RF METER ADJUST, and 3) R16 AF METER ADJUST.

This board contains the following functions: Keyboard Control, Analog to Digital Converter, Mode, Band, Filter Decoder, UART Circuits, Baud Rate Generator (for UART), Remote Control Interface, Frequency Tune Circuits, Channel/ Frequency Scan Circuit, Meter Switching Circuits, -12V Supply, and Remote RF Gain Control.

4.11.1 KEYBOARD CONTROL

U1 is the keyboard control chip (8279). The front panel keys (both those on the keypad assembly and those on the Keypad/Display board) are electrically arranged in a matrix configuration. Three scan lines SL0-SL2 (rows) and eight return lines RL0-RL7 (columns) define which key is depressed. This information is communicated to the microprocessor on the main data bus DB0-DB7 with write command /WR, read command /RD and clock signal ALE.

U1 pin 4 is the IRQ output. This pin is normally low and will go high when a key is closed. It will return low after the key code has been read. U1 pin 9 is the reset input. U1 will be reset when this pin goes high (i.e. on power up). U1 is connected to the data bus only when /CS pin 22 is low (i.e. when not in remote status).

4.11.2 ANALOG TO DIGITAL CONVERTER

U4 is an ADC0804 A to D converter used to send receiver RF signal levels to a Remote Control Unit (RCU). A 0 to +5 VDC signal obtained from the meter circuit is brought into U4 pin 6 where it is digitized to an 8-bit word on the main data bus. R31 and C36 tune its internal clock to approximately 70 kHz.

4.11.3 DECODERS

U5, 6 and 7 decode the 3-bit (A, B, C) mode, filter and band lines to eight open collector outputs for each function. U7 produces /B1 to /B8 to control the eight suboctave filter bands of the High Pass Filter and the Low Pass Filter board. U6 provides eight open collector filter output signals. A similar decoder in the Keypad/Display board provides simultaneous outputs to light the appropriate bar graph LED indicator. VW (very wide), WIDE, NAR (narrow) and VNAR (vary narrow) signals are used to select corresponding bandwidth filters in IF Filter board #1 or #2. ("WIDE" is the only standard filter.) The MED (medium) output selects the USB filter in IF Filter board #1. These signals are used for AM, CW or FSK. The FSK NAR output is bussed to the NAR output. This would be used for a custom FSK offset filter mounted in the NAR position in IF Filter board #2. The FMVW (FM very wide) output is not used since the FM mode signal selects its own very wide filter. This output is bussed to the VW output in the bar graph for a corresponding indication. The SSB/MED output is automatically locked in with USB, LSB or ISB mode selections. The bar graph decoder in the Keypad/Display board busses this output to the MED output to indicate a medium bandwidth filter.

U5 provides seven decoded outputs. The USB and LSB outputs pull in associated filters in IF Filter boards #1 or #2. ISB pulls in both filters simultaneously. The product detector in the Audio Squelch board is always used except in AM or FM. The CW and FSK mode outputs therefore are not used since the product detector is used in

these modes also. The corresponding bar graph decoder in the Keypad/Display board, however, indicates all modes. The AM output selects the AM detector in the Audio Squelch board and disables the 3rd LO in the Reference board. The FM output enables the optional FM board and also disables the 3rd LO.

4.11.4 UART CIRCUITS

The 6402 UART (U2) performs the series/parallel conversions for remote control operation. For transmitting operations, the 8-bit parallel data bus from the µP (U2 pins 26 through 33) is converted to serial data. A start, stop and parity bit is added to form an 11-bit word which exits pin 25(TR0). In receive the serial data enters pin 20 (RR1) where it is converted to 8-bit parallel data, checked for errors and bussed to the µP from U2 pins 12 through 5.

An external write cycle from the µP will send out one serial word if the UART chip is selected and the transmit register is empty (TRE high). When a serial word is received, pin 19 (DR = data ready) will go high to signal the µP that data is ready to read. An external read cycle of the µP will pick up this data and reset DR to low if the UART chip is selected. A logic high on pin 13 (PE), pin 14 (FE) or pin 15 (OE) indicates that a receive error has been detected. The clock rate on pins 17,40 determines the baud rate of the serial data.

4.11.5 BAUD RATE GENERATOR

U3 (8116) is the baud rate generator which determines the rate at which data is transferred between UARTs at two locations. A 4-section dip switch S4 determines the baud rate. See Table 3.1 for switch settings.

4.11.6 REMOTE CONTROL INTERFACE (See Table 3.1 for switch settings.)

U21 through U25, dip switches S1,2,3, and relays K1,K2 interface the UART to external remote control lines to accommodate RS-232, RS-423, RS-422 and MIL-STD-188C formats. U23 A, B are balanced (RS-422) or unbalanced line receivers depending on S1-3 and S1-4 setting. U22 A and U22 B are either balanced or unbalanced line drivers depending on the position of S1-5. Two ports A and B are provided so that multiple receivers may be daisy-chained in a remote-controlled network. For example, on one port are RX A (receive signal), RX A BAL (return line for RX A in an RS-422 format), TX A (transmit signal), and TX A BAL (return for TX A in an RS-422 format). Signals coming into RX A are retransmitted out TX B to the next receiver in a daisy-chain. If the receiver power is off, relays K1 and K2 connect ports A and B so that the daisy chain is not electrically broken. In transmit condition, signals are sent out at both TX A and TX B.

Transmit and receive signals are routed to separate busses A and B and ultimately to UART U2 pins 25 and 20 (TR0 and RR1). Signals are diverted to the appropriate ports by tri-state buffers U24 and U25, controlled by the TXCTL signal from the µP.

When the optional FSK modem is installed, the FSK signals are reduced to TTL signals RX DATA and TX DATA in the modem and brought to P1 pins 15 and 14. The signals are then routed to the same BUS A and BUS B as before.

4.11.7 FREQUENCY TUNE CIRCUIT

The front panel opticoupler assembly puts out pulses on two lines brought in at J3-1 and J3-2. The rate and relative timing of the pulses are decoded in U10A, B; U13A, B, C; U11B; and U12A to produce a signal on either U13-8 (to tune down in frequency) or U13-6 (to tune up). These signals are routed to the µP on the Logic board.

4.11.8 CHANNEL/FREQUENCY SCAN CIRCUIT

In channel or frequency scan mode U9, connected as a one-shot multivibrator, determines the scan rate. The µP initiates a tuning cycle by a TTL low pulse on U9-2 (scan trigger). The output U9-3 goes high which is OR'd with other signals to the DN signal output to the µP (P2-18). The µP monitoring this signal waits for a low before incrementing frequency or channel and initiating another time cycle. The scan rate is adjustable by a variable resistance to +5 VDC (from R14 on the Keypad/Display board).

U8A is shown as a nonretriggerable one-shot producing a scan delay generator. The output U8-6 is OR'd to the previous DN signal to further extend the incrementing period. The delay time is adjustable by R15 on the Keypad/Display board through J2-28. The delay generator is only activated by a received audio signal at U20-2 which exceeds a dc peak level set by R36. When the µP increments frequency or channel in scan mode, it produces a negative pulse on P1-30 which not only starts the scan rate oscillator but also starts a signal inhibit one-shot (U8B) and resets the scan delay generator. The signal inhibit generator produces a negative pulse at U8-10 with a pulse width of 60 milliseconds. This negative output shunts signals from U20A, thus preventing delay triggering from transient signals during frequency changes. With JP1 on E1 pin 1 and 2, U8A is changed to a retriggerable one-shot, allowing the time delay to be extended as long as threshold audio signals are present.

4.11.9 METER/AUDIO SWITCHING

RF signal level meter indication is obtained from S meter outputs from Audio Squelch boards #1 and #2 (AGC A, AGC B) at pins P2-11, P2-10. The signals are buffered and switched by U19-C and U19-D. R15 adjusts the signal to the meter for full scale at +100 dBµV.

Audio level meter signals are produced from unbalanced line audio outputs from Audio Squelch boards #1 and #2 at P2-4 and P2-12. U19A and B are buffer/switches and peak detectors. U18-C is another buffer/switch. R16 adjusts the signal to the meter for full scale dejection at about +10 dBm. U18D amplifies the meter signal for the A to D converter input to about 5 volts maximum.

Speaker audio signals from each of the Audio Squelch boards are brought into P1-31, P1-27. U18A and B are buffer/switches which produce a single audio signal at P1-36 in response to AF1 or AF2 from the Keypad/Display board.

4.11.10 -12 VOLT SUPPLY

U26 is connected as an oscillator producing -12 VDC output in conjunction with Q3 and Q4. This -12 volts is used for line drivers U21A, B which convert TTL signals from the UART to a signal with higher ± excursions.

4.11.11 RF GAIN CONTROL

U14 is an electrically erasable potentiometer used for remote RF gain control. It puts out a 0 to 5 VDC level at pin 5. When pin 7 is low (REMO) U14 output may be changed in increments either up or down (depending on the TTL signal level at pin 2) by pulsing pin 1. The output level is latched otherwise. Either U14 output or the front panel RF gain pot output is selected for the final RF gain output (P2-7) by buffer/switches U20B, C. The RF gain signal is finally applied to both Audio Squelch boards.

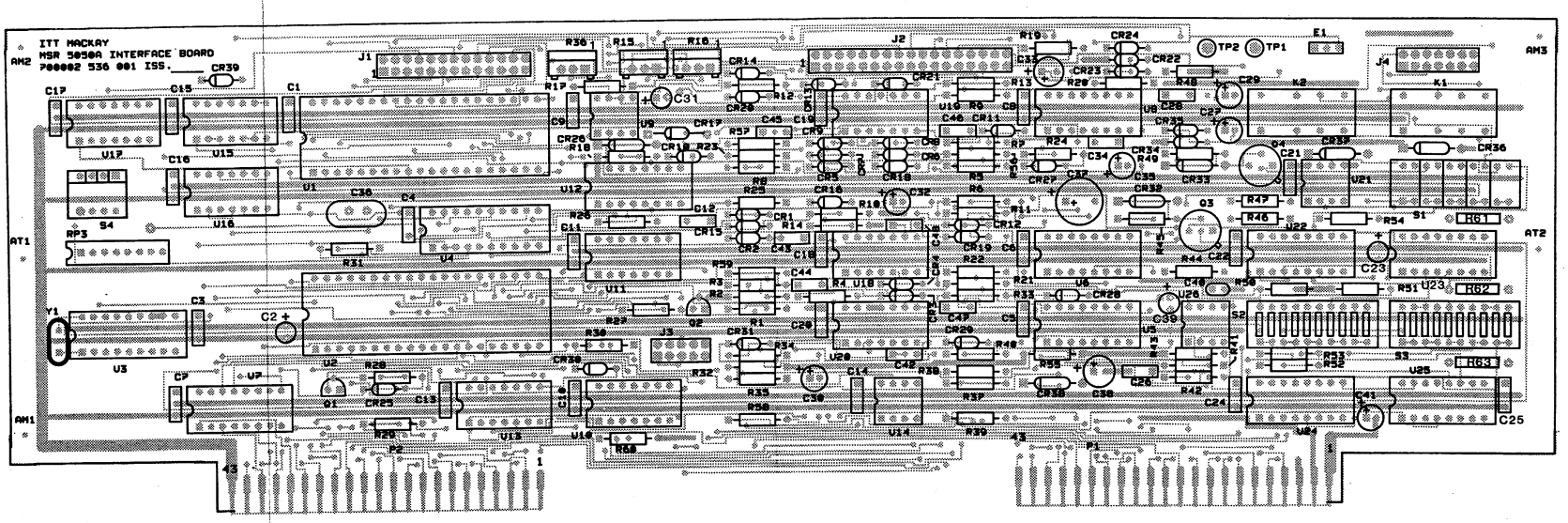


Figure 4.11-1

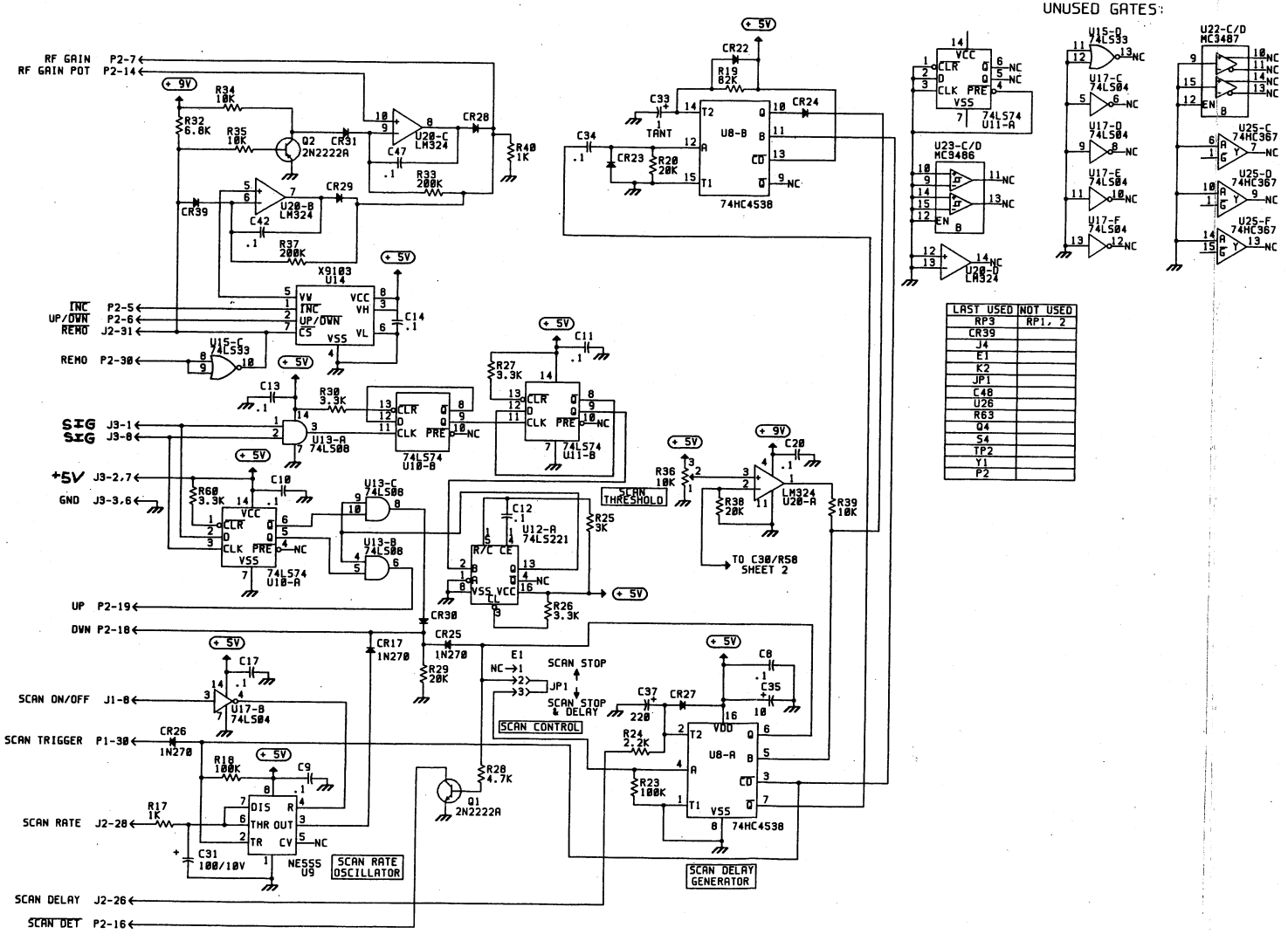
Interface Assembly

Interface (700002-536-001)

PART NUMBER	DESCRIPTION	SYMBOL
600119-419-040	IC SOCKET, 40 POS.	(U1,2)
600119-419-020	IC SOCKET, 20 POS.	(U4)
600302-314-013	CAP. .1UF, MYLAR, 50V	C1,3-22, 24-26, 28,34,
600297-314-031	CAP. 100UF, ALUM, 10V	C2,23,31
600297-314-013	CAP. 10UF, ALUM, 50V	C27,29, 30,35,41
600297-314-016	CAP. 22UF, ALUM, 25V	C32
600202-314-007	CAP. 1UF, 35V, TANT.	C33
615003-306-501	CAP. 150PF, 3%, MICA, 500V	C36
600297-314-037	CAP. 220UF, ALUM, 10V	C37
600297-314-025	CAP. 47UF, ALUM, 25V	C38,39
600268-314-011	CAP. .015UF, CERAMIC, 50V	C40
600302-314-013	CAP. .1UF, MYLAR, 50V	C42-44, 47,48
600109-410-001	DIODE IN4148	CR1-16, 18-24, 27-31,34, 35,39, 40,41
600052-410-001	DIODE IN270	CR17, 25,26
600006-411-007	DIODE IN4734A 5.6V	CR32,33
600011-416-002	DIODE IN4004	CR36,37
600006-411-012	DIODE IN4739A 9.1V	CR38
600198-608-005	CONN. HEADER, 3 PIN, TIN	E1
600174-608-005	CONN. HEADER, 26 PIN, ST.	J1
600174-608-006	CONN. HEADER, 34 PIN, ST.	J2
600174-608-001	CONN. HEADER, 10 PIN, ST.	J3

PART NUMBER	DESCRIPTION	SYMBOL
600174-608-021	CONN. HEADER, 14 PIN, ST.	J4
600190-608-001	CONN, JUMPER, 2 POS.	JP1
600073-403-003	RELAY, DPDT, 5V	K1,2
600080-413-003	PN2222A	Q1,2
600163-413-001	TRANSISTOR 2N2905A	Q3
600082-413-001	TRANSISTOR 2N2219A	Q4
643024-341-075	RES. 43K, 1/4W, 5%	R1,5
610014-341-075	RES. 1K, 1/4W, 5%	R14,17, 22,40
600089-360-010	POT. 10K, 1/2W, CERMET, RT/AN	R15,36
600089-360-014	POT. 100K, 1/2W, CERMET, RT/AN	R16
682024-341-075	RES. 82K, 1/4W, 5%	R19
610024-341-075	RES. 10K, 1/4W, 5%	R2,6,31, 34,35,39 48,50-54 59,61-63 64
620024-341-075	RES. 20K, 1/4W, 5%	R20,29,38
651024-341-075	RES. 51K, 1/4W, 5%	R21
622014-341-075	RES. 2.2K, 1/4W, 5%	R24,44, 45,49
630014-341-075	RES. 3K, 1/4W, 5%	R25
633014-341-075	RES. 3.3K, 1/4W, 5%	R26,27, 30,60
647014-341-075	RES. 4.7K, 1/4W, 5%	R28
620034-341-075	RES. 200K, 1/4W, 5%	R3,4, 9-13, 33,37
668014-341-075	RES. 6.8K, 1/4W, 5%	R32
647004-341-075	RES. 470, 1/4W, 5%	R41
643014-341-075	RES. 4.3K, 1/4W, 5%	R42
610094-341-075	RES. 10, 1/4W, 5%	R43
620094-341-075	RES. 20, 1/4W, 5%	R46,47

PART NUMBER	DESCRIPTION	SYMBOL
620004-341-075	RES. 200, 1/4W, 5%	R55
610004-341-075	RES. 100, 1/4W, 5%	R56,57
633004-341-075	RES. 330, 1/4W, 5%	R58
610034-341-075	RES. 100K, 1/4W, 5%	R7,8, 18,23
600106-340-008	RES. NETWORK 8 PIN, 4.7K	RP3
600244-616-005	DIP SWITCH, SPDT X5	S1
600235-616-010	DIP SWITCH, SPST X10	S2,3
600264-616-001	SWITCH, DIP, 4 POS.	S4
600507-415-101	IC 8279, KEYBD/DISP	U1
600113-415-001	IC 74LS74, DUAL D FLIP-F	U10.11
600392-415-001	IC 74LS221, MONO MLTVB, DUAL	U12
600271-415-001	IC 74LS08, AND, 2-IN QUAD	U13
700101-415-001	IC, X9MME, E2 POT	U14
600219-415-001	IC 74LS33, NOR, 2-IN, QUAD	U15
600411-415-001	IC 741S32, OR, 2-IN	U16
600111-415-001	IC 74LS04, HEX INV	U17
600171-415-001	IC LM324, OP AMP, 741 QUAD	U18-20
600424-415-101	IC 6402, UART, CMOS	U2
700106-415-001	IC, MC3488	U21
700107-415-001	IC, MC3487	U22
700105-415-001	IC, MC3486	U23
700103-415-001	IC, 74HC368	U24
700102-415-001	IC, 74HC367	U25
600617-415-001	IC 8116, BAUD RATE GEN	U3
700104-415-001	IC, ADC0804	U4
600528-415-001	IC 74LS145, BCD TO DECI DEC	U5-7
600998-415-001	IC 74HC4538	U8
600074-415-001	IC NE555, TIMER	U9,26
600170-378-001	CRYSTAL, 5.0688 MHZ	Y1



NOTES:

1. UNLESS OTHERWISE NOTED. ALL RESISTORS ARE IN OHMS, 1/4 W. 5%. CAPACITORS ARE IN MFD. DIODES ARE 1N4148. CR36 AND CR37 ARE 1N4004.

+5V J2-15,17,19,21 — (+5V)

GND J2-1,2,34 —

Figure 4.11-2 (Sheet 1 of 3)

Interface Board Schematic

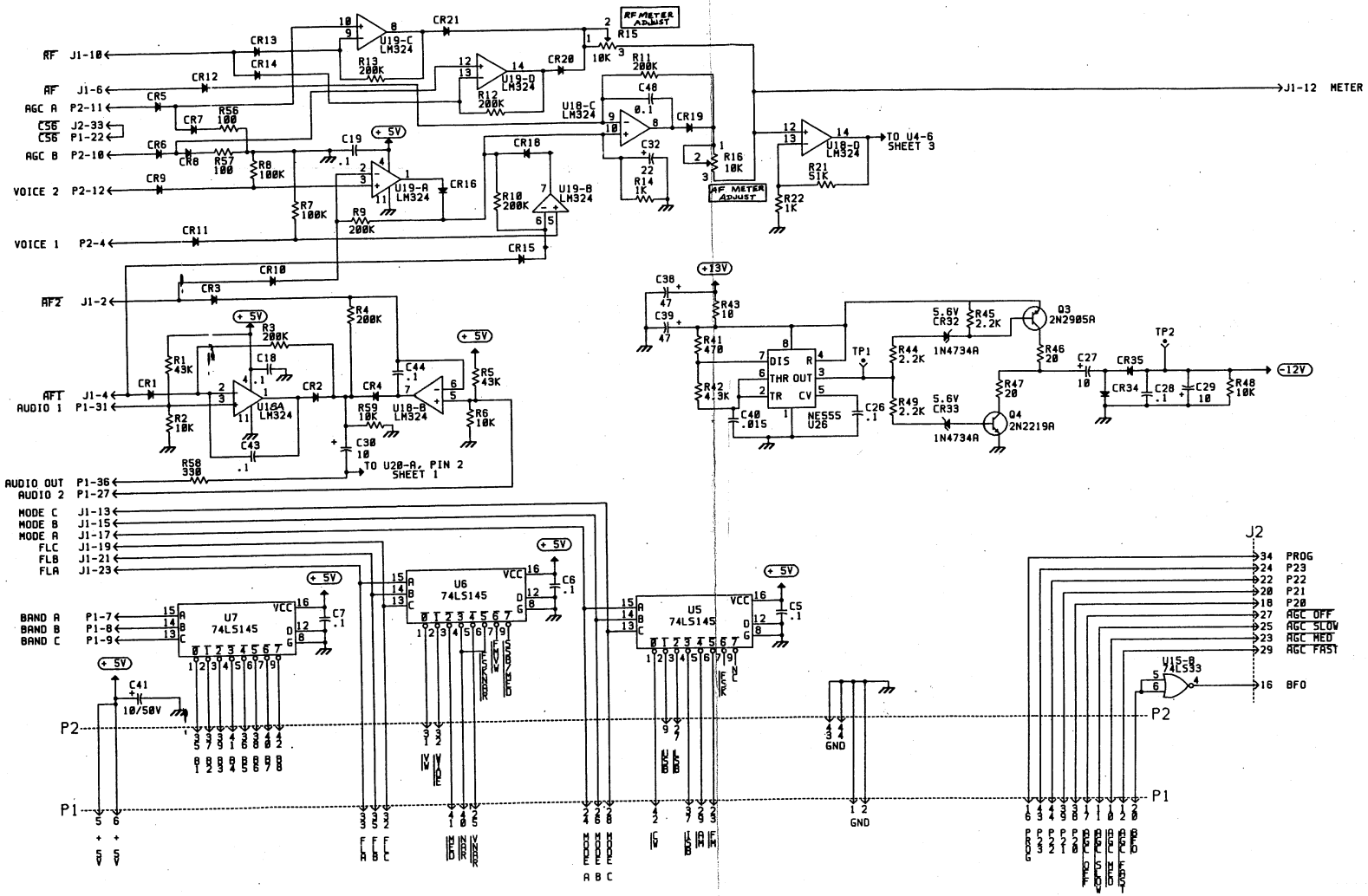


Figure 4.11-2 (Sheet 2 of 3)

Interface Board Schematic

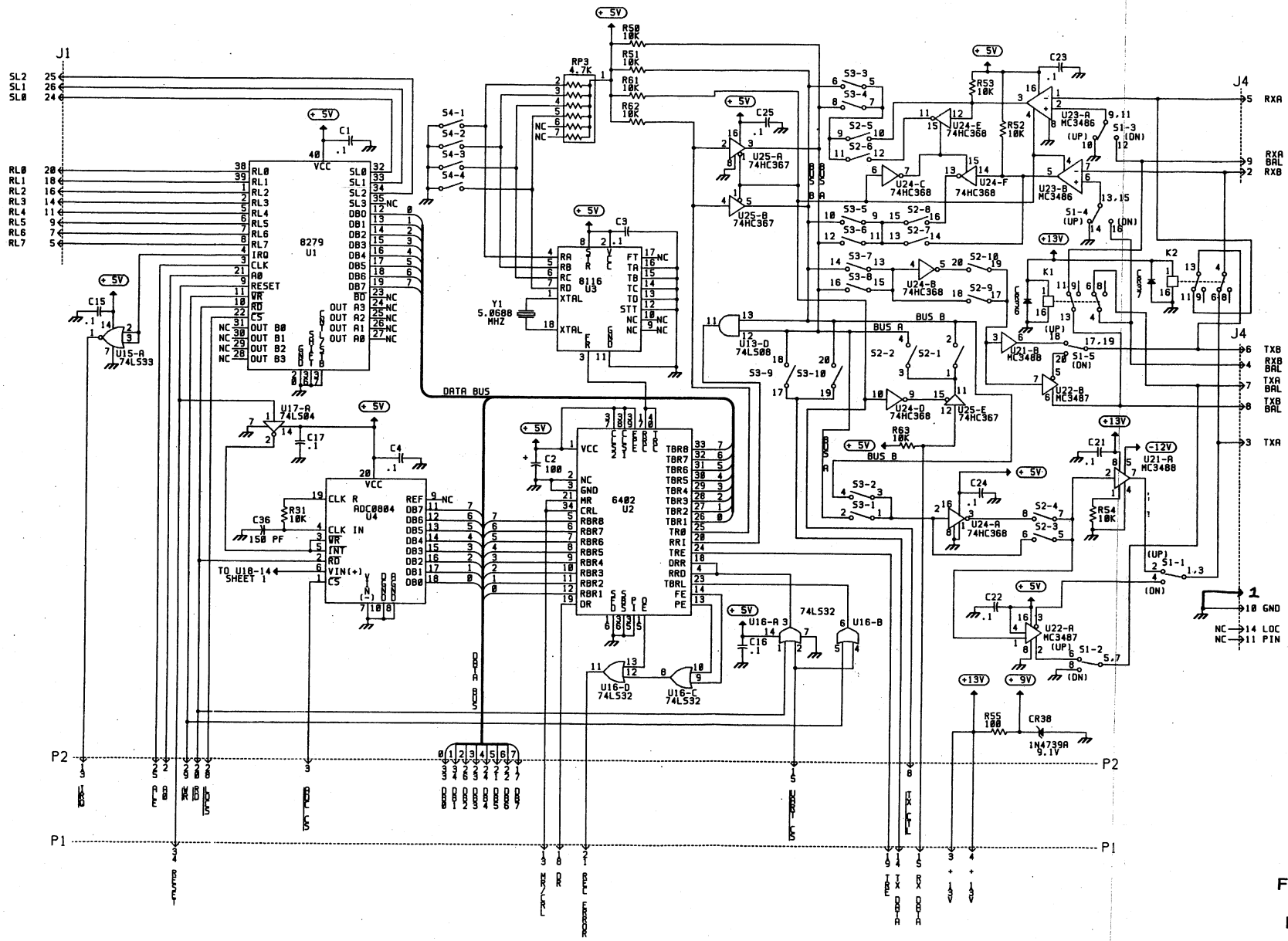


Figure 4.11-2 (Sheet 3 of 3)

Interface Board Schematic

MSR 5050A INTERFACE BOARD A4

PIN CONNECTIONS AND VOLTAGE READINGS

A4P1

	GND	1	2	GND		
	+13 VDC	3	4	+13 VDC		
	+5 VDC	5	6	+5 VDC		
LOGIC "Ø" OR "1"	BAND A	7	8	BAND B	LOGIC "Ø" OR "1"	
LOGIC "Ø" OR "1"	BAND C	9	10	$\overline{\text{AGC MED}}$	LOGIC "Ø" OR "1"	
LOGIC "Ø" OR "1"	$\overline{\text{AGC SLOW}}$	11	12	$\overline{\text{AGC FAST}}$	LOGIC "Ø" OR "1"	
	MR/CTL	13	14	TX DATA		
	RX DATA	15	16	PROG		
LOGIC "Ø" OR "1"	$\overline{\text{AGC OFF}}$	17	18	DR		
	TRE	19	20	$\overline{\text{BFO}}$	LOGIC "Ø" OR "1"	
	REC ERROR	21	22	$\overline{\text{CS6}}$	LOGIC "Ø" OR "1"	
LOGIC "Ø" OR "1"	$\overline{\text{FM}}$	23	24	MODE A	LOGIC "Ø" OR "1"	
LOGIC "Ø" OR "1"	$\overline{\text{VNAR}}$	25	26	MODE B	LOGIC "Ø" OR "1"	
(SPEAKER)	AUDIO 2 IN	27	28	MODE C	LOGIC "Ø" OR "1"	
LOGIC "Ø" OR "1"	$\overline{\text{AM}}$	29	30	SCAN TRIGGER		
(SPEAKER)	AUDIO 1 IN	31	32	FLC	LOGIC "Ø" OR "1"	
LOGIC "Ø" OR "1"	FLA	33	34	RESET		
LOGIC "Ø" OR "1"	FLB	35	36	AUDIO OUT	(SPEAKER)	
LOGIC "Ø" OR "1"	$\overline{\text{ISB}}$	37	38	P20		
	P21	39	40	$\overline{\text{NAR}}$	LOGIC "Ø" OR "1"	
LOGIC "Ø" OR "1"	$\overline{\text{MED}}$	41	42	$\overline{\text{CW}}$	LOGIC "Ø" OR "1"	
	P23	43	44	P22		

MSR 5050A INTERFACE BOARD A4

PIN CONNECTIONS AND VOLTAGE READINGS

A4P2

		1	2	AØ		
LOGIC "Ø" OR "1"	$\overline{\text{AOC CS}}$	3	4	VOICE 1 AUDIO SIGNAL IN (METER)		
LOGIC "Ø" OR "1"	$\overline{\text{INC}}$	5	6	$\overline{\text{UP/DWN}}$	LOGIC "Ø" OR "1"	
0 TO 5 VDC OUT RF GAIN		7	8	$\overline{\text{TX CTL}}$	LOGIC "Ø" OR "1"	
LOGIC "Ø" OR "1"	$\overline{\text{USB}}$	9	10	AGC B	0 TO 6 VDC	
0 TO 6 VDC	AGCA	11	12	VOICE 2 AUDIO SIGNAL IN (METER)		
LOGIC "Ø" OR "1"	$\overline{\text{IRQ}}$	13	14	RF GAIN POT	0 TO 5 VDC IN	
LOGIC "Ø" OR "1"	$\overline{\text{UART CS}}$	15	16	$\overline{\text{SCAN DET}}$	LOGIC "Ø" OR "1"	
	DB7	17	18	DWN	LOGIC "Ø" OR "1"	
LOGIC "Ø" OR "1"	UP	19	20	$\overline{\text{RD}}$	LOGIC "Ø" OR "1"	
	DB5	21	22	DB6		
	DB3	23	24	DB4		
	ALE	25	26	DB2		
LOGIC "Ø" OR "1"	$\overline{\text{LSB}}$	27	28	$\overline{\text{LOCS}}$	LOGIC "Ø" OR "1"	
LOGIC "Ø" OR "1"	$\overline{\text{WR}}$	29	30	REMO	LOGIC "Ø" OR "1"	
LOGIC "Ø" OR "1"	$\overline{\text{VW}}$	31	32	$\overline{\text{WIDE}}$	LOGIC "Ø" OR "1"	
	DBØ	33	34	DB1		
LOGIC "Ø" OR "1"	$\overline{\text{B1}}$	35	36	$\overline{\text{B5}}$	LOGIC "Ø" OR "1"	
LOGIC "Ø" OR "1"	$\overline{\text{B2}}$	37	38	$\overline{\text{B6}}$	LOGIC "Ø" OR "1"	
LOGIC "Ø" OR "1"	$\overline{\text{B3}}$	39	40	$\overline{\text{B7}}$	LOGIC "Ø" OR "1"	
LOGIC "Ø" OR "1"	$\overline{\text{B4}}$	41	42	$\overline{\text{B8}}$	LOGIC "Ø" OR "1"	
	GND	43	44	GND		

MSR 5050A INTERFACE BOARD
A4

PIN CONNECTIONS AND VOLTAGE READINGS

A4J1

	LOC PIN	1	2	$\overline{AF2}$	LOGIC "Ø" OR "1"
		3	4	$\overline{AF1}$	LOGIC "Ø" OR "1"
	RL7	5	6	$\overline{AF}$	LOGIC "Ø" OR "1"
	RL6	7	8	$\overline{SCAN\ ON/OFF}$	LOGIC "Ø" OR "1"
	RL5	9	10	$\overline{RF}$	LOGIC "Ø" OR "1"
	RL4	11	12	METER	0 TO 80 MVDC
LOGIC "Ø" OR "1"	MODE C	13	14	RL3	
LOGIC "Ø" OR "1"	MODE B	15	16	RL2	
LOGIC "Ø" OR "1"	MODE A	17	18	RL1	
LOGIC "Ø" OR "1"	FLC	19	20	RLØ	
LOGIC "Ø" OR "1"	FLB	21	22		
LOGIC "Ø" OR "1"	FLA	23	24	SLØ	
	SL2	25	26	SL1	
		27	28		
		29	30		
		31	32		
		33	34		
		35	36		
		37	38		
		39	40		
		41	42		
		43	44		

MSR 5050A INTERFACE BOARD A4

PIN CONNECTIONS AND VOLTAGE READINGS

A4J2

	GND	1	2	GND		
	GND	3	4	GND		
	NC - SPARE	5	6	NC - SPARE		
	NC - SPARE	7	8	NC - SPARE		
	NC - SPARE	9	10	NC - SPARE		
	NC - SPARE	11	12	NC - SPARE		
	NC - LOC PIN	13	14			
	+5 VDC	15	16	BFO	LOGIC "Ø" OR "1"	
	+5 VDC	17	18	P20		
	+5 VDC	19	20	P21		
	+5 VDC	21	22	P22		
LOGIC "Ø" OR "1"	$\overline{\text{AGC MED}}$	23	24	P23		
LOGIC "Ø" OR "1"	$\overline{\text{AGC SLOW}}$	25	26	SCAN DELAY	Ø to +5 VDC	
LOGIC "Ø" OR "1"	$\overline{\text{AGC OFF}}$	27	28	SCAN RATE	0 to +5 VDC	
LOGIC "Ø" OR "1"	$\overline{\text{AGC FAST}}$	29	30			
LOGIC "Ø" OR "1"	$\overline{\text{REMO}}$	31	32			
LOGIC "Ø" OR "1"	$\overline{\text{CS6}}$	33	34	PROG		
		35	36			
		37	38			
		39	40			
		41	42			
		43	44			

MSR 5050A INTERFACE BOARD A4

PIN CONNECTIONS AND VOLTAGE READINGS

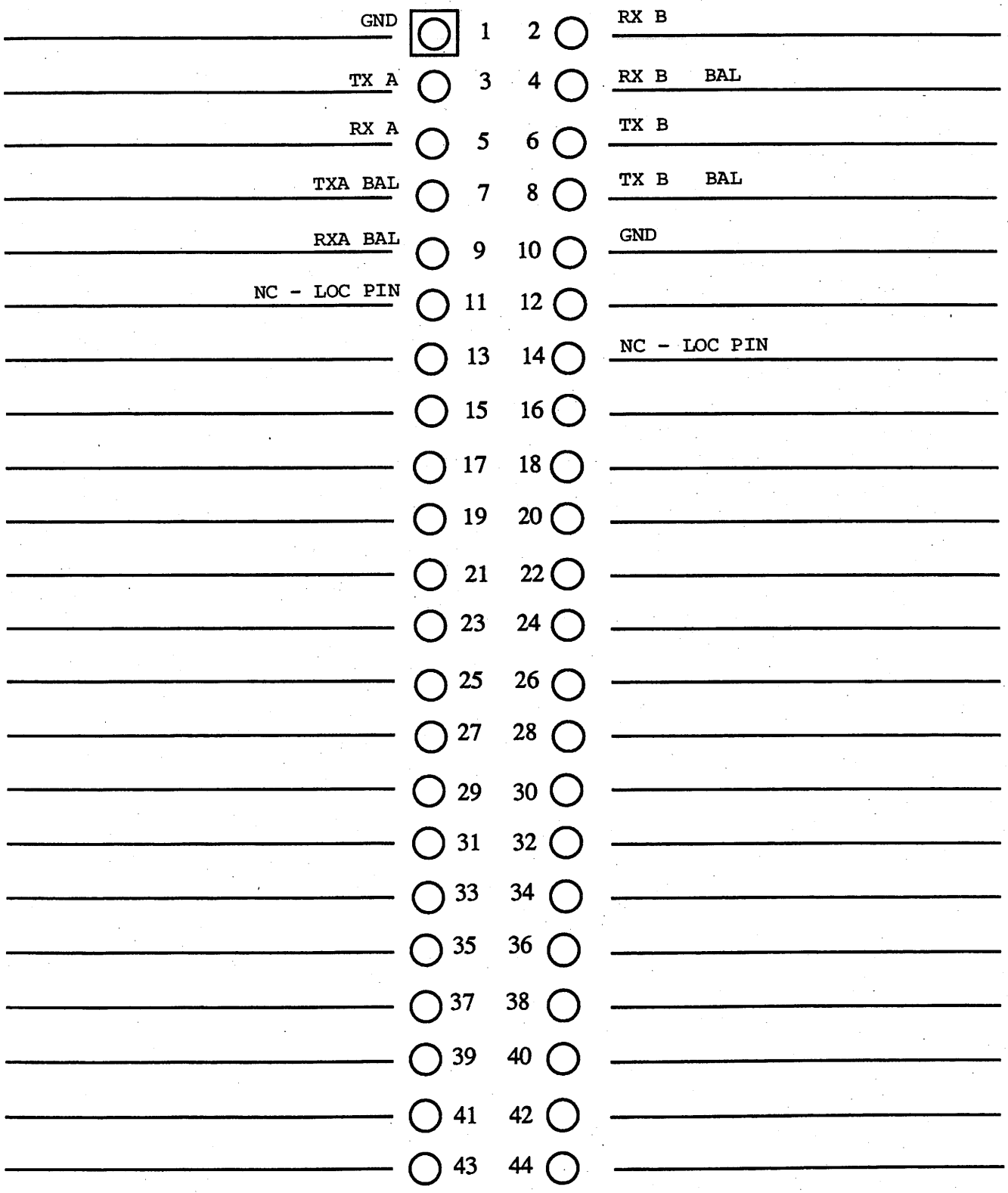
A4J3 (FROM OPTICOUPLER ASSY A1A2 P2)

SIGNAL	1	2	+5 VDC	
GND	3	4		
	5	6	GND	
+5 VDC	7	8	SIGNAL	
	9	10		
	11	12		
	13	14		
	15	16		
	17	18		
	19	20		
	21	22		
	23	24		
	25	26		
	27	28		
	29	30		
	31	32		
	33	34		
	35	36		
	37	38		
	39	40		
	41	42		
	43	44		

MSR 5050A INTERFACE BOARD A4

PIN CONNECTIONS AND VOLTAGE READINGS

A4J4



4.12 LOGIC BOARD, A5

4.12.1 GENERAL DESCRIPTION

This board contains all the circuitry necessary for the control of the 5050A Receiver. An 8035 8-bit microprocessor is used. There are 8k bytes of external ROM for program storage. A 2k byte zero power static RAM is used for data storage. There are six 8243, I/O expander chips, in the system to take care of input and output data. However, only two of them are in this board. An 8214 priority interrupt chip is used to handle the system interrupts. A TL7705 (supply voltage supervisor chip) is used to manage power up and down activity.

4.12.2 MICROPROCESSOR

The 8035 is a 8-bit microprocessor chip that can address up to 4k of external memory directly. Pins 12 through 19 are DB0 through DB7 which are the lower eight bits of address as well as data bus. Port 1, U1-27 through U1-34, is a bi-directional port for data input and output. As output port in address mode, the lower four bits of port 2, U1-21 through 24, are upper four bits of address bus so that 8035 can address up to 2k of external program memory. A software-controlled internal memory band switch can select either MB0 (lower 2k) or MB1 (upper 2k) to make up 4k of total directly addressable memory. /PSEN controls the fetch of instructions from the external memory chips. In I/O expander control mode, these four bits are used in conjunction with PROG (U1-25) signal, for data and command transfer between the processor and the I/O expander.

Other pins of port 2 (U2-35, 36 and 37) are tied to a three to eight decoder chip (74LS138) to select one of six I/O expander chips in the system. U1-11, ALE, is the system clock. It is used to latch the lower eight bits of address to the 8-bit latch U3 during the high to low transition of this signal. The /WR writes data into while the /RD reads from external data memory. T0 and T1 are testable input pins and are used for frequency up and down command in frequency scan mode. T1 is also used to control the channel scan oscillator in channel scan mode. U1-6 is the interrupt input pin. The system will be interrupted and goes to an interrupt routine when it goes low. Y1 is a 6 MHz crystal that controls an on-chip oscillator to generate the 400 kHz system clock ALE. U1-4 is the reset input to provide a system reset whenever it goes low.

4.12.3 INTERRUPT INTERFACE

U2 is an 8214 priority interrupt chip that interfaces with the external interrupt inputs. Priority can be assigned by software. A system interrupt will be generated when an interrupt with level higher than the assigned level is arrived. If there are more than one legal interrupts arriving at the same time, the one with the higher level will be processed first. U2-21 is the /IRQ input which will go low when key closure is detected. /IRQ has the highest priority assigned. U2-17 is Loss of Lock Bite input and U2-16 is Power Supply Bite input that will go low when these failures occur.

4.12.4 MEMORY

4.12.4.1 Program Memory

Two 2732A 4k ROMs (U4 and U15) are used to store instructions for the system control. These two chips are connected in parallel with the processor. A memory chip select signal (U1-31) is provided to select either memory chip 1 (U4) or memory chip 2 (U15). This memory chip select signal determines whether instruction is fetched from U4 (lower 4k) or U15 (upper 4k).

4.12.4.2 Data Memory

Zero power static RAM (U16), Priority Interrupt chip (U2), Keypad chip (U1) and UART chip (U2 in the Interface board) are considered external data memory chips in this system. Selection of these chips is controlled by U1-27, 28 and 29 that tie to the input of a three to eight decoder chip (U9). Output of U9 enables one of these chips. Status of the receiver and channel data is stored in U16. Data stored will be retained, due to the built-in battery, inside the MK48Z02 chip even with Vcc removed from this chip. Since 8035 can address only 256 bytes of external RAM, P16 and P17 (U1-33 and 34) are used to select four pages

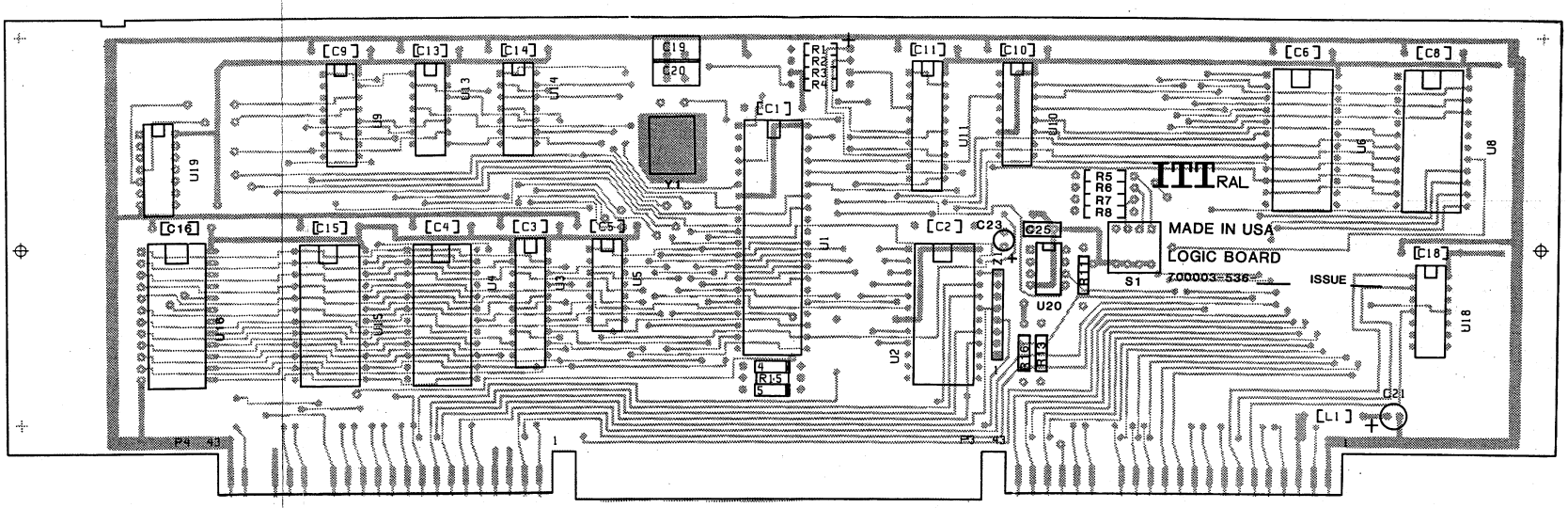
of RAM locations to address up to 1k byte of external RAM. U9-14 provides the MSB of address for the RAM to enable the processor to address up to 2k of external RAM.

4.12.5 I/O EXPANDER

There are six I/O Expander chips (8243) in the system. U6 and U8 are the only two located in this board. Each chip has four 4-bit ports that can be used as input or output port. U6 and U8 pins 11, 10, 9, 8 and 7 are tied to P20 through P23 and PROG pin of the processor for command and data transfer. U6, port 4, (U6-2, 3, 4 and 5) is used as an input port for option selection. When the input pin is low, the option is selected. U6 is selected if U10-11 is low. U8 is selected when U10-12 is low. U10-15, 14, 13 and 10 will select I/O chip CS1, CS2 CS3 and CS6, respectively, located in other boards.

4.12.6 POWER ON RESET

A TL7705 (Supply Voltage Supervisor) is used to handle the power up system reset. This chip will hold the /RESET low when supply voltage reaches 3.6 volts and starts a pre-determined delay period after Vcc reaches 4.5V for the normal microprocessor reset. The value of C23 is selected so that the period is 130 ms. U20-6 (RESET) is the complement output of U20-5 which will stay high for 130 ms after Vcc reaches 4.5V. When the supply voltage drops below 4.5V, /RESET output will go to logic low and stay low for 130 ms when Vcc is recovered back to 4.5V.



PROGRAM CHIPS

U4	PROG IC	700001-412-001
U15	PROG IC	700001-412-002

Logic (700003-536-951)

PART NUMBER	DESCRIPTION	SYMBOL
600119-419-040	IC SOCKET, 40 POS.	(U1)
600272-314-001	CAP. .1UF, CERAMIC, 50V	C1-6, 8-11, 13-16 18
620094-306-501	CAP. 20PF, 5%, MICA, 500V	C19,20
600297-314-016	CAP. 22UF, ALUM, 25V	C21
600202-314-018	CAP. 10UF, 25V, TANT.	C23
600302-314-013	CAP. .1UF, MYLAR, 50V	C25
600052-410-001	DIODE IN270	CR4,5
600125-376-001	CHOKE .33UH	L1
647014-341-075	RES. 4.7K, 1/4W, 5%	R1-8,15,16
622014-341-075	RES. 2.2K, 1/4W, 5%	R11
610014-341-075	RES. 1K, 1/4W, 5%	R13
600264-616-001	SWITCH, DIP, 4 POS.	S1
600218-415-002	IC 8035, UP, 8-BIT	U1
600311-415-001	IC 74LS241, BUF/LN DR	U11
600411-415-001	IC 74LS32, OR, 2-IN	U13
600114-415-001	IC 74LS00, NAND, QUAD 2-IN	U14,U19
600990-415-001	IC MK 48Z02-25, RAM	U16
600016-415-001	IC 7406, HEX INV. ,O/C	U18
600519-415-001	IC 8214, PRIR INT CNTL	U2
600119-419-024	IC SOCKET, 24 POS.	(U2,4,6,8, 15,16)
700123-415-001	I.C. TL7705A	U20
600277-415-002	IC 74LS273 SIG, FF W/CLR	U3
600111-415-001	IC 74LS04, HEX INV	U5
600217-415-101	IC 8243, I/O EXP	U6,8
600309-415-001	IC 74LS138, 3 TO 8 LN DEC/MUX	U9,10
600105-378-001	CRYSTAL, 6.00 MHZ	Y1
600201-537-001	RES NETWORK 4.7K X 7	Z1

Figure 4.12-1

Logic Board Assembly

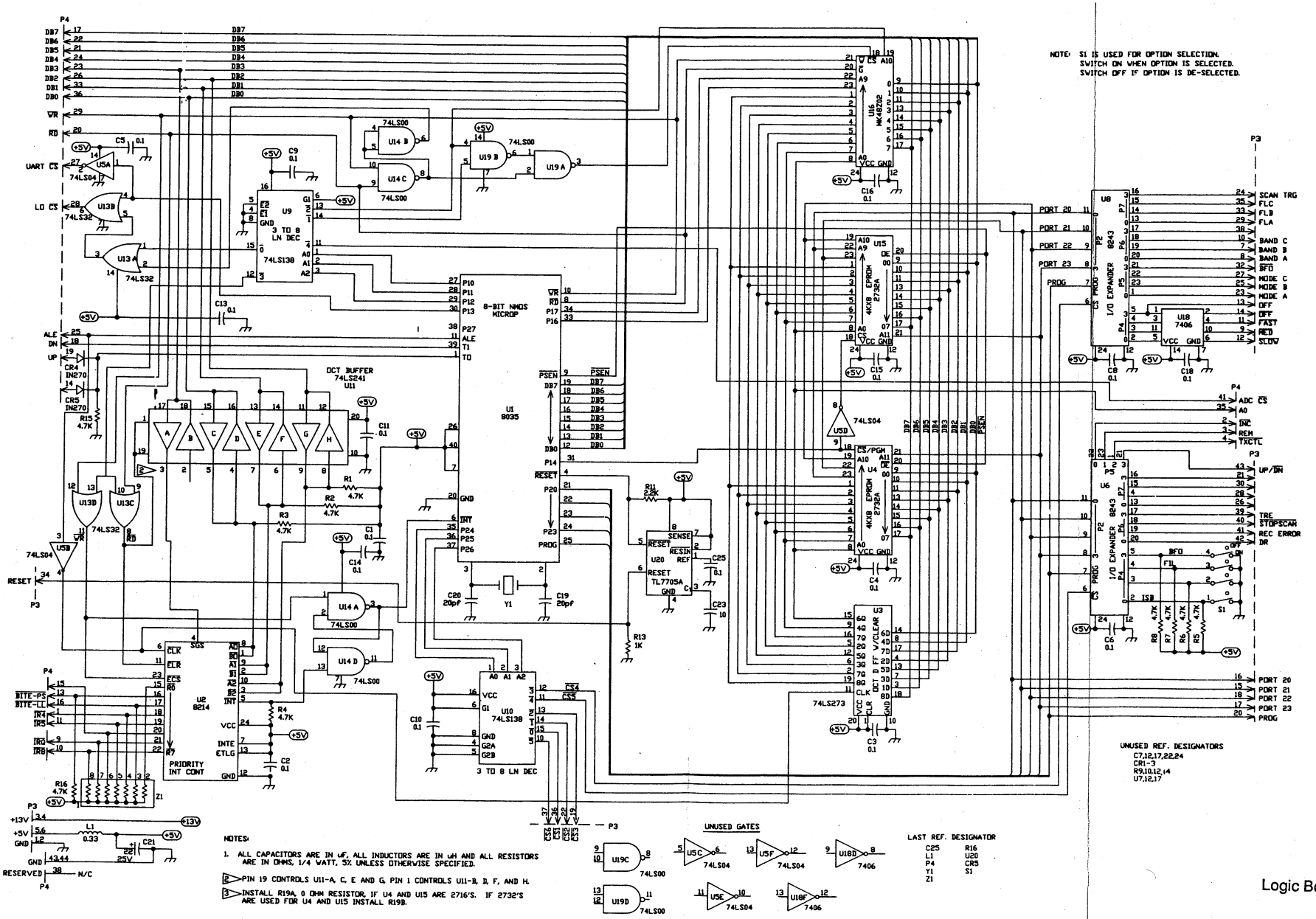


Figure 4.12-2

Logic Board Schematic

MSR 5050A LOGIC BOARD A5

PIN CONNECTIONS AND VOLTAGE READINGS

A5P3 (TO MOTHER BOARD A2P3)

	GND	1	2	GND	
	+13 VDC	3	4	+13 VDC	
	+5 VDC	5	6	+5 VDC	
LOGIC "Ø" or "1"	BAND B	7	8	BAND A	LOGIC "Ø" or "1"
LOGIC "Ø" or "1"	$\overline{\text{MED}}$	9	10	BAND C	LOGIC "Ø" or "1"
LOGIC "Ø" or "1"	$\overline{\text{FAST}}$	11	12	$\overline{\text{SLOW}}$	LOGIC "Ø" or "1"
LOGIC "Ø" or "1"	$\overline{\text{OFF}}$	13	14	$\overline{\text{OFF}}$	LOGIC "Ø" or "1"
	PORT 21	15	16	PORT 20	
	PORT 23	17	18	PORT 22	
LOGIC "Ø" or "1"	$\overline{\text{CS3}}$	19	20	PROG	
	SPARE	21	22	$\overline{\text{CS2}}$	LOGIC "Ø" or "1"
LOGIC "Ø" or "1"	MODE A	23	24	SCAN TRG	LOGIC "Ø" or "1"
LOGIC "Ø" or "1"	MODE B	25	26	SPARE	
LOGIC "Ø" or "1"	MODE C	27	28	SPARE	
LOGIC "Ø" or "1"	FLA	29	30	SPARE	
	NC - SPARE	31	32	$\overline{\text{BFO}}$	LOGIC "Ø" or "1"
LOGIC "Ø" or "1"	FLB	33	34	RESET	LOGIC "Ø" or "1"
LOGIC "Ø" or "1"	FLC	35	36	$\overline{\text{CS1}}$	LOGIC "Ø" or "1"
LOGIC "Ø" or "1"	$\overline{\text{CS6}}$	37	38	NC	
LOGIC "Ø" or "1"	TRE	39	40	$\overline{\text{STOP SCAN}}$	LOGIC "Ø" or "1"
LOGIC "Ø" or "1"	REC ERROR	41	42	DR	LOGIC "Ø" or "1"
LOGIC "Ø" or "1"	UP/$\overline{\text{DN}}$	43	44		

MSR 5050A LOGIC BOARD A5

PIN CONNECTIONS AND VOLTAGE READINGS

A5P4 (TO MOTHER BOARD A2J4)

LOGIC "Ø" OR "1"	$\overline{IR4}$	1	2	$\overline{INC}$	LOGIC "Ø" OR "1"
LOGIC "Ø" OR "1"	REM	3	4	$\overline{TX\ CTL}$	LOGIC "Ø" OR "1"
		5	6		
		7	8		
LOGIC "Ø" OR "1"	$\overline{IRQ}$	9	10	$\overline{IR8}$	LOGIC "Ø" OR "1"
LOGIC "Ø" OR "1"	$\overline{IR5}$	11	12		
LOGIC "Ø" OR "1"	$\overline{BITE - PS}$	13	14		
		15	16	$\overline{BITE - LL}$	LOGIC "Ø" OR "1"
	DB7	17	18	DN	LOGIC "Ø" OR "1"
LOGIC "Ø" OR "1"	UP	19	20	$\overline{RD}$	LOGIC "Ø" OR "1"
	DB5	21	22	DB6	
	DB3	23	24	DB4	
LOGIC "Ø" OR "1"	ALE	25	26	DB2	
LOGIC "Ø" OR "1"	$\overline{UART\ CS}$	27	28		
LOGIC "Ø" OR "1"	$\overline{WR}$	29	30		
		31	32		
	DB1	33	34		
LOGIC "Ø" OR "1"	A0	35	36	DBØ	
		37	38	RESERVED - NC	
		39	40		
LOGIC "Ø" OR "1"	ADC $\overline{CS}$	41	42		
	GND	43	44	GND	

4.13 LOW PASS FILTER BOARD, A6

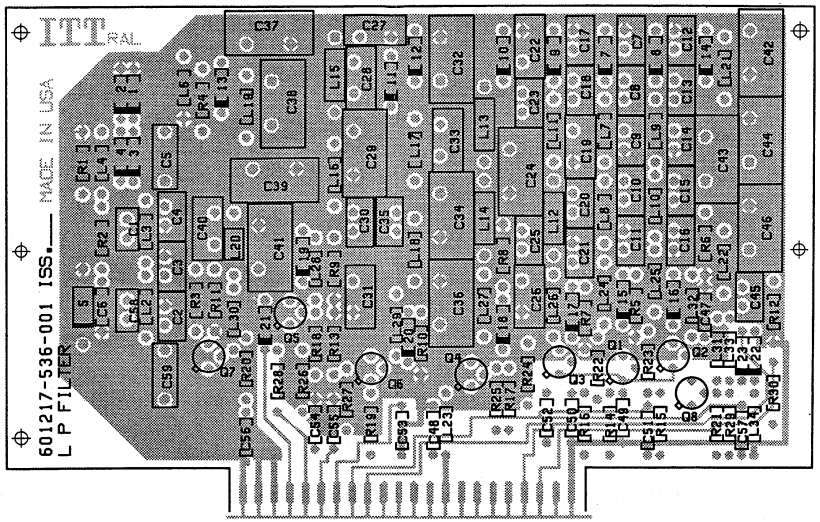
4.13.1 GENERAL

The LP Filter board contains in series: a 10-watt input protection circuit, a 30 MHz low pass filter and a parallel bank of eight selectable low pass filters with cutoff frequencies of 2, 3, 4, 6, 9, 13, 20 and 30 MHz corresponding to bands one through eight, respectively. The LP Filter board is cascaded with a High Pass Filter with complementing cutoff frequencies to produce a selectable band pass response in bands two through eight. The output of the LP Filter (pin 37) feeds the HP Filter whose output is returned to the LP Filter on pin 7. The cascaded output then is routed to the Mixer through CR23 which is always on as long as any band from two to eight is selected. To allow response down to 10 kHz, the HP Filter is bypassed in band one by connecting the output of the two MHz LP filter directly to the Mixer board (pin 5) via CR22 with the HP Filter isolated by CR23, being off. Each filter is a 7-element, elliptic, low pass design with a 35 dB design stop band. Insertion loss, designed for 0.1 dB at the cutoff frequency, is allowed two dB for component Q and manufacturing tolerances.

4.13.2 DETAILED CIRCUIT DESCRIPTION

Band eight is switched by pin diodes CR7 and CR15. When a logic 0 is applied to pin 30, Q1 is saturated and nine volts appear on Q1 collector causing current flow through L24, L7, L8, CR7, CR15, R4, L6, L32, L33, CR23, R30 and L34. The voltage developed across R4 back-biases CR8 through CR14 in the other filters. The voltage across R30 back-biases CR16 through CR22 in the other filters. The selection of bands two through seven are similar with the selected filter output going to pin 37 to a High Pass Filter board whose output is brought back to the low pass filter on pin seven. Forward-biased CR23 conducts the signal to the combined filter output on pin 5. L32 and L33 isolate the RF signal at pin 5 from that at pin 7. When band one is selected by a ground at pin 27, CR22 is biased on, connecting the band one filter output directly to pin 5. The resulting voltage drop across R30 isolates the high pass filter signal at pin 7 by the reverse bias on CR23.

The RF input to the board on pin 42 goes through a 7-element, 35 MHz low pass elliptic filter (C2, L3, C1-4 and C58) to reach the bank of eight filters via C5. A voltage protection circuit at C5, consisting of pin diodes CR1-4 and associated bias circuit, clips input waveforms above a peak-to-peak level of 6.8 volts. The series combination of CR3/CR4 and CR1/CR2 is back-biased 5.6V by the zener voltage of CR5 with the center point at 2.8V by the divider action of R1 and R2. The negative peaks of the input signal are clamped to ground by CR1/CR2. The positive peaks above 5.6V (plus two diode drops) cause CR3/CR4 to conduct through the near-RF-short of C6 and C49 with residual rectified current dissipated by CR5. The output is then limited to a nominal +20 dBm.



Low Pass Filter (601217-536-001)

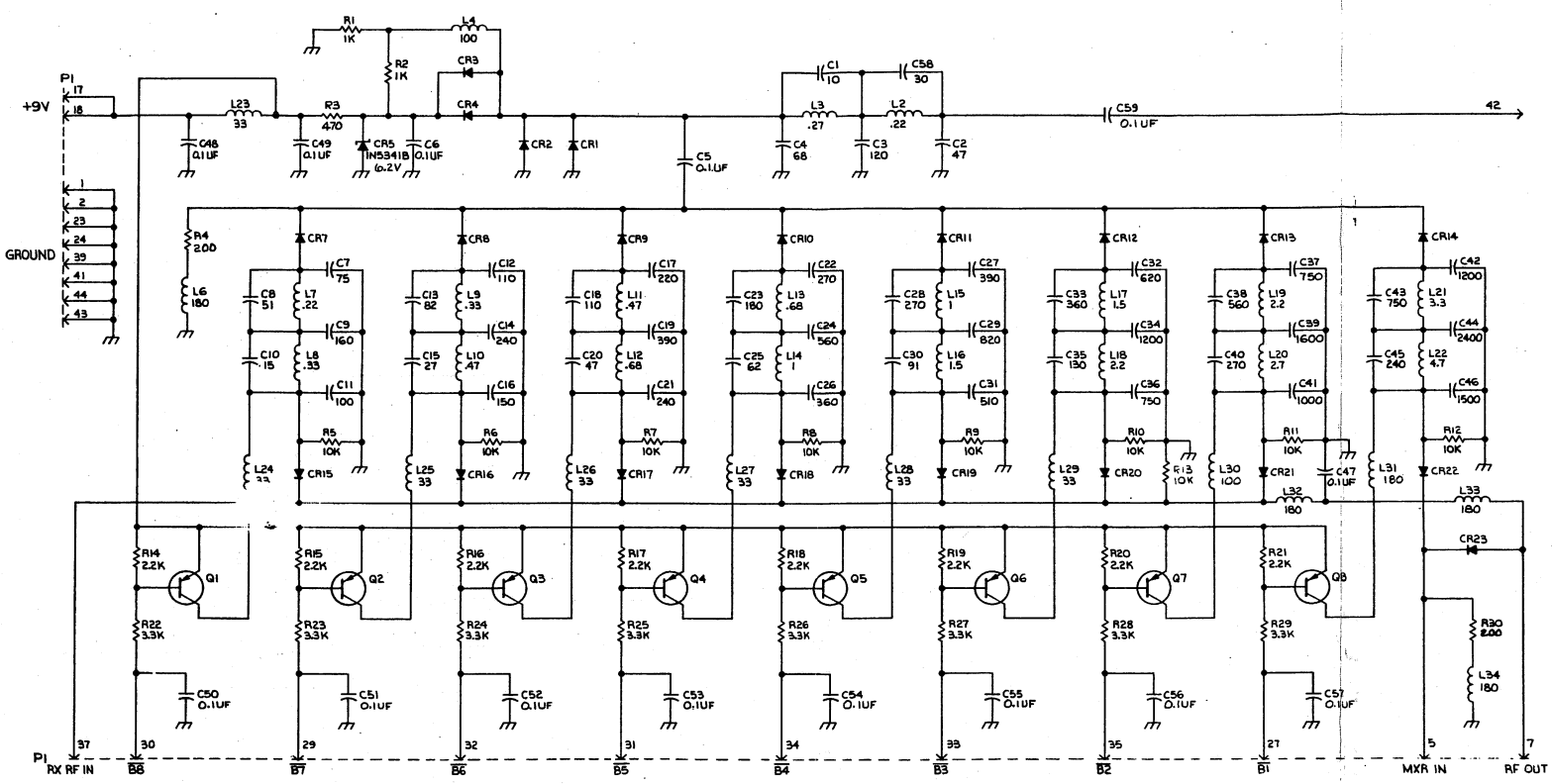
PART NUMBER	DESCRIPTION	SYMBOL
610093-306-501	CAP. 10PF, 3%, MICA, 500V	C1
615093-306-501	CAP. 15PF, 3%, MICA, 500V	C10
610003-306-501	CAP. 100PF, 3%, MICA, 500V	C11
611003-306-501	CAP. 110PF, 3%, MICA, 500V	C12,18
682093-306-501	CAP. 82PF, 3%, MICA, 500V	C13
624003-306-501	CAP. 240PF, 3%, MICA, 500V	C14,21, 45
627093-306-501	CAP. 27PF, 3%, MICA, 500V	C15
615003-306-501	CAP. 150PF, 3%, MICA, 500V	C16
622003-306-501	CAP. 220PF, 3%, MICA, 500V	C17
639003-306-501	CAP. 390PF, 3%, MICA, 500V	C19,27
647093-306-501	CAP. 47PF, 3%, MICA, 500V	C2,20
627003-306-501	CAP. 270PF, 3%, MICA, 500V	C22,28, 40
618003-306-501	CAP. 180PF, 3%, MICA, 500V	C23
656003-306-501	CAP. 560PF, 3%, MICA, 500V	C24,38
662093-306-501	CAP. 62PF, 3%, MICA, 500V	C25

PART NUMBER	DESCRIPTION	SYMBOL
636003-306-501	CAP. 360PF, 3%, MICA, 500V	C26.33
682003-306-501	CAP. 820PF, 3%, MICA, 500V	C29
612003-306-501	CAP. 120PF, 3%, MICA, 500V	C3
691093-306-501	CAP. 91PF, 3%, MICA, 500V	C30
651003-306-501	CAP. 510PF, 3%, MICA, 500V	C31
662003-306-501	CAP. 620PF, 3%, MICA, 500V	C32
612013-306-501	CAP. 1200PF, 3%, MICA, 500V	C34,42
613003-306-501	CAP. 130PF, 3%, MICA, 500V	C35
675003-306-501	CAP. 750PF, 3%, MICA, 500V	C36,37, 43
616013-306-501	CAP. 1600PF, 3%, MICA, 500V	C39
668093-306-501	CAP. 68PF, 3%, MICA, 500V	C4
610013-306-501	CAP. 1000PF, 3%, MICA, 500V	C41
624013-306-501	CAP. 2400PF, 3%, MICA, 500V	C44
615013-306-501	CAP. 1500PF, 3%, MICA, 500V	C46
600204-314-020	CAP. 0.1UF, MYLAR, 100V	C5,59
630093-306-501	CAP. 30PF, 3%, MICA, 500V	C58

PART NUMBER	DESCRIPTION	SYMBOL
600272-314-001	CAP. .1UF, CERAMIC, 50V	C6,47-57
675093-306-501	CAP. 75PF, 3%, MICA, 500V	C7
651093-306-501	CAP. 51PF, 3%, MICA, 500V	C8
616003-306-501	CAP. 160PF, 3%, MICA, 500V	C9
600144-410-001	DIODE HP3188	CR1-4, 7-23
600026-411-009	DIODE, ZENER, IN5341A 6.2V	CR5
600125-376-027	CHOKE .47UH	L10,11
600192-376-006	COIL, .68UH	L12,13
600192-376-008	COIL, 1.00UH	L14,15
600125-376-033	CHOKE 1.5 UH	L16,17
600125-376-016	CHOKE 2.2UH	L18,19
600125-376-003	CHOKE .22UH	L2,7
600121-376-016	CHOKE 2.7UH	L20
600125-376-006	CHOKE 3.3UH	L21
600125-376-030	CHOKE 4.7UH	L22
600125-376-007	CHOKE 33UH	L23-29
600125-376-037	CHOKE .27UH	L3
600125-376-002	CHOKE 100UH	L4,30
600125-376-022	CHOKE 180UH	L6.31-34
600125-376-001	CHOKE .33UH	L8,9
600154-413-001	TRANSISTOR 2N2907A	Q1-8
610014-341-075	RES. 1K, 1/4W, 5%	R1,2
622014-341-075	RES. 2.2K, 1/4W, 5%	R14-21
633014-341-075	RES. 3.3K, 1/4W, 5%	R22-29
647004-341-075	RES. 470, 1/4W, 5%	R3
620004-341-075	RES. 200, 1/4W, 5%	R4,R30
610024-341-075	RES. 10K, 1/4W, 5%	R5-13

Figure 4.13-1

Low Pass Filter Assembly



NOTES

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS RATED IN OHMS, 1/4W, 5%
   ALL CAPACITORS RATED IN PICOFARADS
   ALL INDUCTORS RATED IN MICROHENRYS
   ALL TRANSISTORS ARE 2N2907A
   ALL DIODES ARE HP5082-3188

LAST REF. DESIGNATOR	
C59	Q8
CR23	R30
L34	

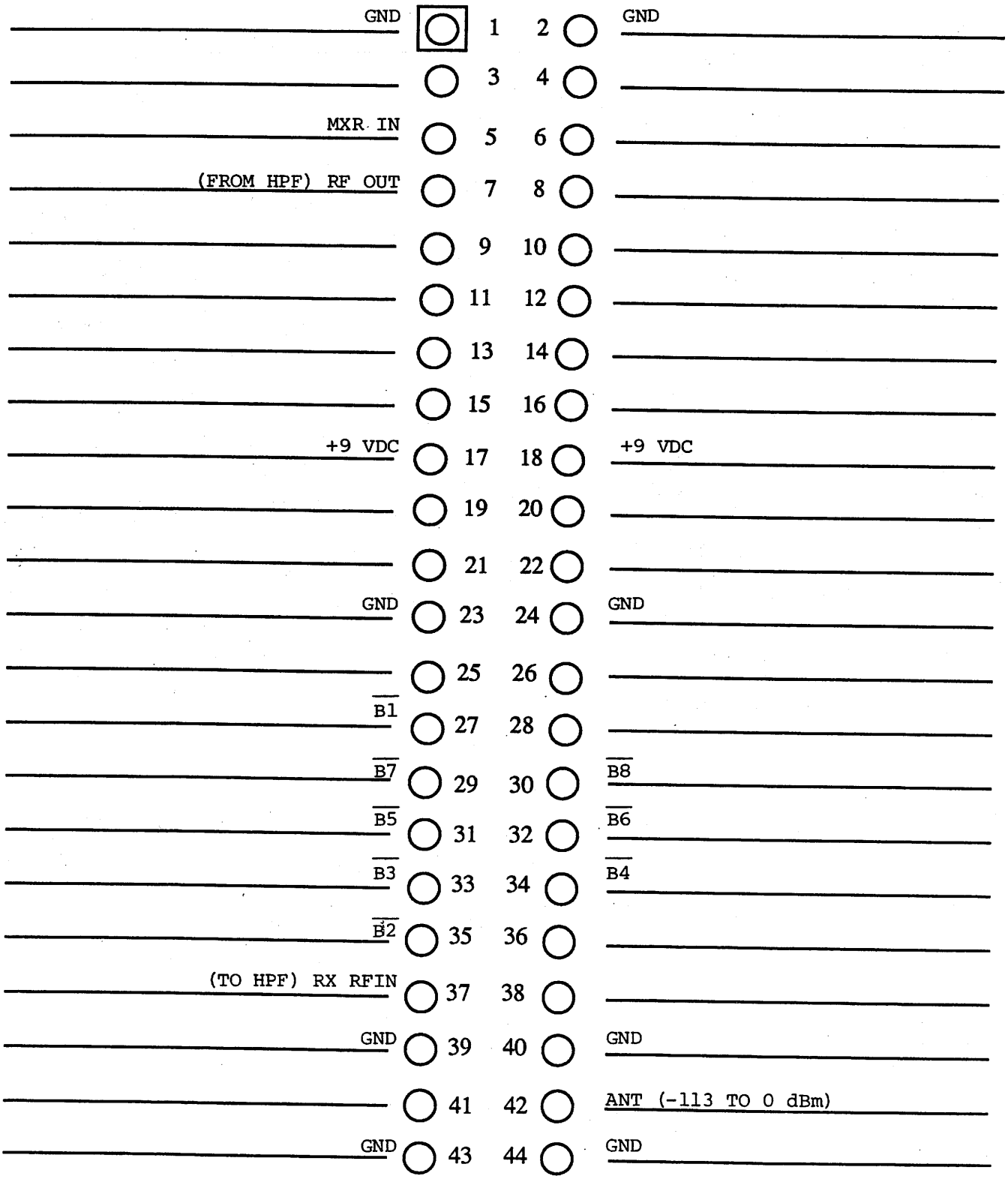
Figure 4.13-2

Low Pass Filter Schematic

LOW PASS FILTER BOARD A6

PIN CONNECTIONS AND VOLTAGE READINGS

A6P1



4.14 HIGH PASS FILTER BOARD, A7

The High Pass Filter board contains eight 1/2 octave high pass filters (elliptic design). The cut-off frequencies are approximately 1.6, 2, 3, 4, 6, 9, 13 and 20 MHz. The stop band attenuation of these filters is 35 dB. The filters are switched with diodes and transistors. The board also contains a broadcast filter and an RF amplifier, used in the receive mode. The board is also used in transmitter applications in the MSR 6700A, MSR 8050 and MSR 8050A. Four potentiometers are used to provide a band switch analog voltage for A3A operation (used in transmit only). A transmit/receive relay (K1) is used to bypass the broadcast filter and RF amplifier in the transmit mode. A filter bypass relay (K2) is used to bypass all High Pass Filter board functions in receive modes below 1.6 MHz when used in the MSR 8050, 8050A.

4.14.1 HIGH PASS FILTERS

Band 1 (B1) is switched by CR1 and CR2. When a logic 0 (ground) is placed on pin 41, Q6 is saturated and 9V appears on the collector of Q6. This voltage causes current to flow through L19, L20, CR1, L18, R50, CR2, L15 and R20. CR1 and CR2 conduct, and all the other band switching diodes (CR3 and 4, CR5 and 6, etc.) are back biased. If band 1 is selected in receive, the signal flow is as follows: Input on pin 42 through K2 (pins 11 and 13), K1 (pins 4 and 6), C106, CR1, C44, C45, C46, CR2 and K1 (pins 11 and 13), and through C27 to the broadcast filter. The RF amplifier provides about 8 dB of gain (1.6 to 30 MHz). The output is taken from T1 through K2 (pins 4 and 6) to pin 11 of P14. Operation of any other band is similar. During the transmit mode, K1 is energized and the signal flow is as follows: Input on pin 5 through K1 (pins 9 and 13), through the band selected, through K1 (pins 4 and 8), and out on pin 21. The maximum receive level is 2V RMS and the transmit level is 3 volts peak to peak.

4.14.2 RF AMPLIFIER

The RF amplifier consists of Q4 and Q5. Q4 and A5 are high level FETs used in the grounded gate configuration for best intermodulation performance.

4.14.3 TRANSMIT SWITCH

Q2 is a switch used to pull in K1 when in the transmit mode. When a ground (logic 0) is placed on pins 7 and 8, the collector of Q2 pulls in K1. Q2's collector voltage is also connected to the solid-state PA to switch the PA biases on during transmit.

4.14.4 A3A CONTROL VOLTAGE

When the A3A transmit mode is desired, a band switched analog voltage is required. The A3A control voltage consists of R8, R9, Q3 and R49. When A3A is desired, a ground is placed on pin 31. This cuts off Q3, allowing the voltage on R10 to appear on pin 9. Pin 9 is connected to the Transmit Modulator board and allows some carrier (-16 to -18 dB) to be inserted in the A3A mode. If band 1 or 2 is selected, CR33 or CR34 conducts, causing 9V to be applied across R49. R49 is adjusted to provide the proper amount of carrier for 1.6 to 3 MHz (bands 1 and 2). In a similar manner, R48 is adjusted for 3 to 9 MHz (bands 3 to 6), R47 is adjusted for 13 to 20 MHz (band 7), and R46 is adjusted for 20 to 30 MHz (band 8).

4.14 5 OVERALL GAIN OR LOSS

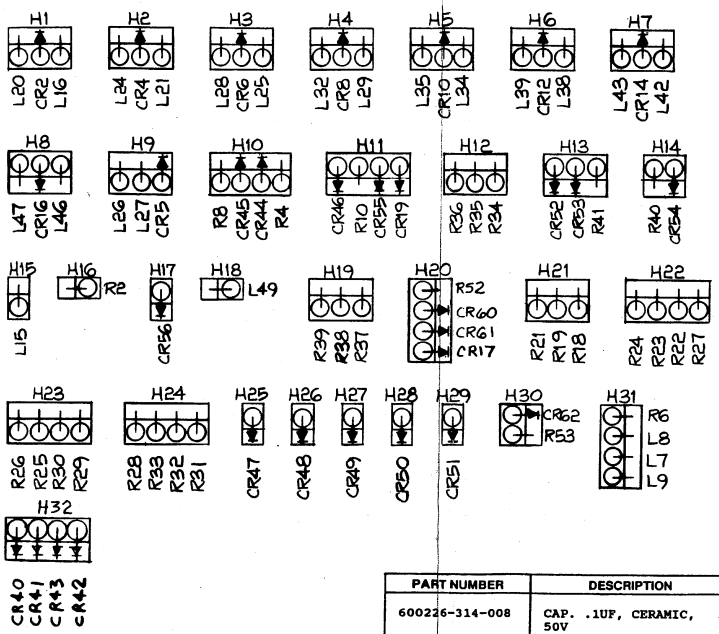
In the receive mode, the overall gain is +4 dB to +8 dB, depending on the band selected. In transmit modes, the loss is -1 dB to -2 dB.

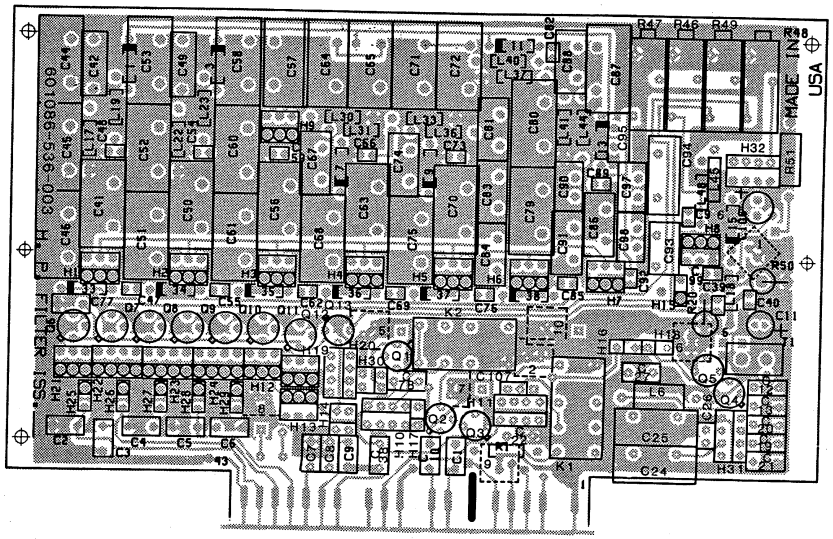
4.14.6 BROADCAST FILTER

The broadcast filter is used only in receive modes at frequencies above 1.6 MHz and provides approximately 35 dB additional attenuation to the broadcast band. The overall rejection of the broadcast band is approximately 70 dB (6 dB cutoff frequency approximately 1.4 kHz).

4.14.7 HF FILTER BYPASS

The high pass filter bypass mode is used to route receive signals directly through the board, bypassing all filter circuitry. This is required for the reception of signals below 1.6 MHz. When in receive mode and below 1.6 MHz, a low (ground) on pin 40 turns on Q1, which switches in K2. The signal path is now: Input on pins 42 through K2 (pins 13 and 9), then through the other half of K2 (pins 8 and 4), then out on P14 (pin 11).





High Pass Filter (601086-536-003)

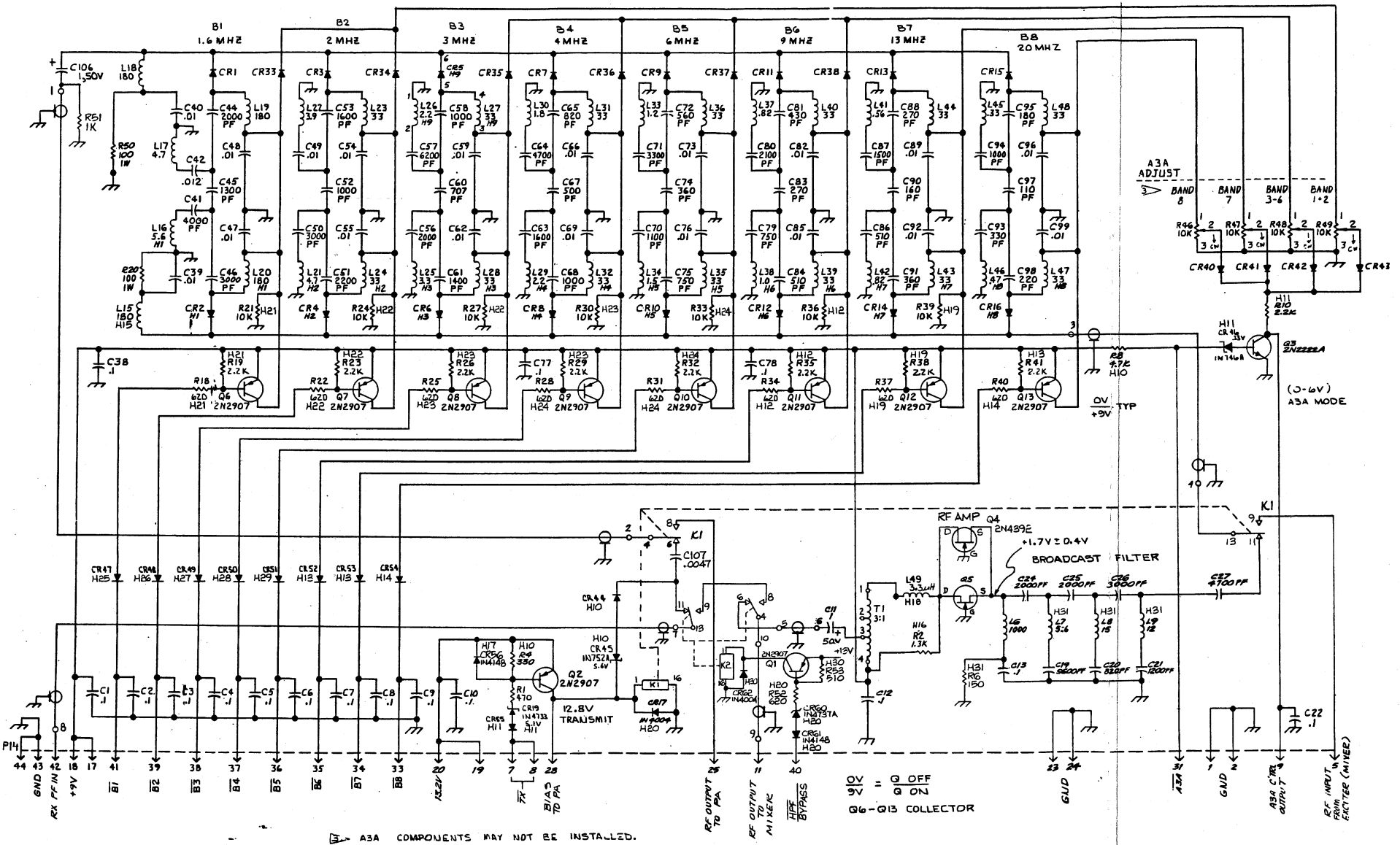
PART NUMBER	DESCRIPTION	SYMBOL
600226-314-008	CAP. .1UF, CERAMIC, 50V	C1-10.12 13,22, 38,77
600268-314-007	CAP. .0047UF, CERAMIC, 50V	C107
600297-314-003	CAP. 1UF, ALUM, 50V	C11,106
600369-314-562	CAP. 5600PF, CERAMIC, 100V	C19
600369-314-821	CAP. 820PF, CERAMIC, 100V	C20
600369-314-122	CAP. 1200PF, CERAMIC, 100V	C21
620013-306-501	CAP. 2000PF, 3%, MICA, 500V	C24.25 44,56
600265-314-026	CAP. 3000PF, CERAMIC, 100V	C26
600369-314-472	CAP. 4700PF, CERAMIC, 100V	C27
600268-314-008	CAP. .01UF, CERAMIC, 50V	C39,40, 47,48, 54,55
640011-306-501	CAP. 4000PF, 1%, MICA, 500V	C41
600204-314-022	CAP. .012UF, MYLAR, 400V	C42
613014-306-501	CAP. 1300PF, 5%, MICA, 500V	C45
630014-306-501	CAP. 3000PF, 5%, MICA, 500V	V46,50
600204-314-001	CAP. .01UF, MYLAR, 400V	C49
622014-306-501	CAP. 2200PF, 5%, MICA, 500V	C51
610013-306-501	CAP. 1000PF, 3%, MICA, 500V	C52.58 68,94
616013-306-501	CAP. 1600PF, 3%, MICA, 500V	C53,63
622014-306-501	CAP. 2200PF, 5%, MICA, 500V	C57
600268-314-008	CAP. .01UF, CERAMIC, 50V	C59,62, 66,69, 73,76
670703-306-501	CAP. 707PF, 3%, MICA, 500V	C60
614013-306-501	CAP. 1400PF, 3%, MICA, 500V	C61
647014-306-501	CAP. 4700PF, 5%, MICA, 500V	C64
682003-306-501	CAP. 820PF, 3%, MICA, 500V	C65
650001-306-501	CAP. 500PF, 1%, MICA, 500V	C67
611013-306-501	CAP. 1100PF, 3%, MICA, 500V	C70

PART NUMBER	DESCRIPTION	SYMBOL
633014-306-501	CAP. 3300PF, 5%, MICA, 500V	C71
656003-306-501	CAP. 560PF, 3%, MICA, 500V	C72
636003-306-501	CAP. 360PF, 3%, MICA, 500V	C74,91
675003-306-501	CAP. 750PF, 3%, MICA, 500V	C75.79
600226-314-008	CAP. .1UF, CERAMIC, 50V	C78
621011-306-501	CAP. 2100PF, 1%, MICA, 500V	C80
643003-306-501	CAP. 430PF, 3%, MICA, 500V	C81
600268-314-008	CAP. .01UF, CERAMIC, 50V	C82,85, 89,92, 96,99
627003-306-501	CAP. 270PF, 3%, MICA, 500V	C83,88
651003-306-501	CAP. 510PF, 3%, MICA, 500V	C84,86
615013-306-501	CAP. 1500PF, 3%, MICA, 500V	C87
616003-306-501	CAP. 160PF, 3%, MICA, 500V	C90
633003-306-501	CAP. 330PF, 3%, MICA, 500V	C93
618004-306-501	CAP. 180PF, 5%, MICA, 500V	C95
611004-306-501	CAP. 110PF, 5%, MICA, 500V	C97
622003-306-501	CAP. 220PF, 3%, MICA, 500V	C98
600144-410-001	DIODE HP3188	CR1-16
600011-416-002	DIODE IN4004	CR17,62
600006-411-006	DIODE, ZE	CR19
600109-410-001	DIODE IN4148	CR33-38, 40-44, 47-56,
600002-411-007	DIODE, ZENER, IN752A 5.6V	CR45
600002-411-001	DIODE, ZENER, 1N746A	CR46
600006-411-010	DIODE, ZENER, IN4737A, 7.5V	CR60
600109-410-001	DIODE IN4148	CR61
600064-419-003	3 POSITION VERTICAL MT	H1-9,12, 13,19,21
600064-419-001	4 POSITION VERTICAL MT	H10,11, 20,22-24, 31
600064-419-004	2 POSITION VERTICAL MT	H14,30
600064-419-005	1 POSITION VERTICAL MT	H15-18, 25-29,

PART NUMBER	DESCRIPTION	SYMBOL
600094-403-003	RELAY, DPDT, 12V, 3A CONTACTS	K1,2
600125-376-022	CHOKE 180UH	L15,18-20
600125-376-030	CHOKE 4.7UH	L17,21
600125-376-018	CHOKE 3.9UH	L22
600125-376-007	CHOKE 33UH	L23,24, 27,28, 31,32,
600125-376-006	CHOKE 3.3UH	L25,L49
600125-376-016	CHOKE 2.2UH	L26,29
600125-376-017	CHOKE 1.8UH	L30
600125-376-041	CHOKE 1.2UH	L33
600125-376-033	CHOKE 1.5 UH	L34
600125-376-007	CHOKE 33UH	L35,36, 39,40, 43,44,
600125-376-039	CHOKE .82UH	L37,42
600125-376-040	CHOKE 1.0UH	L38
600125-376-005	CHOKE .56UH	L41
600125-376-001	CHOKE .33UH	L45
600125-376-027	CHOKE .47UH	L46
600125-376-007	CHOKE 33UH	L47,48
600034-376-001	CHOKE 1000UH	L6
600125-376-043	CHOKE 5.6UH	L7,16
600125-376-013	CHOKE 15UH	L8
600125-376-020	CHOKE 12UH	L9
600154-413-001	TRANSISTOR 2N2907A	Q1,2,6-13
600080-413-001	TRANSISTOR 2N2222A	Q3
600396-413-001	TRANSISTOR 2N4392	Q4,5
647004-341-075	RES. 470, 1/4W, 5%	R1
622014-341-075	RES. 2.2K, 1/4W, 5%	R10,19, 23,26, 29,32,
662004-341-075	RES. 620, 1/4W, 5%	R18,22, 25,28, 31,34,
613014-341-075	RES. 1.3K, 1/4W, 5%	R2
610004-341-325	RES. 100, 1W, 5%	R20,50
610024-341-075	RES. 10K, 1/4W, 5%	R21,24, 27,30, 33,36,
622014-341-075	RES. 2.2K, 1/4W, 5%	R35,38,41
662004-341-075	RES. 620, 1/4W, 5%	R37,40,52
610024-341-075	RES. 10K, 1/4W, 5%	R39,42
633004-341-075	RES. 330, 1/4W, 5%	R4
600063-360-010	POT. 10K, 15 TURN	R46,49
610014-341-075	RES. 1K, 1/4W, 5%	R51
651004-341-075	RES. 510, 1/4, 5%	R53
615004-341-075	RES. 150, 1/4W, 5%	R6
647014-341-075	RES. 4.7K, 1/4W, 5%	R8
600148-512-001	TRANSFORMER, 3:1, TOROID	T1

Figure 4.14-1

High Pass Filter Assembly



NOTES:

1. UNLESS OTHERWISE NOTED :
   RESISTORS ARE IN OHMS, 1/4W, 5%
   CAPACITORS ARE IN MFD
   INDUCTORS ARE IN μH.
2. DIODE CR17 IS IN4004, CR1-16 ARE HP3188, CR19 IN4728, ALL OTHERS ARE IN4148

LAST DESIG. USED
R53 C106. CR62, Q13 L48, K2
DELETED
C19-18, 23, 28-37, 43, C100-105. R47, 48, 7. R11-17, 43-45. L1-5, 10-15. CR20-32, 37. Q1.

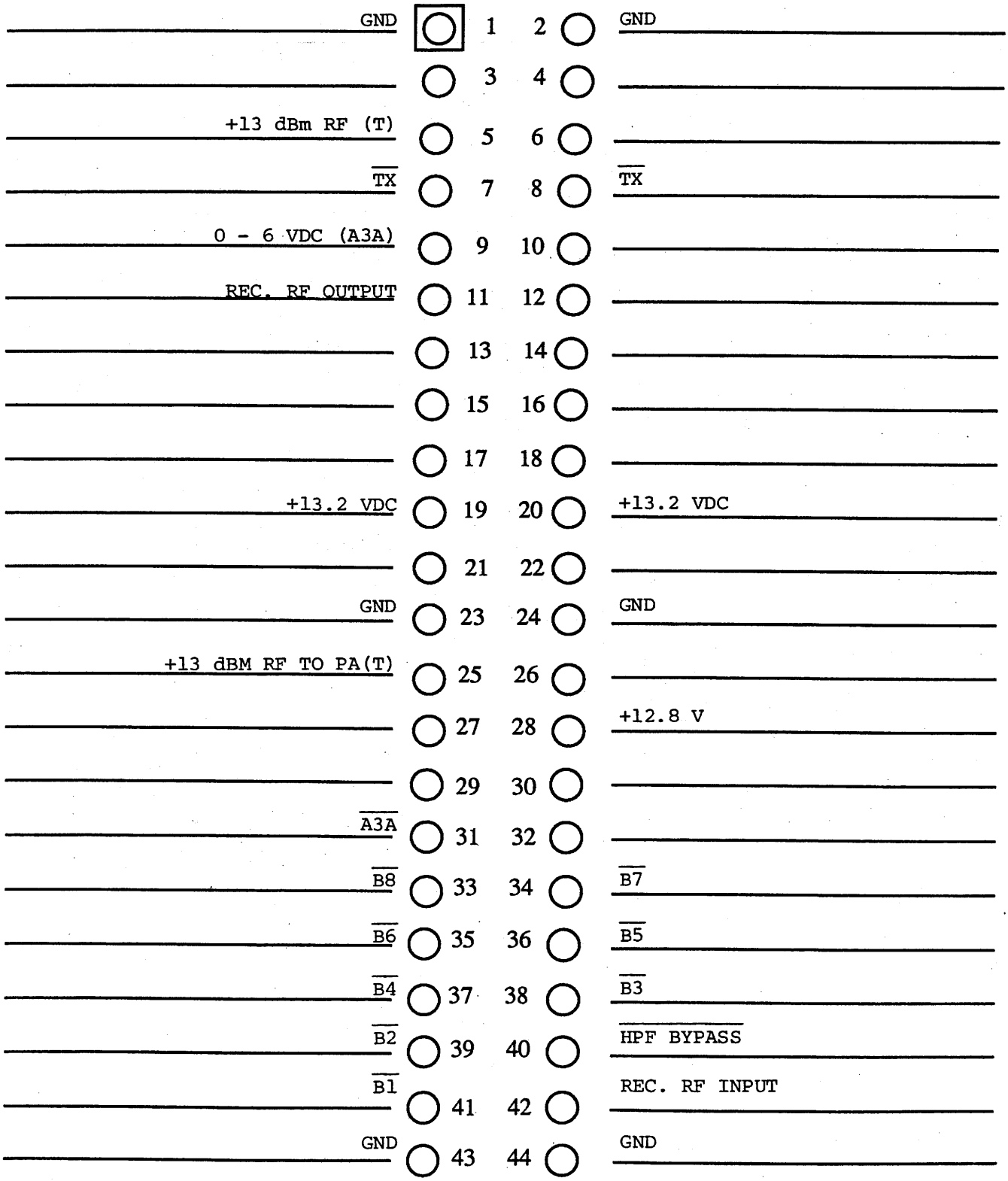
Figure 4.14-2

High Pass Filter Schematic

HIGH PASS FILTER BOARD, A7

PIN CONNECTIONS AND VOLTAGE READINGS

A7P14



4.15 HIGH LEVEL MIXER BOARD, A8

The High Level Mixer board is a bi-directional board, i.e. signal gain in both directions. In receive mode, it converts a 0 to 30 MHz RF input to a 1st IF of 59.53 MHz and subsequently a 2nd IF of 5 MHz. In transmit mode, it converts a 5 MHz input to 59.53 MHz and then to RF outputs of 1.6 to 30 MHz. All circuit interfaces are at 50 ohm impedance levels.

In receive mode, inputs on the RX input are selected by the RF switch and filtered by the 30 MHz LP filter. The 1st mixer, with amplified LO input of +21 dBm, 59.53 MHz to 89.53 MHz, converts the RF signals to a 59.53 MHz IF. The mixer is provided a broadband IF termination by a lossless constant resistance network and a non-reflective crystal filter network. A bilateral amplifier provides 18 dB gain which is controllable by a delayed AGC input of 0 to 9 volts. A second crystal filter at 59.53 MHz controls spurious responses due to the second mixer and complements the selectivity of the first filter and the system information filter for a total of 120 dB ultimate selectivity. The second mixer, with an amplified LO of +10 dBm, converts the 59.53 MHz signals to a 5 MHz IF. The second LO amplifier may be gated off by 9V pulses to accomplish noise blanking.

In transmit, the signal path is reversed with inputs at the 5 MHz IF, converted to a 59.53 MHz IF and amplified by the reversed bilateral amplifier. The RF switch directs the 1.6 to 30 MHz outputs from the 1st mixer to the TX amplifier to produce outputs to +15 dBm.

4.15.1 RX CONTROL

With a TTL low at pins 15 and 16, Q8 saturates putting +9 volts on all RX functions.

4.15.2 RF SWITCH

CR1 is biased to conduction by the current through R1, with L1 and L2 providing a high impedance to the signal path for RF signals. The resulting voltage across R1 biases CR2 off, isolating transmit circuits from the signal path. The input signals are thus conducted through C1, CR1 and C3 to the Low Pass Filter.

4.15.3 LOW PASS FILTER

The low pass filter is a 7-element elliptical design (C4 through C8 and L3 and L4) with a cut-off frequency of 31 MHz. This filter attenuates out-of-band spurious signals in both receive and transmit.

4.15.4 FIRST MIXER

Signals from the low pass filter are applied to pin 1 of the first mixer, MX1, a high level double balanced diode mixer. These signals (0-30 MHz) are modulated with +21 dBm LO signals (59.53 to 89.53 MHz) applied to pin 8 to produce a first IF of 59.53 MHz at pins 3 and 4.

4.15.5 CONSTANT RESISTANCE NETWORK

The constant resistance network provides a 50 ohm load to signals from the mixer at frequencies much greater than the IF frequency. R17 provides the 50 ohm load at high frequencies when C30 is a short, and at low frequencies when L14 is a short. C29 and L1 are series resonant at 59.53 MHz to couple the signal to the 90° hybrid network, maintaining a 50 ohm load at frequencies near 59.53 MHz IF.

4.15.6 90° HYBRID/FILTER NETWORK

This circuit maintains a 50 ohm input impedance by phasing equal mismatches from the two identical crystal filters FL1 and FL2, so that they cancel at the circuit input and add across R18 at an isolated port. T3 with C31 and C32, form a quadrature hybrid tuned broadly to 59.53 MHz at a 50 ohm impedance.

This circuit splits inputs from L13 to equal outputs at L15 and L16 phased 90° apart. L15 and C33 match the 2.3k ohm filter impedance of FL1. L16 and C34 perform the same function for FL2. Matching back down to 50 ohms is accomplished by L19 C35 and L20, C36. L17 and L18 are used to tune the residual capacitance across the filters

to increase the ultimate rejection. A second 90° hybrid (T4, C37, C38) adds the signals from each filter. The total loss through the whole hybrid/filter network is typically 3.0 dB.

4.15.7 BILATERAL AMPLIFIER

The Bilateral Amplifier consists of receive (Q9) and transmit (Q10) amplifiers activated by a 9V RX or 9V TX control signal. These amplifiers switched into the signal path by CR5, CR9 or CR10, CR7 allow reverse signal flow in transmit applications since all other circuits are inherently bilateral.

The amplifiers are feedback controlled to maintain a 50 ohm input/output impedance with gain controlled by feedback resistor impedance and the relatively low broad band collector output impedance of 600 ohms.

In receive, the signal flows through C38, CR5 (biased on through L23) and C44 to Q9. Q9 is biased by R21 and R22 with R21 also serving as a feedback resistor. The gain is set to 18 dB by the ratio of the collector load of 600 ohms and the emitter resistor R23. L25 and C45 match the 600 ohm output to 50 ohms with the output routed through pin diode CR9. The bias through switches CR5 and CR9 produces an 8V drop across L21, R20 at the input and L30, R30 at the output, which reverse biases transmit path pin diode switches CR7 and CR10.

The maximum signal level for strong signals is limited by a delayed AGC (DAGC) signal from pins 39 and 40. The DAGC input (0 to 9 volts) biases shunt pin diodes CR4 and CR8, which attenuate the signal at Q9 input and output for a total of 40 dB at 0 volts DAGC. Bias current is limited by resistors R31 and R29. CR11 delays the output attenuation for optimum linearity. The DAGC circuit is necessary to maintain inband intermodulation rejection of 40 dB at high input signals. The DAGC attenuation varies from 1 dB at 8.3 volts to 40 dB at 0 volts.

In transmit, the circuit of Q10 is connected through CR7, CR10 by the bias produced through L24, L29 by the 9V TX signal. The circuit is identical to that of Q9.

4.15.8 CRYSTAL FILTER

A second crystal filter, FL3 at 59.53 MHz is required to reject spurious responses due to the second conversion - especially the second IF image at 49.53 MHz. This filter, identical to FL1 and FL2, is matched to 50 ohms input and output by L31, L33 and C55, C56 with ultimate rejection improved by L32.

4.15.9 SECOND MIXER AND 5 MHZ FILTER

The 59.53 MHz first IF signal is converted to a second IF of 5 MHz by a second double-balanced diode mixer, MX2. The 5 MHz output signal is filtered by a 5 MHz low pass filter C62, C63, L36 to reject the 59.53 MHz IF feedthrough, the 54.53 MHz second LO, and other undesired mixer outputs.

4.15.10 FIRST LO AMPLIFIER

The first LO amplifier produces a +21dBm signal at MX1 (pin 8) from 0 dBm board inputs from 59.53 to 89.53 MHz at pin 3. Q5 and Q6 are common gate FETs paralleled for a 50 ohm broadband input with a transconductance to produce a 6 dB gain into the 50 ohm load produced by T2. The FETs are self-biased to 10 mA by R16. L8, L9 and C20 form a 40 MHz high pass filter to reduce low frequency noise.

Q4 is a grounded emitter amplifier with 15 dB gain which produces the +21 dBm LO signal required by MX1. Q3 is a bias regulator which maintains the voltage drop across R14 (due to the current of Q4) constant by controlling the base current of Q4 through R15. L12 and C28 broadly tune the output for a relatively flat response from 59.53 to 89.53 MHz. Biased at 100 mA, the amplifier can produce a linear output of 250 milliwatts.

4.15.11 SECOND LO AMPLIFIER

Q11 and Q12 are paralleled JFETs which produce a +10 dBm output at MX2, pin 8 from a 0 dBm, 54.53 MHz second LO input at board pin 41. The FETs are self-biased by R32 to 10 mA. L35

and C12 match the 50 ohm level of MX2 to a 1.2k ohms at the FET drain to produce a 10 dB gain. With a 9V input at board pin 37, Q13 produces an 8V bias across R32, which cuts the LO amplifier off (cutoff voltage of Q11, Q12 is 6.5V maximum) which in turn cuts the mixer off and thus breaks the signal path. This is used as a noise blanker gate in the MSR 8000 and may be used as a transmit inhibit gate in transmit applications.

4.15.12 TRANSMIT AMPLIFIER

Q1 and Q2 are feedback controlled amplifiers which increase the level of signals from the first mixer, MX1 to +17 dBm outputs, 1.6 to 30 MHz at board pin 6. Signals from the mixer, MX1 are routed through the low pass filter (C4-C8, etc.), C3, CR2, C14 and C15 to the base of Q2. Q2 is biased for 2.9 volts at the base by R9, R10 and R11. R7 and R8 produce 30 mA bias current with R7 setting the gain and R9 controlling the input/output impedance of 50 ohms. C18, as well as L7, compensate the high frequency roll off. Q1 is the identical circuit with values changed to produce a capability of 160 milliwatts linear output. In addition, the base bias is changed to add CR3, which compensates for bias changes with temperature.

4.15.13 DC CONTROL

+13 VDC is supplied through L30 to the first LO amplifier circuit. For installations where 13 volts is not connected to the board, CR6 allows the 9 volts to operate the LO circuit at a slightly reduced level. Grounds on pins 7, 8, or 15, 16 saturate the 9 volt TX or 9 volt RX transistor switches (Q7 or Q8) to supply 9 volts to the appropriate circuits.

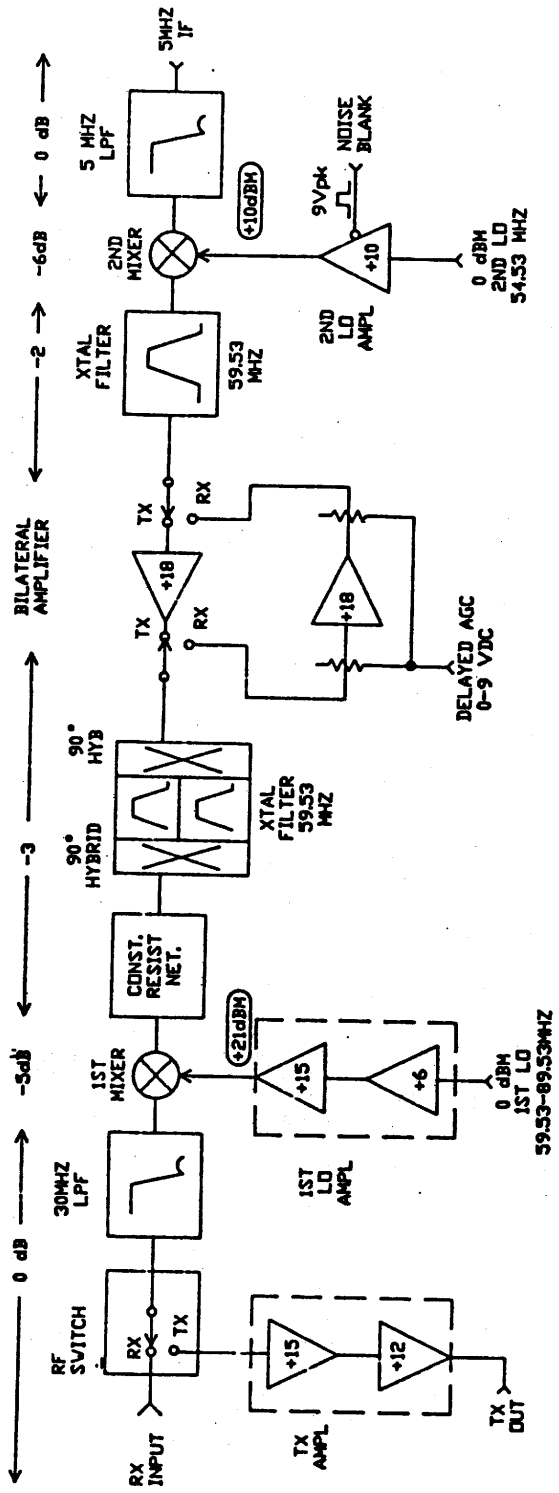
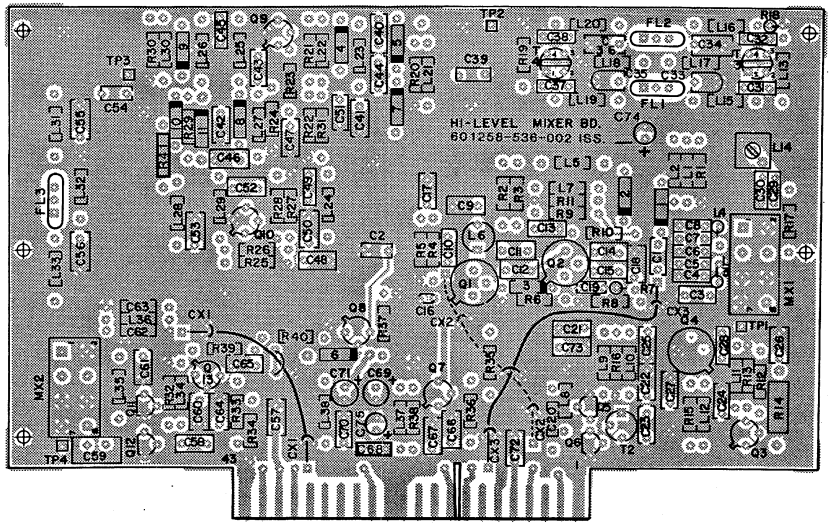


Figure 4.15-1

Block Diagram, High Level Mixer Board



High Level Mixer (601258-536-002)

PART NUMBER	DESCRIPTION	SYMBOL
600170-419-008	THERMAL WASHER	(Q1)
600226-314-014	CAP. 1UF, CERAMIC, 50V	C1,3
600226-314-008	CAP. .1UF, CERAMIC, 50V	C14,15
600210-314-040	CAP. 470PF, CERAMIC, 100V	C16
600210-314-037	CAP. 1500PF, CERAMIC, 100V	C19
600302-314-013	CAP. .1UF, MYLAR, 50V	C2,9-13, 17,18, 24-26, 42,53, 57,70,72
600293-314-430	CAP. 43PF, CERAMIC, 50V	C20
600369-314-181	CAP. 180PF, CERAMIC, 100V	C30
600369-314-270	CAP. 27PF, CERAMIC, 100V	C31,32, 37,38
600052-317-001	CAP. VAR, 3-10PF	C33,35
600269-314-005	CAP. 4.7PF, CERAMIC, 500V	C34,36, 55,56
600369-314-820	CAP. 82PF, CERAMIC, 100V	C4
600369-314-150	CAP. 15PF, CERAMIC, 100V	C5,29, 45,49
600302-314-007	CAP. .01UF, MYLAR, 63V	C58,60, 61,65-68, 73,44, 46-48, 50-52,54 21-23, 27,39-41, 43
600369-314-120	CAP. 12PF, CERAMIC, 100V	C59

PART NUMBER	DESCRIPTION	SYMBOL
600369-314-151	CAP. 150PF, CERAMIC, 100V	C6
600293-314-821	CAP. 820PF, CERAMIC, 50V	C62,63
600302-314-001	CAP. .001UF, MYLAR, 63V	C64
600297-314-003	CAP. 1UF, ALUM, 50V	C69,71
600369-314-470	CAP. 47PF, CERAMIC, 100V	C7
600297-314-025	CAP. 47UF, ALUM, 25V	C74,75
600369-314-680	CAP. 68PF, CERAMIC, 100V	C8,28
600144-410-001	DIODE HP3188	CR1,2,5, 7,9,10
600006-411-007	DIODE IN4734A 5.6V	CR11
600109-410-001	DIODE IN4148	CR3
600156-410-001	DIODE HP3080	CR4,8
600011-416-002	DIODE IN4004	CR6
600060-529-004	FILTER, 59.53 MHZ	FL1-3
600125-376-015	CHOKE 470UH	L1
600125-376-027	CHOKE .47UH	L13
600243-376-008	COIL, VAR, .06uH	L14
600125-376-040	CHOKE 1.0UH	L15,16, 19,20, 31,33
600125-376-028	CHOKE .1UH	L17,18,32
600125-376-022	CHOKE 180UH	L2,5
600125-376-004	CHOKE .39UH	L25,28
600125-376-037	CHOKE .27UH	L3
600125-376-006	CHOKE 3.3UH	L30,37, 38,29, 10,11, 21-24, 26,27
600125-376-005	CHOKE .56UH	L35
600125-376-016	CHOKE 2.2UH	L36
600125-376-031	CHOKE .18UH	L4
600072-376-032	CHOKE 39UH	L6

PART NUMBER	DESCRIPTION	SYMBOL
600125-376-032	CHOKE 10UH	L7,34
600125-376-036	CHOKE .12UH	L8,9,12
600018-455-001	MIXER CNP206	MX1
600007-455-001	MIXER SRA 3H	MX2
600222-413-001	TRANSISTOR 2N4427	Q1
600080-413-001	TRANSISTOR 2N2222A	Q13
600082-413-001	TRANSISTOR 2N2219A	Q2
600154-413-001	TRANSISTOR 2N2907A	Q3,7,8
600399-413-001	TRANSISTOR MRF237	Q4
600259-413-001	TRANSISTOR J310	Q5,6, 11,12
600177-413-001	TRANSISTOR 2N5179	Q9,10
647004-341-075	RES. 470, 1/4W, 5%	R1,15,29
656014-341-075	RES. 5.6K, 1/4W, 5%	R10
633014-341-075	RES. 3.3K, 1/4W, 5%	R11,21,28
627014-341-075	RES. 2.7K, 1/4W, 5%	R12,35-38
611024-341-075	RES. 11K, 1/4W, 5%	R13,41
620094-341-205	RES. 20, 1/2W, 5%	R14
620004-341-075	RES. 200, 1/4W, 5%	R16,32
651094-341-075	RES. 51, 1/4W, 5%	R17-19
630004-341-075	RES. 300, 1/4W, 5%	R2,3
624014-341-075	RES. 2.4K, 1/4W, 5%	R20,30
616014-341-075	RES. 1.6K, 1/4W, 5%	R22,27
668084-341-075	RES. 6.8, 1/4W, 5%	R23,26
622004-341-075	RES. 220, 1/4W, 5%	R24,25
610014-341-075	RES. 1K, 1/4W, 5%	R31
630014-341-075	RES. 3K, 1/4W, 5%	R33
647024-341-075	RES. 47K, 1/4W, 5%	R34,40
600000-341-075	RES. 0, 1/4W, 5%	R39
675084-341-075	RES. 7.5, 1/4W, 5%	R4,5
615004-341-075	RES. 150, 1/4W, 5%	R6
647084-341-075	RES. 4.7, 1/4W, 5%	R7
668094-341-075	RES. 68, 1/4W, 5%	R8
633004-341-075	RES. 330, 1/4W, 5%	R9
600094-512-001	TRANSFORMER, 3:1, BALUN	T2
600164-513-001	TRANSFORMER	T3,4

Figure 4.15-2

High Level Mixer Assembly

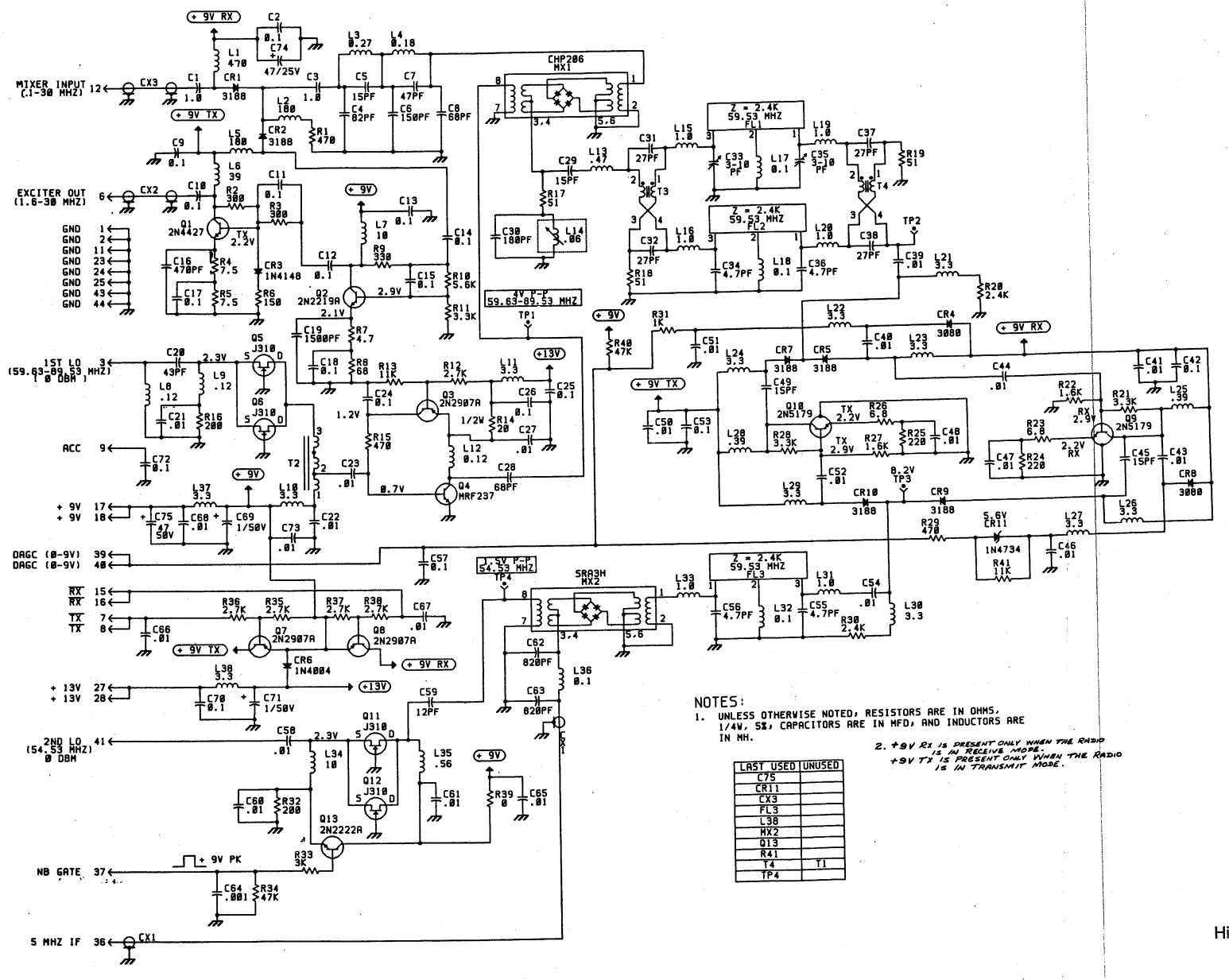


Figure 4.15-3

High Level Mixer Board Schematic

HIGH LEVEL MIXER BOARD, A8

PIN CONNECTIONS AND VOLTAGE READINGS

A8

GND	1	2		GND
0 dBm 59.54 - 89.53 MHz 1st LO	3	4		
	5	6		EXCITER OUT 3 VPP (1.6-30 MHz) T
$\overline{\text{LOGIC}}$ "0" OR 1 $\overline{\text{TX}}$	7	8		$\overline{\text{TX}}$ LOGIC "0" OR 1
GND	9	10		MIXER INPUT .01-29.999 MHz .2uV-200.000uV (R)
	11	12		
	13	14		
LOGIC "0" OR 1 $\overline{\text{RX}}$	15	16		$\overline{\text{RX}}$ LOGIC "0" OR 1
+9 VDC	17	18		+9 VDC
	19	20		
	21	22		
GND	23	24		GND
GND	25	26		
	27	28		
	29	30		
	31	32		
	33	34		
	35	36		IF IN/OUT (-120-70 dBm 5 MHz) (R)
LOGIC "0" OR 1 N.B. GATE	37	38		
0-9 VDC DELAYED AGC	39	40		DELYAED AGC 0-9 VDC
0 dBm 54.53 MHz 2nd LO	41	42		
GND	43	44		GND

4.16 IF FILTER BOARD, A9, A10

The IF Filter board contains up to three selectable 5 MHz crystal filters with amplifiers and circuits to perform in both transmit and receive operations. The transmit circuits, although described, are not used in the MSR 5050A.

The same board (with different filters) is used as A9 in Mother board J14 (IF Filter #1) and as A10 in J12 (IF Filter #2). A10 is installed as part of the receiver IF Filter option to offer more selectable filter bandwidths. As part of the ISB options, it provides an independent LSB signal path simultaneously with a USB path in A9.

The filters in A9 for the standard radio are:

FL1 - USB operation, also used as a medium bandwidth filter for CW, AM and FSK. In transmit it is used for USB, CW, FSK, AME and A3A.

FL2 - LSB operation in both receive and transmit.

FL3 - AM operation in receive only.

Since the frequency is inverted in the Mixer board, the USB pass band is actually on the lower side of 5 MHz.

The appropriate filter is selected by diode steering via mode information from the Interface board. During the receive mode, a 5 MHz IF signal from the High Level Mixer board is passed through the appropriate IF filter and further amplified in three stages. The gain is adjustable by jumpers to produce a 7 μV AGC threshold (for voice reception) or 1 μV threshold (for data reception). An AGC voltage from the Audio Squelch board controls the gain of the amplifiers to maintain a constant IF output over a large range of input levels.

In transmit operation, a 5 MHz double-sideband signal from the Transmit Modulator board is applied. The appropriate filter (FL1 or FL2) removes the unwanted sideband. A hybrid combiner adds a controlled level of 5 MHz carrier to the signal in AME and A3A transmit modes. The signal is then routed to the output through an amplifier with gain controlled by a TGC (Transmit Gain Control) voltage from the Transmit Modulator board.

4.16.1 DETAILED DESCRIPTION

4.16.1.1 Filter Selection

The filters are selected by placing a ground (logic 0) on certain pins on the board connector. When USB is selected, a ground is placed on pin 35 of P1. This action causes AC current flow from the +9V bus through R11, CR2, L7, and CR11. The resulting low resistance of pin diode CR2 creates a signal path from L13 to FL1 input. The high impedance of R11 and L7 prevent loading the signal. The other filter selector diodes, CR5 and CR7 are back-biased by the 9 volts supplied through pull-up resistors R23 and R24, and the near-zero volts at their anodes caused by pulling in CR2.

The filter output is similarly selected by CR3 with current from +9V through R30, CR3 and L8, to the same ground at pin 35. FL1 is also selected by the same action with grounds on pin 29 ($\overline{\text{FSK}}$) through CR21, pin 34 ($\overline{\text{CW}}$) through CR12, pin 33 (AMT) through CR13.

FL2 (LSB) is selected by a similar process with a ground on pin 37, causing current flow from +9V through R11, CR5, L9, and CR14, to connect the input; and current flow through R30, CR4, L10 and C14, to connect the outputs.

FL3 is selected for receive AM operation by a ground on pin 31, which biases Q5 on (the base being pulled to +9 VDC through R26), causing current flow through the input and output selector diodes CR7 and CR6. FL3 is prevented from being selected in AMT (transmit AM operation) by the ground at pin 33 with biases Q5 off through CR15.

4.16.1.2 Receive Path

The 5 MHz receive input from the Mixer board is on pin 36. Q3 provides 22 dB gain with a 50 ohm input and output impedance.

The 50 ohm input is controlled by the series/shunt feedback of R17/R14. L6 and C12 match the 400 ohm collector impedance to 50 ohms. The gain is controlled by the ratio of the collector load to R17. Q3 is biased for 6 mA collector current by R19 for an output third order IM intercept point of +19 dBm, allowing less than -40 dB inband IM distortion at IF inputs up to -28 dBm.

The amplified signal from Q3 passes through CR9 and C13 to the selected filter. CR9 is biased "ON" by the current through R16 and L5 from the "+9R" voltage bus, which is activated in the receive mode by Q9. The voltage developed across R16 back-biases CR8 preventive loading from the transmit circuitry.

The output of the filter is similarly routed through C28 and CR19 with CR19 biased on by current through L14, L15, and C31 from the "+9R" buss. CR20 is biased off by the voltage developed across R31. C30 and C31 couple the 5 MHz signal to Q6 which provides 31 dB voltage gain into a typical 300 ohm load (17 dB power gain). The 56 ohm R33 shunts the high input impedance of Q6, providing an accurate 50 ohm load for the filters. A variable resistor, R3, in the Q6 emitter, adjusts the gain of Q6 to overcome tolerances in the receive signal path and establishes a fixed end-to-end board gain. This adjustment directly effects the AGC threshold for the receiver. Jumper JP2 (and JP3 for Q7) shunts a 22 ohm resistor across the emitter resistor R35 (R40 for Q7) increasing the stage gain by about 6 dB, which reduces the receiver AGC threshold from -90 to -104 dBm. Q6 gain is proportional to the ratio of the load impedance of about 300 ohms (determined mainly by the parallel impedance of R37, R38, R39, the input impedance of Q7 and the off resistance of CR16) to the unbypassed emitter resistance.The gain is reduced by 30 dB in response to an AGC voltage from pin 12, by current through pin diode CR16 which reduces the load resistance of Q6. The response of Q6 is broadly tuned to 5 MHz (loaded Q of 2 by L17 and C33).

The signal is further amplified by Q7 in a nearly identical circuit with 17 dB gain. The output is sharply tuned (loaded Q of 50) by C40 and variable inductor L20 to reduce the broadband noise in the signal path.

The collector load is 500 ohms for this stage. Q8 is an emitter follower which produces a low inpedance output to the following Audio Squelch board through pin 5. A 20 ohm emitter resistor R53, limits the current gain for low impedance output loads which may compromise stability.

U1 is a voltage follower which passes inputs at pin 12 to a 0-6 volt output to pin diode (CR16, CR17) bias resistors (R37, R42), producing up to 6 mA current in each diode. This provides AGC gain cuts of 30 dB for each diode. U1 input is offset by R60.

The overall gain is 55 dB in voice mode, which produces a 7 µV AGC threshold in the radio with a -30 dBm Audio Squelch board AGC input threshold and 67 dB gain in data mode (JP2 and JP3 positioned E2, pin 1-2 and E3, pin 1-2), producing a 1.4 µV AGC threshold- adjustable in both cases by R35.

The AGC gain cut is 60 dB with an AGC input voltage of 8 VDC. The in-band IM rejection is greater than 40 dB at inputs up to -31 dBm. The noise figure is about 4 dB.

4.16.1.3 Transmit Path

The double sideband input to the IF Filter board on pin 4 from the Transmit Modulator is attenuated 3 dB by R27, R28, R29 and applied to the selected filter through C29 and CR20. CR20 is biased "ON" by current through L21, L15, and R31 from the "+9T" buss which is activated by Q10 in transmit mode. The USB or LSB signal emerging from the filter is passed through C13 and CR8 (by bias current from "+9T" through L2, L3, L4, and R16) to a 3 dB combiner circuit tuned at 5 MHz. The combiner, which adds a carrier (pin 39) to the SSB signal in AME or A3A mode, is formed by L3, L4, C9, C10, and R12.

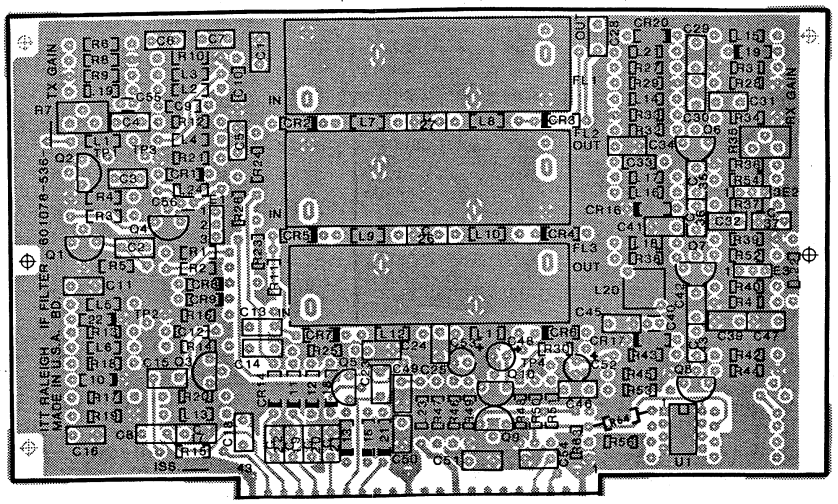
The output of the combiner goes through C7 and C6 to the base of Q2 with R10 imposing a 56 ohm termination to the combiner and consequently, to the filters. Q2 is configured as a common emitter amplifier with maximum gain determined by the ratio of the collector load of 1k (R3/R4 in parallel) and the unbypassed emitter resistor R9, which is adjustable to maintain a precise transmit gain.

The gain is varied by the resistance of pin diode CR1 in the emitter circuit in series with R9 in response to TGC voltage from 2 to 6 VDC at pin 42.

Parallel traps L19/C55 and L24/C56 are tuned to 5 MHz to remove parasitic loading in the emitter circuit to maximize the TGC gain cut to greater than 32 dB. R13 and R20, in conjunction with the diode junction voltages of CR1, Q4 and CR22, delay the TGC action until approximately 2 VDC.

Q1 is an emitter follower producing a 50 ohm output impedance at pin 38 (and pin 40). When used in the MSR 6700A in ISB, two IF Filter boards are paralleled at pin 40.

With a +5.5 VDC TGC input at pin 42, the overall SSB transmit gain from pin 4 to pin 38 or pin 40 is +6 dB and carrier gain from pin 39 to pin 38 or 40 is +13 dB. Both gains are reduced by 32 dB by a TGC input at pin 42 from +5.5 to 2 VDC. Third order IM products are down greater than 40 dB with DSB inputs as high as -10 dBm.



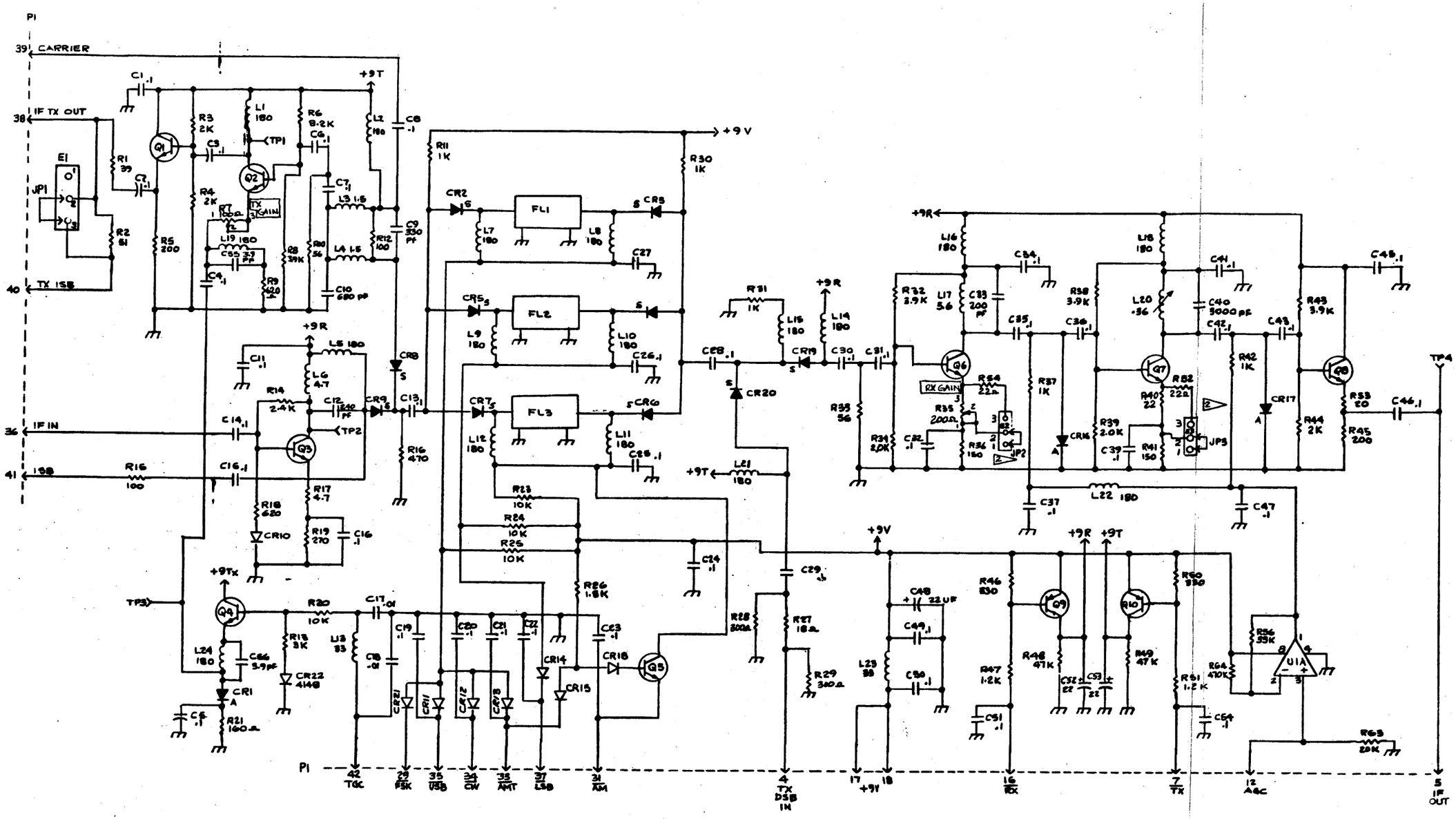
IF Filter (601076-536-010)

PART NUMBER	DESCRIPTION	SYMBOL
600302-314-013	CAP. .1UF, MYLAR, 50V	C1-8,11, 13-16, 19-32,
600293-314-681	CAP. 680PF, CERAMIC, 50V	C10
600293-314-241	CAP. 240PF, CERAMIC, 50V	C12
600302-314-007	CAP. .01UF, MYLAR, 63V	C17,18
600293-314-201	CAP. 200PF, CERAMIC, 50V	C33
600302-314-013	CAP. .1UF, MYLAR, 50V	C34-37, 39,41-43,
600265-314-026	CAP. 3000PF, CERAMIC, 100V	C40
600302-314-013	CAP. .1UF, MYLAR, 50V	C45-47, 49-51,54
600297-314-016	CAP. 22UF, ALUM, 25V	C48,52,53
600265-314-008	CAP. 3.9PF, CERAMIC, 100V	C55,56
600293-314-331	CAP. 330PF, CERAMIC, 50V	C9
600156-410-001	DIODE HP3080	CR1,16,17
600109-410-001	DIODE IN4148	CR10-14, 18,21,22
600052-410-001	DIODE IN270	CR15
600144-410-001	DIODE HP3188	CR2-9, 19,20
600198-608-005	CONN. HEADER, 3 PIN, TIN	E1-3
600084-529-001	FILTER, USB	FL1 (USB)
600083-529-001	FILTER, LSB	FL2 (LSB)
600082-529-001	FILTER, AM, 6KHZ BANDWIDTH	FL3 (AM)
600190-608-001	CONN, JUMPER, 2 POS.	JP1-3
600125-376-022	CHOKE 180UH	L1,2,5, 7-12, 14-16,18
600125-376-007	CHOKE 33UH	L13,23
600125-376-043	CHOKE 5.6UH	L17
600125-376-022	CHOKE 180UH	L19,21, 22,24
600247-376-001	COIL, VAR, .283-.405UH	L20

PART NUMBER	DESCRIPTION	SYMBOL
600125-376-033	CHOKE 1.5 UH	L3,4
600125-376-030	CHOKE 4.7UH	L6
600229-413-003	TRANSISTOR 2N3904 TO-92	Q1-8
600116-413-002	TRANS, 2N3906	Q9,10
639094-341-075	RES. 39, 1/4W, 5%	R1
656094-341-075	RES. 56, 1/4W, 5%	R10,33
610014-341-075	RES. 1K, 1/4W, 5%	R11,30, 31,37,42
610004-341-075	RES. 100, 1/4W, 5%	R12,15
630014-341-075	RES. 3K, 1/4W, 5%	R13
624014-341-075	RES. 2.4K, 1/4W, 5%	R14
647004-341-075	RES. 470, 1/4W, 5%	R16
647084-341-075	RES. 4.7, 1/4W, 5%	R17
627004-341-075	RES. `0, 1/4W, 5%	R19
651094-341-075	RES. ., 1/4W, 5%	R2
610024-341-075	RES.)K, 1/4W, 5%	R20,23-25
616004-341-075	RES. 160, 1/4W, 5%	R21
618014-341-075	RES. 1.8K, 1/4W, 5%	R26
618094-341-075	RES. 18, 1/4W, 5%	R27
630004-341-075	RES. 300, 1/4W, 5%	R28,29
620014-341-075	RES. 2K, 1/4W, 5%	R3,4,34, 39,44
600066-360-005	POT. 200, 1/2W, CERMET, RT/AN	R35
615094-341-075	RES. 150, 1/4W, 5%	R36,41
622094-341-075	RES. 22, 1/4W, 5%	R40,52,54
633004-341-075	RES. 330, 1/4W, 5%	R46,50
612014-341-075	RES. 1.2K, 1/4W, 5%	R47,51
647024-341-075	RES. 47K, 1/4W, 5%	R48,49
620004-341-075	RES. 200, 1/4W, 5%	R5,45
620094-341-075	RES. 20, 1/4W, 5%	R53
633024-341-075	RES. 33K, 1/4W, 5%	R56
682014-341-075	RES. 8.2K, 1/4W, 5%	R6
620024-341-075	RES. 20K, 1/4W, 5%	R63
647034-341-075	RES. 470K, 1/4W, 5%	R64
600066-360-004	POT. 100, 1/2W, CERMET, RT/AN	R7
639014-341-075	RES. 3.9K, 1/4W, 5%	R8,32, 38,43
662004-341-075	RES. 620, 1/4W, 5%	R9,18
600150-415-001	IC LM358, OP AMP, LP DUAL	U1

Figure 4.16-1

IF Filter Assembly



NOTES:

1. JP1 BETWEEN E1-2 AND E1-3 FOR NORMAL OPERATION, BUT FOR A MSR-6700 WITH ISB PUT JP1 BETWEEN E1-1 AND E1-2.
2. PLACE JP2 AND JP3 BETWEEN PINS 1 AND 2 FOR VOICE MODE. CONNECT JP2 AND JP3 BETWEEN PINS 2 AND 3 FOR DATA MODE.

CAPACITORS IN UF
RESISTORS 1/4W 5%

IC = LM1358 GND PINS 1,2, ,24,48,44
CHOKES IN uH 1/4W
TRANSISTORS 2N3904 NPN 2N3906 PNP
DIODES = 1N4148
D_S = HPSO82-3188
D_A = HPSO82-3080

NOT USED	LAST USED
R22,55,57-62	L24
C38	Q10
C44	R64
	C56
	CR22
	JP3
	E3

Figure 4.16-2

IF Filter Board Schematic

IF FILTER BOARD, A9, A10

PIN CONNECTIONS AND VOLTAGE READINGS

A9P1/A10 P1

GND	1	2	GND	
	3	4	TX DSB IN 200 mVPP (-10 dBm) TYPICAL	
-30 dBm IF OUT (R)	5	6		
LOGIC "0" OR 1 $\overline{TX}$	7	8		
	9	10		
	11	12	AGC INPUT 0 TO +6 VDC (R)	
	13	14		
	15	16	$\overline{RX}$ LOGIC "0" OR 1	
+9 VDC	17	18	+9 VDC @ 100 ma $\overline{RX}$/80ma $\overline{TX}$	
	19	20		
	21	22		
GND	23	24	GND	
	25	26		
	27	28		
LOGIC "0" OR 1 $\overline{FSK}$	29	30		
LOGIC "0" OR 1 $\overline{AM}$	31	32		
LOGIC "0" OR 1 $\overline{AMT}$	33	34	$\overline{CW}$ LOGIC "0" OR 1	
LOGIC "0" OR 1 $\overline{USB}$	35	36	REC. IF IN -106 to -20 dBm	
LOGIC "0" OR 1 $\overline{LSB}$	37	38	5 MHz TX IF OUT -8 dBm MAX.	
(AMT) -18 - 25 dBm 5 MHz	39	40	ISB IF OUT (NOT USED)	
ISB OUT (NOT USED)	41	42	TGC +2 TO +5.5 VDC (T)	
GND	43	44	GND	

vided: a balanced 600 ohm output and one converted to a front panel speaker/phone audio via the Speaker Amplifier board, with level adjusted by the front panel volume control. The same board is used as A11 (standard radio) and as A12 (with ISB options).

Located on this board are an input IF amplifier, envelope detector, AGC circuit, delayed AGC circuit, product detector, 3rd LO amplifier, 600 ohm audio amplifier circuit, speaker/sidetone audio circuit, and squelch circuits.

The AGC has a fast attack and front panel selectable fast, medium, or slow decay times. The squelch circuit is a combination of syllabic (responding to frequencies less than 500 Hz modulated at rates less than 5 Hz) with a front panel adjustable carrier squelch. The MSR5050A does not use the carrier squelch function. A jumper JP1 positioned on E1 pins 2 and 3 will allow the 600 ohm audio as well as the speaker audio to be squelched.

4.17.1 DETAILED DESCRIPTION

4.17.1.1 Input IF Amplifier and Envelope Detector

Five MHz input signals from the IF Amplifier, at pin 5, at a level of 20 mV P-P (-30 dBm) will activate the AGC circuits. Q1 is a common emitter amplifier with 36 dB voltage gain to the gate of Q2. The collector load is 650 ohms by R8 in parallel with the loading due to C5 and its 50 ohm termination due to R5, R6, etc. C5 matches the high impedance to the 50 ohm operating impedance of a double balanced diode mixer. R5, R6 and R7 provide 3 dB attenuation and stabilizing impedance to the product detector M1, reducing the 5

SSB, FSK, and CW or the envelope detector signal in AM. The envelope signal is also applied to the AGC circuit at U1 pin 3,10.

4.17.1.2 Product Detector and LO Amplifier

The 5 MHz third LO signal for the product detector is received on pin 12 at a 50 ohm reference -15 dBm level. Q4 provides 19 dB gain to produce a +4 dBm LO drive via matching capacitor C13 to the product detector M1 at pin 8. The 5 MHz IF signal input to the product detector is received via the 3 dB attenuator (R5, R6, and R7) at a level of -10 dBm at pin 1. The detected output of 62 mV RMS is applied to the analog switch U2 at pin 12 with the 5 MHz carrier and image frequencies rejected by C11. The LO and IF levels at the mixer maintain IM distortion less than -40 dBc.

4.17.1.3 600 Ohm Audio and Speaker Audio

The selected AM or product detector signal from U2A, pin 14 is amplified in U4A (by 3.3) to 200 mV RMS by the ratio of R32 to R31. This audio level from SSB (100% modulated) is the same as that from 100% AM modulated signals. The AC ground reference for U4A is a 4.5 volt bus created by U5A and voltage divider R70, R71 from +9V. Inputs and outputs of analog switches U2A, B, and C are also referenced to the same bus to eliminate transient outputs in the audio during switching. The 600 ohm audio signal is routed through the MUTE/SQUELCH switch U2, pin 1 to 15 unless bypassed by JP1 (from E1, pin 1 to 2). Variable resistor R64 attenuates the signal to the 600 ohm line amplifier U4B/Q10. The gain of the amplifier is determined by feedback resistors R60 and R61 with Q10 increasing the output current drive to produce +10 dBm (6.9V P-P) at T1 output when loaded with 600 ohms at board connector pins 14 and 6.

The peak current drive is established by R62, which produces a quiescent current of 25 mA due to the 4.5 VDC bias at Q10 collector. The bias voltage results from the 4.5V bus at U4B, pin 6 and the closed loop DC voltage gain of 1. The 600 ohm output impedance is established by feedback resistor R63 at T1 centertap to ground (150 ohms from T1, pin 4 to pin 5). The ratio of 150 ohms to R63 is the same as that of the primary gain resistors R60 to R61. When the secondary of T1 is not loaded, the voltage gain is determined only by R60 and R61. When loaded by 600 ohms, the reflected impedance between T1, pin 4 and 5 is 150 ohms. This produces a feedback factor with R63 equal to that of R60 and R61, which reduces the gain and consequently the output voltage by a factor of 2 - evidence of a matched 600 ohm source impedance. The single ended 150 ohm output from T1, pin 6 at Audio Squelch board pin 4 is used in the Interface board to develop a dc meter signal proportional to the 600 Ω audio level. The voltage gain of the amplifier circuit is 29 dB to a 600 ohm load at pin 6/14 or to an open circuit load at pin 4. This produces 2.45V RMS (+10 dBm into 600 ohms) with 86 mV RMS input from R64, which allows a 7 dB gain margin from the 200 mV RMS available at R64.

The speaker audio signal goes through analog switch U2, pin 3 to 4 with no bypass jumper. The signal is reduced in amplifier U4C to 150 mV RMS at board pin 3 by the ratio of R67 to R65. This output is amplified to a speaker/phone front panel output in the Speaker Amplifier board with level control by the front panel volume control. An external sidetone signal at pin 27 (i.e. from a transmitter) from the rear panel audio connector is amplified in A4C as a speaker signal.

4.17.1.4 Squelch Circuits

The syllabic squelch circuit is basically a pulse count discriminator and integrator which produces a gating output for slowly changing (less than 5 Hz rate) frequency content of the audio signal. The gating output has a fast attack (50 milliseconds) and long hang-time (2 seconds).

The audio signal is first amplified (U6B, pin 5) by 1000 (R87/R88) in U6B, and squared in U6C to produce a square wave input at U7A, pin 1 for signals down to receiver noise levels. U7A and U7B form a monostable multivibrator with an output pulse width of 0.5 milliseconds and a saturated output level of 4 volts. A differentiator (C49, C50, R86, and R85) and integrator (R84, R83, C51, and C52) produce a DC voltage output proportional to the average frequency of the audio signal. U6A is an integrator with a gain of 10, determined by R81/R82 and a time constant of 73 milliseconds (R81, C45). This reduces the output due to fast frequency changes greater than 5 Hz. R80 is normally set to attenuate the signal by .27, but may be adjusted in unusually noisy environments to prevent squelch breaks by noise. U5D is an absolute value amplifier which produces a negative output when the peak voltage changes from R80 exceed the forward voltage drop of either CR17 or CR18. The one-shot voltage formed by U7D, U7C is triggered through CR16 and resets in about 2 seconds (unless retriggered) due to the time constant C43, R75.

The resultant +9 VDC positive output from U7C through CR15, forces comparator U5B input (U5B, pin 5) high, which in turn enables the 600 ohm audio gate U2B and the speaker audio gate U2C by +9V on U2, pin 9 and 10.

The squelch gates are also enabled through comparator U5B by another comparator, U5C, which is driven by the front panel squelch on/off control through attenuator R73/R72. With the squelch control pushed in, the wiper outputs +9 VDC to Audio Squelch board pin 10 and is attenuated to 4.9 VDC, which exceeds the 4.5V comparator reference voltage at U5C, pin 9, thus enabling the squelch gate. In other radios, Q8 is used as a carrier squelch with the front panel squelch pot varying the threshold.

4.17.1.5 AGC Circuits

U1A is a X75 amplifier/peak detector which amplifies signals from Q3 that exceed a reference voltage of .24 VDC (Set by R25/R26). AGC is disabled (AGC off) by pulling up U1A pin 2 through CR23. The gain is set by R23/R24. The AGC attack time is limited by the charging time of C23 through R95 and R22 to less than 10 milliseconds.

CR24 bypasses R96 to reduce the attack time for large signal changes. The decay time is determined by the discharge time constant of C23 through R23 for three seconds in slow AGC, through R39 for 200 milliseconds in medium AGC, and through R38 for less than 50 milliseconds in fast AGC.

U1C is identical to U1A, but with a gain of 260 (by R28/R27) and a fast charge/ discharge time. The outputs of both amplifiers are compared in U1D. The output of U1C is normally higher than U1A, therefore U1D output is low. If the signal level suddenly falls, the output of U1C follows, but the output of U1A remains high due to the slow decay of C23.

The output of U1D goes high as the U1C output falls below U1A, which will switch on Q6 or Q7 (depending on the state of open collector comparators U3A and U3B). The outputs of U3A and U3B go negative as the input voltage on board pin 38 exceeds the reference voltages for each comparator as determined by R36, R35, and R34. For an input above 7.7 VDC, both comparator outputs are negative, both Q6 and Q7 are prohibited from turn on by U1D, and the decay time is slow. Between +7.7 volts and +3 volts, U3A output is high which allows Q6 to be enabled by U1D output and the decay through R39 is medium (about 200 milliseconds). An input below +3 VDC causes both comparator outputs to go high allowing both Q6 and Q7 to be enabled. The decay is fast through R39 and R38 in parallel. An external ground on pin 41 will dump the AGC voltage, putting the receiver in a high gain status. The receiver RF/IF gain is manually controlled by an external 0 to 5 volts at pin 34, either from the remote gain pot or the front panel RF gain pot. The control of AGC voltage by signal level is inhibited by a TTL +3 volts at pin 29.

U1B provides an additional gain of 2 (by R43/ R44) to output the receiver AGC voltage at pin 11. This voltage controls the IF Filter board gain, maintaining a constant IF input level to the Audio Squelch board and consequently, a constant audio output level. RF gain is varied by a 0 to +5 VDC input at pin 34 which replaces the AGC voltage at U1B pin 5. The "S" meter output at pin 42 is adjustable by R44 (normally set at 2k ohms). A delayed AGC signal to control Mixer board gain is produced by a current amplifier (U4D and Q9). The AGC voltage input is attenuated by R47/R48. The offset voltage which determines the voltage at which DAGC becomes active is set by R52 (for 4.0V at R52 pin 2); DAGC current gain is adjusted by R53 (normally set at 100 ohms).

4.17.1.6 Miscellaneous Circuits

Diodes CR5, CR6, CR7, and CR24 control the U2A audio switch to direct product detector signals to the audio output circuits with a ground on pins 35, 36, 37 or 39 ($\overline{\text{USB}}$, $\overline{\text{CW}}$, $\overline{\text{LSB}}$, or $\overline{\text{FSK}}$). If no grounds are applied, the switch passes AM audio signals from the envelope detector. (In the MSR 5050A pin 37 is grounded in all modes except AM.) Diodes CR8 and CR9 from $\overline{\text{FSK}}$ and $\overline{\text{CW}}$ ground signal inputs cause U3A and U3B outputs to go high, resulting in a fast AGC decay rate (not used in the MSR 5050A). Q5 applies +9 volts to the 3rd LO amplifier, Q3, and to IF amplifier and envelope detector circuits (Q1, Q2, Q3), only in receive with a ground on pins 15 and 16.

CR26, 27 and R102 are mounted on the rear of the board for REV A artwork P.C. boards.

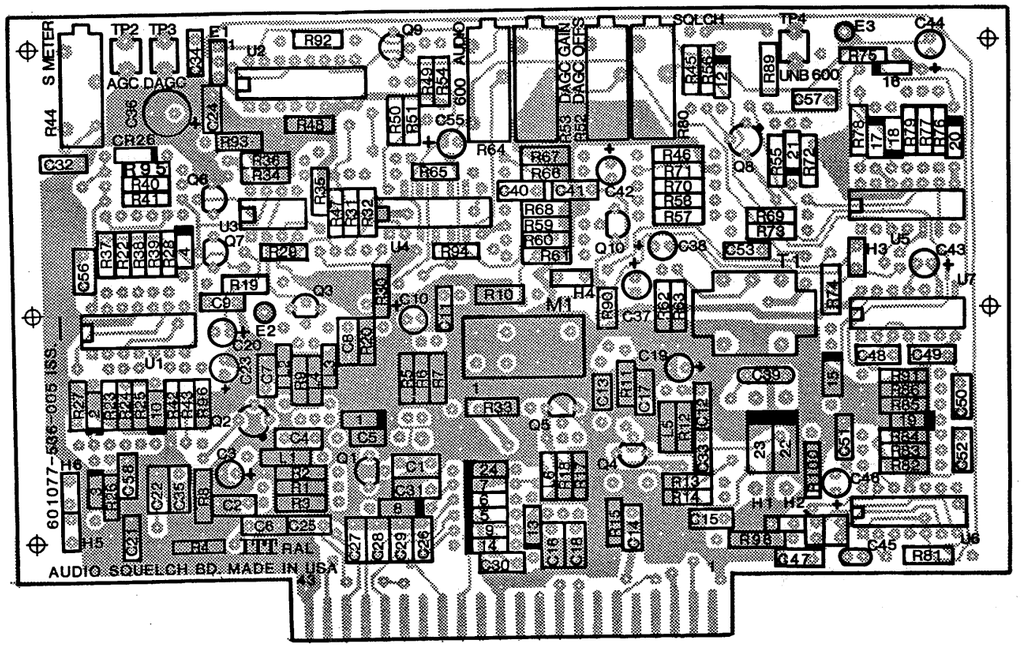


Figure 4.17-1

Audio Squelch Assembly

Audio Squelch (601077-536-005)

PART NUMBER	DESCRIPTION	SYMBOL
600302-314-013	CAP. .1UF, MYLAR, 50V	C1,2,4, 6-8, 11,12,
600297-314-006	CAP. 2.2UF, ALUM, 50V	C10,20,44
600302-314-013	CAP. .1UF, MYLAR, 50V	C14-18, 21,22, 24-32,
600202-314-020	CAP. 15UF, 20V, TANT.	C23
600297-314-016	CAP. 22UF, ALUM, 25V	C3,19,37, 38,42,55
600302-314-013	CAP. .1UF, MYLAR, 50V	C35,47, 53,58
600297-314-032	CAP. 100UF, ALUM, 25V	C36
600189-314-018	CAP. .01UF, 500V	C39
600302-314-015	CAP. .22UF, MYLAR, 50V	C40,41
600202-314-018	CAP. 10UF, 25V, TANT.	C43
600268-314-012	CAP. .022UF, CERAMIC, 50V	C45
600202-314-007	CAP. 1UF, 35V, TANT.	C46
600293-314-121	CAP., 120PF, 50V	C5,13
600302-314-009	CAP. .022UF, MYLAR, 63V	C56
600302-314-007	CAP. .01UF, MYLAR, 63V	C9,33,34, 48-52,57
600109-410-001	DIODE IN4148	CR1-21, 24-27
600028-411-001	DIODE, VOLT.SUPRESSOR P6KE6,8A	CR22,23
600198-608-005	CONN. HEADER, 3 PIN, TIN	E1
600261-230-001	TERMINAL	E2,3
600190-608-001	CONN, JUMPER, 2 POS.	JP1
600125-376-034	CHOKE 8.2UH	L1,5
600125-376-022	CHOKE 180UH	L2,3,4
600125-376-011	CHOKE 33UH	L6
600008-455-001	MIXER SLB-1	M1

PART NUMBER	DESCRIPTION	SYMBOL
600229-413-003	TRANSISTOR 2N3904 TO-92	Q1,3,4, 6,7,9
600396-413-001	TRANSISTOR 2N4392	Q2,8
600116-413-002	TRANS, 2N3906	Q5,10
600025-419-001	TRANSISTOR PAD	Q8
639014-341-075	RES. 3.9K, 1/4W, 5%	R1,11
651094-341-075	RES. 51, 1/4W, 5%	R10
610014-341-075	RES. 1K, 1/4W, 5%	R12,18, 19,22, 37,45,46, 49,59,68, 90,95,99
618094-341-075	RES. 18, 1/4W, 5%	R13
613004-341-075	RES. 130, 1/4W, 5%	R14
633004-341-075	RES. 330, 1/4W, 5%	R17
620014-341-075	RES. 2K, 1/4W, 5%	R2,15,51
618014-341-075	RES. 1.8K, 1/4W, 5%	R24,38
656014-341-075	RES. 5.6K, 1/4W, 5%	R25
615004-341-075	RES. 150, 1/4W, 5%	R26
615014-341-075	RES. 1.5K, 1/4W, 5%	R27
639034-341-075	RES. 390K, 1/4W, 5%	R28
610024-341-075	RES. 10K, 1/4W, 5%	R29-31, 40,41, 48,50, 69-71,73, 74,76,77, 92-94,98, 100,101
647084-341-075	RES. 4.7, 1/4W, 5%	R3
633024-341-075	RES. 33K, 1/4W, 5%	R32
651024-341-075	RES. 51K, 1/4W, 5%	R33,66
630014-341-075	RES. 3K, 1/4W, 5%	R34,102
647014-341-075	RES. 4.7K, 1/4W, 5%	R35
675014-341-075	RES. 7.5K, 1/4W, 5%	R39
622004-341-075	RES. 220, 1/4W, 5%	R4,20
610034-341-075	RES. 100K, 1/4W, 5%	R42,43, 55,67, 83,84,

PART NUMBER	DESCRIPTION	SYMBOL
600063-360-010	POT. 10K, 15 TURN	R44,52, 64,80
630024-341-075	RES. 30K, 1/4W, 5%	R47
618004-341-075	RES. 180, 1/4W, 5%	R5,7,62
600063-360-005	POT. 200, 15 TURN	R53
620024-341-075	RES. 20K, 1/4W, 5%	R56
610094-341-075	RES. 10, 1/4W, 5%	R58
630094-341-075	RES. 30, 1/4W, 5%	R6,54
630121-342-059	RES. 30.1K, 1/8W, 1%	R60
690901-342-059	RES. 909, 1/8W, 1%	R61
647581-342-059	RES. 4.75, 1/8W, 1%	R63
615034-341-075	RES. 150K, 1/4W, 5%	R65,23
612024-341-075	RES. 12K, 1/4W, 5%	R72
633034-341-075	RES. 330K, 1/4W, 5%	R75,82
610044-341-075	RES. 1M, 1/4W, 5%	R78,79
613014-341-075	RES. 1.3K, 1/4W, 5%	R8,36
633044-341-075	RES. 3.3M, 1/4W, 5%	R81,87
620034-341-075	RES. 200K, 1/4W, 5%	R85,86
633014-341-075	RES. 3.3K, 1/4W, 5%	R88
610034-341-075	RES. 100K, 1/4W, 5%	R89
651004-341-075	RES. 510, 1/4, 5%	R9,57
647024-341-075	RES. 47K, 1/4W, 5%	R91
647094-341-075	RES. 47, 1/4W, 5%	R96
635234-501-001	TRANSFORMER, 600 OHM, AUDIO	T1
600114-611-002	RED TEST POINT	TP2
600114-611-003	ORANGE TEST POINT	TP3
600114-611-004	YELLOW TEST POINT	TP4
600171-415-001	IC LM324, OP AMP, 741 QUAD	U1,4-6
600908-415-001	IC 4053, MUX/DEMUX	U2
600486-415-001	IC LM393, DUAL VOL COMP	U3
600078-415-101	IC MC14001B, NOR QUAD 2-IN	U7

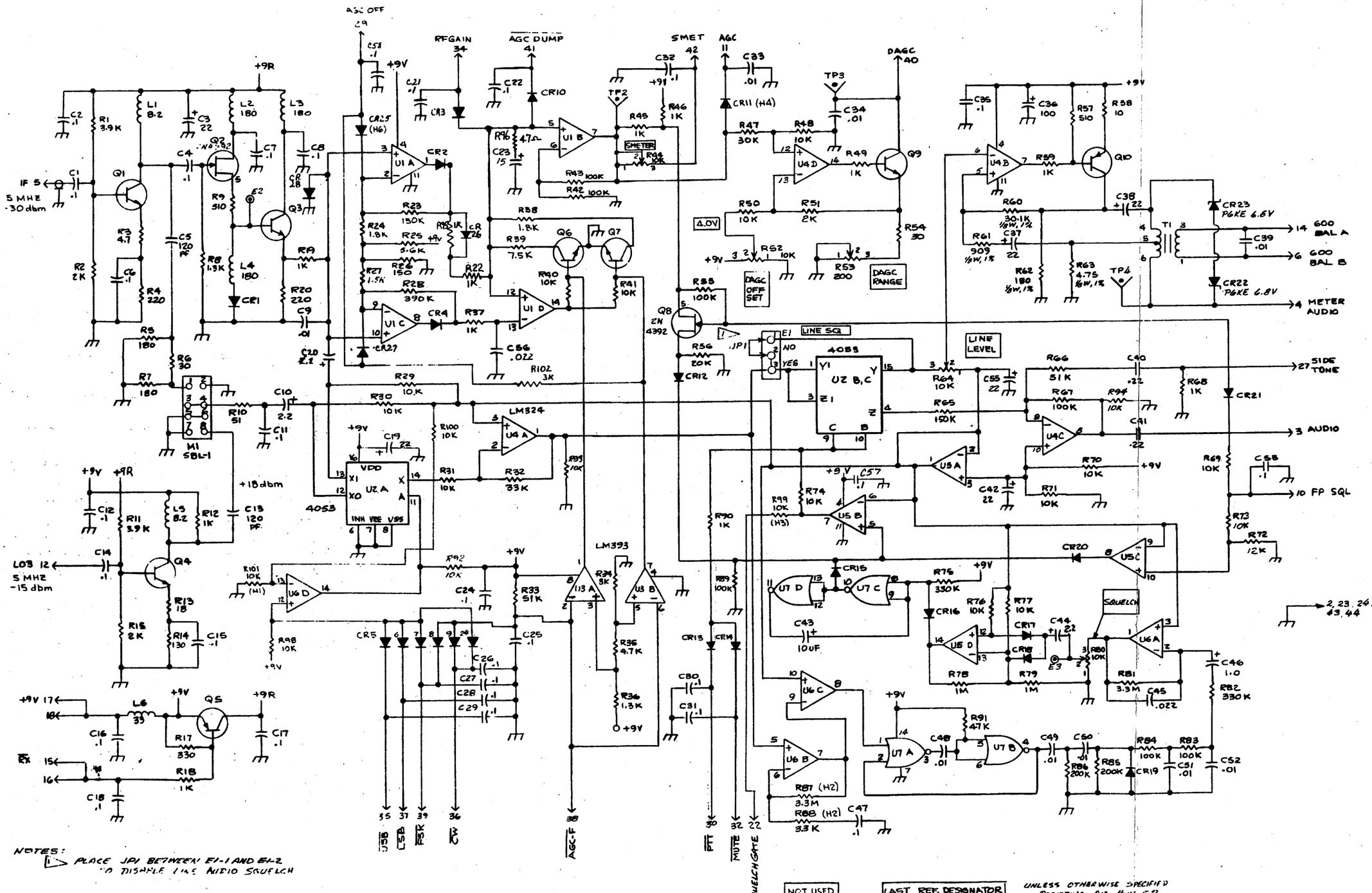


Figure 4.17-2

Audio Squelch Board Schematic

AUDIO/SQUELCH BOARD, A11, A12

PIN CONNECTIONS AND VOLTAGE READINGS

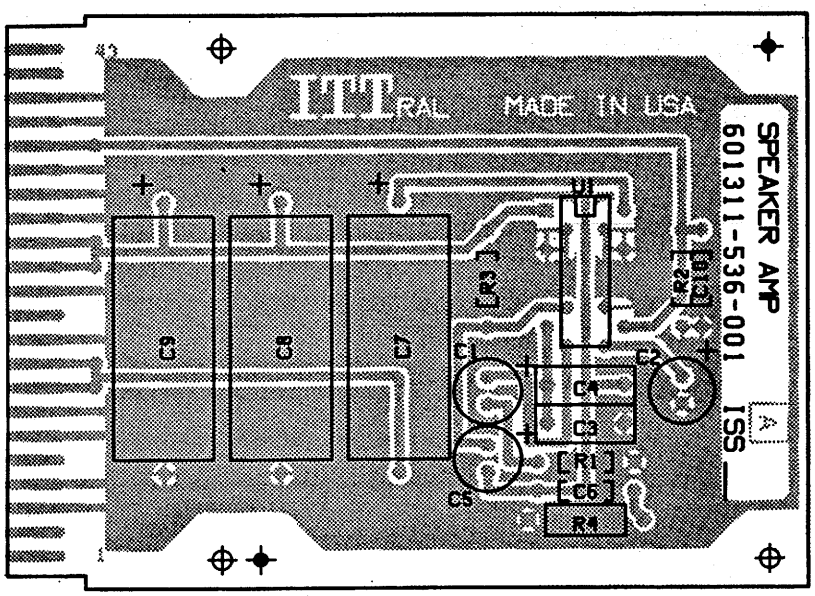
A11P1, A12P1

GND	1	2	GND
.3-3 kHz 0 to 0.15 VRMS AUDIO	3	4	METER AUDIO 0 TO 1.2 VRMS
5 MHz -30 dBm IF IN	5	6	600 OHM REC. AUDIO OUT 0-2.4 VRMS
LOGIC "0" OR 1 $\overline{TX}$	7	8	
0 to +6 VDC (A3A) ACC "OR"	9	10	F.P. SQUELCH Ø V/4.5V (ON/OFF)
0 to +6 VDC AGC	11	12	3rd LO IN -15 dBm 5 MHz
	13	14	600 OHM REC. AUDIO OUT 0-2.4 VRMS
LOGIC "0" OR 1 $\overline{RX}$	15	16	$\overline{RX}$ LOGIC "0" OR 1
+9 VDC	17	18	+9 VDC (85 ma)
	19	20	
	21	22	SQUELCH GATE +7V/OV
GND	23	24	GND
	25	26	THRESH (FUTURE USE)
1 kHz 150 mVRMS SIDETONE	27	28	N.B. ON LOGIC "0" OR 1 (N.C)
LOGIC Ø OR 1 AGC OFF	29	30	$\overline{PTT}$ LOGIC "0" OR 1
	31	32	$\overline{MUTE}$ LOGIC "0" OR 1
	33	34	"RF" GAIN 0 to 5 VDC
LOGIC "0" OR 1 $\overline{USB}$	35	36	$\overline{CW}$ LOGIC "0" OR 1
LOGIC "0" OR 1 $\overline{LSB}$	37	38	AGC-F 0 to +9 VDC
LOGIC "0" OR 1 $\overline{FSK}$	39	40	DELAYED AGC +1 to +9 VDC
LOGIC 0 OR 1 AGC DUMP	41	42	"S" MTR 0 to 6 VDC
GND	43	44	GND

*OPTION NORMALLY NOT USED

4.18 SPEAKER AMPLIFIER BOARD, A13

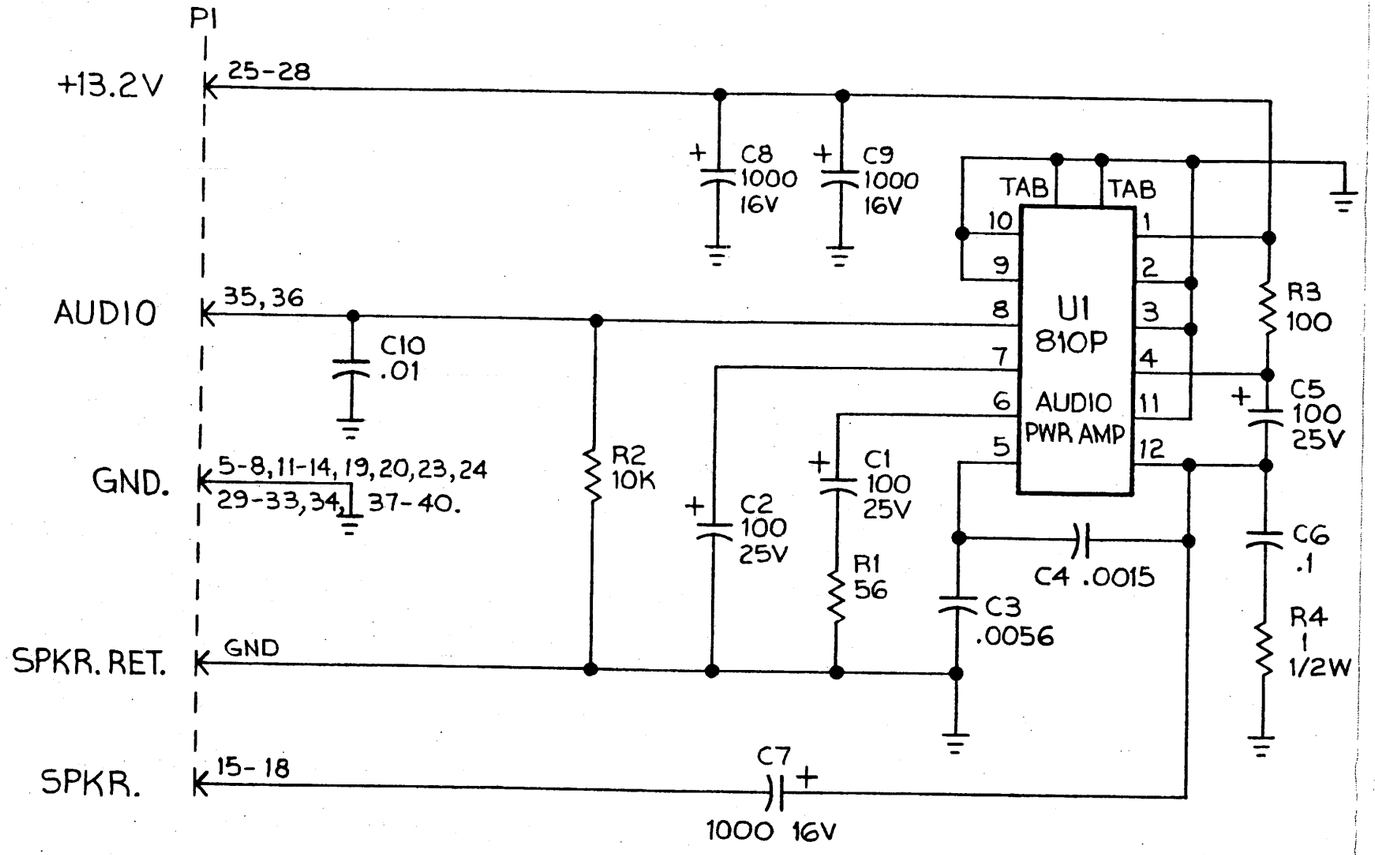
The Speaker Amplifier U1 is a monolithic audio amplifier in noninverting configuration. R1 sets the voltage gain at 37 dB. C3, 4, 6 and R4 are compensating elements. C5 is a bootstrap capacitor which allows the output to drive close to the supply voltage. The output, pin 12, is internally biased at half the supply voltage. The circuit is normally driven from the tap of a 10k potentiometer and drives a 3.2 ohm output speaker.



Speaker Amplifier (601311-536-001)

PART NUMBER	DESCRIPTION	SYMBOL
600184-419-001	HEATSINK	(U1)
600297-314-032	CAP. 100UF, ALUM, 25V	C1,2,5
600272-314-003	CAP. .01UF, CERAMIC, 50V	C10
600204-314-045	CAP. .0056UF, MYLAR, 630V	C3
600204-314-040	CAP. .0015UF, MYLAR, 630V	C4
600272-314-001	CAP. .1UF, CERAMIC, 50V	C6
600259-314-108	CAP. 1000UF, ALUM, 16V	C7,8,9
656094-341-075	RES. 56, 1/4W, 5%	R1
610024-341-075	RES. 10K, 1/4W, 5%	R2
610004-341-075	RES. 100, 1/4W, 5%	R3
610084-341-205	RES. 1, 1/2W, 5%	R4
600216-415-001	IC 810P, AUDIO AMP	U1

Figure 4.18-1 Speaker Amplifier Assembly



NOTES

1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS RATED IN OHMS, 1/4W, 5% AND ALL CAPACITORS RATED IN MFD.

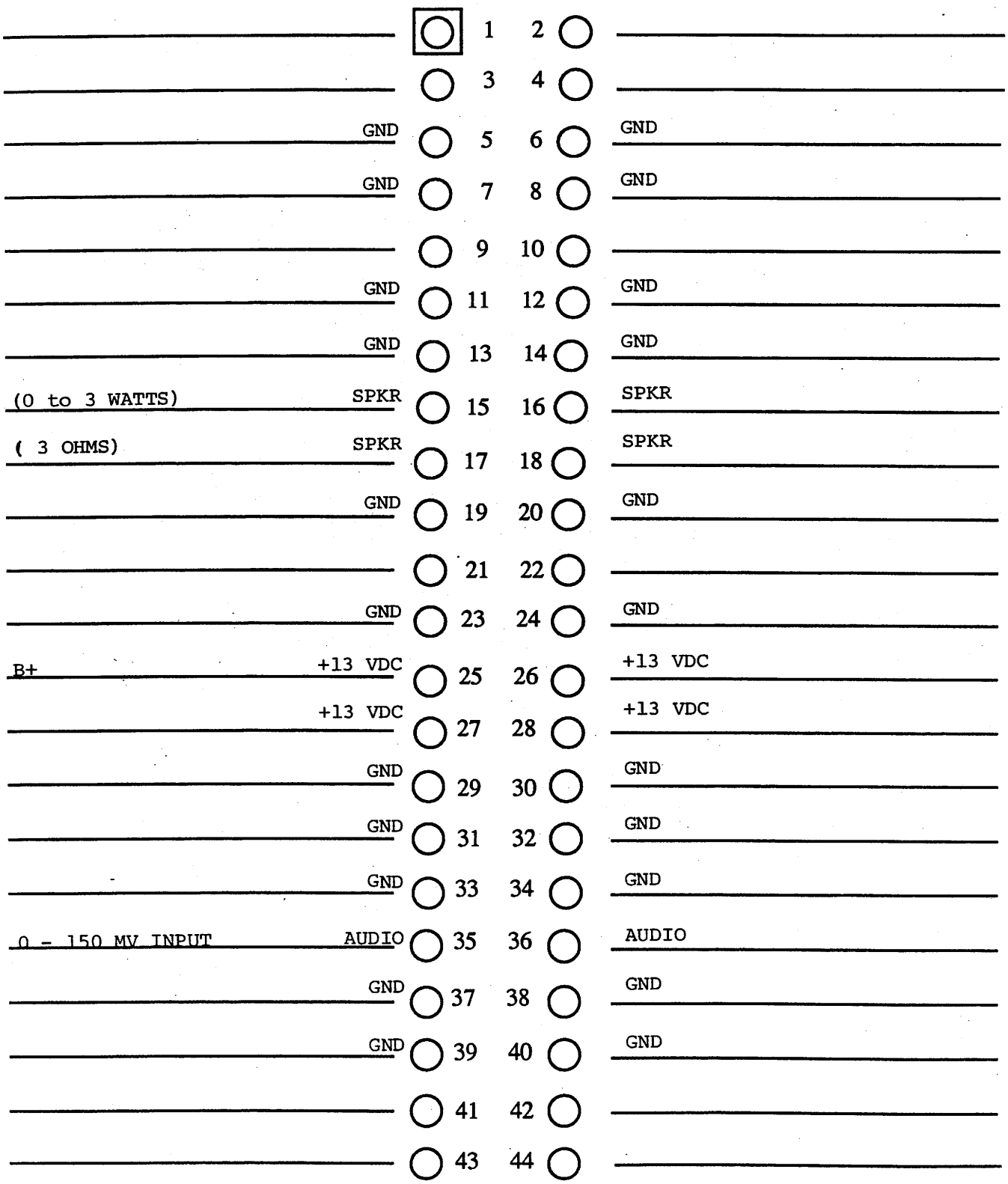
Figure 4.18-2

Speaker Amplifier Board Schematic

SPEAKER AMPLIFIER BOARD A13

PIN CONNECTIONS AND VOLTAGE READINGS

A13-P1



4.19 SYNTHESIZER BOARDS

This section electrically groups the synthesizer boards which produce the three local oscillator signals for frequency translation. Included are the Reference board A19, the Minor Loop board, A18, the Translator Loop board A17 and the Major Loop board A16. The third LO is normally a fixed five MHz signal from the Reference board. With the BFO option, the third LO is obtained from the optional BFO board. Figure 4.19-1 is a block diagram showing the interconnections and major functions within the boards.

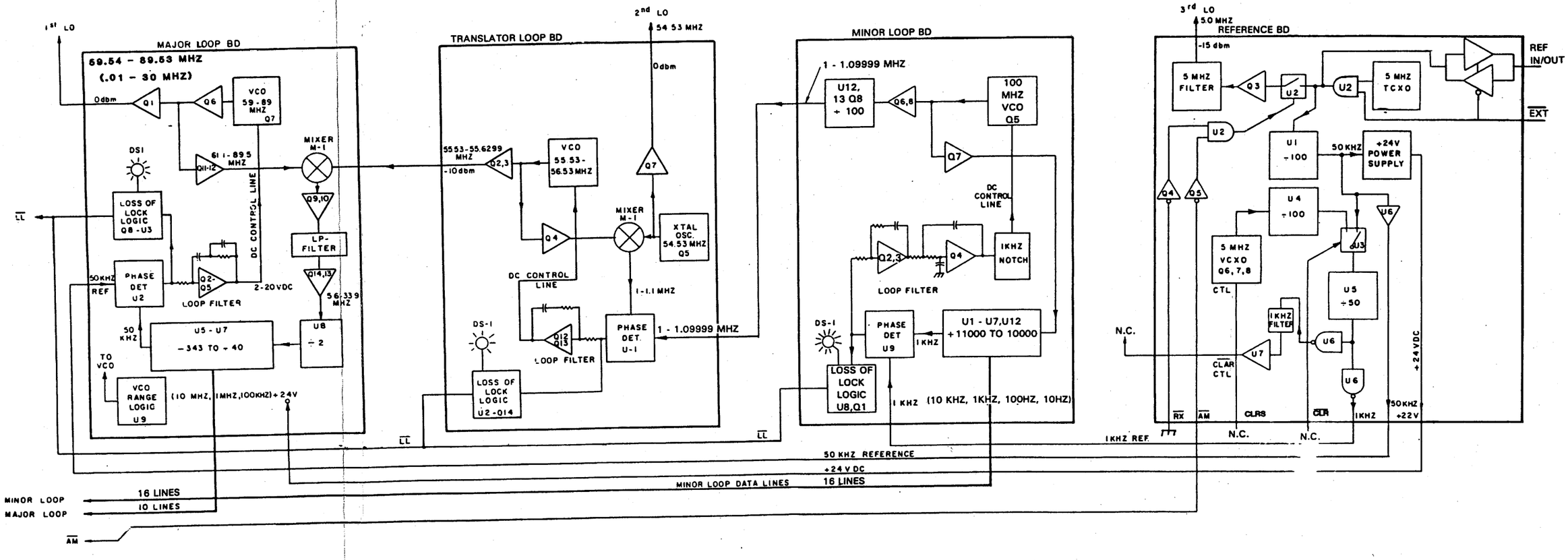


Figure 4.19-1

Synthesizer Block Diagram

4.19.1 REFERENCE BOARD

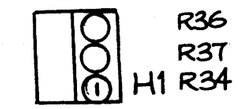
The Reference board contains the 5 MHz temperature compensated crystal oscillator (TCXO), from which are derived the 50 kHz reference for the major loop, the 1 kHz reference for the minor loop, the 1 kHz CW tone and the 5 MHz third LO signal. This board also contains the clarifier oscillator and a +24 volt bias supply for the major loop.

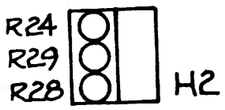
The TCXO output is connected to a coax connector J1 via a jumper and then to a nand gate buffer. With a high stability oven controlled oscillator (OCXO) installed in the radio, the jumper is removed and OCXO output replaces the TCXO signal via connector J1. Tristate buffers (U3) allow an external (rear panel) reference signal to be input to U2 pin 1 or allows the internal reference (either TCXO or OCXO) to be output via P9-12 depending on the $\overline{\text{EXT}}$ TTL input to P9-14 (from rear panel switch). Conditioned to accept an external reference, the internal signal at U2-10 is disabled by the TTL low at U2-9.

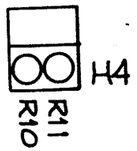
From U2 pin 8, the 5 MHz splits into two paths. One goes to the third LO switch, pin 1 of U2. The other goes to U1, a dual decade counter, which is connected to divide-by-100. The output of U1 on pin 3 is buffered by U6 pin 8, to become the 50 kHz reference signal to the Major Loop board. The 50 kHz signal also drives the voltage multiplier from U6 pin 10. Transistors Q1 and Q2 are high current drivers which drive the voltage multiplier with a 50 kHz square wave of approximately 11.5 volts peak-to-peak amplitude. Diodes CR2 through CR6 and associated capacitors form a voltage multiplier. The output is regulated to +24 volts at TP1 by zener CR1, and is designed to supply approximately 2 mA to the Major Loop board.

The $\overline{\text{AM}}$ and $\overline{\text{RX}}$ lines are buffered and inverted by Q4, Q5 and associated circuitry, and routed to pins 4 and 5 of U2. If the radio is in AM receive, the $\overline{\text{AM}}$ and $\overline{\text{RX}}$ lines will both be low, so pins 4 and 5 of U2 will both be high. This drives pin 6 (U2) low, which makes pin 3 high, inhibiting the third LO output. Transistor Q3 is an emitter-follower which drives the third LO output through a harmonic filter made up of L12, L6, L7, L11 and associated capacitors. The third LO output level is adjustable with R9. The output level is normally set to 0 dBm (.225 volts RMS).

The clarifier (not used in some radios) shifts the receive frequency by substituting a variable 1 kHz reference for the fixed 1 kHz, which normally supplies the minor loop. The clarifier oscillator, Q6, is a Colpitts configuration crystal oscillator whose operating frequency is determined principally by Y1, L10 and varicaps CR13 and CR12. The CLARIFIER control on the front panel varies the bias on the varicaps from 0 volts to +9 volts. This causes the frequency of the nominally 5 MHz oscillator to shift at least ±1250 Hz. The output is buffered by Q7, which drives U4, a dual decade counter which is connected to divide by 100 and gives a 50 kHz output at pin 9. The clarifier will be ON only if the RX line is low and CLRS (clarifier switch) line is low. If this is true, U2 pins 13 and 12 will be high, pin 11 will be low. This disables the pin 11 gate of U3. Since pin 3 is high, Q8 is turned on, which enables the clarifier oscillator. The 50 kHz at U3 pin 8, is now being supplied by the clarifier oscillator rather than the TCXO. U5 is connected to divide by 50 to produce 1 kHz at its output, pin 3. When the clarifier is on, the 1 kHz at TP3 will vary at least ±0.25 kHz with the clarifier control setting. The 1 kHz reference signal to the minor loop is provided by U6 pin 6. U6 pin 3 drives a three section RC filter which converts the square wave at pin 3 into a sine wave at R25. The lower amplifier of U7 is simply a voltage follower used to bias the upper half output at one half of the supply voltage. Pin 1 of U7 provides the 1 kHz tone output. Additional filtering of the signal is provided by C31 and R24. The frequency of the TCXO Y2 can be adjusted by first removing the access screw on the cover. A small screwdriver may be then used to adjust the frequency.







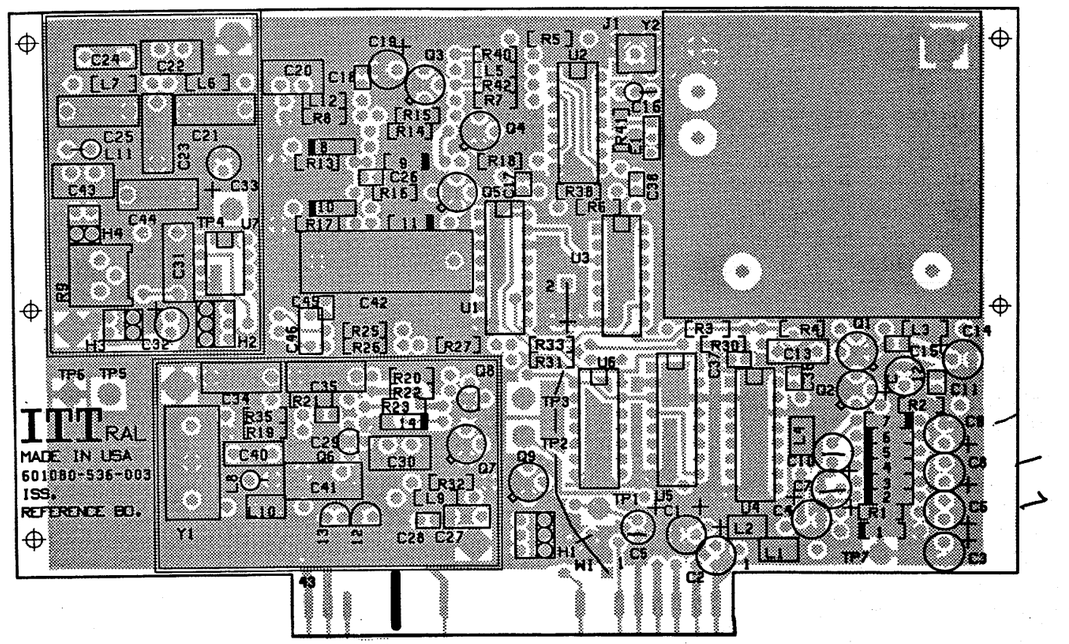


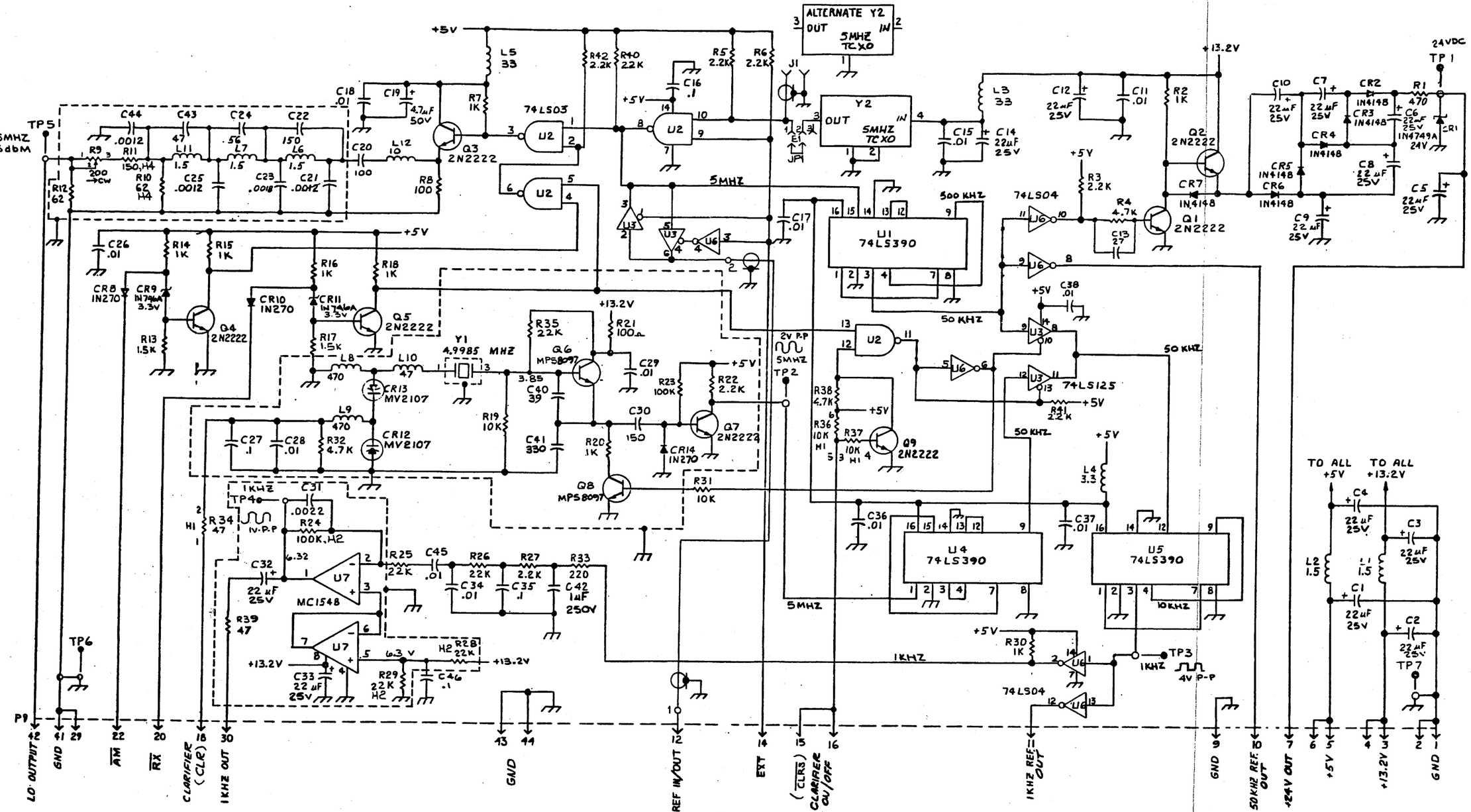
Figure 4.19-2

Reference Assembly

Reference (601080-536-003)

PART NUMBER	DESCRIPTION	SYMBOL
600417-230-001	STANDOFF #2-56X .81	
600014-608-022	22 AWG BUSS WIRE	
600297-314-016	CAP. 22UF, ALUM, 25V	C1-10,12, 14,32,33
600268-314-008	CAP. .01UF, CERAMIC, 50V	C11, 15-18, 26,28
600269-314-016	CAP. 27PF, CERAMIC, 500V	C13
600297-314-010	CAP. 4.7UF, ALUM, 50V	C19
610003-306-501	CAP. 100PF, 3%, MICA, 500V	C20
600204-314-039	CAP. .0012UF, MYLAR, 630V	C21,25 44
615003-306-501	CAP. 150PF, 3%, MICA, 500V	C22,30
600204-314-041	CAP. .0018UF, MYLAR, 630V	C23
600269-314-024	CAP. 56PF, CERAMIC, 100V	C24
600226-314-008	CAP. .1UF, CERAMIC, 50V	C27,46
600204-314-029	CAP. .0022UF, MYLAR, 1KV	C31
600204-314-001	CAP. .01UF, MYLAR, 400V	C34
600204-314-020	CAP. 0.1UF, MYLAR, 100V	C35
600269-314-020	CAP. 39PF, CERAMIC, 100V	C40
633003-306-501	CAP. 330PF, 3%, MICA, 500V	C41
600204-314-008	CAP. 1UF, MYLAR, 250V	C42
647093-306-501	CAP. 47PF, 3%, MICA, 500V	C43
600006-411-052	DIODE IN4749A 24V	CR1
600123-410-004	DIODE, VARACTOR, MV2107	CR12,13
600109-410-001	DIODE IN4148	CR2-7,15
600052-410-001	DIODE IN270	CR8,10,14
600002-411-001	DIODE, ZENER, 1N746A	CR9,11
600198-608-002	CONN. HEADER, 3 PIN, GOLD	E1

PART NUMBER	DESCRIPTION	SYMBOL
600064-419-003	3 POSITION VERTICAL MT	H1,2
600064-419-004	2 POSITION VERTICAL MT.	H3,4
600198-606-002	CONN MALE MIN. RF, PC MOUNT	J1
600190-608-001	CONN, JUMPER, 2 POS.	JP1
600125-376-033	CHOKE 1.5 UH	L1,2,6, 7,11
600072-376-033	CHOKE 47UH	L10
600125-376-032	CHOKE 10UH	L12
600125-376-007	CHOKE 33UH	L3,5
600125-376-006	CHOKE 3.3UH	L4
600125-376-015	CHOKE 470UH	L8,9
600080-413-001	TRANSISTOR 2N2222A	Q1-5, 7,9
600025-419-001	TRANSISTOR PAD	Q1-9
600278-413-001	TRANSISTOR MPS8097	Q6,8
647004-341-075	RES. 470, 1/4W, 5%	R1
662094-341-075	RES. 62, 1/4W, 5%	R10,12
615004-341-075	RES. 150, 1/4W, 5%	R11
615014-341-075	RES. 1.5K, 1/4W, 5%	R13,17
610024-341-075	RES. 10K, 1/4W, 5%	R19,31, 36,37
610014-341-075	RES. 1K, 1/4W, 5%	R2,7, 14-16, 18,20 30
610034-341-075	RES. 100K, 1/4W, 5%	R23,24
622024-341-075	RES. 22K, 1/4W, 5%	R25,26, 28,29,35
622014-341-075	RES. 2.2K, 1/4W, 5%	R3,5,6, 22,27 40,42
622004-341-075	RES. 220, 1/4W, 5%	R33
647094-341-075	RES. 47, 1/4W, 5%	R34,39
647014-341-075	RES. 4.7K, 1/4W, 5%	R4,32,38
610004-341-075	RES. 100, 1/4W, 5%	R8,21
600072-360-005	POT. 200, 1/2W, CERMET, TOP	R9
600535-415-001	IC 74LS390, 2 DEC RIP CNTR	U1,4,5
600239-415-001	IC 74LS03, NAND, O/C, 2-IN	U2
600274-415-001	IC 74LS125, BUFFER 3-ST	U3
600111-415-001	IC 74LS04, HEX INV	U6
600039-415-002	IC SN72558P	U7
600123-378-002	CRYSTAL, 4.99850 MHZ	Y1
600167-378-001	TCXO, 5MHZ	Y2



GRP-003

NOTES:

1. UNLESS OTHERWISE NOTED. RESISTORS ARE IN OHMS, 1/4W, ±5%; CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS (pF), VALUES LESS THAN ONE ARE IN MICROFARADS (μF); INDUCTORS ARE IN MICROHENRYS (μH).

Figure 4.19-3

Reference Board Schematic

REFERENCE BOARD, A19

PIN CONNECTIONS AND VOLTAGE READINGS

A19P9

GND	1	2	GND
+13 VDC	3	4	+13.2 VDC
+5 VDC	5	6	+5 VDC
+24V (±2V)	7	8	
GND	9	10	50 kHz REF.
(N.C.) 1 kHz REF. (W/CLARI.,+25 kHz)	11	12	REF. IN/OUT 5 MHz
	13	14	$\overline{\text{EXT}}$ REF
(N.C.) $\overline{\text{CLRS}}$	15	16	$\overline{\text{CLRS}}$ (N.C.)
	17	18	CLR (N.C.)
	19	20	$\overline{\text{RX}}$ (GND)
	21	22	$\overline{\text{AM}}$ LOGIC 1 OR 0
	23	24	
	25	26	
	27	28	
GND	29	30	1 kHz OUT
	31	32	
	33	34	
	35	36	
	37	38	
	39	40	
GND	41	42	5 MHz-15 dBm (3rd LO)
GND	43	44	GND

4.19.2 MINOR LOOP BOARD, A18

The Minor Loop generates the small (10 Hz) steps in the synthesizer. Its output, a 1.000 to 1.09999 MHz signal, is the reference for the Translator Loop.

The VCO (Q5, C1, C2, L1 and CR1) is a Colpitts oscillator whose frequency (100.000 to 109.999 MHz) is determined by the DC voltage at the junction of CR1 and C1. The VCO output drives two isolation buffers. The first (Q6 and associated components) drives a divide by 10 prescaler U12, whose output drives U13, a divide by 10 counter. The Minor Loop output (pin 12 of U13) is passed through a filter and then applied to Q8. The second buffer (Q7 and associated components) drives U11 which drives programmable divider U1 through U6.

The programmable divider functions in the following manner: U3, U4, U5 and U6 are parallel-loadable UP/DOWN counters which are cascaded and permanently connected to count DOWN. Counter U6 is the most significant digit and is permanently connected to load 10 each time its load line goes low; U1 is the least significant.

U7 is an array of open collector inverters which have their outputs connected together to form a NOR gate. The output (pins 2,4,6,8,10 and 12) can only go high if all the inputs (pins 1,3,5,9,11 and 13) are low. The U7 inputs are connected so that the output goes high when the counter (U6-U3) contains the number 002. To understand the operation, assume that the counter has just been loaded with the number 1240. The counters begin counting down. Because the D input (pin 2) is low, pin 5 of U2 (Q) stays low and pin 6 ($\overline{Q}$) stays high. After 10,000 pulses, U6 underflows and pin 1 (U7) goes low.

After another 100 pulses, U5 underflows and U7 (pin 3) goes low. After another 20 pulses, U4 underflows and U7 (pin 5) goes low. After another 2 pulses, pins 9,11 and 13 of U7 are low, so the "output" of number 0020 and the D input (pin 2 of U2) goes high again loading U1, U3, U5, and U6 with the divide number. The next pulse (number 000) toggles pin 6 high and pin 5 low. The cycle can now repeat. U1 controls the least significant number. When it overflows, it gets U2 (pin 9) which sets U11 to divide by 10 or 11.

The output of the programmable divider (U2, pin 5) is fed to the phase/frequency detector U9, where it is compared with the 1 kHz reference. If the divider output is too low in frequency (lagging the 1 kHz reference in phase), the phase detector output (pins 5 and 10) goes down. This causes the voltage of the VCO control line to rise, which raises the frequency to correct the error.

The Loop Amplifier consists of Q2 and Q3, which form a high input impedance inverting stage. The amplifier and feedback components (R20, R19, C31 and C32) form an active loop filter which determines the overall loop stability. Transistor Q4 with components R17, R16, C28 and C27, forms an active low pass filter with a sharp corner and steep roll-off to attenuate reference sidebands. Compo-nents R11, R10 and R12, and C24, C25 and C23, form a Twin-T notch filter centered on 1 kHz to further attenuate the first order sidebands.

The loss-of-lock circuitry works as follows: phase detector outputs pin 11 and pin 4 are normally high with nearly 100 percent duty cycle in a properly locked loop. This means that the base and therefore, the emitter of Q1 is also high, driving pin 2 of U8 low. This makes pins 12 and 4 of U8 high so the LED is off. When the loop loses lock, the duty cycle will drop at either pin 11 or pin 4 of U9. This discharges C35 through R24 faster than it can be recharged by R22 so the base voltage of Q1 drops, causing pin 2 of U8 to go high. This turns on the LED and drives the LL line low. The pin number (11 or 4) that goes low in loss-of-lock, depends on whether the VCO frequency is too high or too low.

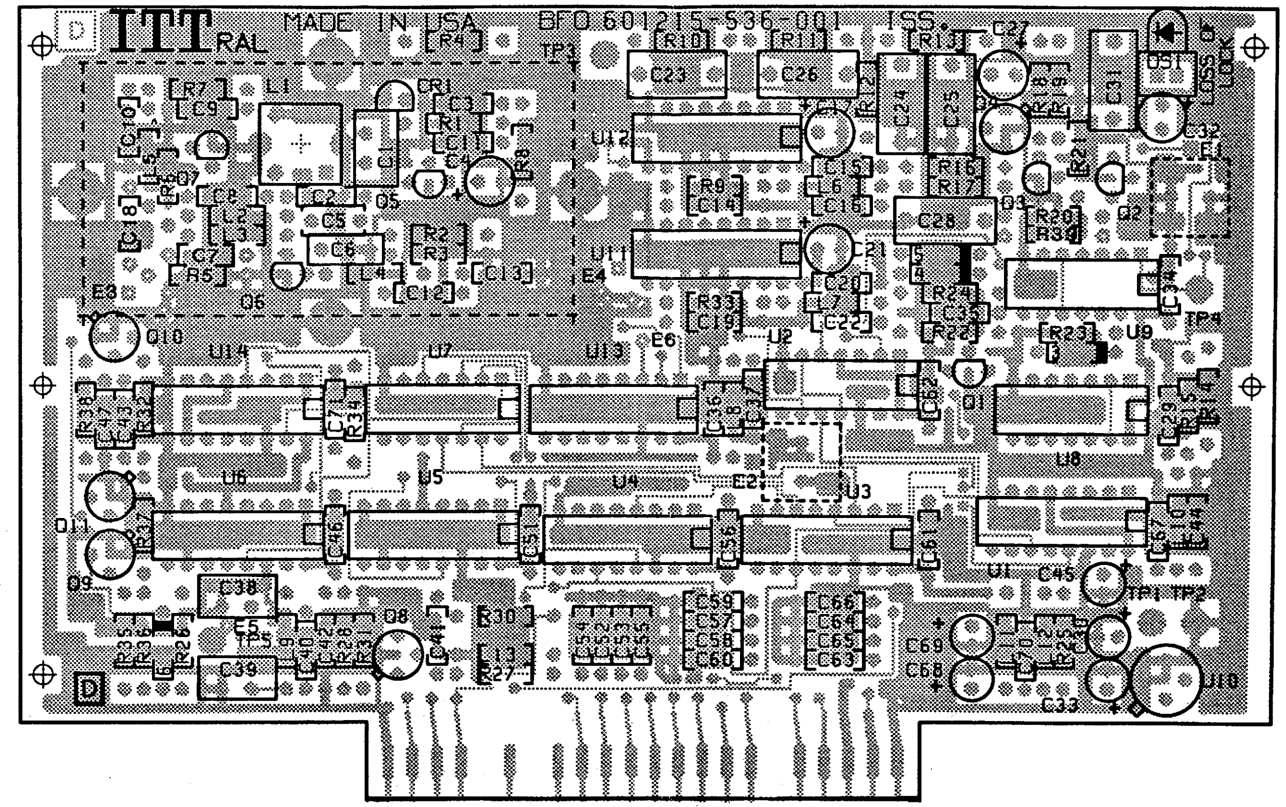
An on-card 8-volt regulator (U10) supplies the linear circuits with clean power. Table 4.19-2 lists the Minor Loop output frequency and divider input frequency information.

Table 4.19-1 MINOR LOOP IN LOCK VOLTAGES

LAST 4 DIGITS OF FREQUENCY	ADJUST	DC VOLTS AT TP3
0000	L1	2.2 ± .02V
9999		5.5 - 6.5V

Table 4.19-2 MINOR LOOP FREQUENCY INFORMATION

LAST 3 DIGITS OF RX or TX FREQ. MHz	VCO FREQ MHz	PROGRAM NUMBER		
		10 kHz	1 kHz	100 Hz
000	1.0000	0	0	0
001	1.0001	0	0	1
002	1.0002	0	0	2
003	1.0003	0	0	3
004	1.0004	0	0	4
005	1.0005	0	0	5
006	1.0006	0	0	6
007	1.0007	0	0	7
008	1.0008	0	0	8
009	1.0009	0	0	9
010	1.0010	0	1	0
020	1.0020	0	2	0
030	1.0030	0	3	0
040	1.0040	0	4	0
050	1.0050	0	5	0
060	1.0060	0	6	0
070	1.0070	0	7	0
080	1.0080	0	8	0
090	1.0090	0	9	0
100	1.0100	1	0	0
200	1.0200	2	0	0
300	1.0300	3	0	0
400	1.0400	4	0	0
500	1.0500	5	0	0
600	1.0600	6	0	0
700	1.0700	7	0	0
800	1.0800	8	0	0
900	1.0900	9	0	0



Minor Loop (601214-536-001)

PART NUMBER	DESCRIPTION	SYMBOL
647093-306-501	CAP. 47PF, 3%, MICA, 500V	C10
600272-314-001	CAP. .1UF, CERAMIC, 50V	C3,7-9, 11,12,15, 16,18,20, 22,29,34, 35,37,40, 41,46,47, 51-67, 70,71
600272-314-003	CAP. .01UF, CERAMIC, 50V	C18,20 22,29 34,35
600272-314-005	CAP. 470PF, CERAMIC, 50V	C2,10 13,43
600204-314-027	CAP., 100V MYLAR	C23-26, 28,31
600297-314-016	CAP. 22UF, ALUM, 25V	C30,33, 45,68, 69
647093-306-501	CAP. 47PF, 3%, MICA, 500V	C38,39
600202-314-007	CAP. 1UF, 35V, TANT.	C4,17,21 27,32
600269-314-006	CAP. 5.6PF, CERAMIC, 500V	C5
600269-314-020	CAP. 39PF, CERAMIC, 100V	C6
600123-410-003	DIODE, VARACTOR, MV2106	CR1
600109-410-001	DIODE IN4148	CR3-6
600036-390-001	LED, RED	DS1
600173-376-001	COIL, VAR, .1UH	L1
600125-376-028	CHOKE .1UH	L2,3
600125-376-027	CHOKE .47UH	L4,5
600125-376-016	CHOKE 2.2UH	L6,7
600125-376-006	CHOKE 3.3UH	L8,10-12
600125-376-008	CHOKE 47UH	L9,13

PART NUMBER	DESCRIPTION	SYMBOL
600278-413-001	TRANSISTOR MPS8097	Q1-3
600154-413-001	TRANSISTOR 2N2907A	Q4
600259-413-001	TRANSISTOR J310	Q5-7
600080-413-001	TRANSISTOR 2N2222A	Q8-11
610024-341-075	RES. 10K, 1/4W, 5%	R1,38
652311-342-059	RES., 5.23K, 1/8W, 1%	R10,11
626111-342-059	RES. 2.61K 1/8W 1%	R12
633004-341-075	RES. 330, 1/4W, 5%	R14
620014-341-075	RES. 2K, 1/4W, 5%	R15,20,23
636014-341-075	RES. 3.6K, 1/4W, 5%	R16,17
647014-341-075	RES. 4.7K, 1/4W, 5%	R18,24, 32,35,36
630024-341-075	RES. 30K, 1/4W, 5%	R19
622004-341-075	RES. 220, 1/4W, 5%	R2,3
610034-341-075	RES. 100K, 1/4W, 5%	R21,22
647004-341-075	RES. 470, 1/4W, 5%	R27,34
633014-341-075	RES. 3.3K, 1/4W, 5%	R28
662004-341-075	RES. 620, 1/4W, 5%	R30
622014-341-075	RES. 2.2K, 1/4W, 5%	R31
622024-341-075	RES. 22K, 1/4W, 5%	R37
622054-341-075	RES. 22M, 1/4W, 5%	R39
610094-341-075	RES. 10, 1/4W, 5%	R4
612004-341-075	RES. 120, 1/4W, 5%	R5,6
610004-341-075	RES. 100, 1/4W, 5%	R7,8
610014-341-075	RES. 1K, 1/4W, 5%	R9,13, 26,33
651094-341-075	RES. 51, 1/4W, 5%	R25
600225-415-001	IC 74LS192, UP/DN CNTR, SYNC	U1,3-6,14
600157-415-001	IC 74S74, D FLIP-F, DUAL	U2
600240-415-001	IC 74LS05, HEX INV, O/C	U7,8
600092-415-001	IC MC4044, PHASE DET.	U9
600526-415-001	IC 78M08, 8V REG	U10
600241-415-001	IC 2013, 2-MOD	U11,12
600535-415-001	IC 74LS390, 2 DEC RIP CNTR	V13

Figure 4.19-4

Minor Loop Assembly

NOTES

1. UNLESS OTHERWISE SPECIFIED; ALL RESISTORS ARE RATED IN OHMS, 1/4W ±5%; ALL CAPACITORS RATED IN MICROFARADS; ALL INDUCTORS RATED IN MICROHENRIES.

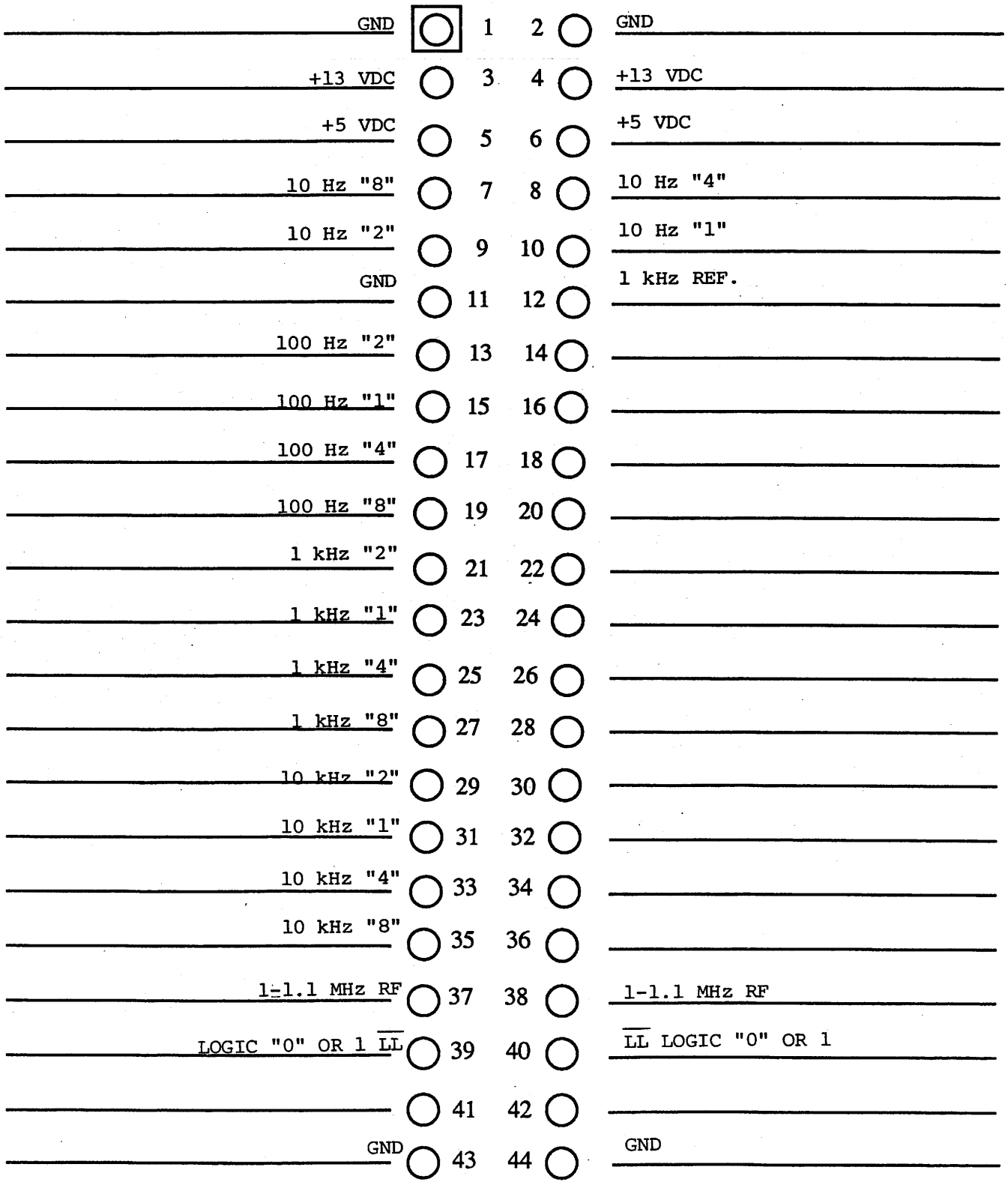
Figure 4.19-5

Minor Loop Board Schematic

MINOR LOOP BOARD, A18

PIN CONNECTIONS AND VOLTAGE READINGS

A18P1



4.19.3 TRANSLATOR LOOP BOARD, A17

The Translator Loop board provides the 55.530 to 55.6299 MHz signal for use by the Major Loop and provides the 54.53 MHz second LO for the Receiver/Exciter.

The second LO signal is generated by a Colpitts configuration crystal oscillator, Q6 and associated components. The crystal is a parallel resonant type and is adjusted on frequency by trimmer C61. An uncompensated crystal can be used because both the first and second LO signals are derived from it, so any 54.53 MHz frequency drift cancels in the transmit and receive frequency, leaving the overall frequency stability dependent only on the TCXO reference oscillator.

The output of the 54.53 MHz oscillator is split into two paths. One path goes to buffer Q5, which drives mixer M1. The other path goes to buffer Q7, which provides the 0 dBm second LO output. The output amplitude can be adjusted to 0 dBm by C64. Components L13, C39, C46 and C41 form a harmonic filter.

The Translator output is the sum of the second LO (54.53 MHz) and the Minor Loop output (1.00000 to 1.09999 MHz).

The VCO, consisting of Q1, L6, C63, C60 and associated components, is a Colpitts oscillator whose frequency is varied by changing the control line voltage at TP6. A change in the DC voltage here will change the bias on varicap CR4, changing the VCO tank capacitance and thus, the VCO frequency.

The output signal is split into two paths. One path goes through output level adjust C15, then to cascode amplifier Q2 and Q3.

The cascode amplifier provides excellent reverse isolation and a -10 dBm output level through Harmonic Filter L3, L2 and associated capacitors. The other path from the VCO goes to buffer Q4, which drives pin 8 of mixer M1. The output of the mixer (pins 3 and 4) is a 1.00000 to 1.09999 MHz signal. This signal is amplified by a 15 dB amplifier (Q8, Q9 and associated components) and then coupled through R54 and C57 to Lowpass Filter L14, L16, C54, C55 and C56, to provide a 100 millivolt p-p signal at TP4. From here, the signal is amplified by high gain common emitter amplifiers Q10 and Q11 to generate a 4 volt p-p waveform for the loop input to the phase/frequency detector (pin 1). the reference frequency is the 1.00000 to 1.09999 MHz signal from the Minor Loop and is fed to pin 3 of U1. Thus, the loop translator causes the VCO to generate a frequency, which when 54.53 MHz is subtracted by M2, is the same as the minor loop input frequency.

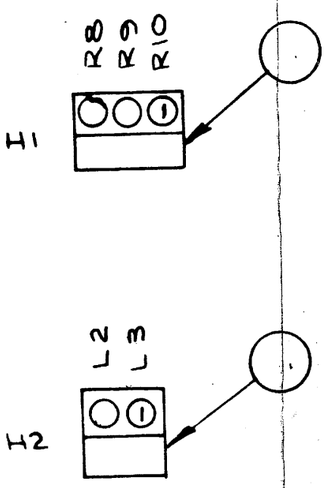
The output of phase detector, U1 is at pins 5 and 10 and is a high impedance when the loop is locked. This output is connected to a lead-lag type active loop filter consisting of Q12, Q13, R42, R41,C48, C47 and R40. The filter output goes through R43 to TP6. Diode CR7 prevents the voltage at TP6 from dropping below 4.3 volts and the VCO frequency from falling below 54.53 MHz, which would cause a false lock. The loss-of-lock circuitry works as follows.

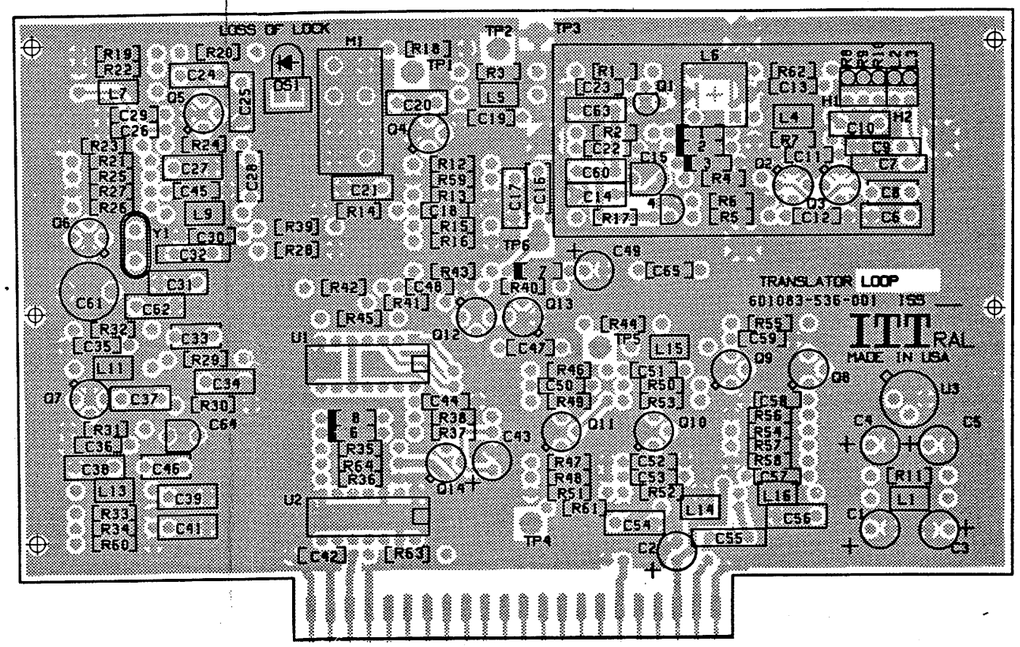
Phase detector outputs, pin 11 and pin 4, are normally high with nearly 100% duty cycle in a properly locked loop. This means that the base, and therefore the emitter of Q14 is also high, driving pin 6 of U2 low. This makes pins 8 and 10 of U2 high, so the LED is off. When the loop loses lock, the duty cycle will drop at either pin 11 or pin 4 (of U1). This discharges C43 through R37 faster than it can be recharged by R38, so the base voltage of Q14 drops causing pin 6 of U2 to go high. This turns on the LED and drives the LL line low. The pin number (11 or 4) that goes low in loss-of-lock depends on whether the VCO frequency is too high or too low.

As an on-card 8-volt regulator, U3 supplies the linear circuits with clean power.

Table 4.19-3 TRANSLATOR IN LOCK VOLTAGES

LAST 4 DIGITS OF FREQUENCY	ADJUST	DC VOLTS AT TP3
0000	L6	5.6 - 5.8V
9999		5.9 -6.2V





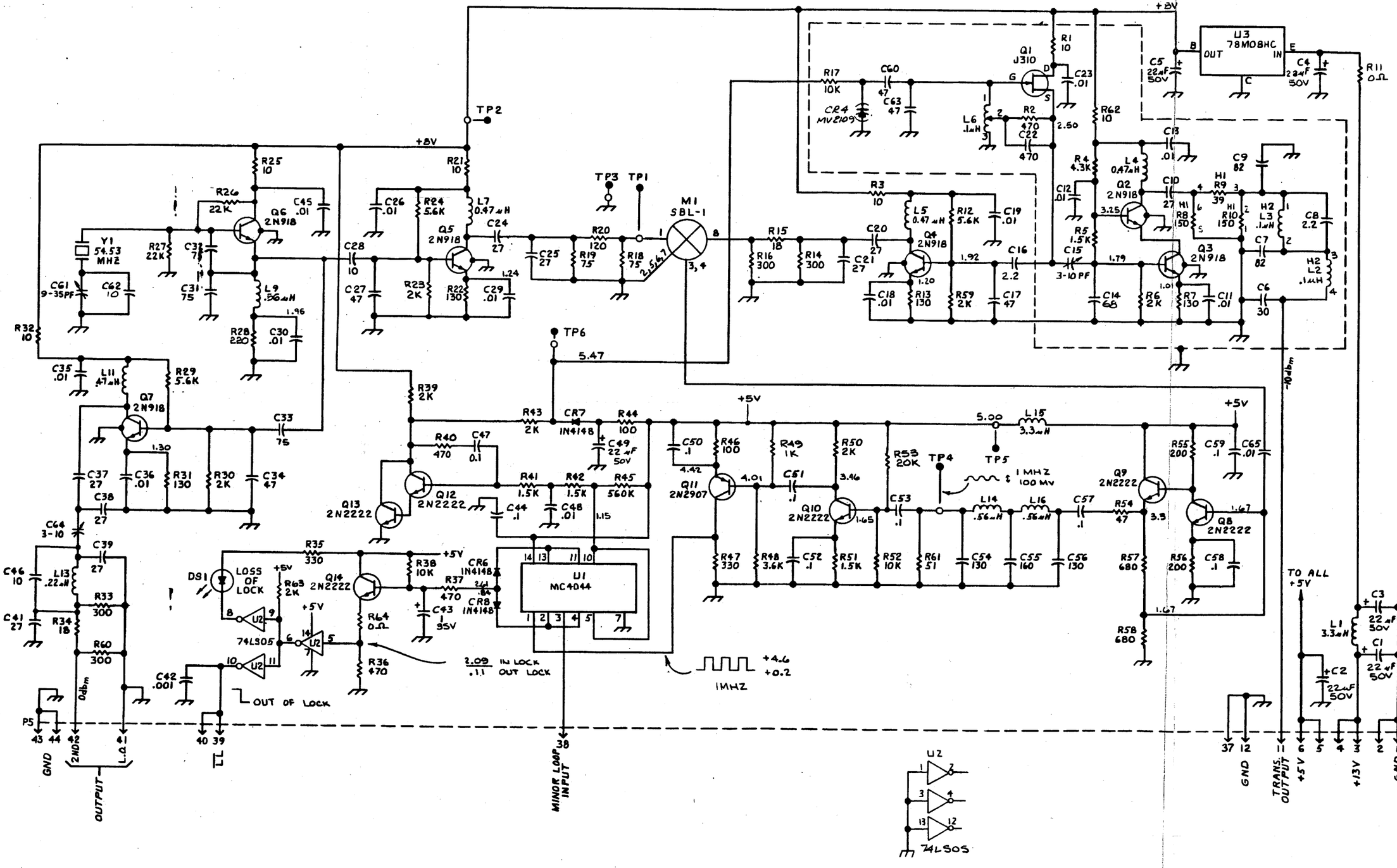
Translator Loop (601083-536-001)

PART NUMBER	DESCRIPTION	SYMBOL
600145-419-001	HEATSINK	
600297-314-018	CAP. 22UF, ALUM, 50V	C1-5,49
600269-314-016	CAP. 27PF, CERAMIC, 500V	C10,20, 21,24,25, 37-39,41
600272-314-003	CAP. .01UF, CERAMIC, 50V	C11-13, 18,19, 23,26, 29,30,35, 36,45,48, 65
600269-314-026	CAP. 68PF, CERAMIC, 100V	C14
600052-317-001	CAP. VAR, 3-10PF	C15,64
600269-314-022	CAP. 47PF, CERAMIC, 100V	C17,2[illegible], 34,6[illegible]63
600272-314-005	CAP. 470PF, CERAMIC, 50V	C22
600269-314-009	CAP. 10PF, CERAMIC, 500V	C28,46,62
600269-314-027	CAP. 75PF, CERAMIC, 100V	C31,32,33
600272-314-008	CAP. .001UF, CERAMIC, 50V	C42
600202-314-007	CAP. 1UF, 35V, TANT.	C43
600272-314-001	CAP. .1UF, CERAMIC, 50V	C44,50-53
600204-314-020	CAP. 0.1UF, MYLAR, 100V	C47
600269-314-033	CAP. 130PF, CERAMIC, 100V	C54,65
600269-314-035	CAP. 160PF, CERAMIC, 100V	C55
600269-314-017	CAP. 30PF, CERAMIC, 500V	C6
600018-317-004	CAP. VAR, 9-35PF	C61
600269-314-028	CAP. 82PF, CERAMIC, 100V	C7,9
600269-314-002	CAP. 2.2PF, CERAMIC, 500V	C8,16
600123-410-008	DIODE, VARACTOR, MV2109	CR4
600109-410-001	DIODE IN4148	CR6-8
600036-390-001	LED, RED	DS1
600064-419-003	3 POSITION VERTICAL MT	H1
600064-419-004	2 POSITION VERTICAL MT.	H2
600125-376-006	CHOKE 3.3UH	L1,15
600125-376-003	CHOKE .22UH	L13
600125-376-028	CHOKE .1UH	L2,3
600125-376-027	CHOKE .47UH	L4,5,7,11
600173-376-001	COIL, VAR, .1UH	L6

PART NUMBER	DESCRIPTION	SYMBOL
600125-376-005	CHOKE .56UH	L9,14,16
600008-455-001	MIXER SLB-1	M1
600259-413-001	TRANSISTOR J310	Q1
600154-413-001	TRANSISTOR 2N2907A	Q11
600025-419-001	TRANSISTOR PAD	Q2-14
600085-413-001	TRANSISTOR 2N918	Q2-7
600080-413-001	TRANSISTOR 2N2222A	Q8-10, 12-14
610094-341-075	RES. 10, 1/4W, 5%	R1,3,21, 25,32,62
600000-341-075	RES. 0, 1/4W, 5%	R11,64
656014-341-075	RES. 5.6K, 1/4W, 5%	R12,24,29
630004-341-075	RES. 300, 1/4W, 5%	R14,16, 33,60
618094-341-075	RES. 18, 1/4W, 5%	R15,34
610024-341-075	RES. 10K, 1/4W, 5%	R17,38,52
675094-341-075	RES. 75, 1/4W, 5%	R18,19
647004-341-075	RES. 470, 1/4W, 5%	R2,36
612004-341-075	RES. 120, 1/4W, 5%	R20
622024-341-075	RES. 22K, 1/4W, 5%	R26,27
622004-341-075	RES. 220, 1/4W, 5%	R28
633004-341-075	RES. 330, 1/4W, 5%	R35,47
643014-341-075	RES. 4.3K, 1/4W, 5%	R4
610004-341-075	RES. 100, 1/4W, 5%	R44,46
656034-341-075	RES. 560K, 1/4W, 5%	R45
636014-341-075	RES. 3.6K, 1/4W, 5%	R48
610014-341-075	RES. 1K, 1/4W, 5%	R49
615014-341-075	RES. 1.5K, 1/4W, 5%	R5,41, 42,51
620024-341-075	RES. 20K, 1/4W, 5%	R53
647094-341-075	RES. 47, 1/4W, 5%	R54
620004-341-075	RES. 200, 1/4W, 5%	R55,56
668004-341-075	RES. 680, 1/4W, 5%	R57,58
620014-341-075	RES. 2K, 1/4W, 5%	R6,23,30, 39,43, 50,59,63
651094-341-075	RES. 51, 1/4W, 5%	R61
613004-341-075	RES. 130, 1/4W, 5%	R7,13, 22,31
615004-341-075	RES. 150, 1/4W, 5%	R8,10
639094-341-075	RES. 39, 1/4W, 5%	R9
600261-230-001	TERMINAL	TP1-6
600092-415-001	IC MC4044, PHASE DET.	U1
600240-415-001	IC 74LS05, HEX INV, O/C	U2
600017-419-001	TRANSISTOR PAD	U3
600526-415-001	IC 78M08, 8V REG	U3
600005-635-001	LED MOUNT	XDS1
600163-378-001	CRYSTAL, 54.53 MHZ	Y1

Figure 4.19-6

Translator Loop Assembly



NOTES:
1. UNLESS OTHERWISE NOTED:
   RESISTORS ARE IN OHMS, 1/4W, ±5%
   CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS (pF), VALUES LESS THAN ONE ARE MICROFARADS(uF).

LAST DESIG. USED
R64, C63, CR8, DS1, L16, Q14, M1, TP6, U3, Y1
DELETED
L8, L10, CR1-3

Figure 4.19-7

Translator Loop Board Schematic

TRANSLATOR LOOP BOARD, A17

PIN CONNECTIONS AND VOLTAGE READINGS

A17-P5

GND	1	2	GND
+13 VDC	3	4	+13 VDC
	5	6	+5 VDC
	7	8	
	9	10	
(-10 dBm) 55.53-55.6299 MHz	11	12	GND
	13	14	
	15	16	
	17	18	
	19	20	
	21	22	
	23	24	
	25	26	
	27	28	
	29	30	
	31	32	
	33	34	
	35	36	
GND	37	38	MINOR LOOP INPUT 1-1.1 MHz
LOGIC "0" OR 1 $\overline{LL}$	39	40	$\overline{LL}$ LOGIC "0" OR 1
(2nd LO) 54.53 MHz -10 dBm	41	42	54.53 MHz -10 dBm (2nd LO)
GND	43	44	GND

4.19.4 MAJOR LOOP BOARD, A16

The Major Loop provides the first local oscillator (LO) signal (59.53 MHz to 89.53 MHz) for the first mixer in the signal path. The loop itself uses a 50 kHz reference frequency and generates 10 MHz, 1 MHz and 100 kHz steps. Smaller step sizes are possible by stepping the translator RF input to the Major Loop from 55.53 MHz to 55.6299 MHz. The Translator Loop takes 10 Hz steps over this range, which also gives the Major loop output 10 Hz steps. The smaller step sizes are actually generated by the Minor Loop, so different step sizes are possible by changing Minor Loops.

The VCO, Q7 is a Colpitts oscillator with three switched ranges. The VCO control line is the junction of varicaps CR7 and CR8 driven through decoupling choke, L4. The oscillator covers 59.53 MHz to 89.53 MHz in three course ranges (see Table 4.19-4). This keeps the loop gain expression kvkp/N * nearly constant, which insures that loop dynamics (stability, settling time) are constant throughout the range. Range switching is accomplished by pin diodes CR13 and CR2. The top range has only varicaps CR7 and CR8 in combination with L3 determining the VCO frequency. In the middle range, CR2 is turned on, which puts C71 and C73 in parallel with the varicaps. In the low range, CR2 remains on and CR13 turned on, which adds parallel capacitors C72 and C74 to the tank circuit. Diodes CR4, CR5 and CR6 limit the oscillation amplitude. Resistor R23 sets the static FET operating point, and unbypassed resistor R13 degenerates the gain slightly to limit high order harmonic production. The output of Q6 is taken from 3:1 broadband transformer L1 (L7 and L8 are similar transformers) and fed to two additional buffers. Cascode amplifiers Q12 and Q11 provide extremely good reverse isolation (70 to 80 dB) and feeds mixer M1.

The first LO output is from buffer Q1. Components L9, L10, C42, C43 and C77 provide harmonic filtering. R52 is used to adjust the output level.

The Translator Loop frequency is fed to pin 1 of mixer M1 and the VCO is fed to pin 8. The output on pins 3 and 4 is amplified to Q9 and Q10 and fed to a bandpass filter consisting of L5, L6 and associated capacitors. The filter passes the difference frequency of 4 to 33.9 MHz to be further amplified by Q13 and Q14. Both the sum FVCO + FTRANS and difference FVCO - FTRANS are present in the mixer output. The output is fed to the clock input of U8, which is a D flip-flop connected to toggle (÷2). Resistors R44 and R48 bias U8's clock input at threshold for reliable triggering. The presence of the ÷2 is compensated for by using a 50 kHz (not 100 kHz) reference signal for the loop.

The programmable divider determines the VCO frequency in the following manner: the output of the programmable divider (U8, pin 9) is always 50 kHz if the loop is locked. The input frequency (U8, pin 9) is always 50 kHz if the loop is locked. The input frequency (U8, pin 11) then is N x 50 kHz where N is the programmed divide number. Working back up to the VCO: (N x 50 kHz x 2) + FTRANS + FVCO.

The programmable divider functions in the following manner: U5, U6 and U7 are parallel - loadable UP/DOWN counters which are cascaded and permanently connected to count DOWN. Counter U5 is the most significant digit; U7 the least significant. U4 is an array of open collector inverters which have their outputs connected together to form a NOR gate. The output (pins 4,6,8,10 and 12) can only go high if all the inputs (pins 3,5,9,11 and 13) are low. The U4 inputs are connected so that the output goes high when the counter (U5-U7) contains the number 002. To understand the operation, assume that the counter has just been loaded with the number 124. The counters begin counting down. Because of the D input, pin 12 is low, pin 9 of U8 (Q) stays low and pin 8 ($\overline{Q}$) stays high. After 100 pulses, U5 underflows and U4, pin 3 goes low. After another 2 pulses, U6 underflows and U4, pin 5 goes low. After another 2 pulses, pins 9, 11 and 13 of U8 are low, so the "output" of U4, pins 4,6,8,10 and 12 can go high.

The counter now contains the number 002 and the D input, pin 12 of U8 goes high (this is the programmable divider output pulse). The pin goes low, again loading U5, U6 and U7 with the divide number. The next pulse (number 000) toggles pin 8 high and pin 9 low. The cycle can now repeat.

The output of the programmable divider (U8, pin 9) is fed to the phase/frequency detector U2, where it is compared with the 50 kHz reference. If the divider output is too low in frequency or lagging the 50 kHz reference in phase, the phase detector output (pins 5 and 10) goes down. This causes the voltage of the VCO control line to rise, which raises the frequency to correct the error.

The loop amplifier consists of Q5, Q4 and Q3, which form a high input impedance inverting stage.The amplifier and feed-back components (C7, R12, R11 and C8) form an active loop filter which determines the overall loop stability. Transistor Q2, with components R10, R58, C12 and C66, forms an active lowpass filter with a sharp corner and steep roll-off to attenuate the reference sidebands. The amplifier and active lowpass are fed +24 volts from the Reference board. The +24 volts is needed to increase the varicap range.

The loss-of-lock circuitry works as follows: phase detector outputs, pin 11 and pin 4, are normally high with nearly 100% duty cycle in a properly locked loop. This means that the base, and therefore the emitter of Q8, is also high, driving pin 4 of U3 low. This makes pins 2 and 6 of U3 high so the LED is off. When the loop loses lock, the duty cycle will drop at either pin 11 or 4 (of U2). This discharges C25 through R32 faster than it can be recharged by R25, so the base voltage of Q8 drops, causing pin 4 of U3 to go high. This turns on the LED and drives the LL line low. The pin number (11 or 4) that goes low in loss-of-lock, depends on whether the VCO frequency is too high or too low.

An on-card 8-volt regulator, U1, supplies the linear circuits with clean power.

While a complete discussion of loop theory is beyond the scope of this technical description, the following is an extremely simplified explanation.

The loop response time and setting time depends on the time constants of the loop filter components and the loop "gain" kvkp/N. Where kv is the VCO transfer constant in Radian/Sec/Volt, kp is the phase detector constant in Volts/Radian, and N is the programmable divide number. Typical numbers for the major loop might be:

kv = 3.14 x 106
kp = .44 so kvkp = 11.1 x 103
N = 124

Table 4.19-4 lists Major Loop VCO output frequency and divider program information.

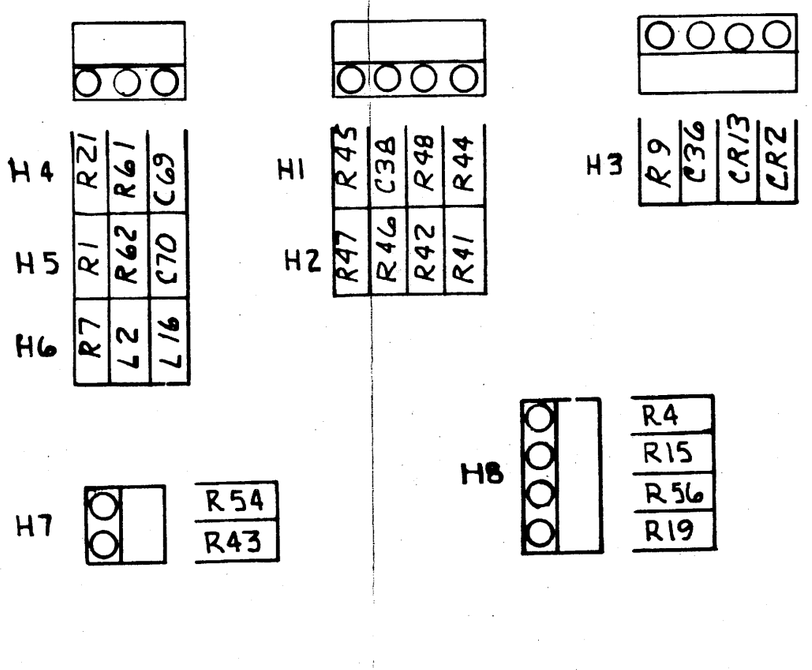
Table 4.19-4

MAJOR LOOP FREQUENCY INFORMATION

FIRST 3 DIGITS OF RX or TX FREQ. MHz	VCO FREQ. MHz	PROGRAM NUMBER	U9 PIN 8	U9 PIN 6	CR13	CR2
160 5.90	61.13 65.43	056 to 099	LOW	LOW	ON	ON
6.00 15.90	65.53 75.43	100 to 199	HIGH	LOW	ON	OFF
16.00 29.90	75.53 89.43	200 to 399	HIGH	HIGH	OFF	OFF

FIRST 3 DIGITS OF FREQUENCY MHz	ADJUST	DC VOLTS TP2
29.9	L3	18.4 to 18.6
16.0		3.6 to 5.00
15.9	C72	18.2 to 18.7
06.0		2.9 to 4.5
05.9	C73	18.2 to 18.7
01.6		5.50 to 5.70

Major Loop In-Lock Loop Voltage



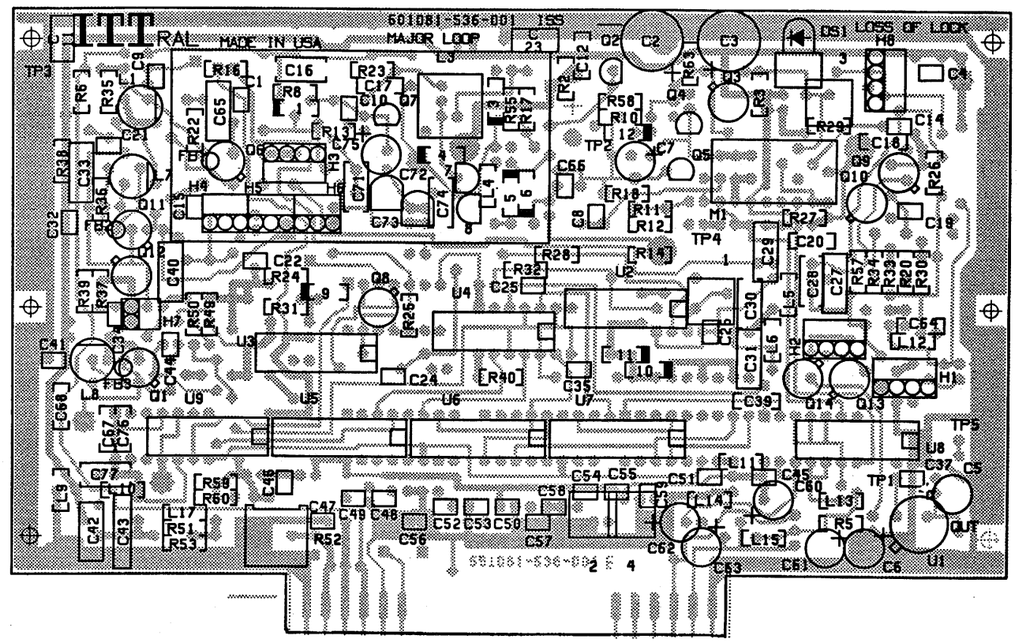


Figure 4.19-8

Major Loop Assembly

Major Loop (601081-536-001)

PART NUMBER	DESCRIPTION	SYMBOL
600145-419-001	HEATSINK	
600025-419-001	TRANSISTOR PAD	
600268-314-008	CAP. .01UF, CERAMIC 50V	C1,4,9, 10,14,19, 21,22, 24-26,32, 34,35,37, 41,44-59
600226-314-014	CAP. 1UF, CERAMIC, 50V	C11,23
600272-314-008	CAP. .001UF, CERAMIC, 50V	C12
600267-314-002	CAP. 100PF, CERAMIC, 100V	C15
600269-314-002	CAP. 2.2PF, CERAMIC, 500V	C16,28
600272-314-005	CAP. 470PF, CERAMIC, 50V	C17,36 68,69,70
600272-314-001	CAP. .1UF, CERAMIC, 50V	C18,20, 38,64, 67,76
600297-314-026	CAP. 47UF, ALUM, 50V	C2,3
600269-314-012	CAP. 18PF, CERAMIC, 500V	C27,31
600269-314-014	CAP. 22PF, CERAMIC, 500V	C29
600269-314-001	CAP. 10PF, CERAMIC, 500V	C30
600269-314-022	CAP. 47PF, CERAMIC, 100V	C33,40,65
600272-314-007	CAP. .01UF, CERAMIC, 100V	C39
600269-314-016	CAP. 27PF, CERAMIC, 500V	C42
600269-314-027	CAP. 75PF, CERAMIC, 100V	C43
600297-314-016	CAP. 22UF, ALUM, 25V	C5,6,60, 61,62, 63,75
600268-314-004	CAP. .0027UF, CERAMIC, 50V	C66
600202-314-003	CAP. .22UF, 35V, TANT.	C7
600269-314-009	CAP. 10PF, CERAMIC, 500V	C81
600052-317-001	CAP. VAR, 3-10PF	C72,73
600269-314-007	CAP. 6.8PF, CERAMIC, 500V	C74
600269-314-011	CAP. 15PF, CERAMIC, 500V	C77
600268-314-011	CAP. .015UF, CERAMIC, 50V	C8
600006-411-001	DIODE, ZENER, IN4728A 4V	CR1
600144-410-001	DIODE HP3188	CR2,13
600109-410-001	DIODE IN4148	CR3-6, 9-12
600123-410-009	DIODE, VARACTOR, MV2112	CR7,8
600036-390-001	LED, RED	DS1
600017-419-001	TRANSISTOR PAD	FOR U1,L7
600064-419-001	4 POSITION VERTICAL MT	H1-3,H8
600064-419-003	3 POSITION VERTICAL MT	H4-6
600064-419-004	2 POSITION VERTICAL MT	H7
600094-512-001	TRANSFORMER, 3:1, BALUN	L1,7,8
600125-376-006	CHOKE 3.3UH	L11,13-15
600125-376-040	CHOKE 1.0UH	L12
600125-376-032	CHOKE 10UH	L17
600125-376-030	CHOKE 4.7UH	L2,16
600173-376-001	COIL, VAR, .1UH	L3
600125-376-007	CHOKE 33UH	L4
600125-376-033	CHOKE 1.5 UH	L5,6
600125-376-028	CHOKE .1UH	L9,10
600008-455-001	MIXER SLB-1	M1
600085-413-001	TRANSISTOR 2N918	Q1,6,9-14
600278-413-001	TRANSISTOR MPS8097	Q2,4,5
600080-413-001	TRANSISTOR 2N2222A	Q3,8
600259-413-001	TRANSISTOR J310	Q7
620014-341-075	RES. 2K, 1/4W, 5%	R1,7,12, 22,24,31, 39,44,49
620024-341-075	RES. 20K, 1/4W, 5%	R10,58
615014-341-075	RES. 1.5K, 1/4W, 5%	R11,37
651094-341-075	RES. 51, 1/4W, 5%	R13,26, 27,29
610044-341-075	RES. 1M, 1/4W, 5%	R14
622004-341-075	RES. 220, 1/4W, 5%	R15,19
656014-341-075	RES. 5.6K, 1/4W, 5%	R16,43
622024-341-075	RES. 22K, 1/4W, 5%	R17,59-62
610034-341-075	RES. 100K, 1/4W, 5%	R18,25
639014-341-075	RES. 3.9K, 1/4W, 5%	R2,9
682004-341-075	RES. 820, 1/4W, 5%	R20,57
613004-341-075	RES. 130, 1/4W, 5%	R21,41, 46,50,54
633004-341-075	RES. 330, 1/4W, 5%	R28
647024-341-075	RES. 47K, 1/4W, 5%	R3,63
636004-341-075	RES. 360, 1/4W, 5%	R30
618024-341-075	RES. 18K, 1/4W, 5%	R32
627004-341-075	RES. 270, 1/4W, 5%	R33
651004-341-075	RES. 510, 1/4, 5%	R34
643014-341-075	RES. 4.3K, 1/4W, 5%	R36
647004-341-075	RES. 470, 1/4W, 5%	R4,23, 40,45,47
610014-341-075	RES. 1K, 1/4W, 5%	R42
662004-341-075	RES. 620, 1/4W, 5%	R48
600000-341-075	RES. 0, 1/4W, 5%	R5
618004-341-075	RES. 180, 1/4W, 5%	R51,53
600072-360-004	POT. 100, 1/2W, CERMET, TOP	R52
627014-341-075	RES. 2.7K, 1/4W, 5%	R55
624094-341-075	RES. 24, 1/4W, 5%	R56
610094-341-075	RES. 10, 1/4W, 5%	R6,35,38
610004-341-075	RES. 100, 1/4W, 5%	R8
600261-230-001	TERMINAL	TP1-5
600526-415-001	IC 78M08, 8V REG	U1
600092-415-001	IC MC4044, PHASE DET.	U2
600240-415-001	IC 74LS05, HEX INV, O/C	U3,4
600225-415-001	IC 74LS192, UP/DN CNTR, SYNC	U5,6,7
600157-415-001	IC 74S74, D FLIP-F, DUAL	U8
600221-415-001	IC 74LS26, NAND, HV, QUAD	U9
600005-635-001	LED MOUNT	XDS1

NOTES:
1. UNLESS OTHERWISE NOTED.
   RESISTORS ARE IN OHMS, 1/4W, ±5%
   CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS (pF), VALUES LESS THAN ONE ARE MICROFARADS (μF).

LAST DESIG. USED
R63, C77, CR13, L17, U9, Q14, M1, TP3, FB3, DS1
DELETED
:3

Figure 4.19-9

Major Loop Board Schematic

MAJOR LOOP BOARD, A16

PIN CONNECTIONS AND VOLTAGE READINGS

A16P3

GND	1	2	GND	
+13 VDC	3	4	+13 VDC	
	5	6		
+24 VDC	7	8	+24 VDC	
50 kHz REF.	9	10	GND	
GND	11	12	55.53-55.6299 MHz -10 dBm	
	13	14		
	15	16		
	17	18		
100 kHz "2"	19	20		
100 kHz "1"	21	22		
100 kHz "4"	23	24		
100 kHz "8"	25	26		
1 MHz "2"	27	28		
1 MHz "1"	29	30		
1 MHz "4"	31	32		
1 MHz "8"	33	34		
10 MHz "2"	35	36		
10 MHz "1"	37	38		
LOGIC "Ø" or "1" $\overline{LL}$	39	40	$\overline{LL}$ LOGIC "Ø" or "1"	
	41	42	59.63-89.53 MHz 0 dBm (1stLO)	
GND	43	44	GND	

SECTION 5

OPTIONS

5.1 TONE KEY AND FSK MODEM OPTION (Tone Key/Modem Board A14)

This factory-installed option provides two separate remote control features: 1) Tone keying for increased CW keying rate (MSR 6700A) and 2) FSK communication between MSR 5050A/ 6700A and the MSR 6420 remote control unit over a telephone line or a pair of wires.

The option (P/N 700015-700-001) consists of the Tone Key/Modem board (P/N 602025-536-002) which is plugged into the Mother board.

Whenever this board is used, the radio must be correctly configured to accept it.

MSR 5050A

Turn S1 on the Tone Key/Modem board to SERIAL KEY. The tone key circuitry does not apply to the receiver and S1 turns off the tone oscillator on the board.

Set switches S1, S2 and S3 on the Interface board according to Table 3.1. This configures the unit to accept FSK control at 300 Baud.

See the Mother board technical description in Section 4 for jumper settings to configure the CNTL/STAT lines.

MSR 6700A

If tone keying is desired, and the radio's standard audio or switched standard audio lines are connected to an MSR 6420 which is configured for tone key operation, set S1 on the Tone Key/ Modem board to TONE KEY. Otherwise, make sure that S1 is set to SERIAL KEY.

Whenever this board is installed, even if tone keying is not used, the radio's standard audio lines must be routed through the board. See the Mother board technical description in Section 4 for correct audio configuration. An additional Mother board jumper allows the user to enable tone keying only while the radio is being remotely controlled.

If the modem circuitry is being used, set switches S1, S2 and S3 on the Interface board per Table 3.1. This configures the unit to accept FSK control at 300 Baud. Jumpers on the Mother board must be correctly set to configure the CNTL/STAT lines for use with the Tone Key/ Modem board alone, or the Tone Key/Modem board in conjunction with the Audio Interface board.

5.1.1 FSK MODEM CIRCUIT

This circuit provides frequency-shift-keyed (FSK) communication between the radio and the RCU at 300 Baud. The circuit transmits and receives binary data over standard telephone lines or a pair of wires. The modem will operate at 300 Baud only.

5.1.1.1 FSK Modem Theory

A brief description of FSK modem theory is provided to allow the user to understand the operation of this circuit.

Two FSK modems are required for data transmission. At the transmit end of the signal path, a modem modulates a digital signal by converting the logic 1 (high) and logic 0 (low) signals into separate audio frequency tones. The tones are transmitted over a pair of lines to the second modem at the receive end of the signal path. This modem demodulates the audio tones by converting them back into a serial digital data stream.

Two-way communication is required, so each modem must be able to modulate and transmit as well as receive and demodulate.

The Mackay FSK remote control circuitry uses this pair of audio tones:

Logic 1: 2225 Hz
Logic 0: 2025 Hz

The tones are passed between the modem circuit in the RCU and the modem on the radio's Tone Key/Modem board over balanced 600 ohm audio lines called the CNTL/STAT lines. The RCU sends CONTROL commands to the radio, which replies with STATUS information.

5.1.1.2 Modem IC U1

The heart of the FSK modem circuitry is U1, a single chip modem circuit. The chip operates at 300 Baud and contains modulation, demodulation and filtering. All necessary audio tones are generated by crystal oscillator circuitry, along with crystal Y1 and capacitors C6 and C7. The oscillator frequency can be measured at TP4.

Digital data to be transmitted comes into the board on pin 18 and is fed directly to pin 10 of U1. This data is converted to audio tones and leaves the chip on pin 16. The tones can be monitored at TP6.

Received tones reach pin 15 of U1 from either of two places: the TXA line (when the Audio I/O board is also used) or from the output of U3B. These tones, which may be monitored at TP5, are converted into serial digital data by U1. This digital data stream leaves the chip at pin 4 and the board at pin 19, and may be monitored at TP1.

A carrier-detect indicator, DS1, is provided to show when the modem has acquired a carrier signal from another modem and communication between the two is possible. The carrier light is driven by pin 2 of U1 and buffered by U2A and U2B. U1-2 goes low when a carrier is detected. Components R2 and C8 determine the time constant of the carrier detector.

The frequencies of transmitted and received tones depend on whether the modem is in the ORIGINATE or ANSWER mode; this depends on the state of U1-12. If U1-12 is high, the modem is in the ORIGINATE mode, and if low, in the ANSWER mode. This O/$\overline{A}$ line is controlled by the MSR 5050A/6700A microprocessor.

The radio is normally waiting to receive a CONTROL command from the RCU. The O/$\overline{A}$ line will be high so that the modem is set to receive using the 2025/2225 Hz pair of tones. After a command has been received, the radio replies with the transmission of a STATUS signal to the RCU. The O/$\overline{A}$ line goes low, causing the modem to transmit on the 2025/2225 Hz pair.

5.1.1.3 Active Hybrid U3

The active hybrid allows the modem to receive input tones from, and couple transmit tones into, a single 600 ohm line. The transmit tones are buffered by U3A, which drives output transformer T1 through terminating resistor R14. Received tones are amplified and buffered by U3B.

If the 600 ohm line is exactly 600 ohms, the transmit signals from U3A are prevented from entering the receive port of U1 by the cancelling effect of the differential input of U3B. In actual practice, only 10 dB of cancellation is provided and no more is needed because of effective filtering built into U1.

If the Addressable Audio I/0 option is installed in the radio, the external FSK 600Ω lines come into the Audio Interface board instead of the Tone Key/Modem board. Analog gates U6D, U6C are opened by a ground on pin 40 caused by the insertion of the Audio Interface board. This disconnects active hybrid U3; and the U1 Modem chip RCVA, TXA signals go to the Audio Interface board instead.

5.1.2 TONE KEY CIRCUIT (MSR 6700A only)

When the MSR 6700A system is in the Tone Key mode, the RCU uses a 2930 Hz tone mixed with the standard audio to signal the exciter to transmit. This allows extremely fast CW keying rates which are not limited by digital command communication delays. If normal keying is desired, the board can be switched to the Serial Key mode, bypassing the Tone Key circuitry.

When the RCU is keyed, a 2930 Hz tone is mixed with the standard audio and sent to the exciter. The exciter detects this tone and keys (transmits)

whenever the tone is present. A notch filter removes the 2930 Hz keying tone before the audio signal is sent on to modulate the RF carrier in the exciter.

5.1.2.1 Tone Key IC U5

The heart of the tone key circuitry is U5, a single-frequency bandpass filter, band reject filter, and tone generator, with a selectable-input buffer amplifier.

The tone generator frequency is controlled by an external crystal. The standard crystal supplied produces a 2930 Hz tone. Other crystals may be used to provide tones from 1500 Hz to 3400 Hz. The band reject filter is used to "notch out" all audio at the tone frequency. The bandpass filter extracts the tone from the input audio signal to allow detection of the keying tone. The selectable-input buffer amplifier can be switched to amplify either the unfiltered audio input, or the filtered audio input with the keying frequency has been notched out. The state of the notch-enable line, pin 10, determines which signal will be amplified. A low on pin 10 switches in the notched audio, and a high causes the unfiltered audio to be amplified. The buffered signal leaves the IC on pin 9.

Switch S1 in the Tone Key position:

Standard audio comes into the board on pins P1-23 and P1-25, and into U5 on pin 1. The notch-enable line, U5-10 is low so the audio is notched at 2930 Hz before leaving U5 at pin 9. The audio signal is amplified by U7C and leaves the board at P1-31.

When the RCU is keyed, a 2930 Hz tone is present on the incoming audio. This tone passes through the bandpass filter on the chip, leaving U5 on pin 12. The keying tone is amplified and rectified by U7A. U7B and associated circuitry are used as a variable threshold detector. The purpose of the variable threshold is to keep the exciter key pulse duration identical to that of the key pulse at the RCU. This is accomplished by triggering the detector always on the leading edge of the rectified keying pulse signal. When the RCU is first keyed, the signal level at U7-12 is low and begins to rise. The threshold is now relatively low, set by R30. U7B-14 switches to high as the rectified tone begins to rise. When the RCU is unkeyed, the rectified signal at U7B-14 begins to drop. The threshold at U7B-14 is raised so that U7B-14 switches to low as the rectified keying tone signal begins to drop,rather than after it has decayed to a low level. This preserves the correct key pulse duration. The threshold is raised by the rectifying action of CR11, R39 and C32.

While the keying tone is detected, U7B-14 is high. DS1 lights to indicate the keyed condition U2D inverts this high level to a low level signal which keys the exciter via the REMOTE KEY input to the Coupler Interface board.

The RADIO select line, P1-39, can be used to allow tone keying only when the exciter is being remotely controlled by the RCU. A jumper on the exciter Mother board is used to enable or disable this control feature. See Section 3 of this manual for jumper setting instructions.

Switch S1 in the Serial Key Mode:

Switch S1 jumpers REMOTE KEY IN and REMOTE KEY OUT together. This removes control of the REMOTE KEY line from the Tone Key board.

The notch-enable line (U5-10) is no longer low so the standard audio signal coming into the chip does not pass through the notch filter before exiting at U5-9.

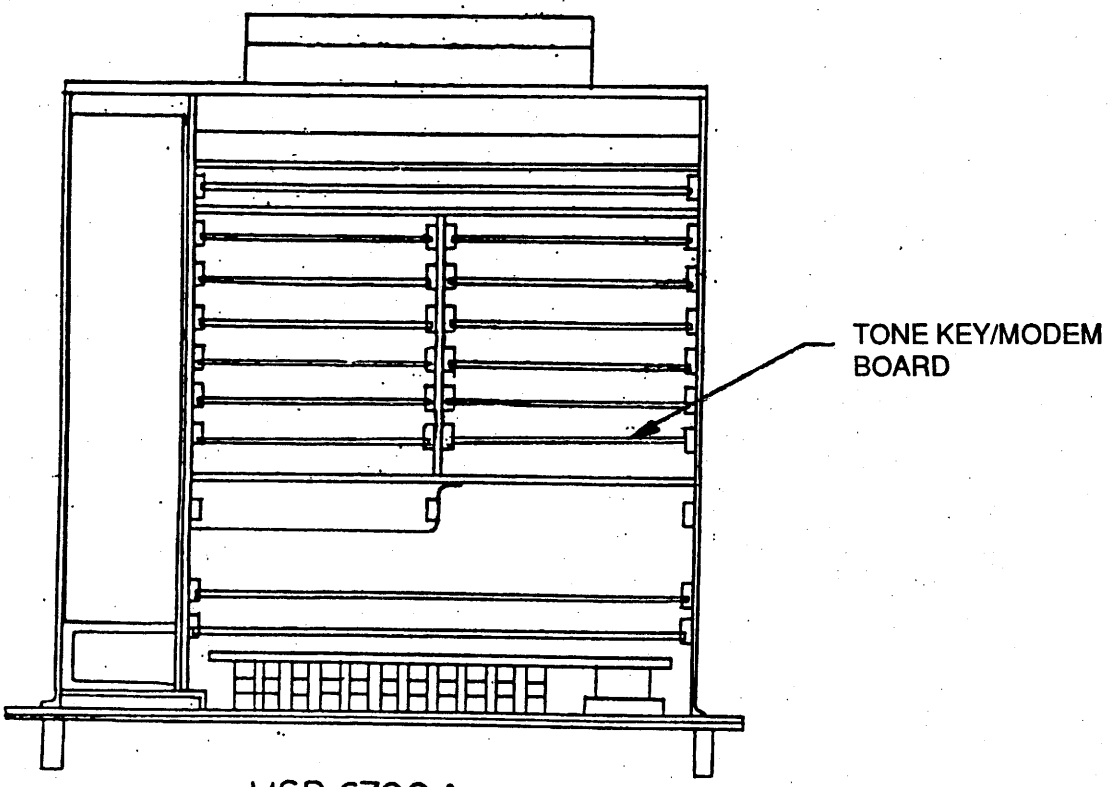
5.1.2.3 Audio Ground Reference Voltage

Resistors R27 and R28 set up a reference "audio ground voltage", VAG, which is one-half of the +13v supply voltage level. VAG is used as a dc reference voltage in the audio portions of the tone key circuitry. This prevents the need for a negative supply voltage for U5, U6 and U7.

5.1.2.4 On-Board Power Generation

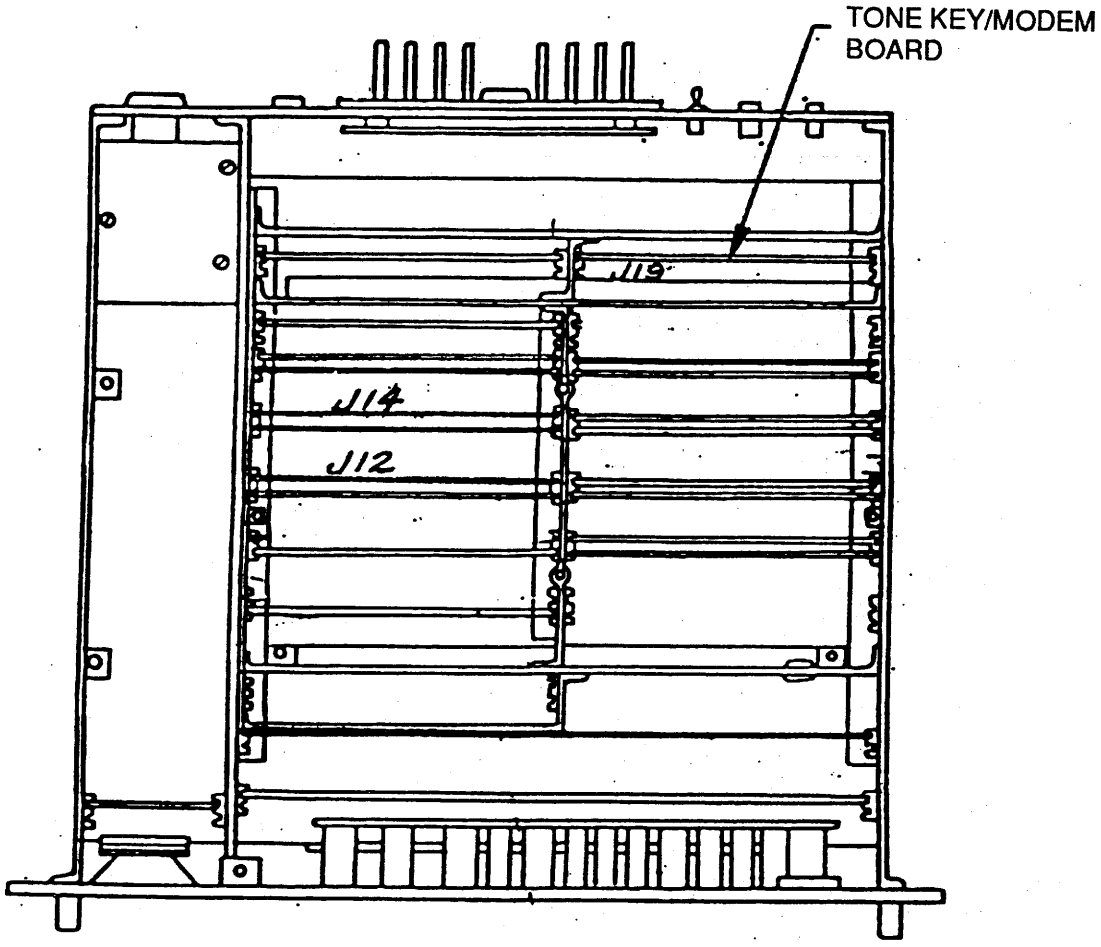
Positive 12 volts is generated from the +13v line by zener diode CR1 and resistor R1. Negative 5 volts is generated by U4, NE 555 timer IC, and

associated circuitry as follows: The output of U4 is a 10 kHz square wave at U4-3. When U4-3 is high, C14 is charged via R6 and CR4. When U4-3 goes low, the charge on C14 is transferred to C13 via CR3. Note that a negative voltage is transferred to C13. Zener diode CR2 limits the negative voltage to -5v. C11 and C12 provide additional filtering.



NOTE: SLIDE SWITCH ON BOARD TO LEFT FOR "SERIAL KEY", TO RIGHT FOR "TONE KEY". REFER TO RADIO MANUAL FOR POSITION OF JUMPERS ON MOTHER BOARD.

Figure 5.1-1 Installation, MSR 6700A



NOTE: REFER TO RADIO MANUAL FOR POSITION OF JUMPERS ON MOTHER BOARD.

Figure 5.1-2 Installation, MSR 5050A

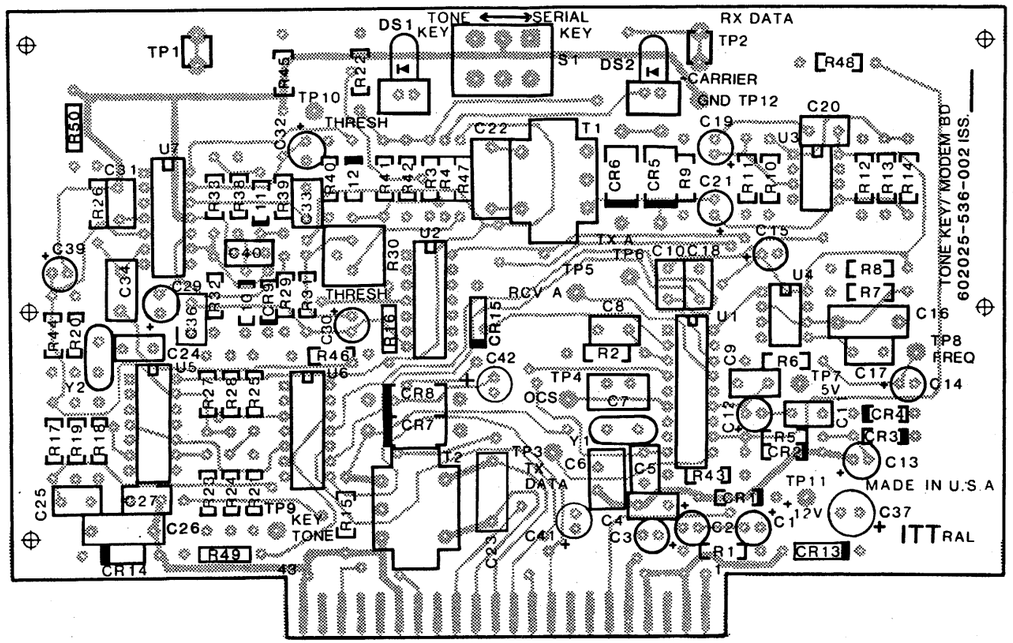


Figure 5.1-3

Tone Key/Modem Assembly

Tone Key/Modem (602025-536-002)

PART NUMBER	DESCRIPTION	SYMBOL
600202-314-018	CAP. 10UF, 25V, TANT.	C1-3, 12-15,19, 28,30,41, 42
600204-314-003	CAP. .015UF, 400V	C16
600297-314-016	CAP. 22UF, ALUM, 25V	C21
600204-314-001	CAP. .01UF, MYLAR, 400V	C22,23
600302-314-013	CAP. .1UF, MYLAR, 50V	C25,27, 31,33,40
600204-314-026	CAP., .047UF, 250V	C26
600202-314-007	CAP. 1UF, 35V, TANT.	C29,32
647003-306-501	CAP. 470PF, 3%, MICA, 500V	C34
600302-314-015	CAP. .22UF, MYLAR, 5[illegible]	C36
600297-314-032	CAP. 100UF, ALUM, 25[illegible]	C37
600202-314-022	CAP. 22UF, 15V, TANT	C39
600302-314-013	CAP. .1UF, MYLAR, 50[illegible]	C4,5,9, 10,18, 20,24,
615091-306-501	CAP. 15PF, 1%, MICA, 500V	C6,7
600302-314-007	CAP. .01UF, MYLAR, 63V	C8,11,17
600033-411-022	DIODE, ZENER, 1N4242B	CR1
600052-410-001	DIODE IN270	CR12, 14,15
600011-416-002	DIODE IN4004	CR13
600006-411-006	DIODE, ZE	CR2
600109-410-001	DIODE IN4148	CR3,4, 9-11
600028-411-001	DIODE, VOLT.SUPRESSOR P6KE6,8A	CR5-8
600043-390-002	LED, YEL	DS1,2
636094-341-075	RES, 36,1/4W, 5%	R1
682014-341-075	RES. 8.2K, 1/4W, 5%	R10
615004-341-075	RES. 150, 1/4W, 5%	R14
662004-341-075	RES. 620, 1/4W, 5%	R15

PART NUMBER	DESCRIPTION	SYMBOL
647024-341-075	RES. 47K, 1/4W, 5%	R17,21, 44,46
610014-341-075	RES. 1K, 1/4W, 5%	R18,31, 32,39,47
639014-341-075	RES. 3.9K, 1/4W, 5%	R19,48
610044-341-075	RES. 1M, 1/4W, 5%	R2,20
620024-341-075	RES. 20K, 1/4W, 5%	R23,25
611024-341-075	RES. 11K, 1/4W, 5%	R26
610024-341-075	RES. 10K, 1/4W, 5%	R27-29, 33,38,49,
610024-341-075	RES. 10K, 1/4W, 5%	R3,11-13, 16,22,24,
600072-360-007	RES. 1K POT	R30
647004-341-075	RES. 470, 1/4W, 5%	R4,5,8,45
610024-341-075	RES. 10K, 1,[illegible]W, 5%	R40-43,
620014-341-075	RES. 2K, 1/[illegible], 5%	R50
610004-341-075	RES. 100, 1,[illegible]W, 5%	R6
647014-341-075	RES. 4.7K, 1/4W, 5%	R7
622024-341-075	RES. 22K, 1/4W, 5%	R9
600130-616-001	SWITCH, SLIDE, DPDT, PC MOUNT	S1
635234-501-001	TRANSFORMER, 600 OHM, AUDIO	T1,2
600114-611-001	BROWN TEST POINT	TP1
600114-611-002	RED TEST POINT	TP2
600871-415-001	TMS 99532	U1
600016-415-001	IC 7406, HEX INV. ,O/C	U2
600039-415-002	IC SN72558P	U3
600074-415-001	IC NE555, TIMER	U4
601003-415-001	IC S3526B, 2600 HZ BAND PASS	U5
600186-415-001	IC MC14066B, QUAD BIL SWITCH	U6
600171-415-001	IC LM324, OP AMP, 741 QUAD	U7
600206-378-001	CRYSTAL	Y1
600206-378-001	CRYSTAL	Y2

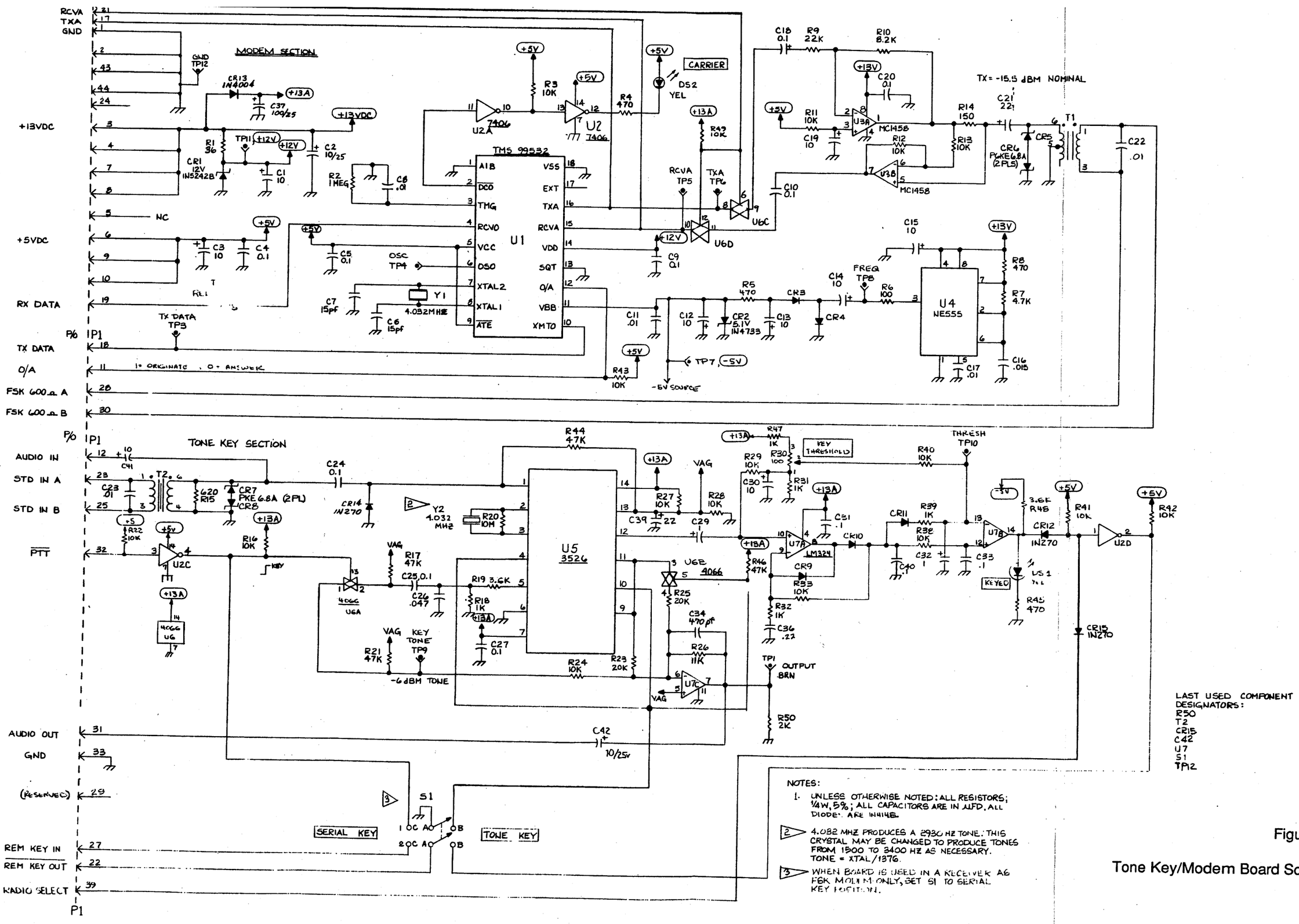


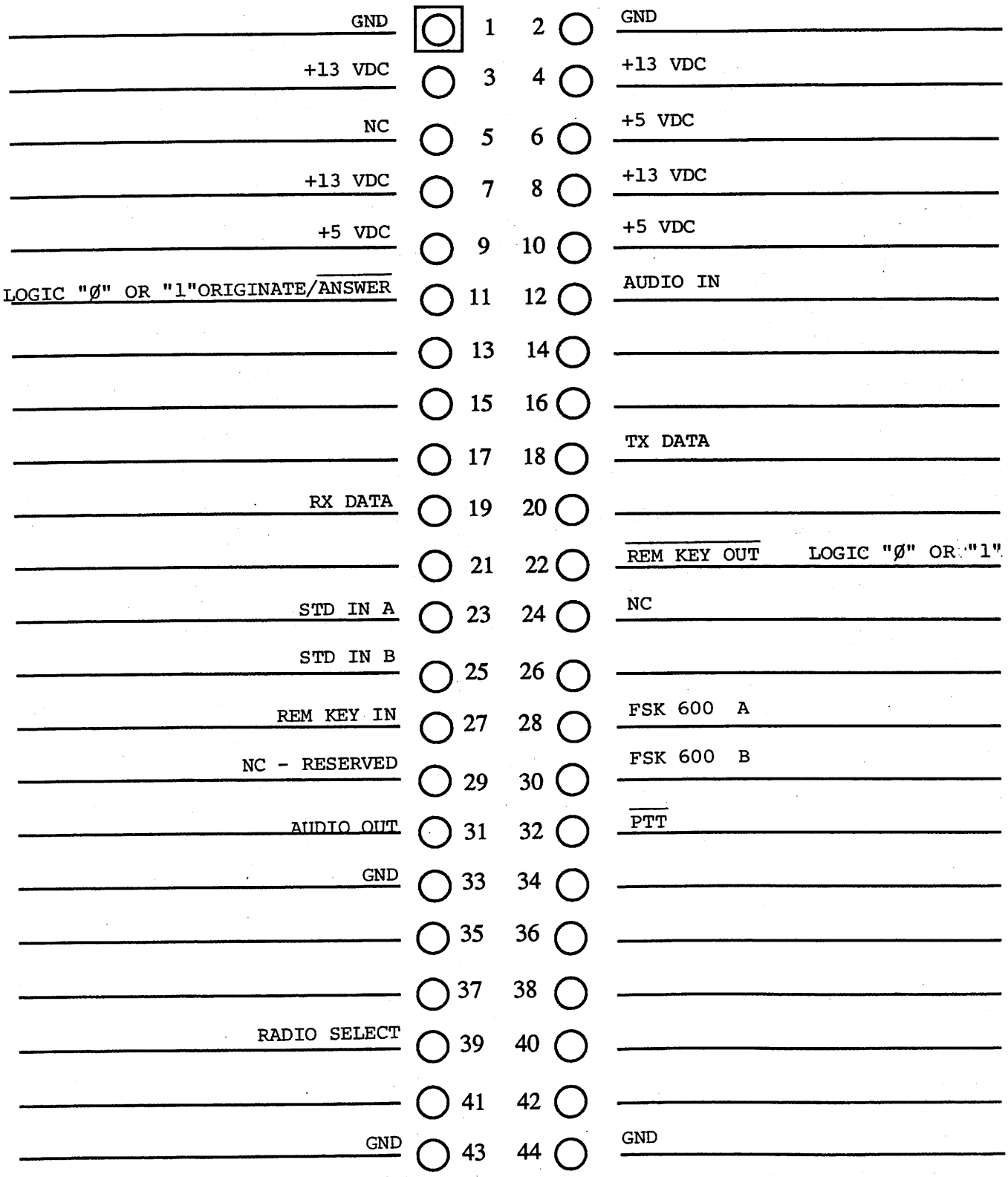
Figure 5.1-4

Tone Key/Modem Board Schematic

MSR 5050A TONE KEY MODEM BOARD A14

PIN CONNECTIONS AND VOLTAGE READINGS

A14P1



5.2 ADDRESSABLE AUDIO I/O OPTION (Audio Interface Board A15)

5.2.1 GENERAL

The Audio Interface board is used in systems with a single MSR 6420 Remote Control Unit controlling more than one MSR 5050A, MSR 6700A (single-remote, multi-radio systems).

The audio portion of the board is put in series with the radio's 600Ω audio lines to provide proper routing of audio signals. The remainder of the board is used in conjunction with the modem circuitry of the Tone Key/Modem board for passing 300 baud FSK Modem Control/Status information between the RCU and the radios.

The Tone Key/Modem board works by itself as a 300 baud modem for single-remote, single-radio systems. The board is automatically reconfigured for multi-radio systems when the Audio Interface board is plugged into the radio.

When the Audio Interface board is not installed, jumper plugs on the radio maintain continuity of the 600Ω audio lines. (See Section 3, option jumpers.)

The simplified block diagram (Figure 5.2-1) shows how the radios are connected in a single-remote, multi-radio configuration. Each radio has both switched and unswitched audio lines. The switched lines are connected through relays to a parallel audio bus. Only one switched audio relay is ever closed at any time. Refer to the MSR 6420 for system installation details.

The 300 BAUD FSK CNTL/STAT lines are "daisy-chained" from one radio to the next, so control commands originated by the RCU are heard by all radios. The commands are preceded by an address code which identifies the radio that should execute the command. One of the commands selects which switched-audio relay is closed at any time. The radios, upon command, provides status information to the RCU.

The RCU and radios can be configured by switches on the Interface board so that another communciation mode (RS-232, IEEE 488, etc.) can be used instead of the 300 baud modem. (See Section 3, Table 3.1 for switch settings). In these cases, the Tone Key/Modem board is not required.

5.2.2 AUDIO CONTROL CIRCUIT

The audio control circuitry routes the 600Ω audio lines and controls the switched audio.

The board must be configured to control outgoing audio or incoming audio by correctly setting switches S1 and S2.

MSR 6700A - All 6 switch positions up
MSR 5050A - All 6 switch positions down

Figure 5.2-5 shows all switches set for MSR 5050A operation. The remainder of this explanation will pertain to MSR 5050A operation. The circuit operates similarly when used in the MSR 6700A with the audio signals traveling in the opposite direction.

Standard audio enters the board at T3 and flows through U1C, leaving the board on pins 16 and 18. Similarly, ISB audio enters at T6, flows through U2-B and exits at pins 40 and 42.

5.2.3 CIRCUIT DESCRIPTION

Refer to the Audio Interface board schematic, Figure 5.2-5 and also to the Tone Key/Modem board schematic, Figure 5.1-4.

5.2.3.1 300 Baud Modem Circuit

The modem circuit receives control commands from the RCU and returns status information on the CNTL/STAT lines. The circuit is normally in the receive mode, with the ORIGINATE/ANSWER line, pin 15, high. This keeps FET Q1 and Q4 on and FET Q5 off.

Audio frequency control commands from the RCU enter through transformer T1 or T2 and leave the board at the other transformer to continue on to the next radio in the chain. These commands are received by U1A and pass through Q1 to the modem chip on the Tone Key/Modem board.

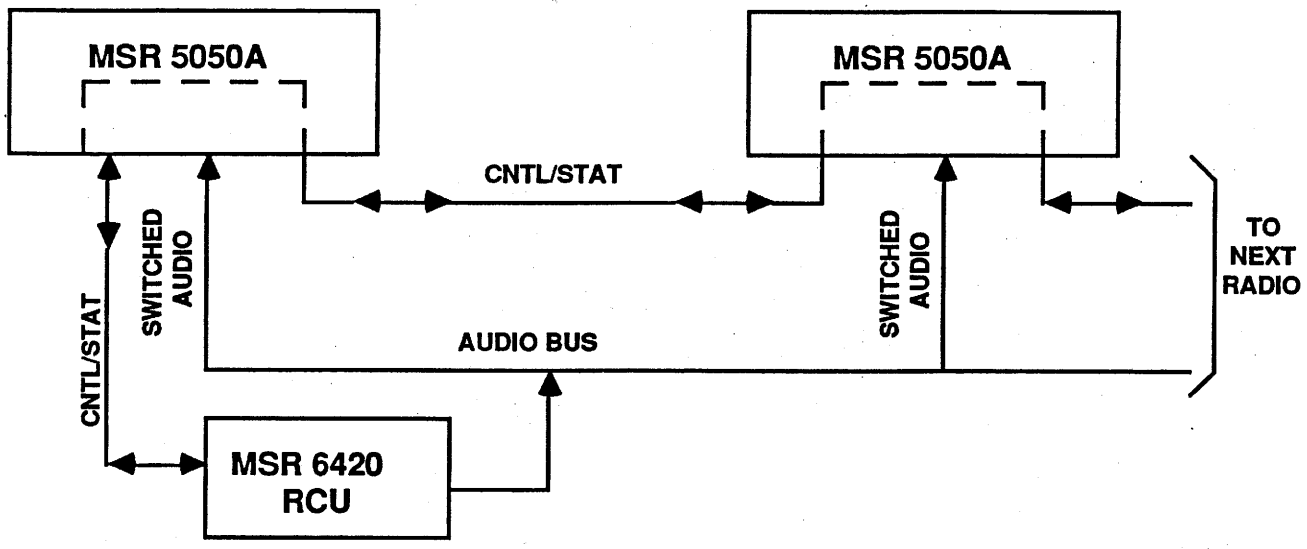
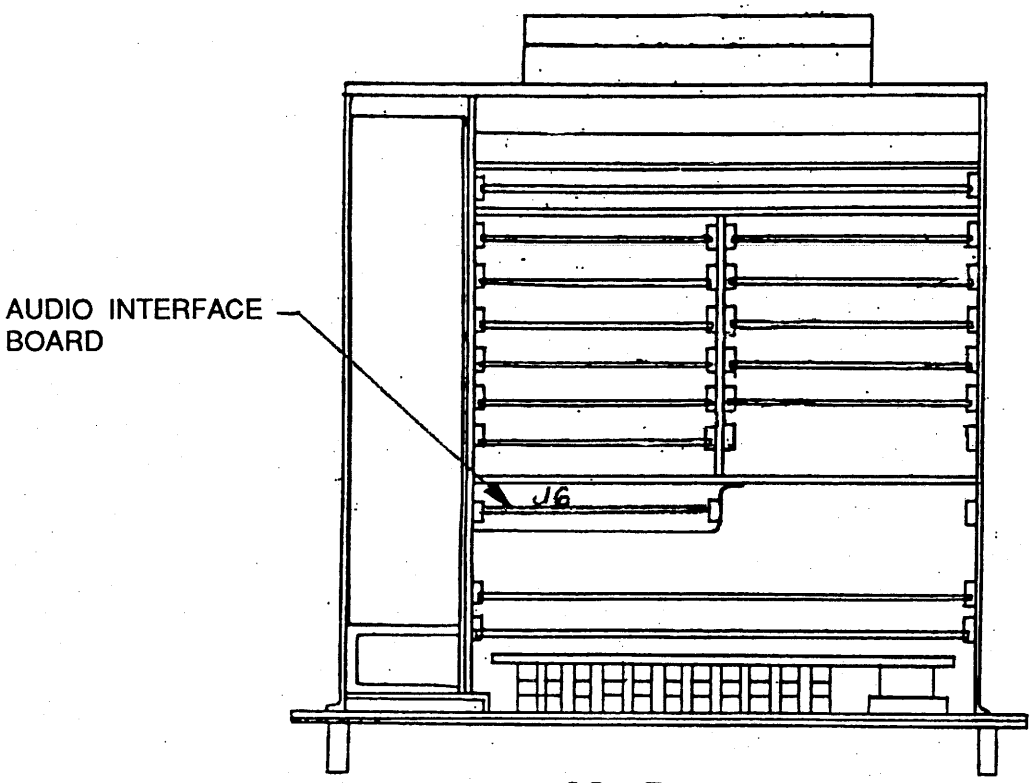


Figure 5.2-1 Remote Interconnect Diagram

If the radio receives a status request from the RCU, the ORIGINATE/ANSWER line switches to low. Q1 and Q4 are turned off and Q5 on. Audio frequency status signal tones from the radio's modem chip come in on pin 17 and flow through U1B and Q5 to resistors R4/R5. The signal is split and travels out of the radio in both directions on the CNTL/STAT lines. To properly terminate the 600Ω CNTL/STAT lines, an unused port should be terminated with a 600Ω resistor.

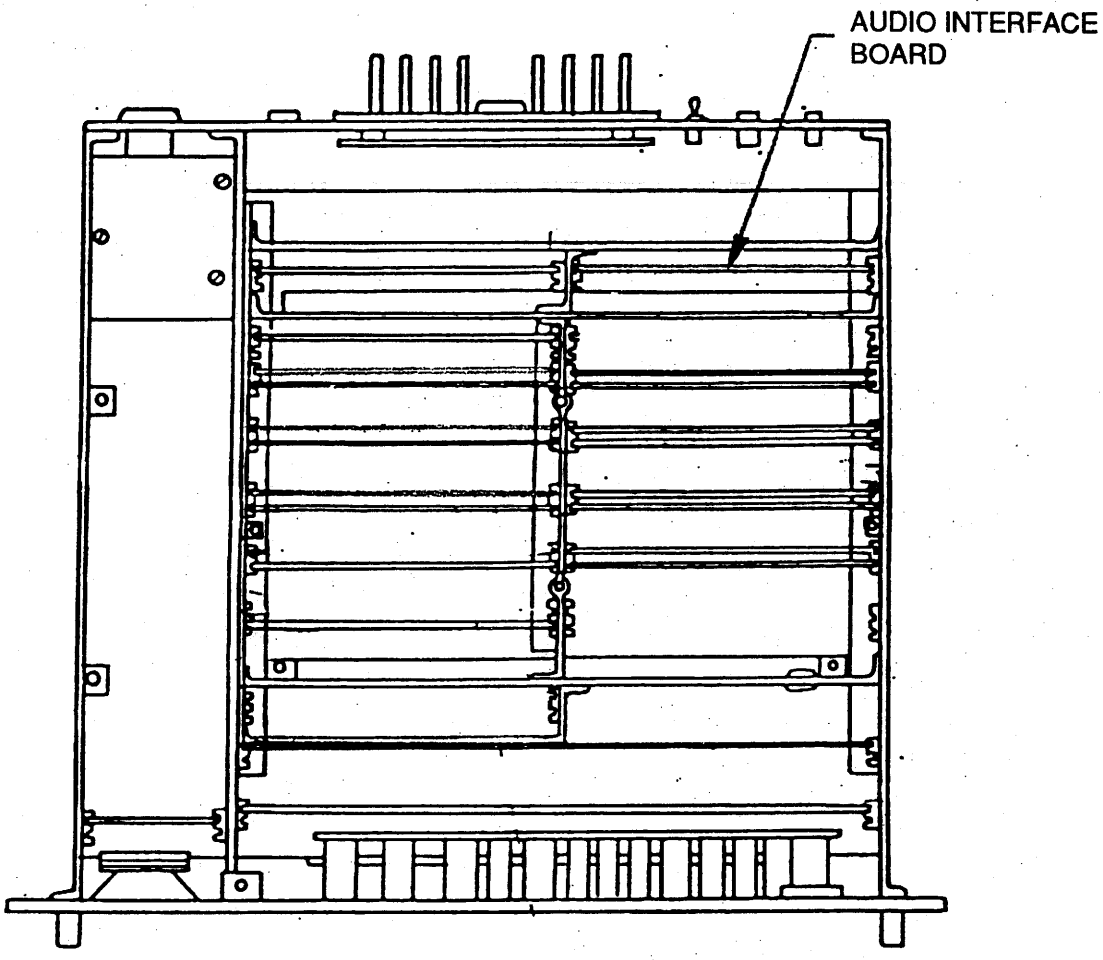
Audio signals may be sent to a particular radio from the RCU using the audio bus and the switched audio inputs. When commanded by the RCU, that particular radio takes the RADIO SELECT (RADSEL) line, pin 19, high. Relay K2 is closed connecting the radio to the audio bus. Switched standard audio enters the board through T4 and is mixed with the standard audio from T3 at U1-C. Radios configured for ISB may also receive switched ISB audio signals from an ISB audio bus.



TOP VIEW
COVER REMOVED

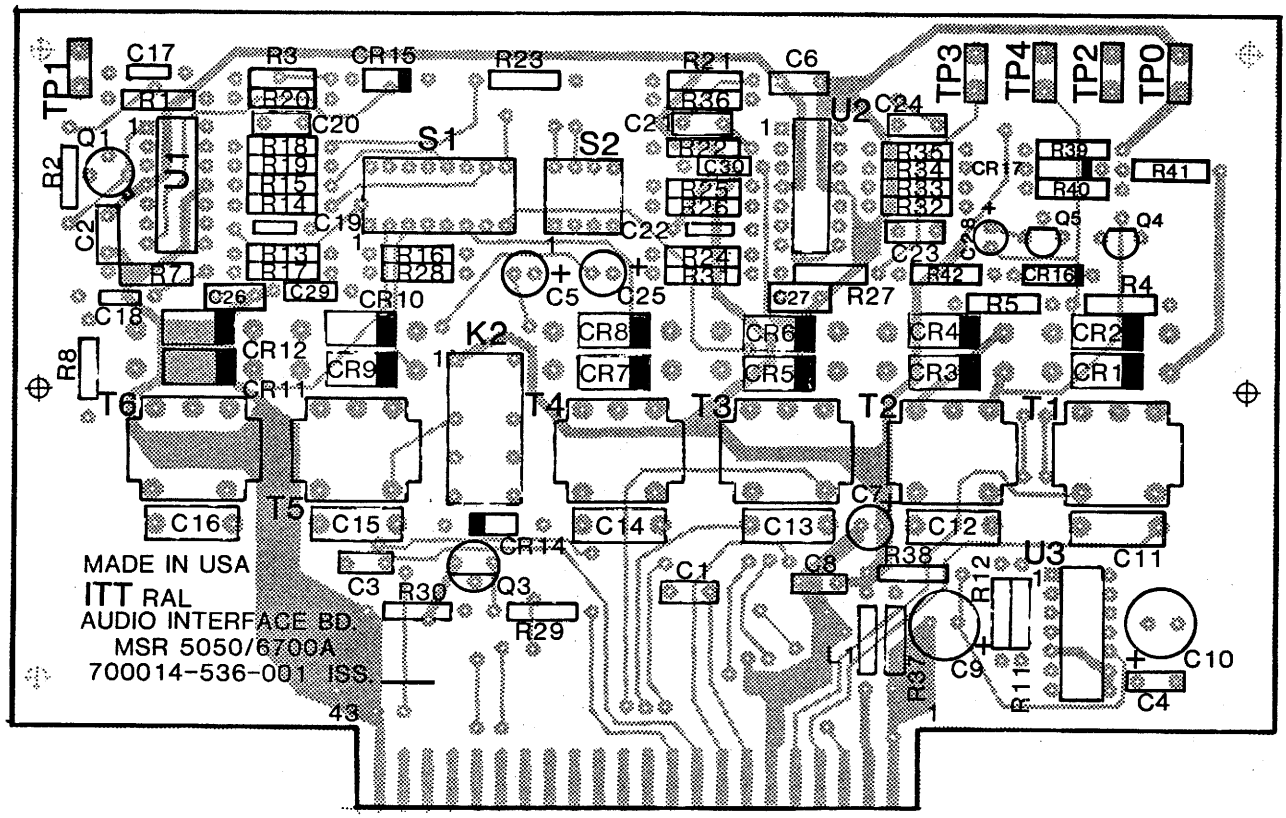
NOTE: ALL SWITCHES ON BOARD IN "UP" POSITION. REFER TO RADIO MANUAL FOR POSITION OF JUMPERS ON MOTHER BOARD.

Figure 5.2-2 Installation, MSR 6700A



NOTE: ALL SWITCHES ON BOARD IN "DOWN" POSITION. REFER TO RADIO MANUAL FOR POSITION OF JUMPERS ON MOTHER BOARD.

Figure 5.2-3 Installation, MSR 5050A

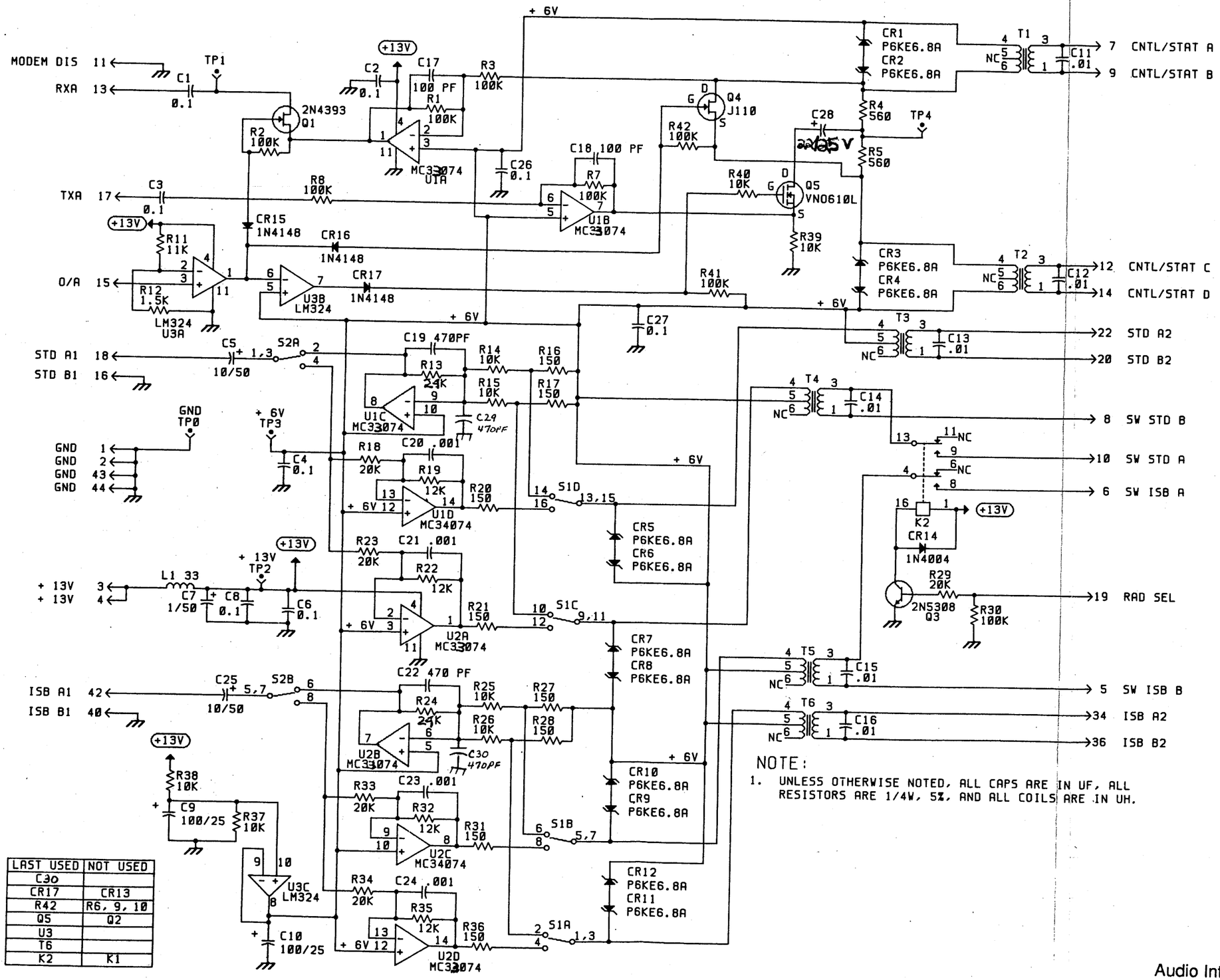


Audio Interface (700014-536-001)

PART NUMBER	DESCRIPTION	SYMBOL
600302-314-013	CAP. .1UF, MYLAR, 50V	C1-4,6, 8,26,27
600204-314-001	CAP. .01UF, MYLAR, 400V	C11-16
600293-314-101	CAP 100PF 50V 5%	C17,18
600272-314-005	CAP. 470PF, CERAMIC, 50V	C19,22, 29,30
600302-314-001	CAP. .001UF, MYLAR, 63V	C20,21, 23,24
600297-314-016	CAP. 22UF, ALUM, 25V	C28
600297-314-013	CAP. 10UF, ALUM, 50V	C5,25
600297-314-003	CAP. 1UF, ALUM, 50V	C7
600297-314-032	CAP. 100UF, ALUM, 25V	C9,10
600028-411-001	DIODE, VOLT.SUPRESSOR P6KE6,8A	CR1-12
600011-416-002	DIODE IN4004	CR14
600109-410-001	DIODE IN4148	CR15,16, 17
600094-403-003	RELAY, DPDT, 12V, 3A CONTACTS	K2
600125-376-011	CHOKE 33UH	L1
700001-413-001	TRANSISTOR, 2N4393	Q1
600221-413-002	TRANSISTOR 2N5308	Q3
600349-413-001	TRANSISTOR J 110, JFET	Q4
600390-413-001	POWER MOSFET,VN0610L	Q5
610034-341-075	RES. 100K, 1/4W, 5%	R1-3 7, 8,30, 41,42

PART NUMBER	DESCRIPTION	SYMBOL
611024-341-075	RES. 11K, 1/4W, 5%	R11
615014-341-075	RES. 1.5K, 1/4W, 5%	R12
624024-341-075	RES 24K, 1/4W, 5%	R13,24
610024-341-075	RES. 10K, 1/4W, 5%	R14,15, 25,26, 37-40
615004-341-075	RES. 150, 1/4W, 5%	R16,17, 20,21,27 28,31,36
620024-341-075	RES. 20K, 1/4W, 5%	R18,23, 29,33,34
612024-341-075	RES. 12K, 1/4W, 5%	R19,22, 32,35
656004-341-075	RES., 560, 1/4W, 5%	R4,5
600244-616-004	SWITCH, 4 X SPDT, DIP	S1
600244-616-002	SWITCH, 2 X SPDT, DIP	S2
635234-501-001	TRANSFORMER, 600 OHM, AUDIO	T1-6
600114-611-010	BLACK TEST POINT	TP0
600114-611-001	BROWN TEST POINT	TP1
600114-611-002	RED TEST POINT	TP2
600114-611-003	ORANGE TEST POINT	TP3
600114-611-004	YELLOW TEST POINT	TP4
700121-415-001	IC, QUAD OP AMP, MC33074	U1,2
600171-415-001	IC LM324, OP AMP, 741 QUAD	U3

Figure 5.2-4 Audio Interface Assembly



LAST USED	NOT USED
C30	
CR17	CR13
R42	R6, 9, 10
Q5	Q2
U3	
T6	
K2	K1

NOTE:

1. UNLESS OTHERWISE NOTED, ALL CAPS ARE IN UF, ALL RESISTORS ARE 1/4W, 5%, AND ALL COILS ARE IN UH.

Figure 5.2-5

Audio Interface Board Schematic

MSR 5050A/6700A AUDIO INTERFACE BOARD A15

PIN CONNECTIONS AND VOLTAGE READINGS

A15P1

GND	1	2	GND
+13 VDC	3	4	+13 VDC
SW ISB B	5	6	SW ISB A
CNTL/STAT A	7	8	SW STD B
CNTL/STAT B	9	10	SW STD A
MODEM DISABLE (GND)	11	12	CNTL/STAT C
RXA	13	14	CNTL/STAT D
O/A	15	16	STD B1 (GND)
TXA	17	18	STD A1
RADIO SEL	19	20	STD B2
	21	22	STD A2
	23	24	
	25	26	
	27	28	
	29	30	
	31	32	
	33	34	ISB A2
	35	36	ISB B2
	37	38	
	39	40	ISB B1 (GND)
	41	42	ISB A1
GND	43	44	GND

5.3 PRESELECTOR OPTION

5.3.1 GENERAL

The Preselector Option (P/N 700007-700-001) adds front end selectivity to the Receiver to prevent interference from strong off-channel interference. It may also be added to an exciter or transceiver to reduce broadboard noise at the LPA input.

The standard Preselector Option consists of:

a) MSR 6300 Preselector, P/N 699038-000 (separate manual supplied)
b) 12 VDC/1.6 Amp Power Supply, P/N 600055-391-001 (separate manual supplied)
c) Preselector Interface Cable, P/N 600878-540-002.

Additional components of the Preselector Option are added depending on the radio involved as follows:

a) 700007-700-001 - BCD Interface Kit (MSR 5050A) 700022-700
b) 700007-700-002 - BCD Interface Kit (MSR 6700A); 700021-700 Signal Routing Kit - 600279-700 (MSR 6700A)

5.3.2 DESCRIPTION

(Refer to Figure 5.3-1 for typical installation.)

The Preselector is a digitally-tuned bandpass filter with 38 dB rejection at Fo ±10%. It is tuned to the radio operating frequency by 14 BCD input signals provided from the radio by the BCD Interface Kit. It tunes from 1.6 to 10 MHz in 20 kHz steps and 10 MHz to 29.9 MHz in 100 kHz steps with a 3 dB bandpass of Fo ±1% and a gain of -1 ±3 dB. The Preselector and Receiver are protected from large steady state antenna signals by relays which open the antenna circuit at two watts (with an accompanying indicator light). Gas tubes protect the Preselector and Receiver from transients on the antenna line. The Preselector is automatically bypassed (and indicated by a front panel light) below 1.6 MHz allowing the Receiver to tune to 10 kHz. In transmit mode, the exciter path is broken for the same condition preventing RF input to the PA below 1.6 MHz. A front panel switch can be operated to bypass the internal amplifier allowing 10 dB less gain for operation under extreme signal interference where receiver sensitivity is not critical. The amplifier is always in the circuit in transmit - independent of switch position.

The power supply provides +12 VDC at up to 1.6 amperes for the Preselector. With this supply, the Preselector must be internally strapped in the "LO V" regulator bypass position. The power supply may be operated from 115 VAC, 47 to 400 Hz. To operate from 230 VAC, the power supply cover must be removed to move a black and white wire on separate transformer terminals to a common terminal "D" as described in the power supply manual.

The Preselector Interface Connector interconnects the Receiver and Preselector with 14 BCD lines, a TRANSMIT status line, and a signal common. Two lines branch out from the Preselector mating connector to connect to the power supply for 12 VDC. A standard cable length of 4.5 feet provides ample strain relief while extending individual units from the rack for service or inspection.

To operate as an exciter postselector, a signal routing kit must be added to the MSR 6700A or MSR 8050A. This kit consists of a jumper cable and rear panel connectors which allow the Preselector to be electrically inserted before the PA.

The Preselector can be used with a transceiver to add filtering in both the receive path to the antenna and in the transmit path (before the PA). Relays in the Preselector operate with a TX signal from the transceiver to transfer the filter circuits between the two paths.

5.3.3 CHECKOUT PROCEDURES

5.3.3.1 Test

Preliminary (Refer to Figures 5.3-1and 5.3-2 for typical installation.)

Equipment is connected and power applied. The

radio has been previously tested. Ensure that the internal preselector jumper is in the "LO V" position to bypass the internal regulator for +12 volt operation. Ensure that the power supply transformer is internally wired for the desired line voltage. Normal configuration is 115 VAC, 47 to 400 Hz. Operation from 230 VAC is obtained by moving (and soldering) a black and a white wire from separate transformer taps to a single tap labeled "D". (Refer to the power supply manual.)

5.3.3.2 Operation

(Preselector amplifier switch "ON".) Verify RECEIVE and TRANSMIT operation on the following frequencies (to ensure that all six preselector bands are functional): 1.6, 2.6, 4.3, 6.9, 11.3, 18.4, and 29.9 MHz.

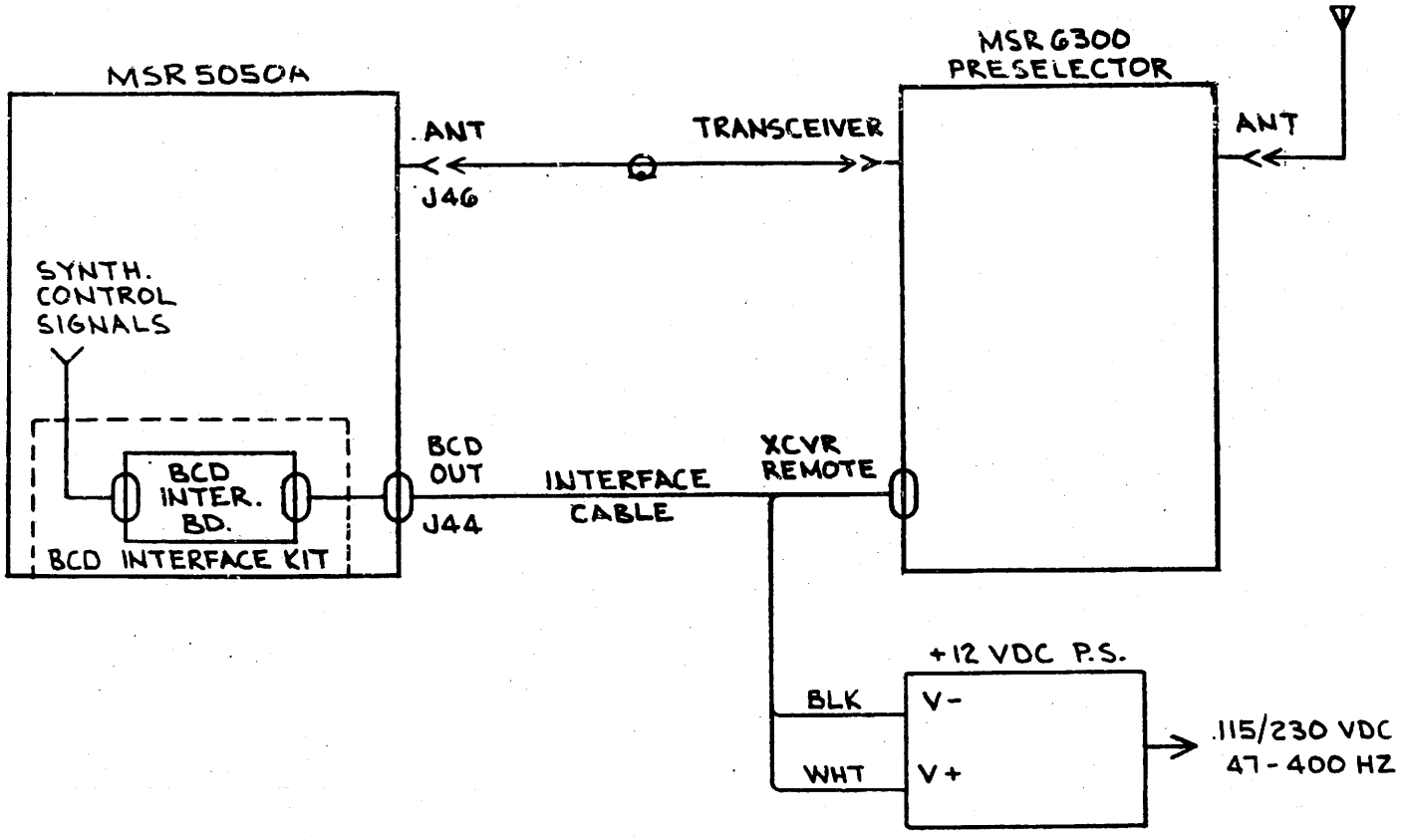


Figure 5.3-1 Typical Installation, MSR 5050A

5.4 BCD INTERFACE KIT

5.4.1 GENERAL

The BCD Interface Kit provides a rear panel BCD output (positive TTL) representing the tuned frequency of the radio from 10 kHz to 29.99 MHz. The outputs appear on J44, a 25-pin subminiature "D" connector, which is added to the rear panel as part of the kit. The kit is required to drive the MSR 6300 Preselector.

5.4.2 DESCRIPTION

The BCD Interface Kit is a factory-installed option consisting of a BCD input cable, a BCD output cable (which contains J44, the rear panel connector) and a BCD Interface board. The BCD interface board creates the BCD output signals by subtracting 4 MHz from the modified BCD code used by the frequency synthesizer in the radio. The BCD input cable is soldered to the radio Mother board and brings the 10 MHz, 1 MHz, 100 kHz, and 10 kHz modified BCD code to the BCD Interface board for conversion.

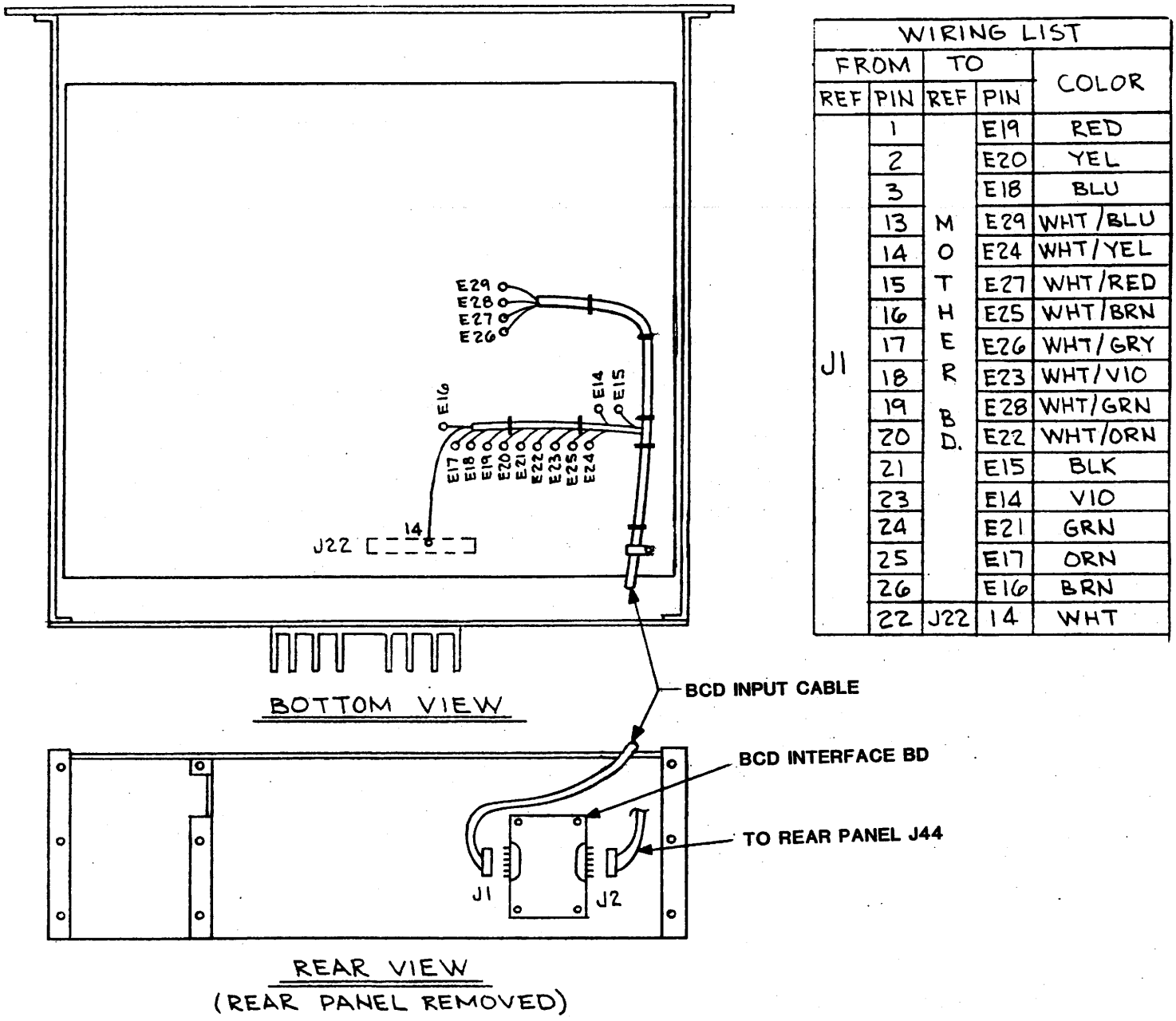
5.4.3 EXTERNAL INTERFACE

Pin assignments for the rear panel connector J44 (BCD OUT) are as follows:

PIN	DESCRIPTION	FREQUENCY
12	10K1	10 kHz x 1
25	10K2	10 kHz x 2
23	10K4	10 kHz x 4
21	10K8	10 kHz x 8
11	100K1	100 kHz x 1
13	100K2	100 kHz x 2
24	100K4	100 kHz x 4
22	100K8	100 kHz x 8
15	1M1	1 MHz x 1
14	1M2	1 MHz x 2
1	1M4	1 MHz x 4
5	1M8	1 MHz x 8
17	10M1	10 MHz x 1
16	10M2	10 MHz x 2
2	SIGNAL GND	
20	$\overline{TX}$	

BCD Interface Kit (700022-700-001)

PART NUMBER	DESCRIPTION	SYMBOL
600116-204-001	SCREW, SET	
690440-207-075	4-40X 7/16 PH SCREW	
642004-217-005	#4 SPLIT WASHER	
602021-536-002	BCD INTERFACE PBA	
600877-540-001	BCD INPUT CABLE	



WIRING LIST				
FROM		TO		COLOR
REF	PIN	REF	PIN	
J1	1	MOTHER BD.	E19	RED
	2		E20	YEL
	3		E18	BLU
	13		E29	WHT/BLU
	14		E24	WHT/YEL
	15		E27	WHT/RED
	16		E25	WHT/BRN
	17		E26	WHT/GRY
	18		E23	WHT/VIO
	19		E28	WHT/GRN
	20		E22	WHT/ORN
	21		E15	BLK
	23		E14	VIO
	24		E21	GRN
	25		E17	ORN
	26		E16	BRN
	22	J22	14	WHT

Figure 5.4-1 Installation, MSR 5050A

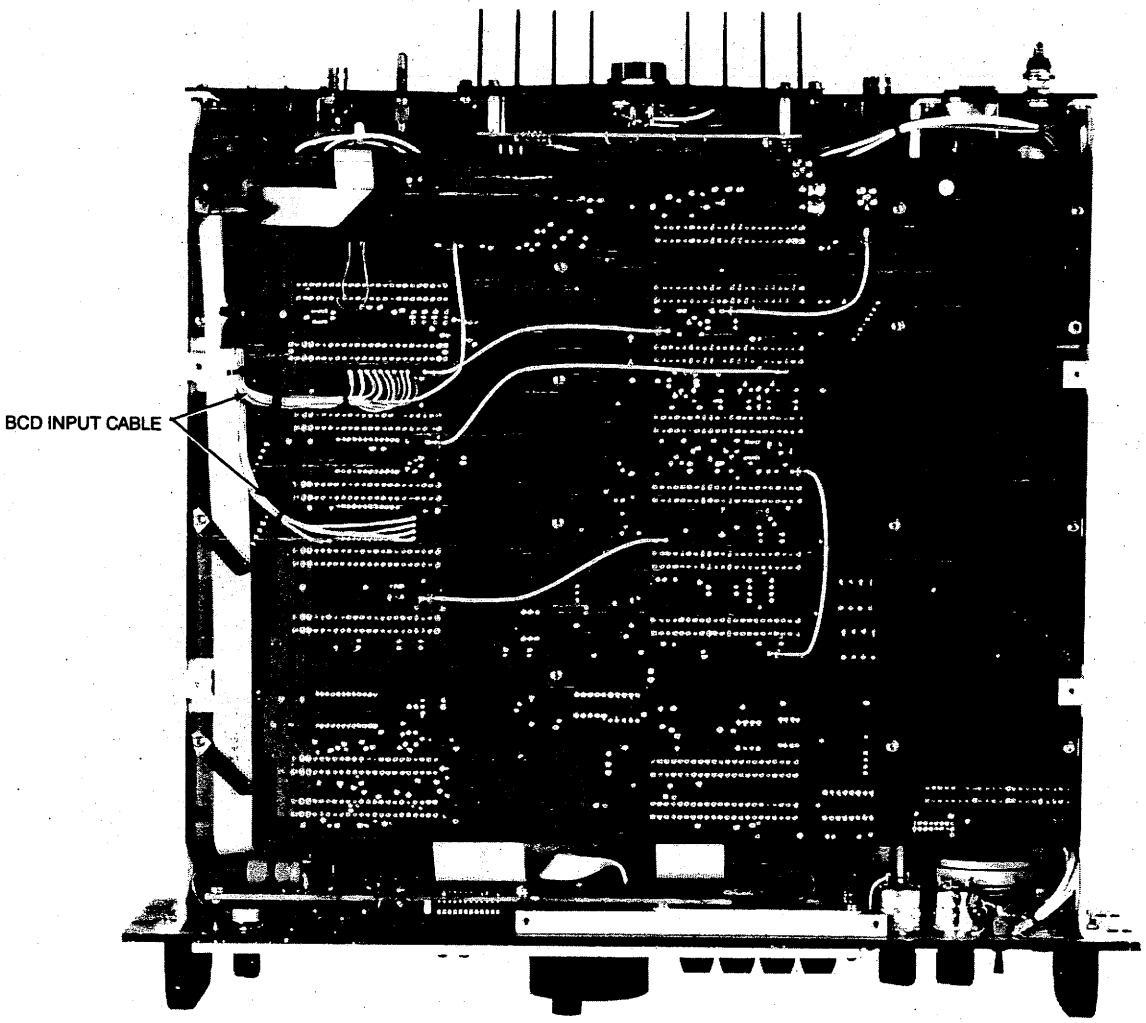


Figure 5.4-2

MSR 5050A Bottom View with BCD Interface Kit

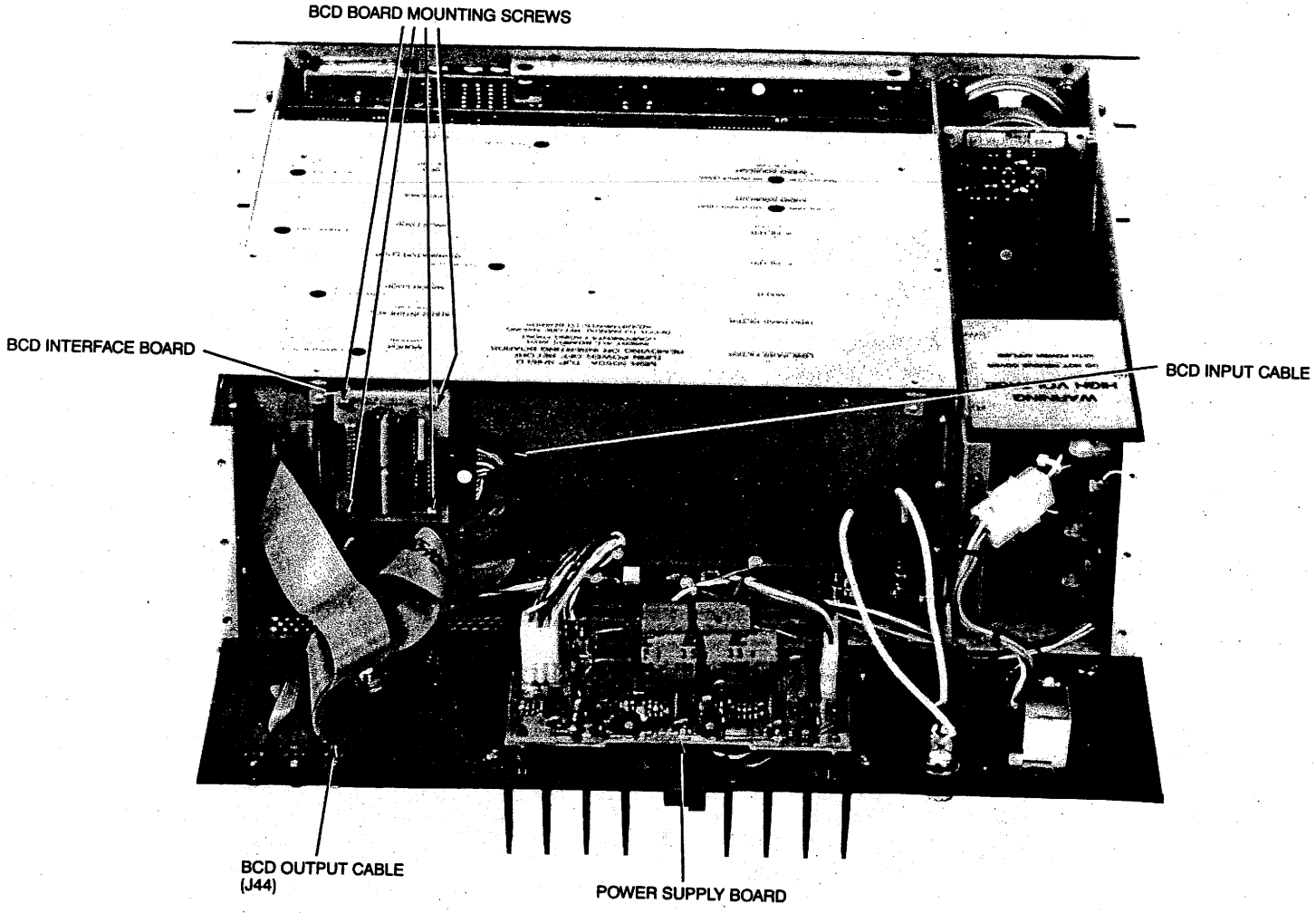


Figure 5.4-3

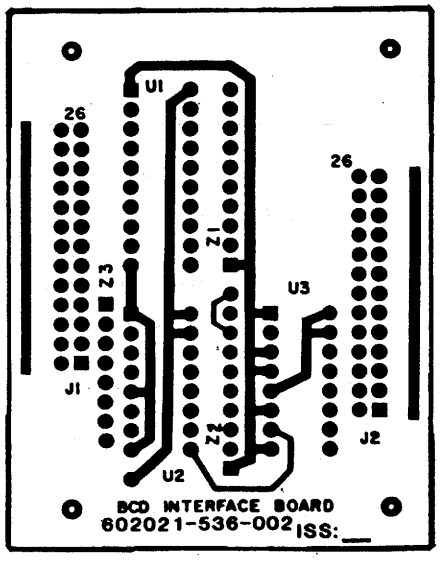
MSR 5050A Rear Panel Inside View with BCD Interface

5.4.4 BCD INTERFACE BOARD, A22

The BCD Interface board (P/N 602021-536) modifies the BCD synthesizer control signals in the MSR 5050A/MSR 6700A to BCD outputs corresponding to the input frequency to which the radios are tuned. This is done by logically subtracting 4 MHz from the BCD synthesizer signals. This board is used as part of a Preselector/ Postselector option for the radios where BCD frequency information is required to tune the Preselector.

U2 and U3 are CMOS NBCD adders which are converted to subtract 4 from the 10 MHz and 1 MHz BCD inputs. U2 is conditioned to subtract 4 from the "MHz" inputs by adding the 9's complement of 4 + 1 (U2, pins 3, 15) and biasing the "CARRY" input high (U2, pin 7). U3 is conditioned to subtract "0" from the "10 MHz" inputs adding the "9" complement of 8 + 1 (pins 5, 15).

U1 is an octal tri-state buffer which provides buffered BCD outputs from the "10 kHz" and "100 kHz" decades. These outputs are independent of the 10 MHz, 1 MHz signals and are not affected by the 4 MHz subtraction.



BCD Interface (602021-536-002)

PART NUMBER	DESCRIPTION	SYMBOL
600380-314-002	CAP SIP .1UF X 9	Z1,2
600282-415-001	IC 74LS244, 3-ST BUFFER	U1
601012-415-001	IC 4560, NBCD ADDER	U2,3
600201-537-001	RES NETWORK 4.7K X 7	Z3
600174-608-015	HEADER, 26 PIN	J1,2

Figure 5.4-4 BCD Interface Assembly

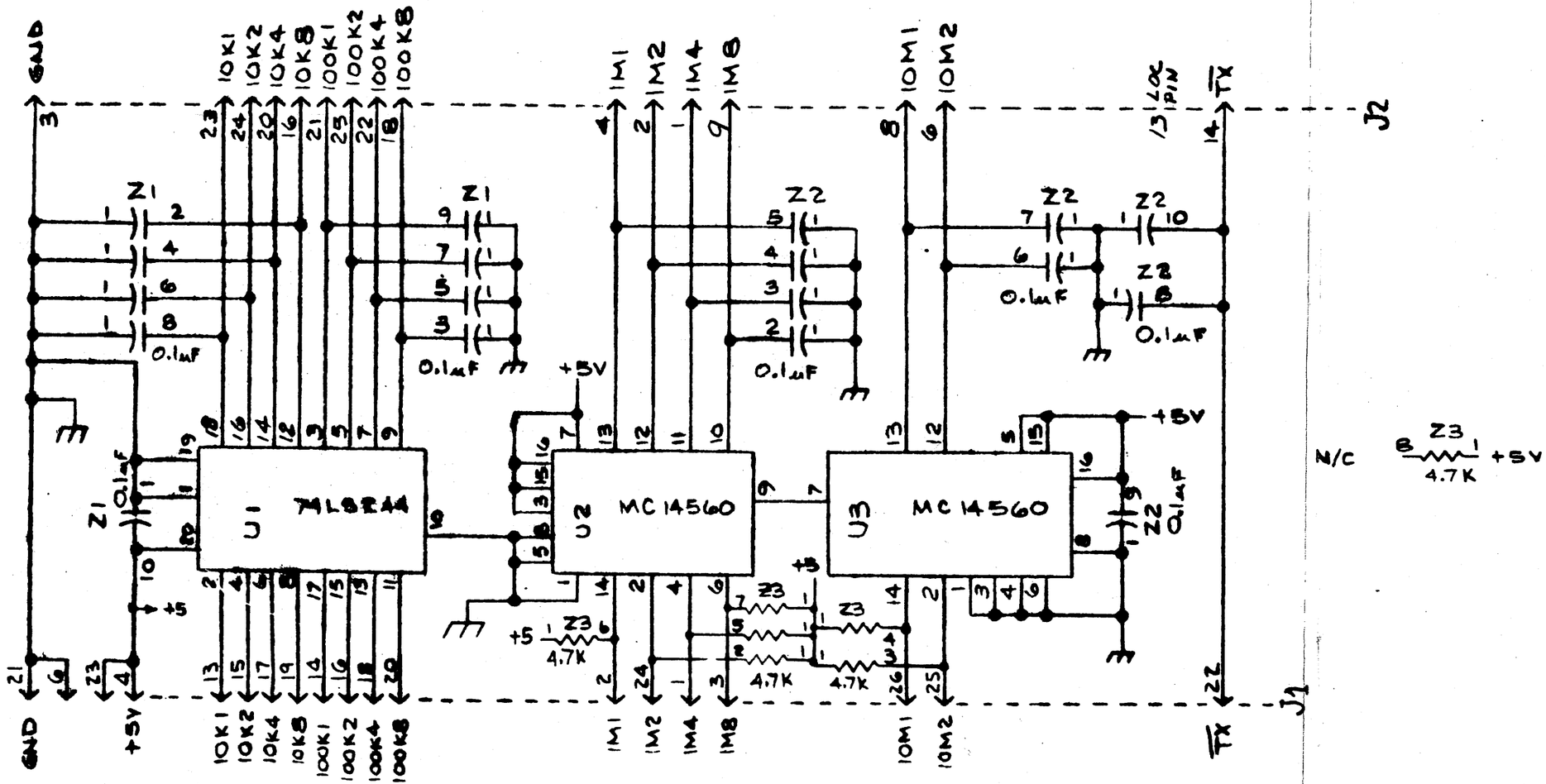


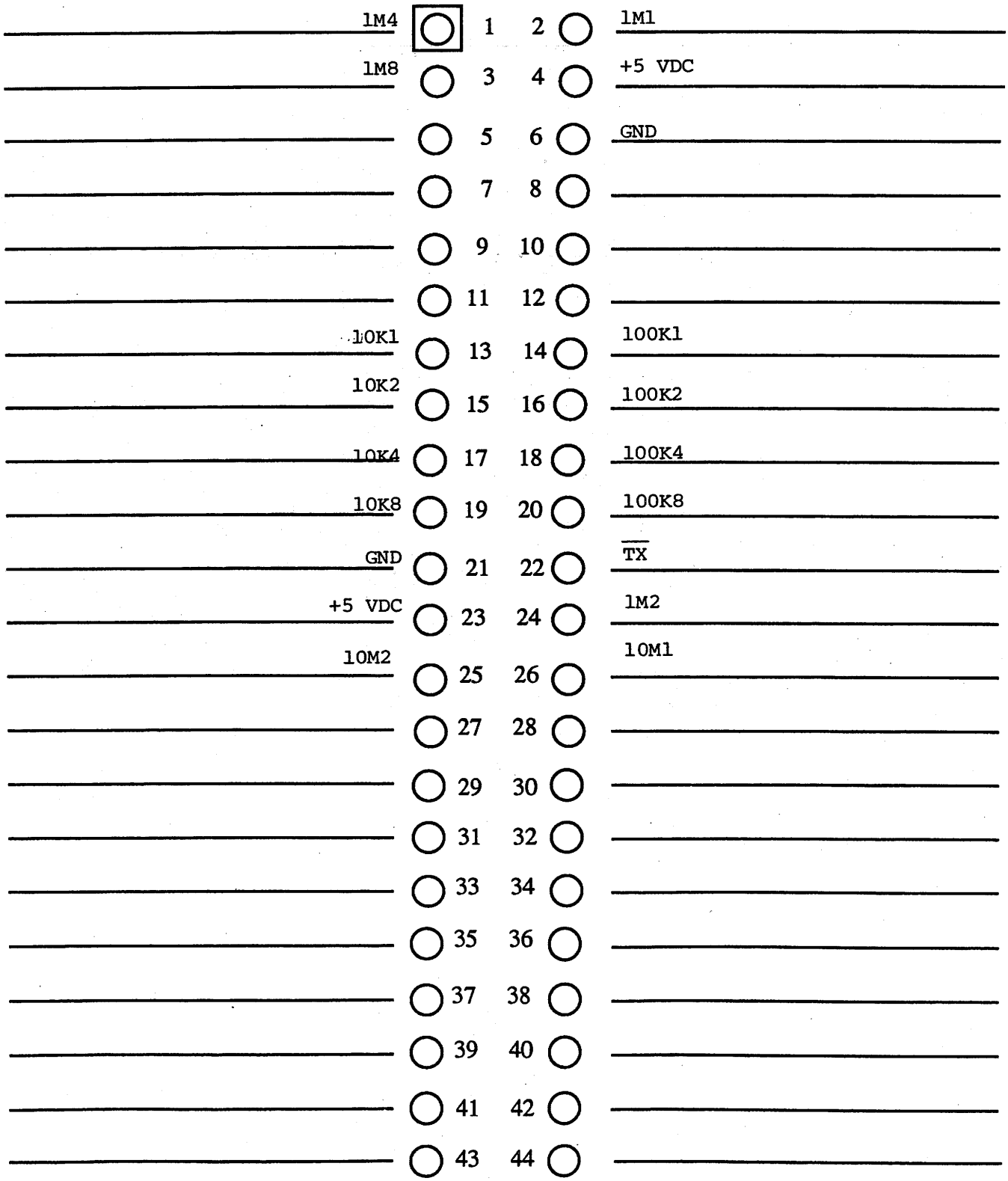
Figure 5.4-5

BCD Interface Board Schematic

BCD INTERFACE BOARD, A22

PIN CONNECTIONS AND VOLTAGE READINGS

A22J1

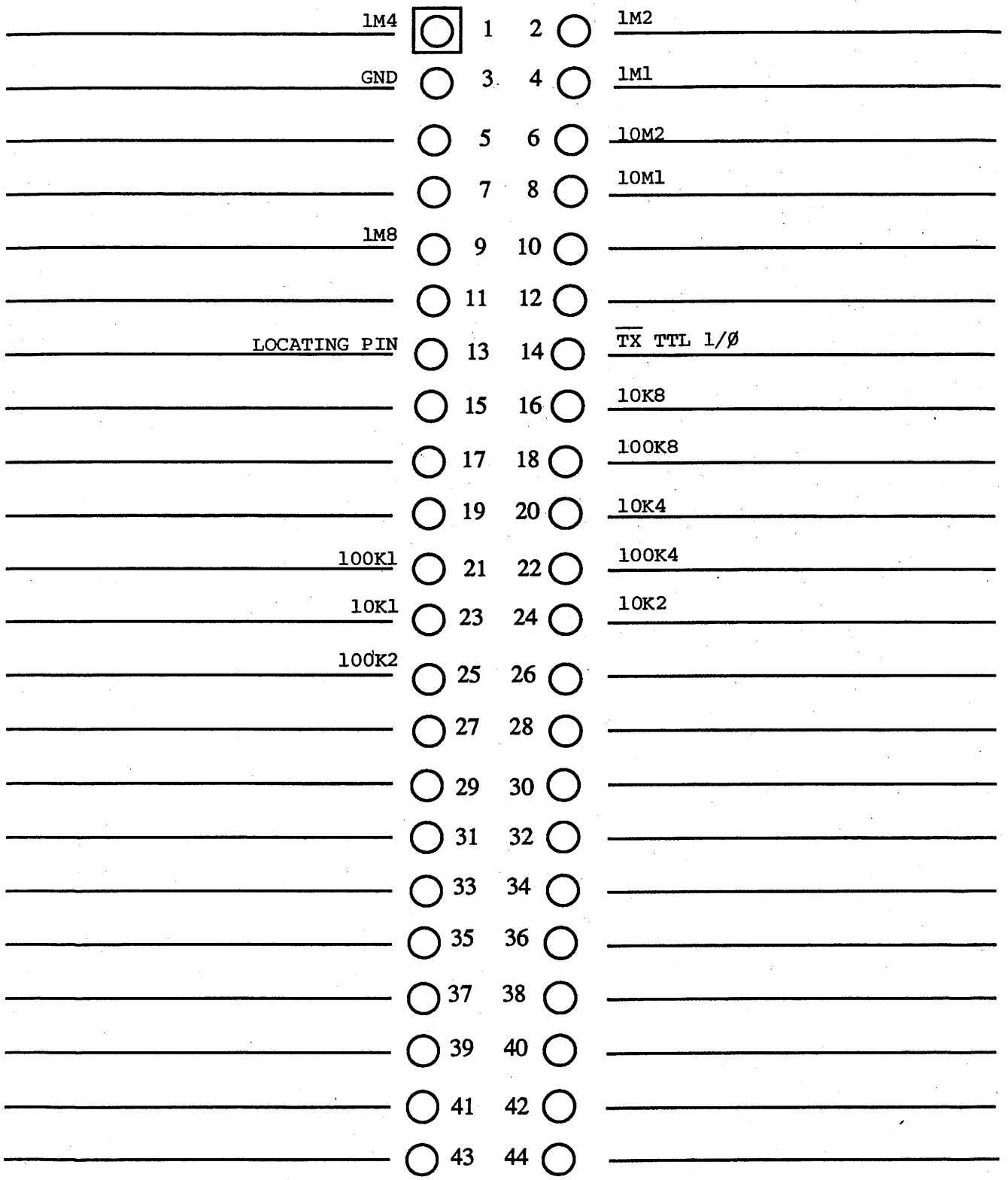


NOTE: ALL SIGNALS EXCEPT GND, +5V, $\overline{TX}$ ARE STATIC TTL LEVELS (HIGH FOR ENABLE) REPRESENTING 4 MHz HIGHER THAN RADIO FREQUENCY IN BCD, FORMAT.

BCD INTERFACE BOARD, A22

PIN CONNECTIONS AND VOLTAGE READINGS

A22J2



NOTE: ALL SIGNALS EXCEPT GND, +5 VDC, $\overline{TX}$ ARE STATIC TTL SIGNALS (HIGH ENABLE) REPRESENTING RADIO FREQUENCY IN BCD FORMAT.

5.5 HIGH STABILITY REFERENCE OPTION (OCXO, A21)

This factory-installed option provides a high stability OCXO with frequency stability of $\pm 1 \times 10^{-8}$ from 0°C to 65°C. With this option, the MSR 5050A tuning frequency can be held to ± 0.3 Hz at 30 MHz.

5.5.1 TECHNICAL CHARACTERISTICS

Output Frequency: 5,000,000 Hz

Output Wave Form: TTL

Frequency Stability:
Ambient = $\pm 1 \times 10^{-8}$ from 0°C to 65°C
Aging = $\pm 1 \times 10^{-6}$ per year

Warm-Up: 30 minutes from 25°C

Power Requirement: Oscillator and Oven = +13.5 VDC ± 15%, 670 mA max. during warm-up, 200 mA steady state.

5.5.2 INSTALLATION (Figures 5.5-1, 5.5-2)

The OCXO assembly with cables (figure 5.5-3) is mounted on the front of the card cage in two predrilled holes. The top shield and several PCB modules should be removed to obtain access. The 13 VDC power is obtained via the two wires which are routed under the Mother board and soldered to E31, E32 at the rear of the Mother board. The coax cable is routed into the grommetted hole as shown, to plug into J1 of the Reference board, A19. JP1 on the Reference board is moved down (E1 pins 2,3) to disconnect the TCXO used as the standard reference oscillator.

The OCXO output may be monitored at its output cable connector or at the rear panel REF IN/OUT Connector (through a buffer gate).

High Stability Option (700402-700-001)

PART NUMBER	DESCRIPTION	SYMBOL
600272-314-001	CAP. .1UF, CERAMIC, 50V	C1
600173-378-001	CRYSTAL	OCXO
600440-540-003	COAX CABLE ASSY	
600006-100-090	20 AWG WIRE, WH/BLK	
600006-100-000	20 AWG WIRE, BLACK	

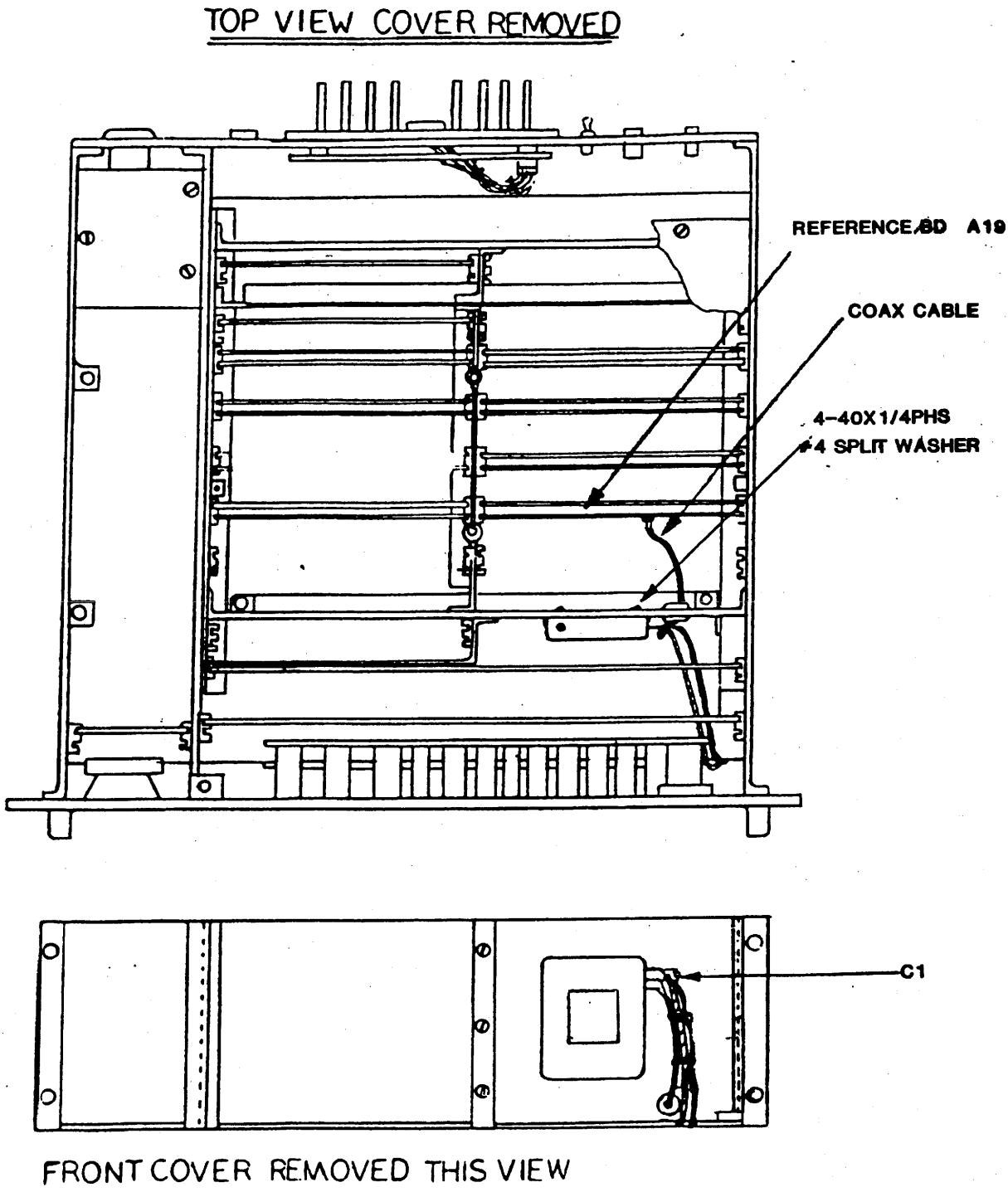
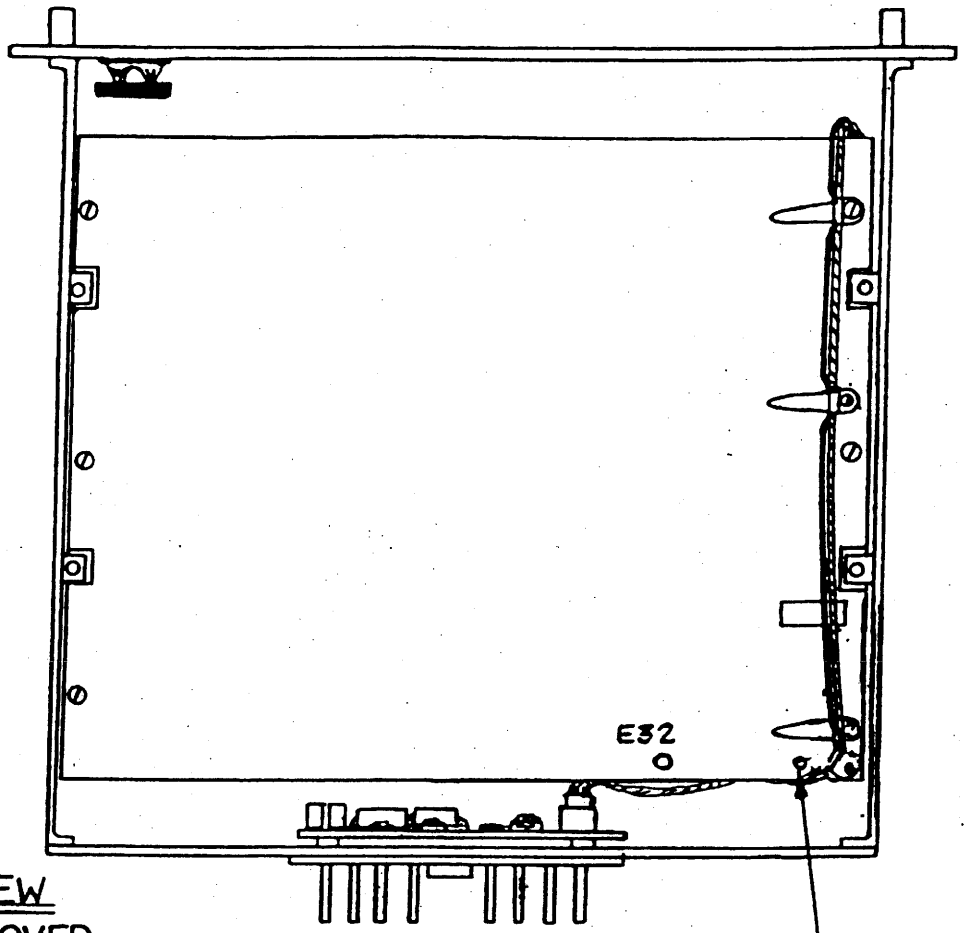


Figure 5.5-1 Installation, MSR 5050A



BOTTOM VIEW
COVER REMOVED

NOTES :

1. ROUTE WHT/BLK & BLK WIRES ALONG BOTTOM OF MOTHER BD. & UNDER CABLE CLAMPS PER FIGURE.

Figure 5.5-2 Installation, MSR 5050A

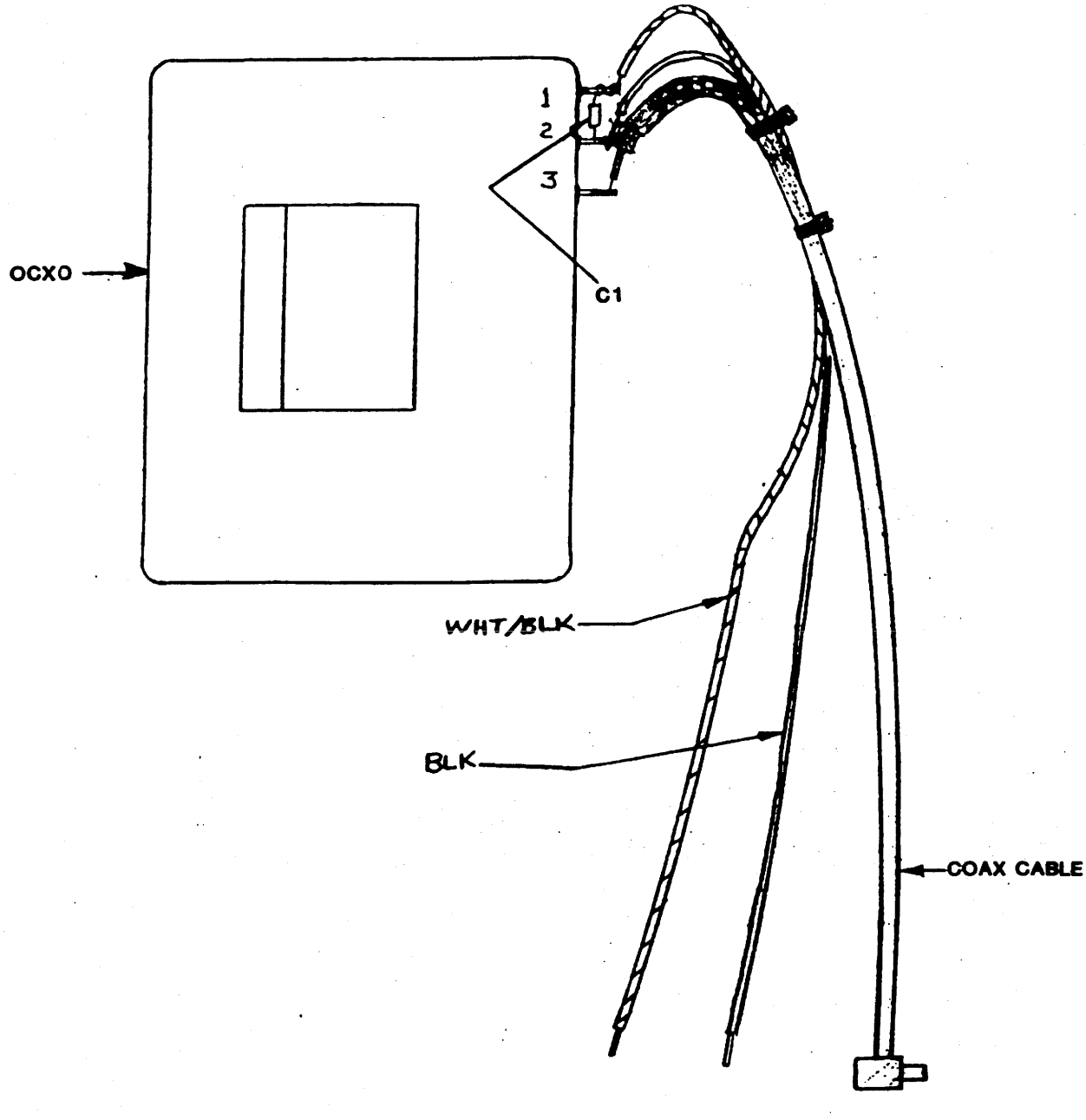


Figure 5.5-3 OCXO Assembly

5.6 ISB OPTION

5.6.1 GENERAL

The ISB Option adds a second simultaneous IF and audio signal path to the MSR 5050A Receiver. This is accomplished by adding an IF Filter Board containing an LSB Filter and an Audio Squelch board in order to AGC and demodulate the second channel. The MSR 5050A Mother board is altered by moving a jumper to reroute the LSB enable signal to IF Filter No. 2. S1-I on the Logic board is enabled to allow the radio to activate ISB controls.

5.6.2 SPECIFICATIONS

Detection Mode: Simultaneous USB and LSB

Controls: Mode Key - Pushbutton key cycles through all Modes by successive pushes. LED bar graph indicates choice.

Monitor Keys - USB and LSB momentary pushbutton keys with LED's to indicate status. Causes corresponding speaker and meter indications.

Output: Same specification for audio level, distortion, AGC, etc. as USB or LSB in the standard radio except USB and LSB occur simultaneously on rear panel J42 pins 23,24 and pins 22, 21.

Sensitivity: Same as USB or LSB - -113 dBm for 10 dB (S+N)/N.

5.6.3 INSTALLATION

The MSR 5050A to be modified has previously been adjusted and tested. Remove top cover and top shield. Move jumper JP37 on the Mother board to the right (to E37 pins 1,2). Move option switch S1-1 on the Logic board to the down position. Install Audio Squelch board No. 2 in J8. For -001 option, also install IF Filter board No. 2 in J12.

5.6.4 ADJUSTMENTS/TESTS (Audio Measurements Made Across 600Ω Load)

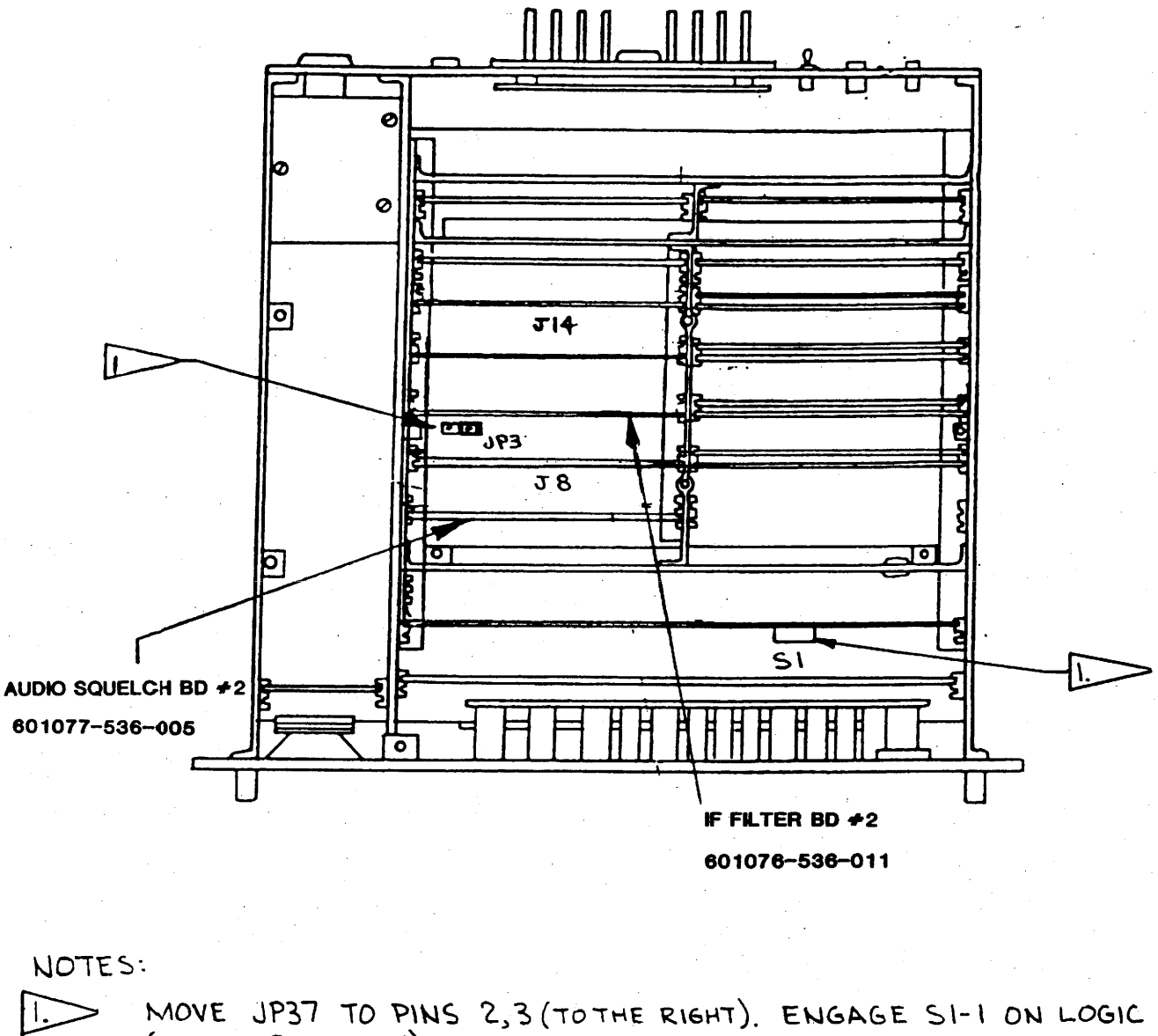
Tune receiver to 11.246 MHz, ISB mode, AGC fast. Connect signal generator to antenna connector J46; set to 11.247 MHz, unmodulated, -113 dBm (0.5 μV). Note audio level on standard 600 ohm output (J42-23,24). Measure sensitivity S+N/N (10 dB minimum). Change generator to 11.245 MHz. ISB audio output level (J42-21,22) should be the same as before. Adjust IF Filter board R35 (IF gain) if necessary. Measure sensitivity S+N/N (10 dB minimum).

Increase generator level to 50 μV (-73 dBm). Audio level (J42-22,21) should be 0 dBm. Adjust ISB line level R64 on Audio squelch board No. 2 if necessary. Press "AF" meter key; press "LSB" meter key (note 1 kHz tone in speaker).

Front panel meter should indicate 0 dBm. If not, recheck meter adjustment (Interface board R16) in USB mode (600 ohm line output should be loaded).

Increase generator level to -7 dBm (100 mV). Press "RF" meter key. Meter should indicate 100 dBμV. Adjust R44 on Audio Squelch board No. 2 if necessary to account for differences from the No. 1 Audio Squelch board. (R15 on the Interface board adjusts the RF meter for both standard and ISB channels.)

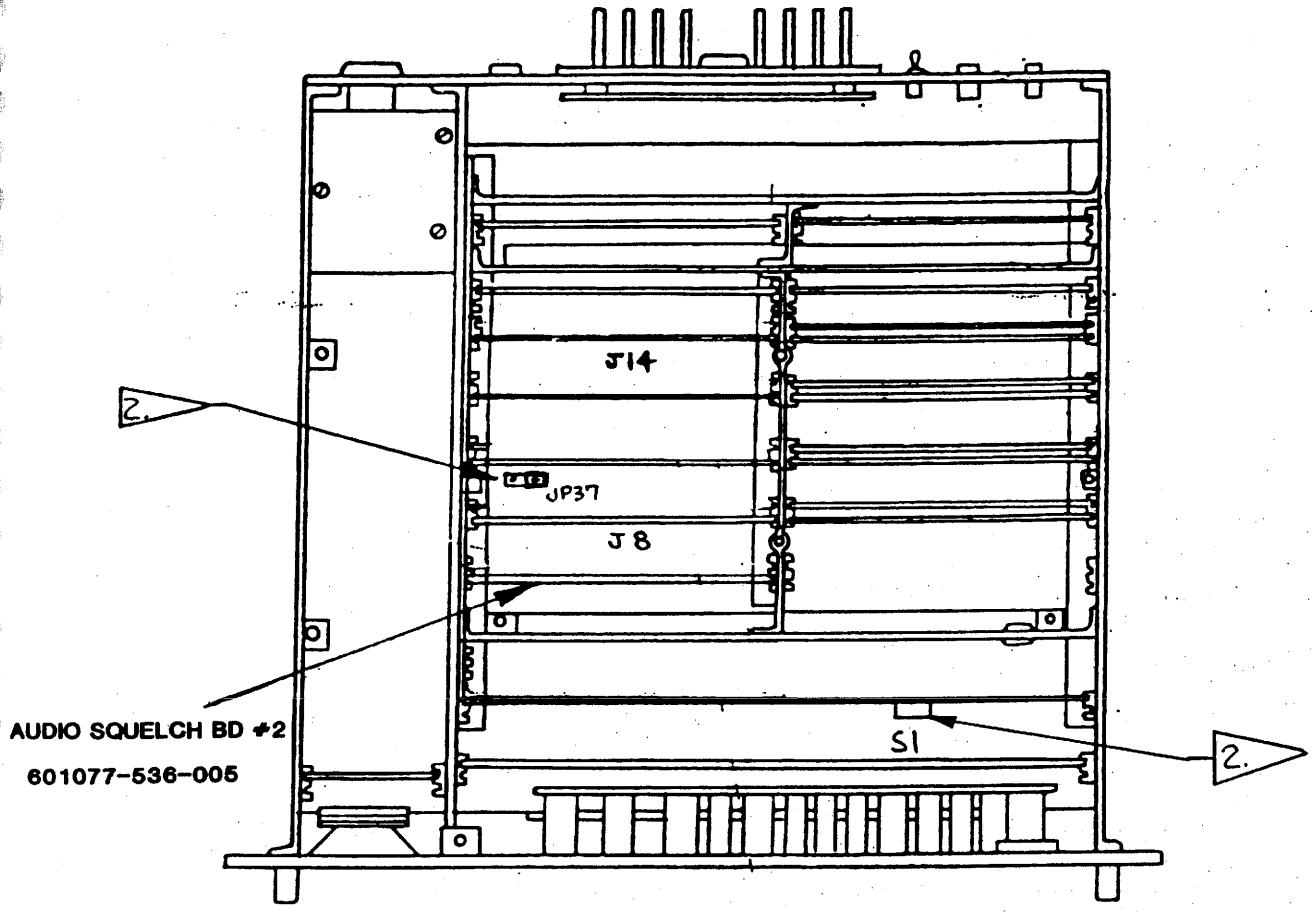
Change generator level from AGC threshold (level at which barely perceptible meter reading occurs - approximately -90 dBm) to +13 dBm. Audio output level should change 3dB or less. If not, repeat alignment for IF Filter and Audio Squelch boards in ISB mode for the No. 2 boards (see Table 4.6-2).



NOTES:

1. MOVE JP37 TO PINS 2,3 (TO THE RIGHT). ENGAGE S1-1 ON LOGIC BOARD (DOWN POSITION).

Figure 5.6-1 Installation -001 (Option A)



NOTES:

1. THIS OPTION IS INSTALLED AFTER IF FILTER OPTION IS INSTALLED.

2. MOVE JP37 TO PINS 2,3 (TO THE RIGHT). ENGAGE S1-1 ON LOGIC BOARD. (DOWN POSITION).

Figure 5.6-2 Installation -002 (Option B)

5.6.5 IF FILTER BOARD NO. 2, A10

The IF Filter board added for ISB option-001 is 601076-536-011, which is the same as the standard board 601076-536-010 (see Section 4.16) with the following exceptions:

FL1 is an LSB filter 600083-529-001
FL2 and FL3 are not used.

Pin outs, schematic, and assembly are otherwise identical.

5.6.6 AUDIO SQUELCH BOARD NO. 2, A12

The Audio Squelch board (601077-536-005) is identical to that used in the standard radio. See Section 4.17.

5.7 BFO OPTION (BFO BOARD, A20)

5.7.1 GENERAL

The BFO Option adds a synthesized 3rd LO to the MSR 5050A by adding a plug-in BFO board and by manipulating jumpers. One jumper reroutes the 3rd LO signal from the BFO board instead of the fixed 5 MHz output of the Reference board. A second jumper grounds a disable line to the Reference board which internally gates off the fixed 5 MHz signal to reduce interference. Enabling a switch on the Logic board alters the MSR 5050A microprocessor program to recognize, address, and execute BFO control inputs.

5.7.2 SPECIFICATIONS

Tuning Range:	0 to ± 7.99 kHz
Tuning Resolution:	10 Hz steps
Controls:	Rotary tune knob - with ± BFO offset frequency proportional to CW (+) or CCW (-) knob position. BFO Key - Enable BFO mode. Tune Rate key -selects 10 Hz, 100 Hz, or lock.
Indicators:	Display - Four 7-segment readouts indicate 1 kHz, 100 Hz, and 10 Hz tuned offset with a "-" indicating negative offset. Mode Indicator - BFO key is lighted when BFO mode is enabled. Tune Rate Indicator-LEDs indicate 10 Hz or 1 KHz tune rate.
Operation:	Mode - Press BFO key to enable variable knob tuning. Entry - Tune knob CW or CCW for + or - offsets to a limit of ± 7.99 kHz. Termination - Clear (C) key terminates the BFO mode at any time and tunes the BFO offset to previously stored offset. Enter (E) key terminates the BFO mode at any time with the BFO offset displayed.

5.7.3 INSTALLATION (Refer to Figure 5.7-1)

The MSR 5050A to be modified should have been previously tested. Check that the IF Filter board has been installed in J14 as part of the standard radio or as part of the ISB or Filter Option.

With the MSR 5050A top cover and shield removed, unplug the Logic board and position dip switch S1-4 in the down position. Locate two-pin shorting jumpers JP9 and JP10 on the Mother board near J7. Move to the right (pins 2, 3 on headers E9, E10). Install the BFO board in J7.

5.7.4 CHECKOUT

5.7.4.1 Knob Tuning

Turn on power - VOLUME 1/4 turn, speaker on. Connect coax from MSR 5050A rear panel REF output (J41) to antenna connector J46. Tune frequency to 5.000 MHz. Select CW mode, wide BW. Press BFO (key lights). Turn tune knob clockwise. Display should indicate increasing frequency to 7.99 kHz (with corresponding tone from speaker) in 10 Hz steps. Turn tune knob CCW. Display should indicate decreasing frequency through 0.00 to indicate decreasing frequency through 0.00 to -7.99 kHz with tone from speaker decreasing corresponding to 0.00 and then increasing to 7.99 kHz.

5.7.4.2 Test Storage

Press CHAN, 8, 8, FREQ, 5, E, BFO, Tune Rate

(indicates 10 Hz). Rotate Tune Knob clockwise until offset indicates 1.00. Press E. Press mode key until CW indicated, press Filter Key until wide indicated. Press E. Displays indicate accordingly. Speaker emits 1 kHz tone. Turn power off, then on. Displays, tone and key lights should return as before. Press CHAN, 0, 1, E. All conditions change. Press CHAN, 8, 8: Tone and key lights same as previous step. Press E (Enter) - displays and key lights indicate stored data and 1 kHz tone is present. Test is complete. Reinstall top shield and cover.

5.7.5 BFO BOARD, A20

5.7.5.1 Description

The BFO generates the L03 output for the Audio Squelch board. It outputs a 4.99000 to 5.00999 MHz signal in 10 Hz steps.

The VCO (Q5, C1, C2, L1, and CR1) is a Colpitts Oscillator whose frequency (100.000 to 100.999 MHz) is determined by the DC voltage at the junction of CR1 and C1. The VCO output drives two isolation buffers. The first (Q6 and associated components) drives a divide by 2 counter U13. The output of U13 is passed through a filter and then applied to Q8. The second buffer (Q7 and associated components) drives a divide by 10/11 prescaler U11, whose output drives programmable dividers U1 through U14.

The programmable divider functions in the following manner: U3, U4, U5, U6, and U14 are parallel-loadable UP/DOWN counters which are cascaded and permanently connected to count DOWN. Counter U14 determines the most significant digit and is connected to load 5 when BFO SIGN is high and load 4 when BFO SIGN is low. The BFO SIGN is also connected to Q11 which controls what is loaded into U6 and U5. When BFO SIGN is high, Q11 is on - causing U6 and U5 to load 0; when BFO SIGN is low, Q11 is off - causing U6 and U5 to load 9. U7 is an array of open collector inverters which have their outputs, along with collector of Q10, connected together to form a NOR gate. The output (pins 2, 4, 6, 8, 10, 12, and collector of Q10) can only go high if all the inputs (pins 1, 3, 5, 9, 11, 13, and base of Q10) are low. The U7 inputs and Q10 are connected so that the output goes high when the counter (U14-U3) contains the number 02. To understand the operation, assume that the counter has just been loaded with the number 14, and BFO SIGN is high. The counters begin counting down. Because the D input (pin 2) is low, pin 5 of U2 (Q) stays low and pin 6 ($\overline{Q}$) stays high. After 50,000 pulses U14 underflows and causes the collector of Q10 to go high. After another 10,000 pulses U6 underflows and U7 (pin 1) goes low. After another 1,000 pulses U5 underflows and Q7 (pin 3) goes low. After another 100 pulses U4 underflows and U7 (pin 5) goes low. After another 2 pulses pins 9, 11, and 13 of U7 are low; so the "output" of number 02 and the D input (pin 2 of U2) goes high (this is the programmable divider output pulse) and pin 6 goes low - again loading U3, U4, U5, U6, and U14 with the divide number. The next pulse (number 00) toggles pin 6 high and pin 5 low. The cycle can now repeat. U1 controls the least significant number; when it underflows, it sets U2 (pin 9) which sets U11 to divide by 10 or 11.

The output of the programmable divider U2 (pin 5) is fed to the phase/frequency detector U9, where it is compared with 200 Hz from the output of the divide by 5 divider U13. If the divider output is too low in frequency or lagging the 200 Hz reference in phase, the phase detector output (pins 5 and 10) goes down. This causes the voltage of the VCO control line to rise, which raises the frequency to correct the error.

The loop amplifier consists of Q2 and Q3, which form a high input impedance inverting stage. The amplifier and feedback components (R20, R19, C31, and C32) form an active loop filter which determines the overall loop stability. Transistor Q4 with components R17, R16, C28, and C27 form an active low pass filter with a sharp corner and steep rolloff to attenuate the reference side-bands.

Components R11, R10, and R12 and C24, C25, C26, and C23 form a Twin-T notch filter centered on 1 KHz to further attenuate the first order sidebands.

The loss-of-lock circuitry works as follows: phase

detector outputs (pin 11 and pin 4) are normally high with nearly 100 percent duty cycle in a properly locked loop. This means that the base and, therefore, the emitter of Q1 is also high; driving pin 2 of U8 low. This makes pin 12 and 4 of U8 high so the LED is off. When the loop loses lock, the duty cycle will drop at either pin 11 or pin 4 (of U9). This discharges C35 through R24 faster than it can be recharged by R22; so the base voltage of Q1 drops - causing pin 2 of U8 to go high. This turns on the LED and drives the LL line low. The pin number (11 or 4) that goes low in loss-of-lock depends on whether the VCO frequency is too high or too low.

An on-card 8V regulator (U10) supplies the linear circuits with clean power.

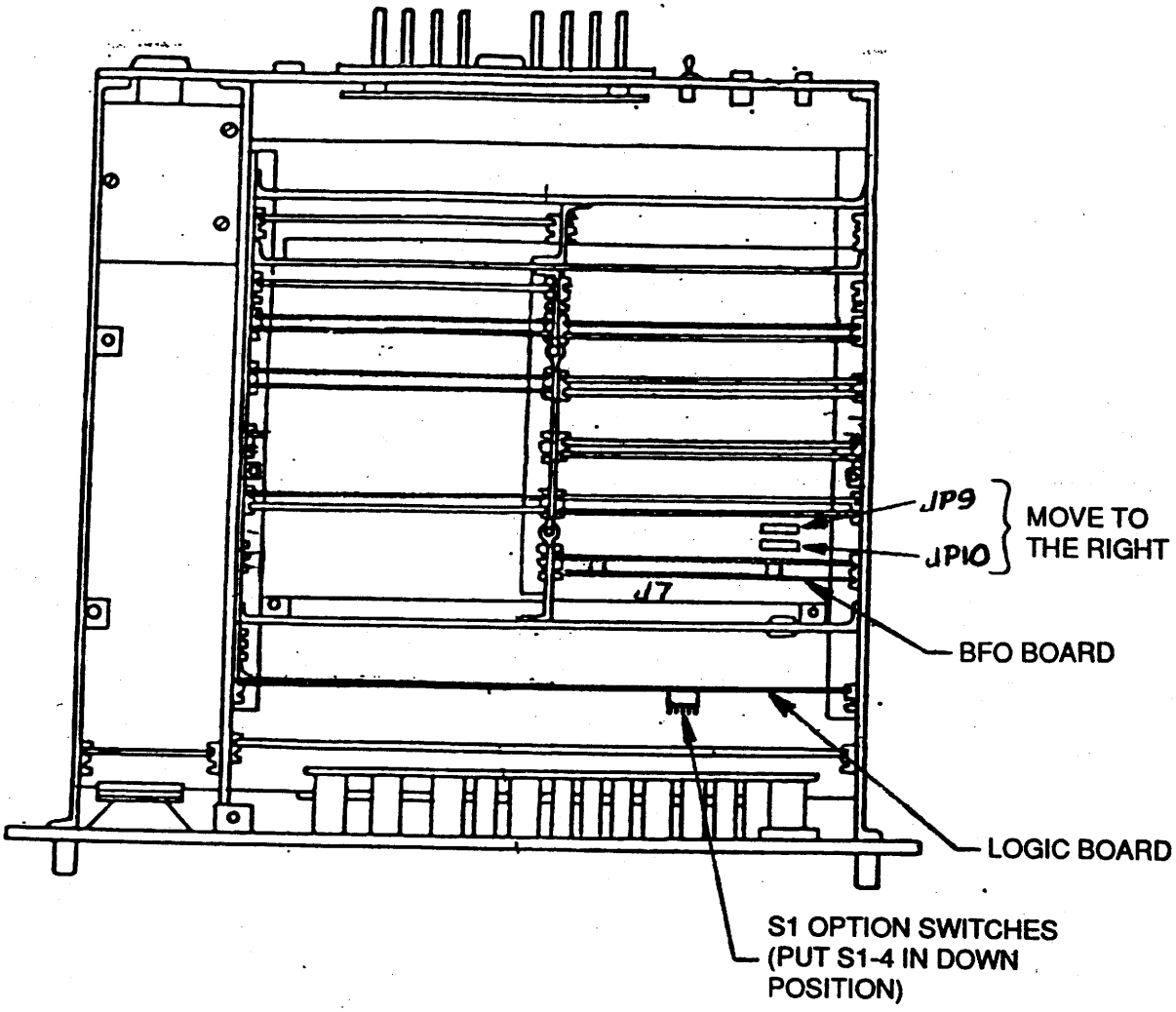
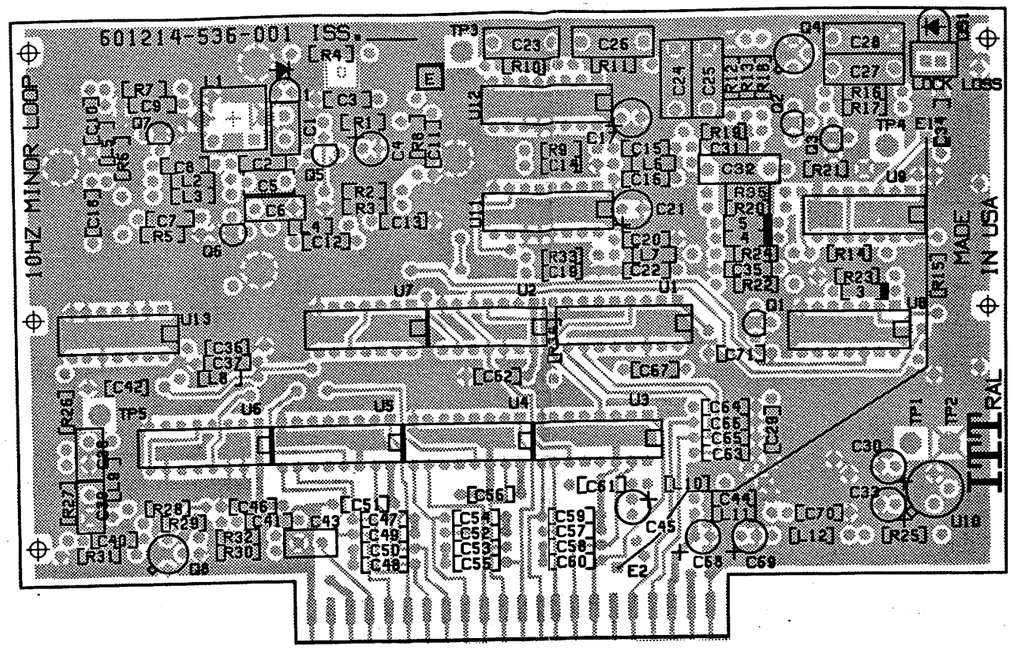


Figure 5.7-1 Installation, BFO Option



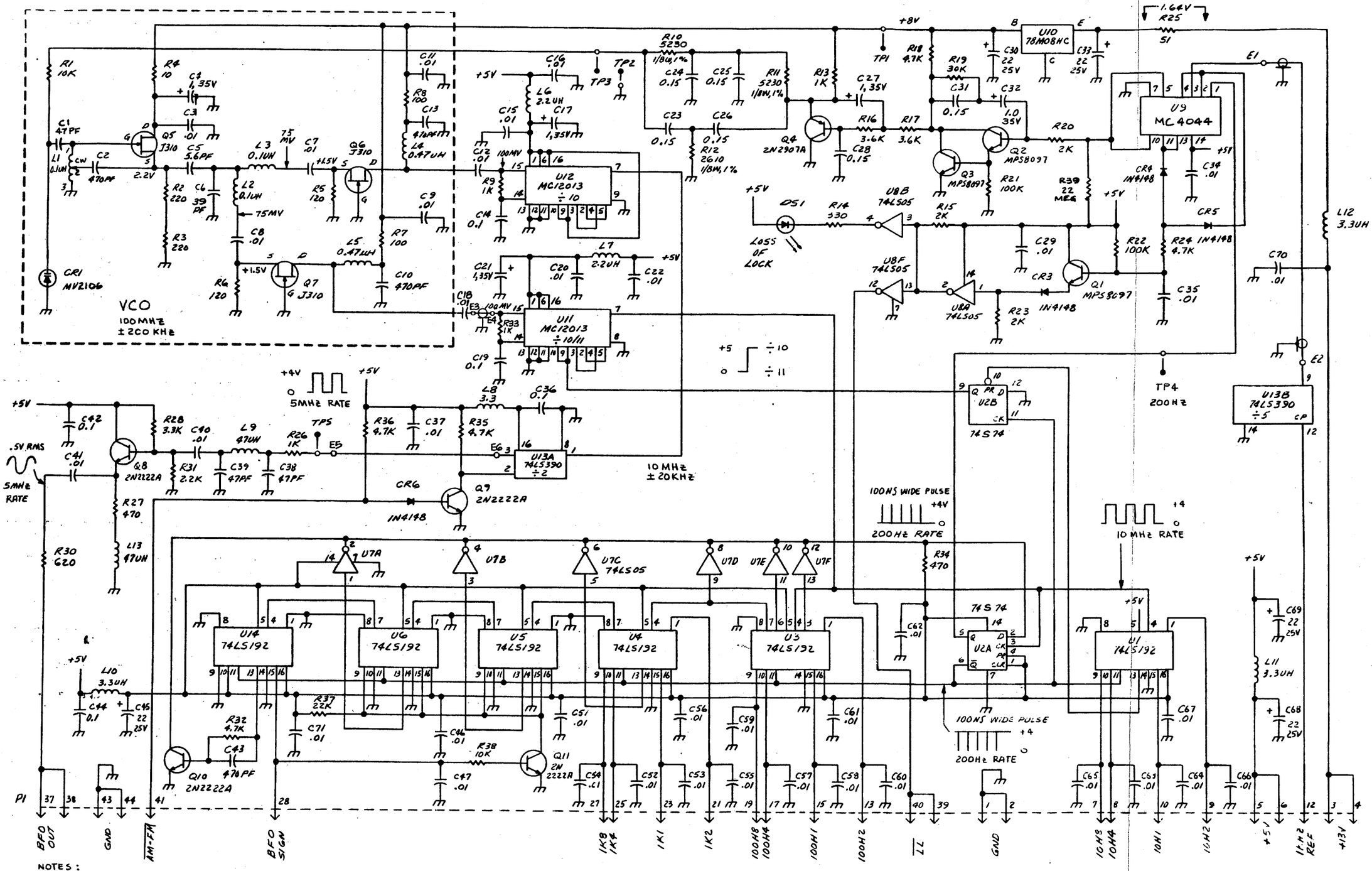
BFO (601215-536-001)

PART NUMBER	DESCRIPTION	SYMBOL
647093-306-501	CAP. 47PF, 3%, MICA, 500V	C10
600272-314-001	CAP. .1UF, CERAMIC, 50V	C3,7-9, 11,12,15, 16,18,20, 22,29,34, 35,37,40, 41,46,47, 51-67, 70,71
600272-314-003	CAP. .01UF, CERAMIC, 50V	C18,20 22,29 34,35
600272-314-005	CAP. 470PF, CERAMIC, 50V	C2,10 13,43
600204-314-027	CAP., 100V MYLAR	C23-26, 28,31
600297-314-016	CAP. 22UF, ALUM, 25V	C30,33, 45,68, 69
647093-306-501	CAP. 47PF, 3%, MICA, 500V	C38,39
600202-314-007	CAP. 1UF, 35V, TANT.	C4,17,21 27,32
600269-314-006	CAP. 5.6PF, CERAMIC, 500V	C5
600269-314-020	CAP. 39PF, CERAMIC, 100V	C6
600123-410-003	DIODE, VARACTOR, MV2106	CR1
600109-410-001	DIODE IN4148	CR3-6
600036-390-001	LED, RED	DS1
600173-376-001	COIL, VAR, .1UH	L1
600125-376-028	CHOKE .1UH	L2,3
600125-376-027	CHOKE .47UH	L4,5
600125-376-016	CHOKE 2.2UH	L6,7
600125-376-006	CHOKE 3.3UH	L8,10-12
600125-376-008	CHOKE 47UH	L9,13

PART NUMBER	DESCRIPTION	SYMBOL
600278-413-001	TRANSISTOR MPS8097	Q1-3
600154-413-001	TRANSISTOR 2N2907A	Q4
600259-413-001	TRANSISTOR J310	Q5-7
600080-413-001	TRANSISTOR 2N2222A	Q8-11
610024-341-075	RES. 10K, 1/4W, 5%	R1,38
652311-342-059	RES., 5.23K, 1/8W, 1%	R10,11
626111-342-059	RES. 2.61K 1/8W 1%	R12
633004-341-075	RES. 330, 1/4W, 5%	R14
620014-341-075	RES. 2K, 1/4W, 5%	R15,20,23
636014-341-075	RES. 3.6K, 1/4W, 5%	R16,17
647014-341-075	RES. 4.7K, 1/4W, 5%	R18,24, 32,35,36
630024-341-075	RES. 30K, 1/4W, 5%	R19
622004-341-075	RES. 220, 1/4W, 5%	R2,3
610034-341-075	RES. 100K, 1/4W, 5%	R21,22
647004-341-075	RES. 470, 1/4W, 5%	R27,34
633014-341-075	RES. 3.3K, 1/4W, 5%	R28
662004-341-075	RES. 620, 1/4W, 5%	R30
622014-341-075	RES. 2.2K, 1/4W, 5%	R31
622024-341-075	RES. 22K, 1/4W, 5%	R37
622054-341-075	RES. 22M, 1/4W, 5%	R39
610094-341-075	RES. 10, 1/4W, 5%	R4
612004-341-075	RES. 120, 1/4W, 5%	R5,6
610004-341-075	RES. 100, 1/4W, 5%	R7,8
610014-341-075	RES. 1K, 1/4W, 5%	R9,13, 26,33
651094-341-075	RES. 51, 1/4W, 5%	R25
600225-415-001	IC 74LS192, UP/DN CNTR, SYNC	U1,3-6,14
600157-415-001	IC 74S74, D FLIP-F, DUAL	U2
600240-415-001	IC 74LS05, HEX INV, O/C	U7,8
600092-415-001	IC MC4044, PHASE DET.	U9
600526-415-001	IC 78M08, 8V REG	U10
600241-415-001	IC 2013, 2-MOD	U11,12
600535-415-001	IC 74LS390, 2 DEC RIP CNTR	V13

Figure 5.7-2

BFO Assembly



NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL CAPACITOR VALUES ARE IN MICROFARADS, ALL RESISTOR VALUES ARE IN OHMS, 1/4W ±5%.

Figure 5.7-3

BFO Board Schematic

MSR 5050A BFO BOARD A20

PIN CONNECTIONS AND VOLTAGE READINGS

A20P1

	GND	1	2	GND	
	+13 VDC	3	4	+13 VDC	
	+5 VDC	5	6	+5 VDC	
LOGIC "Ø" OR "1"	10H's - 8	7	8	10H's - 4	LOGIC "Ø" OR "1"
LOGIC "Ø" OR "1"	10H's - 2	9	10	10H's - 1	LOGIC "Ø" OR "1"
		11	12	1 kHz REF	
LOGIC "Ø" OR "1"	100H's - 2	13	14		
LOGIC "Ø" OR "1"	100H's - 1	15	16		
LOGIC "Ø" OR "1"	100H's - 4	17	18		
LOGIC "Ø" OR "1"	100H's - 8	19	20		
LOGIC "Ø" OR "1"	1K's - 2	21	22		
LOGIC "Ø" OR "1"	1K's - 1	23	24		
LOGIC "Ø" OR "1"	1K's - 4	25	26		
LOGIC "Ø" OR "1"	1K's - 8	27	28	BFO SIGN	LOGIC "Ø" OR "1"
		29	30		
		31	32		
		33	34		
		35	36		
0.5 V RMS - 5 MHz	BFO OUT	37	38	BFO OUT	0.5 VRMS - 5 MHz
LOGIC "Ø" OR "1"	$\overline{LL}$	39	40	$\overline{LL}$	LOGIC "Ø" OR "1"
LOGIC "Ø" OR "1"	$\overline{AM - FM}$	41	42		
	GND	43	44	GND	

5.8 IF FILTER OPTION

5.8.1 GENERAL

The IF Filter Option increases the number of selectable bandwidths in the MSR 5050A Receiver. This is accomplished by adding an IF Filter board to the standard radio which has been previously tested with the standard (-010) IF Filter board. IF Filter board No. 2 has an LSB filter, a 1 kHz (NAR) filter, and a 400 Hz (VNAR) filter. When two filter boards are used, the LSB filter is enabled by selecting FL1 in IF Filter No. 2 instead of FL2 in IF Filter No. 1 board. IF Filter board No. 1 has a USB filter in FL1, a 6 kHz (WIDE) filter in FL3, and a 16 kHz (VWIDE) filter in FL2 (in place of the LSB filter). This allows the maximum complement of filters. Placing S1-3 in the down position on the Logic board conditions the radio program to enable the additional filter bandwidth controls. Specifications are also detailed with the IF Filter board (601076-536-XXX, Section 4.16) and the MSR5050A Performance Specifications.

In the IF Filter Option all AM and CW filters are centered on the tuned receiver frequency; when the MED bandwidth key is selected in conjunction with AM, CW or FSK, the USB filter is enabled. The first LO is offset 1.7 kHz low while the frequency display remains unchanged. This centers incoming signals at the indicated frequency in the center of the offset USB filter. For CW and FSK, the BFO is also offset 1.7 kHz low to produce a zero beat for incoming signals at the indicated frequency. For this reason the IF Filter Option must be accompanied by the BFO Option 600107-700 instead of the fixed 5 MHz, 3rd LO from the Reference board in the standard radio. Figure 5.8-1 shows the complement of filters for the Filter Option. Refer to Section 4.16 for detailed information on the IF/Filter boards.

5.8.2 INSTALLATION

The MSR 5050A to be modified should have been previously tested with a standard IF Filter board. Remove the top cover and shield. Locate and move jumper JP37 on the Mother board to the right (to E37 pins 1,2). Place dip switch S1-3 on the Logic board in the down position. Plug IF Filter 601076-536-013 into J14. Plug IF Filter 601076-536-019 into J12. Figure 5.8-2 shows the locations of components involved.

	STANDARD RADIO	FILTER P/N
1A14 601076-536-010	FL1 USB	600084-529
	FL2 LSB	600083-529
	FL3 AM 6 kHz	600082-529

MSR 5050A with FILTER OPTION

IF Filter #1 1A14 601076-536-013	FL1 USB	600084-529
	FL2 AM 16 kHz	600093-529
	FL3 AM 6 kHz	600082-529
IF Filter #2 1A12 601076-536-019	FL1 LSB	600083-529
	FL2 CW 1 kHz	700004-529
	FL3 CW 400 Hz	700005-529

Figure 5.8-1 Filter Complements

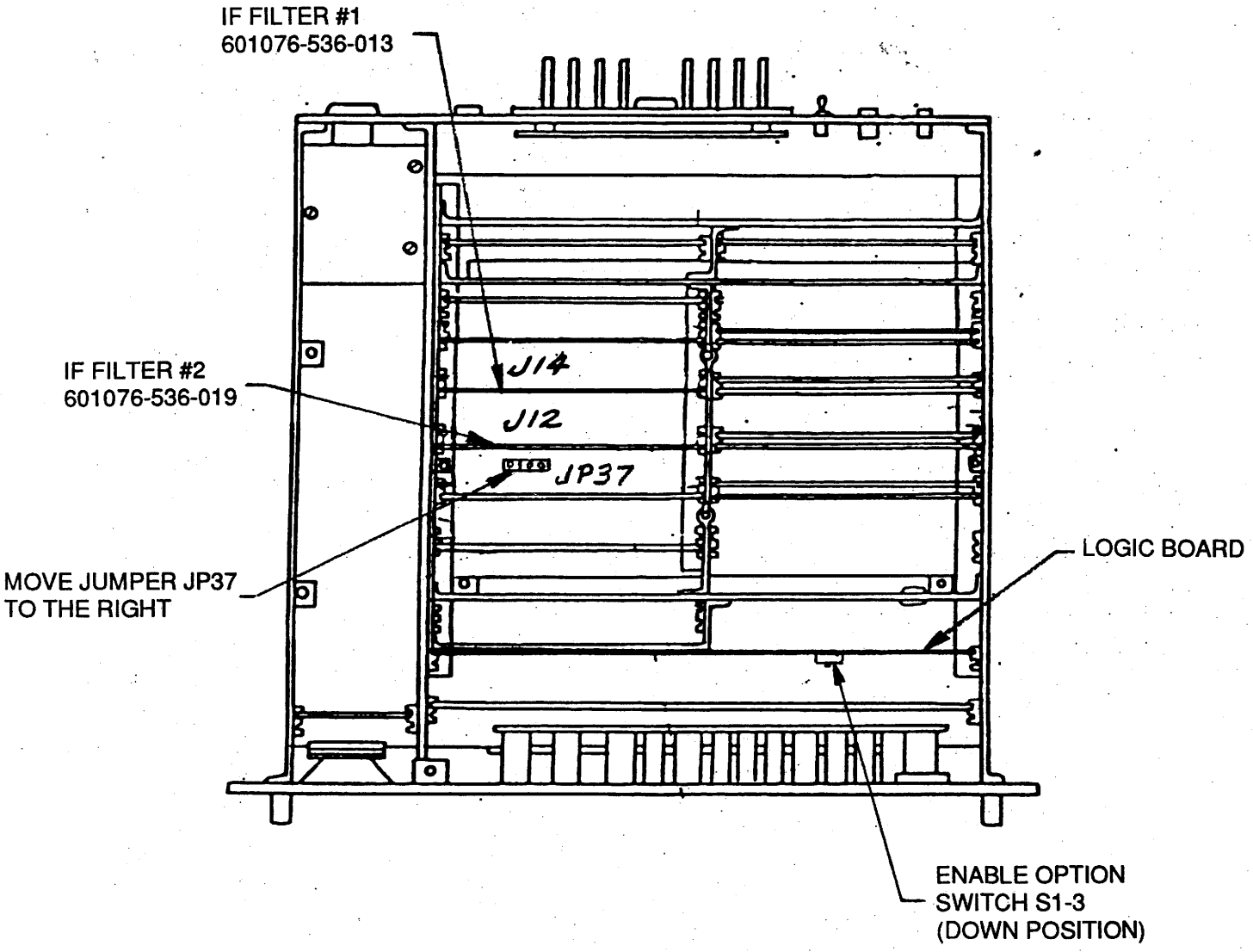


Figure 5.8-2 Installation

Table 5.8-1 SELECTIVITY SPECIFICATIONS

MODE KEY	FILTER KEY	BW 6 dB	BW 60 dB
USB	MED	+.3/+3 kHz	-1.5/4.5 kHz
LSB	MED	-.3/-3 kHz	+1.5/-4.5 kHz
ISB	MED	(Same as USB & LSB)	
AM, CW, FSK	MED	-1.4/+1.3 kHz	-3.2/+2.8 kHz
AM, CW, FSK	WIDE	±2.5 kHz	±9 kHz
AM, CW, FSK	VWIDE	* ±6 kHz	±20 kHz
AM, CW, FSK	NAR	±500 Hz	±3 kHz
AM, CW, FSK	VNAR	±200 Hz	±2 kHz

* BW 3 dB

Table 5.8-2 SENSITIVITY SPECIFICATIONS

(10 dB (S + N)/N, 2 to 30 MHz)

MODE KEY	FILTER KEY	BW 6 dB
SSB		-113 dBm
CW, FSK	VWIDE	-107 dBm
CW, FSK	WIDE	-110 dBm
CW, FSK	MED	-113 dBm
CW, FSK	NAR	-117 dBm
CW, FSK	VNAR	-120 dBm
AM (30% MOD)	VWIDE	-91 dBm
AM (30% MOD)	WIDE	-97 dBm
AM (30% MOD)	MED	-95 dBm

5.9 DATA FILTER OPTION

The Data Filter option (P/N 700418-700-XXX) substitutes controlled group delay filters for the LSB and USB filters in the IF Filter boards. The filter characteristics conform to those specified in MIL-STD 188-203-1 for TADIL A data modems. They will be compatible with most high speed multitone RF data modems where tight control of amplitude and group delay (timing) in the pass-band is required. The specifications for the USB filter (P/N 600127-529-001) are as follows. (LSB filter P/N 600128-529-001 has identical specs with mirrored frequencies):

BW 2 dB +450 to +3050 Hz
BW 3 dB +300 to >+3050 Hz
BW 60 dB -400 to +4400 Hz
Ripple 2 dB maximum
Diff. Time Delay 815 to 3050 Hz, 500 μS max.
(Frequencies are referenced to the carrier and amplitudes are referenced to peak passband response.)

Option 700418-700-001 (for the standard radio) replaces IF Filter board #1 (A9) P/N 601076-536-010 with P/N 601076-536-020. The new board is identical except for FL1 and FL2. (See Section 4.16):

FL1 = P/N 600127-529-001 (vs. 600084-529-001) (USB)

FL2 = P/N 600128-529-001 (vs. 600083-529-001) (LSB)

FL3 = same as old board (600082-529-001) (AM)

Option 700418-700-002 (for a radio with ISB Option A) replaces IF Filter board #1 (A9) P/N 601076-539-010 with P/N 601076-536-021. It also replaces IF Filter board #2 (A10) P/N 601076-536-011 with P/N 601076-536-022. (See Section 4.16 and 5.6.)

IF Filter board 601076-536-021 is identical to 601076-536-010 except for filters FL1, FL2 and FL3:

FL1 = 600127-529-001 (vs. 600084-529-001) (USB)

FL2 is vacant (vs. 600083-529-001) (Not Used With ISB Option)

FL3 = same as old board 600082-529-001 (AM)

IF Filter board 601076-536-022 is identical to 601076-536-011 except for filter FL1:

FL1 is 600128-529-001 (vs. 600083-529-001) (LSB)

FL2,3 are vacant on both boards.

The USB filter on IF Filter board #1 is used in CW (with MED filter selected) and in FSK (with MED filter selected) and will have the same group delay and response as in USB mode.

The AM mode also uses the USB filter for the MED filter selection. The first and second LOs are offset 1.7 kHz to electrically center the response on the radio tuned frequency.

APPENDIX I

PROTOCOL SPECIFICATIONS

INTRODUCTION

The MSR 5050A receiver, MSR 6700A exciter, and MSR 8050A transceiver have built- in remote control capability which can be accessed either by an MSR 6420 Universal Remote Control unit, or by the CSW 1000 communications program which runs on a PC. When the "Remote" key is pressed on the front panel, the radio will be ready for remote control. The radio waits for a "command string" from the Remote Control Unit (RCU) and then responds by returning a "Status string". Commands range from a "Status request" to radio control commands. There must be at least a 100 mS delay from the time the radio returns status, before the next command is sent to the radio.

The radios can communicate using RS-232C, RS-422, RS-423, MIL-STD-188C or FSK. Communication Baud rates available are 300, 600, 1200, 2400, 4800 and 9600. The format is 1 Start bit, 1 Stop bit, 8 Data bits, Even Parity, and Half Duplex. (There are 11 bits transferred per word). The least significant data bit is sent first. See Figure A1.1.

RADIO COMMANDS

The radio command string consists of the following parts:

The Sync Word: This is always the first word of any command. See Figure A1.2. The Sync word has the format:

Bits 6-7 => (2 High Order Bits) always 1.
Bit 5 => PTT (1=on, 0=off) Always "0" for an MSR 5050A. A "1" will cause an MSR 6700A and an MSR 8050A to key. A "0" will cause an MSR 6700A and an MSR 8050A to unkey.
Bit 4 => Specifies whether command that follows refers to Transmit or Receive Frequency. (1=Xmt, 0=Rcv)
Bit 3 => Specifies whether all radios in Remote Control Network should change their Switched Audio or not. (0=Change Switched Audio, 1=Not Change Switched Audio)
Bits 0-2 => Always 000 for Remote to Radio commands. Always 111 for Remote to Remote commands.

NOTE: Bit 4 is important for MSR 8050A. Bit 4 is meaningless for MSR 5050A and MSR 6700A.

NOTE: Bit 3 is important for jointly controlled MSR 5050A/MSR 6700A pairs. When this bit is low, any radio in the Remote Control Network not addressed in the Command String that follows will deselect its Switched Audio. Of course, the radio that is addressed will turn on its Switched Audio path. When this bit is high, any radio in the Remote Control Network will not change its Switched Audio path, regardless of whether it has its Switched Audio path on or not, and regardless of whether it is addressed or not in the Command String that follows. Thus, if the Remote is controlling a 5050A/6700A pair, this bit provides the means by which both radios can be alternately addressed without causing either radio to deselect its Switched Audio path.

NOTE: Bits 0-2 are used by the radio to determine if the command that follows is a command for a radio or a command for another remote.

The Radio Address: This is always the second word of any command string, and it is a 2 -digit BCD number. The radio address is programmed at the radio, and is set while the radio is in local mode.

BCD

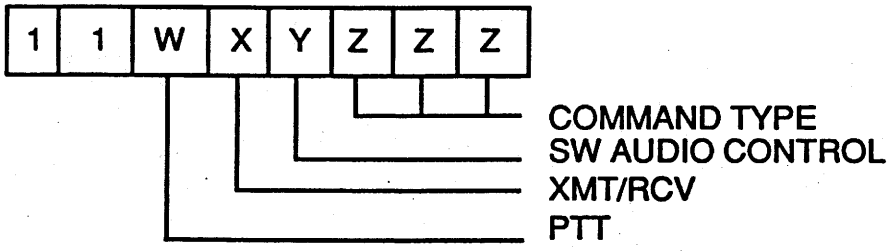
MSD	LSD

Figure A1.1 Protocol Word Format

START	DATA 1	DATA 2	DATA 3	DATA 4	DATA 5	DATA 6	DATA 7	DATA 8	PARITY	STOP

(EVEN PARITY)

Figure A1.2 Sync Word Format



The Command Word: This is always the third word of a command string. It is the actual command. (See the command word list.)

The Data Word(s): The needed data words for a command follow the command word. The number and type of data words depends on the command. Data words may not be omitted.

THE COMMAND WORD LIST

The command words are given as hexadecimal numbers, the data words which follow are BCD unless otherwise stated. These commands are used in all radios unless otherwise stated.

STATUS REQUEST

(Sync), (ADDR), (7F), (Remote Addr.)

The radio will return status (refer to the status string format) to the remote specified by the data word. The radio will continue to make all responses to this remote until another status request changes the remote address. Bit 4 of the Sync Word causes an MSR 8050A to select Transmit Mode if it is a "1" and Receive Mode if it is a "0". The MSR 8050A returns either the transmit or the receive information for the channel, depending on whether Bit 4 of the Sync Word is a "1" or a "0", respectively. Bit 4 of the Sync Word has no effect, of course, if the radio is an MSR 5050A or an MSR 6700A, since those radios only contain either receive information or transmit information, respectively.

CHANNEL RECALL

(Sync), (ADDR), (1A), (Channel Number)

The radio will "look up" the information for the channel specified by the data word. If the radio is an MSR 8050A, the radio will "look up" either the transmit or the receive information for the channel, depending on whether Bit 4 of the Sync Word is a "1" or a "0", respectively. Bit 4 of the Sync Word has no effect, of course, if the radio is an MSR 5050A or an MSR 6700A, since those radios only contain either receive information or transmit information, respectively. That channel information is returned through the return status, but the channel is not selected by the radio (the radio does not switch channels).

CHANNEL SELECT

(Sync), (ADDR), (0B), (Channel Number)

The radio will switch to the channel number specified by the data word. Bit 4 of the Sync Word has no effect, since the channel is selected regardless of whether it contains transmit information or receive information or both.

CHANNEL DATA SAVE

(Sync), (ADDR), (1B), (10 MHz, MHz), (100 KHz, 10 KHz), (1 KHz, 100Hz), (10Hz, Mode), (AGC, Filter), (BF01), (BF02), (Pwr. Lev.)

The radio will save the data given in the currently selected channel. Zeros are inserted where the above given data does not pertain to the type of radio being controlled. If the radio is an MSR 8050A, the radio will save either the transmit or the receive frequency for the channel, depending on whether Bit 4 of the Sync Word is a "1" or a "0", respectively. Bit 4 of the Sync Word has no effect, of course, if the radio is an MSR 5050A or an MSR 6700A, since those radios only contain either receive frequency or transmit frequency respectively. The first 3 data bytes are Frequency (in BCD). The other bytes are:

DATA BYTE #	BITS	USAGE
4	4-7	10 Hz. Freq.
4	0-3	Mode
5	4-7	AGC
5	0-3	Filter
6	6-7	Always 0
6	4-5	Tuning Rate
6	3	BFO Sign
6	0-2	BFO 1 KHz
7	4-7	BFO 100 Hz
7	0-3	BFO 10 Hz
8	2-7	Always 0
8	0-1	Power Level

MODE SELECT

(Sync), (ADDR), (0F), (Mode)

The radio will select the Mode specified in the data byte. Refer to the code translation table for Mode. If the radio is an MSR 8050A, the radio will select either a transmit mode or a receive mode for the channel, depending on whether Bit 4 of the

Sync Word is a "1" or a "0", respectively. Bit 4 of theSync Word has no effect, of course, if the radio is an MSR 5050A or an MSR 6700A, since those radios offer only one mode per channel.

POWER LEVEL SELECT

(MSR 6700A and MSR 8050A ONLY)
(Sync), (ADDR), (1C), (Power Level)

The radio will select the power level specified in the data byte. Refer to the code translation table for Power Level. Bit 4 of the Sync Word has no effect.

FREQUENCY SELECT

(Sync), (ADDR), (0D), (10 MHz, 1 MHz), (100 KHz, 10 KHz), (1 KHz, 100 Hz), (10 Hz, 0000)

The radio will select the frequency specified in the data. If the radio is an MSR 8050A, the radio will select either a transmit or a receive frequency for the channel, depending on whether Bit 4 of the Sync Word is a "1" or a "0", respectively. Bit 4 of the Sync Word has no effect, of course, if the radio is an MSR 5050A or an MSR 6700A, since those radios only contain one frequency per channel.

AGC SELECT

(MSR 5050A AND MSR 8050A ONLY)
(Sync), (ADDR), (1D), (AGC)

The radio will select the AGC specified in the data byte. Refer to the translation table for AGC. Bit 4 of the Sync Word has no effect.

FILTER SELECT

(MSR 5050A ONLY)
(Sync), (ADDR), (1E), (Filter)

The radio will select the Filter specified in the data byte. Refer to the translation table for Filter. Bit 4 of the Sync Word has no effect.

METER SELECT

(Sync), (ADDR), (1F), (Meter Meaning)

The radio's meter will change to the function specified in the data byte. Refer to the translation table for Meter Meaning. Bit 4 of the Sync Word has no effect.

START TUNE CYCLE

(MSR 6700A AND MSR 8050A ONLY)
(Sync), (ADDR), (03), (Tune Type)

The radio will initiate a tune cycle (assuming there is a coupler in the system). The type of tune (RF or Silent) is determined by the data byte. 1 => Silent, 2 => R.F. Tune. Bit 4 of the Sync Word has no effect.

TOGGLE COUPLER BYPASS

(MSR 6700A AND MSR 8050A ONLY)
(Sync), (ADDR), (20)

The radio will toggle the coupler bypass. This command has no data bytes. Bit 4 of the Sync Word has no effect.

BFO SELECT

(MSR 5050A ONLY)
(Sync), (ADDR), (21), (BFO1), (BFO2)

The radio will select the BFO value determined by the data bytes. Refer to the translation table for BFO. Bit 4 of the Sync Word has no effect.

SWITCH REMOTE CONTROL

(Sync), (ADDR), (22), (CONTROL MODE)

If the control mode is 0 the radio will switch to local operation. If the control mode is non-zero, the radio will switch to Remote control. Bit 4 of the Sync Word has no effect.

RF GAIN SELECT

(MSR 5050A AND MSR 8050A ONLY)
(Sync), (ADDR), (0E), (RF GAIN)

The radio will select the RF Gain Level based on the non-BCD number that it detects in the RF GAIN Byte of this Command String. The number in the RF GAIN Byte must be a hexadecimal number between 0H and 14H. Since the remotely controlled RF Gain function in the radio has a 20-step range, a hexadecimal 14 translates to a decimal 20, which produces maximum RF Gain in the Radio. A 0AH translates to a decimal 10, which produces the median RF Gain Level. A 0H of course produces zero or minimum RF Gain in the Radio. Bit 4 of the Sync Word has no effect.

ERROR HANDLING AND RESPONSES

The radios do error checking to protect themselves and attached equipment. The radios use error checking to trap invalid Sync Words, invalid Addresses, invalid Commands and invalid Data. If a radio receives an improper Address or an improper Command, it will not respond. Instead, it will ignore the data in the Command string and wait for the next valid Command sequence. If the radio receives improper Data Words, it will change the improper Data to a default value, after which it will return its current Status.

Radios check for receive errors which are caused by one of the following:

A Parity Error (Parity is Even).
A Framing Error.
An Overrun Error.

If there is a receive error in any byte of a Command String, the radio will ignore the rest of the Command String and wait for the next valid Command String with no errors. Note that there must be at least 100 mS delay from the time the radio returns Status, before the next Command is sent to the radio. Otherwise, a receive error could occur.

Radios check for valid Commands in a Command Sequence. Radios will not attempt to execute Commands that are not part of their Command Library. For example, an MSR 5050A receiver will not execute a coupler command, and an MSR 6700A exciter will not select AGC.

Radios check to determine if certain Data words have non-BCD characters in them. If these Data Words have non-BCD characters in them, the radio will change the improper Data to a default value, after which it will return its current Status.

Radios check every word for Sync Word characteristics. The only word that may have ones in the two high order bit positions is the Sync Word. If the radio sees any word with the two high order bits set, it will interpret that word as a Sync word and thus the start of a new Command String.

1	1	X	X	X	X	X	X

This combination only applies to the Sync Word.

Radios will inform their respective Remotes if they are experiencing a BITE Fault. The radio does this by shortening its Status String to four Bytes, as follows:

(Sync), (ADDR), (30), (BITE Fault)

Note the radio sends an illegal frequency of 30 MHz in the third Byte to inform the Remote of a BITE Fault. In a normal Status String, the third Byte contains the 10 MHz/1 MHz information, which will never be higher than 29, unless a BITE Fault has occurred. The fourth Byte in the BITE Fault String contains either a 1 or a 2. The meaning of these BITE Fault numbers is described as follows:

1 = Radio Power Supply BITE Fault
2 = Radio Synthesizer Loss of Lock BITE Fault

OPERATION IN LOCAL MODE

If the radio is in LOCAL mode, it is not ready to talk to a Remote, but it does monitor to see if a Remote sends a Command. If a Remote sends a Command to the radio while it is in LOCAL mode, then the radio will return Status. However, Bit 4 in the Return Status Sync word will be set to indicate that the radio is in LOCAL mode. The radio will not carry out any Commands while it is in LOCAL mode. It will only return Status. If the radio is busy doing something while in LOCAL mode, (such as changing frequency), then the radio will not be able to respond to the Remote. The Remote Control can use the "Switch Remote Control" command to put the radio into Remote mode (refer to the section on Remote Control Commands).

THE RADIO STATUS STRING

Once the radio has seen and identified a command string, the radio will carry out whatever commands are necessary, and then return its status. The status string gives to the Remote current radio data, such as the currently selected channel, frequency, mode, AGC, filter, band, BFO, power level, meter data, and coupler data. The information which is returned depends on the type of radio. For example, coupler data and power level only apply to the MSR 6700A and MSR 8050A, while AGC only applies to the MSR 5050A and MSR 8050A. Refer to the section for the specific radio.

There must be at least 100 mS delay from the time the radio returns status, before the next command is sent to the radio.

All radios have the same first two bytes in the return status. The first byte is the Sync Word. The format for the Sync word is similar to the one used for command Sync Words described in the section on Commands.

Sync Word Format

Bits 6-7 => (2 High Order Bits) always 1.

Bit 5 => PTT (1=on, 0=off) Always "0" for an MSR 5050A. A "1" indicates that an MSR 6700A or an MSR 8050A is keyed. A "0" indicates that an MSR 6700A or an MSR 8050A is unkeyed.

Bit 4 => Local response flag. (1=radio is in local mode, 0=radio is in remote).

Bits 0-3 => Radio type.
1 - MSR 8050A
2 - MSR 6700A
3 - MSR 5050A

The second byte of return status is the remote address. This is the address of the last remote to do a status request (7F Hex) of the radio. The remote adress is a two digit BCD number (00-99).

NORMAL RETURN STATUS FOR THE MSR 5050A RECEIVER

BYTE #	DATA
1	(Sync Word)
2	(Remote Address)
3	(10 MHz, 1 MHz)
(Frequency)	Bit 7 => Always 0
	Bit 6 => Always 0
	Bits 4-5 => 10 MHz
	Bits 0-3 => 1 MHz
4	(100 KHz, 10 KHz)
5	(1 KHz, 100 Hz)
6	(10 Hz, Mode)
7	(Channel Number)
8	(Meter Data)
	Bits 0-4 => Strength (0-20).
	Bits 5-6 => Meter Meaning.
	Bit 7 => Always 0.
9	(The Radio's Address)
10	(AGC, Filter)
11	(BFO1)
12	(BFO2)

NORMAL RETURN STATUS FOR THE MSR 6700A EXCITER

BYTE #	DATA
1	(Sync Word)
2	(Remote Address)
3	(10 MHz, 1 MHz)
(Frequency)	Bit 7 => Always 0
	Bit 6 => Always 1
	Bits 4-5 => 10 MHz
	Bits 0-3 => 1 MHz
4	(100 KHz, 10 KHz)
5	(1 KHz, 100 Hz)
6	(10 Hz, Mode)
7	(Channel Number)
8	(Meter Data)
	Bits 0-4 => Strength (0-20).
	Bits 5-6 => Meter Meaning.
	Bit 7 => Always 0.
9	(The Radio's Address)
10	(Coupler/Power Data)
	Bit 7 => Always 0
	Bit 6 => Fault (1=True)
	Bit 5 => Ready(1=True)
	Bit 4 => Coupler Bypass(1=True)
	Bit 3 => Silent Tuning (1=True)
	Bit 2 => R.F. Tuning (1=True)
	Bits 0-1 => Power Level

NORMAL RETURN STATUS FOR THE MSR 8050A TRANSCEIVER

BYTE #	DATA
1	(Sync Word)
2	(Remote Address)
3	(10MHz, 1 MHz)
(Frequency)	Bit 7 => Always 0
	Bit 6 => 1=Xmt Freq, 0=Rcv Freq
	Bits 4-5 => 10 MHz
	Bits 0-3 => 1 MHz
4	(100 KHz, 10 KHz)
5	(1 KHz, 100 Hz)
6	(10 Hz, Mode)
7	(Channel Number)
8	(Meter Data)
	Bits 0-4 => Strength (0-20).
	Bits 5-6 => Meter Meaning.
	Bit 7 => Always 0.
9	(The Radio's Address)
10	Bits 0-3 => AGC
	Bits 4-7 => Unused (Normally 0's)
11	(Coupler/Power Data)
	Bit 7 => Always 0
	Bit 6 => Fault (1=True)
	Bit 5 => Ready (1=True)
	Bit 4 => Coupler Bypass (1=True)
	Bit 3 => Silent Tuning (1=True)
	Bit 2 => R.F. Tuning (1=True)
	Bits 0-1 => Power Level

TRANSLATION TABLES

TYPE	CODE	MEANING
MODE	0	ISB
	1	AM
	2	CW
	3	USB
	4	LSB
	5	FSK
	6	A3A
	7	FM
	8	DATA
AGC	0	Off
	1	Slow
	2	Medium
	3	Fast
FILTER	0	Very Wide
	1	Wide
	2	Medium
	3	Narrow
	4	Very Narrow
	5	(Unused)
	6	FM
	7	SSB
BF01		
(bits 6-7)		Always 0
(bits 4-5)		Tuning Rate (below)
(bit 3)	0	Minus
	1	Plus
(bits 0-2)		1 KHz
BF02		(100 Hz, 10 Hz)
POWER LEVEL	0	Level 1 (25 watts)
	1	Level 2 (125 watts)
	2	Level 3 (500 watts)
	3	Level 4 (1000 watts)
TUNING RATE	0	Lock
	1	10 Hz
	2	1 KHz
	3	100 KHz
METER MEANING	0	Forward Power
	1	Reflected Power
	2	Signal Strength
	3	Audio Level

P.O. Box 58649
Raleigh, North Carolina 2[illegible]358
(919) 850-3000 TELEX: 4[illegible]8
FAX: (919) 850-3022