MICRO-TEL

MICROWAVE MEASUREMENT
& SURVEILLANCE EQUIPMENT

Micro-Tel Corporation
an Adams-Russell Company
10713 Gilroy Road
Hunt Valley, MD 21230

OPERATING & MAINTENANCE

MANUAL FOR

PR-700B

RECEIVERS

March 1982

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A1	* 81B10-005		Simplified Block Diagram Bands 1 and 2
A1	* 81B10-006		Simplified Block Diagram Bands 3-7
A1	81R10-1002		System Wiring Diagram
A1B1A1	* 81D111-011	* 81A111-364	DVM/Meter Amplifier
A1B1A2		* 81A112-382	Tuning Logic
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* SCHEMATIC'S ALREADY IN MASTER MANUAL

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A8B1A2		* 81B81-317	Band H-L
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A8B2	* 81D82-016	* 81B82-313(2)	Preselector High Frequency
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A9B2		* 81A92-159	10.7 MHz
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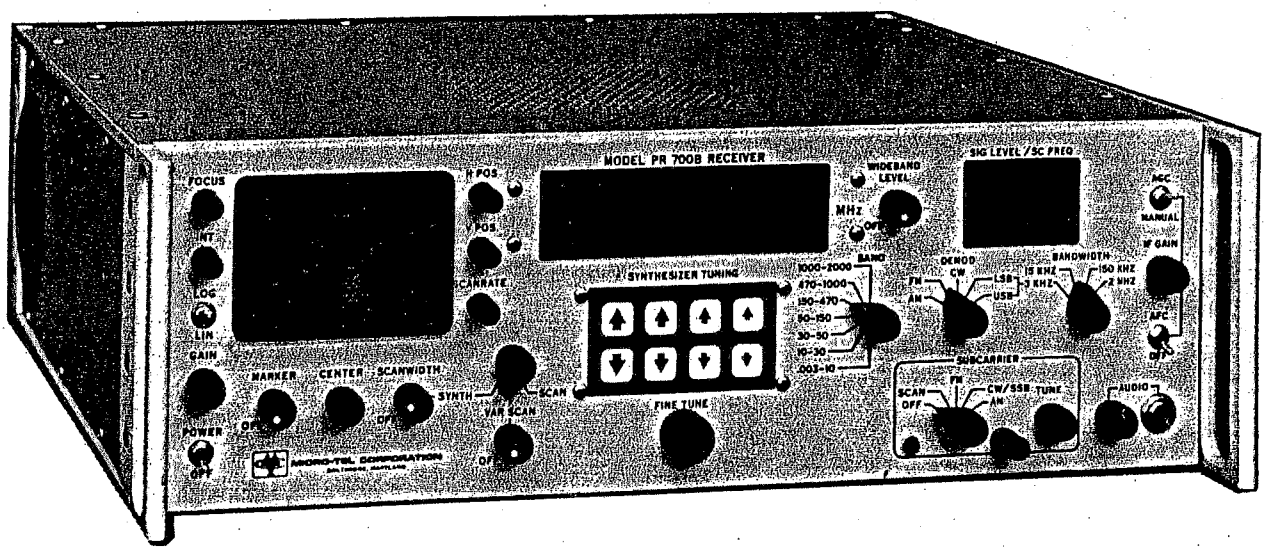
A14	* 81C140-049	* 81B140-326	+24V Battery Charger



PR-700B RECEIVER

FRONT VIEW

1.0 GENERAL DESCRIPTION

This section provides an introductory description of the Micro-Tel PR-700 Series Surveillance Receivers.

1.1 INTRODUCTION

The Micro-Tel Model PR-700 Surveillance Receiver covers the entire frequency range from 3 kHz to 2000 MHz. It is designed for both surveillance and monitoring applications. Its most significant features are:

* Multi-Mode Tuner. Fast Scan and Incremental Scan for rapid, wideband sweeps.

* Digital Frequency Control and Readout with resolutions and accuracies down to 10 Hz and 100 Hz respectively.

* Panoramic Display, with Simultaneous Sweep and Demodulation in the Synthesized Tuning Mode.

* Bandwidths of 3 kHz, 15 kHz, 150 kHz, 2 MHz and 20 MHz.

* Subcarrier Receiver tunable from 10 kHz to 200 kHz.

The PR-700 may be operated from 115/230 VAC, 50 to 60 Hz or 24 VDC power sources. This receiver complements the Micro-Tel MSR-901 and MSR-902 Attache Case Receivers covering 1-18 GHz. The panoramic frequency display in the PR-700 may serve as the display for the MSR receivers; additionally the PR-700 may be used as a second demodulator for the microwave receiver.

Three operating modes are provided: In the SCAN mode, the entire band selected is displayed on the CRT, and a movable marker allows the operator to select a particular signal for further analysis. In VAR SCAN, the CRT displays an adjustable sector up to 10% of frequency centered on the marker. In the MAN mode, the synthesizer becomes operational, the CRT display has adjustable widths up to 2.5 MHz, and simultaneous audio output is provided in the switch selected bandwidths. A 20 MHz wideband IF output plus AM and FM demodulated outputs are provided. The receiver demodulates AM, FM, CW, LSB and USB in 3 and 15 kHz bandwidths and AM, FM and CW in 150 kHz and 2 MHz bandwidths. The demodulator outputs are available along with the wideband (20 MHz) outputs.

Manual tuning is controlled by four UP/DOWN pushbuttons and a FINE TUNE optical encoder with 10 Hz resolution.

AM, CW/SSB and FM demodulation of sub-carrier signals are provided, and a sub-carrier spectrum of 200 kHz can be displayed on the CRT. The sub-carrier TUNE controls a marker in the sub-carrier mode. This marker can be set to a signal observed on the CRT; when switched out of SCAN, the demodulated subcarrier can be fine tuned and heard in the audio output. A variable BFO control allows demodulation of single or double side band signals.

1.2 PRINCIPLES OF OPERATION

For a general understanding of the Model PR-700, refer to the simplified overall block diagram (Drawings Numbers 81B10-005 and 81B10-006). Individual functions are described in later sections.

The RF input covers 3 kHz to 2 GHz from 2 antenna input connectors; one covering 3 kHz to 50 MHz and the second covering 50 MHz to 2 GHz.

Refer to Figure 81B10-005.

The incoming RF is ultimately converted to 10.7 MHz for demodulation via several conversion paths. The 3 kHz to 30 MHz input after going through switched preselection filters (A8B1), up-converted in the A3B3 module to

to 45 MHz. The local oscillator is a synthesized 45 to 75 MHz source (A4B1, A4B2, A4B3, A4B4) tunable in 10 Hz increments. This 45 MHz intermediate frequency is then down converted to 10.7 MHz in the main IF module (A3B1) by a phase locked 55.7 MHz local oscillator in the A9 Module. Refer to 81B10-006. Signals from 30 MHz to 470 MHz after going through appropriate preselection filters in A8B2 are converted to a 685 MHz center frequency in 10 MHz increments in the A8B4 module via a phase locked YIG oscillator. This 10 MHz wide bandpass is then down converted to a 165 MHz center frequency in the A8B6 module by a 520 MHz phase locked local oscillator consisting of A8B16 and A8B11. This 165 MHz bandpass is then down converted again to a 15 MHz center frequency in the A8B7 module via a 180 MHz phase locked local oscillator. This 15 MHz center frequency, 10 MHz wide bandpass is then fed to the same preselection filters A8B1) and conversion processes as a 10-20 MHz signal in the low band antenna input. Signals from 470 MHz to 2000 MHz after going through a YIG preselector are first converted to 165 MHz (A8B6) via a phase locked YIG oscillator tuned in 10 MHz increments. This 10 MHz wide bandpass then follows the same signal path as the 50-470 MHz bands after conversion to 165 MHz.

1.3 SPECIFICATIONS

BAND	FREQUENCY - MHz	NOISE FIGURE
1	.003-10	* 15-30 dB
2	10-30	12-18 dB
3	30-50	10-12 dB
4	50-150	10-12 dB
5	150-470	10-12 dB
6	470-1000	12-16 dB
7	1000-2000	15-25 dB

*Increase from 30 dB at 50 kHz to 40 dB at 3 kHz

Preselection: Switched 1/2 octave filters from 2 to 470 MHz. Tracked YIG filter from 470 to 2000 MHz. Low pass filters below 2 MHz.

Tuning Modes:

SCAN: Continuous sweep of selected band. Rate variable from .1 to 30 Hz.

VAR SCAN: Sweeps 0 to 10% of band about selected frequency.

SYNTHESIZE: Tunes selected band with 4 UP/DOWN push-buttons plus FINE TUNE optical encoder.

Remote: Provides a parallel input for external control of frequency, mode, bandwidth and demodulation. Band information is generated automatically in this mode from the frequency input.

Pushbutton Tuning Rates: .003-50 MHz: 2500, 400, 30, 3 kHz/sec.
50-150 MHz: 25, 4, .300, .030 MHz/sec.
150-2000 MHz: 250, 40, 3, .300 MHz/sec.

Encoder: 250 increments per revolution, 10 Hz per increment.

Frequency Display: Eight digit LED.

Resolution: 100 Hz

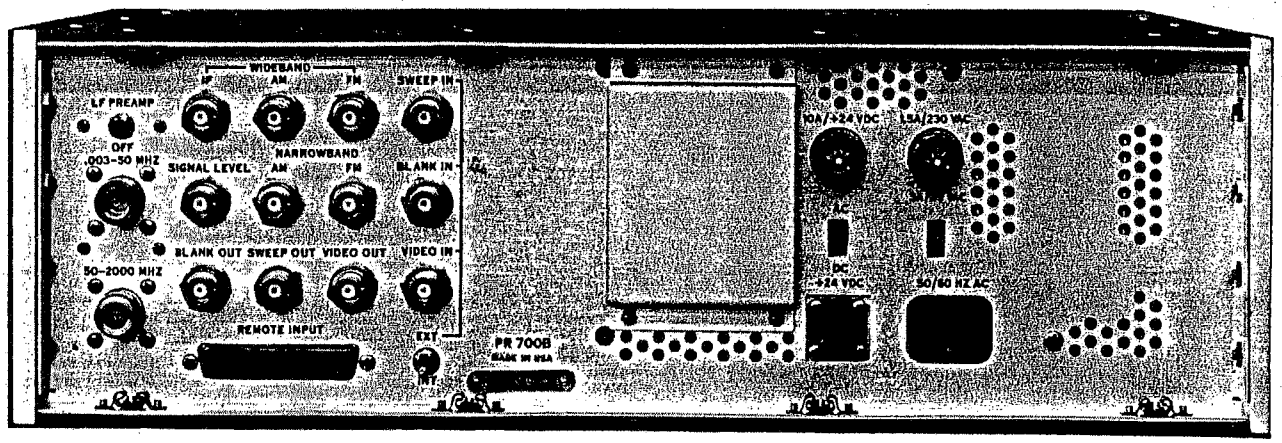
Accuracy: .001%

Stability: .001%, 0 to 50°C

Audio Demodulators: AM, FM, CW, LSB, USB

Audio Bandwidths:	3, 15, 150 kHz, 2 MHz
Demodulator Outputs: (DC coupled)	Wideband (20 MHz) AM and FM, Narrow Band 3, 15, 150 kHz, 2 MHz AM and FM.
IF Outputs:	160 MHz (20 MHz BW).
Panoramic Display:	
Full Band:	100% of selected band.
VAR SCAN:	0 to 10% of band.
MAN:	0 to 2.5 MHz.
SUBCARRIER:	0 to 200 kHz.
Sweep Rate:	.1 to 30 Hz.
Display:	LOG or LIN.
LOG Range:	40 dB
Outputs:	Sweep, $\pm$1.5V Blank, +5V
Inputs:	Switch selects internal or external. External requires $\pm$1.5V Sweep, +5V Blanking, 0 to +10V Video.
Markers:	
SCAN Mode:	CRT blanking pulse, positioned by Synthesizer tuning. Frequency display reads marker frequency.
SYNTHESIZE Mode:	IF marker with center adjustment aligns audio and video channels.
IF Gain Control:	Manual and AGC.
AFC:	Digitally increments or decrements synthesizer tuning to track signal.
Audio:	600 ohm, headset level.
SIG Level/SC Frequency Display:	3 digit LED - displays relative signal strength in normal demod modes. Displays subcarrier frequency in double-demod mode.
Subcarrier Demodulator:	Demodulates FM, CW/SSB, AM. Tuning range 0 to 200 kHz. Bandwidth 10 kHz.

IF Rejection:	80 dB below 30 MHz 60 dB 30 MHz to 1 GHz 50 dB 1 GHz to 2 Ghz
Image Rejection:	70 dB below 30 MHz 50 dB above 30 MHz
LO Radiation:	-70 dBm, maximum
Power Required:	115/230 volts, 47 to 62 Hz or +24 VDC
Physical Description:	
Receiver:	5 1/4 x 16 2/4 x 17 1/4 inches. 41 pounds
Battery Charger:	115/230 volts, 50-60 Hz. 2 5/8 x 1 3/4 x 9 inches. 2 pounds.
Battery:	24V NiCad 1 1/4 hour operation. 16 hour charge.



PR-700B RECEIVER

REAR PANEL

2.0 INSTALLATION

The PR-700 Receiver as received is ready to operate. The following accessories may be included with the receiver.

Headphones (1000 ohms)
24V Battery
Battery Charger

Plug the headphones into the front panel AUDIO jack. Set the input power selector switch to the correct voltage (115/230V) before connecting the power cord to the source. THE RECEIVER WILL BE DAMAGED IF IT IS CONNECTED TO A 230 VOLT SOURCE WITH THE SWITCH IN ITS 115 VOLT POSITION.

The PR-700 has two type N antenna inputs, one for the frequency range of .003 to 50 MHz and one for 50 to 2000 MHz. Appropriate antennas must be connected to these inputs. A preamplifier is included in the low frequency input, and may be switched out if the receiver is placed in a noisy environment or if a large antenna is used below 50 MHz.

External signal processors may be connected to the appropriate WIDEBAND or NARROWBAND outputs. Connection to these will not affect the audio output or panoramic display. An external oscilloscope may be connected to the BLANK and SWEEP outputs.

The PR-700 oscilloscope display circuits can be used with other receivers such as the Micro-Tel Models MSR-901 and MSR-902 Receivers by connecting their display outputs to the corresponding display input connectors, and switching the adjacent toggle switch to EXT.

3.0 OPERATION

This section contains operating instructions for the PR-700A Receiver. It is very important to read these instructions carefully, and to refer to them if questions of operation or performance arise. The PR-700A covers a wide range of frequencies and performance parameters. Its full potential can be realized only by a through understanding of its operating priciples.

3.1 TUNING

Most important to proper operation of the PR-700A is the full understanding of the tuning modes and the correct functions of the associated controls which include the following:

SYNTHESIZER TUNING Pushbuttons and FINE TUNE Knob
BAND Switch
MODE Switch
SCANWIDTH Control
CENTER Control
SCAN RATE
MARKER

First set the BAND switch to the frequency range of interest. Next set the MODE switch to the desired position. Operation in all three modes is described in the following paragraphs. The Subcarrier Receiver Must Be Turned OFF Until The Main Carrier Is Receiver. See section 3.5 of this manual.

The SYNTHesize mode provides the greatest operating utility, along with the best frequency accuracy and stability. The SCAN and VAR SCAN modes may often be used to search a given spectrum for coarse signal location and may be more convenient than the SYNTHesize mode because the panoramic display covers a wider range, 2.5 MHz maximum in the SYNTHesize mode. Once a signal is located in the SCAN or VAR SCAN mode and centered on the scope display, it may shift as much as one percent in frequency when the receiver is switched to the MANual mode. Frequency accuracy in the SYNTHesized mode is typically .001% compared to about 1% in SCAN and VAR SCAN.

3.1.1 SYNTHESIZE

When the MODE switch is in its SYNTHesize mode, the receiver frequency control is fully synthesized with accuracy and stability crystal controlled at all frequencies. The receiver is tuned continuously by the FINE tuning knob or the pushbuttons. All demodulators except the wideband (20 MHz) ones operate simultaneously with the panormaic display, but the maximum dispersion of this display is 2.5 MHz. The SCAN RATE control varies the number of scans per second from 0.1 to 30 per second. The scan dispersion may be varied from zero to 2.5 MHz by the SCANWIDTH control, and when this control is fully counterclockwise in its OFF position, signal amplitude vs. time is displayed. The MARKER control turns on and varies the amplitude of an IF marker which will be seen on the display above the baseline and will also appear in the demodulator outputs. The CENTER control varies the center frequency of the independent video channel and is used to center the marker on the display to assure that the demodulated output is the signal at the center of the display.

3.1.2 VAR SCAN

When the MODE switch is in its VAR SCAN position, the receiver is continually scanning over a small portion of the selected frequency BAND, and the spectrum of this portion of the band is displayed on the front panel CRT. The number of scans per second can be varied from 0.1 to 30 by the SCAN RATE control. The center frequency of the scan is

tuneable over the full band using the tuning knob or the pushbutttons, and is displayed on the digital frequency readout with a typical accuracy of one percent. The frequency dispersion of the scan may be varied from zero to ten percent of the center frequency by the VAR SCAN control. The CENTER, MARKER and SCANWIDTH controls are inoperative in this mode. When the VAR SCAN control is rotated fully counterclockwise into its OFF position, the sweep is disabled and the receiver may be tuned to any frequency within the selected band with no sweep interference in the demodulator and audio outputs; the CRT displays signal amplitude vs. time. There is no MARKER.

Operation in the VAR SCAN mode with the SCANWIDTH set to OFF is identical to operation in the SYNTHesize mode with the following exceptions.

1. In the SYNTHesize mode, the internal synthesizer operates so the frequency accuracy is .001 percent, compared to typically one percent in the VAR SCAN mode.

2. The wideband (20 MHz) outputs are useable only in the VAR SCAN mode. In the SYNTHesize mode, the tuning before these wideband outputs is not continuous and steps in 10 MHz increments. The wideband channel should be turned off when not in use to prevent radiation from the unterminated outputs.

3.1.3 SCAN

When the MODE switch is in its SCAN position, the receiver is continually scanning over the entire range of the selected frequency BAND, and the specturm is displayed on the front panel CRT. The number of scans per second can be varied from 0.1 to 30 by the SCAN RATE control. A CRT blanking marker is tuned by the pushbuttons or the FINE TUNE knob and the marker frequency is displayed on the digital frequency readout with a typical accuracy of one percent. The MARKER, CENTER and SCANWIDTH controls are inoperative in this mode. The demodulator outputs and audio outputs will be modulated by the sweep.

3.1.4 AFC

The automatic frequency control circuits operate in the SYNTHesize mode only, and are activated by the AFC toggle switch. With this switch in its on (up) position, the receiver will track a slowly drifting signal. The receiver will track a signal over the entire band if there are no stonger signals encountered in the process. Tracking is done in the synthesizer circuits so the accuracy and the stability of the synthesizer are maintained with the AFC on. The accuracy and resolution of the digital frequency display are also unchanged.

The AFC must be turned OFF when tuning the receiver, and turned ON only when the signal is centered in the selected bandwidth.

3.2 DEMODULATORS/BANDWIDTH

3.2.1 WIDEBAND (20 MHz)

Three wideband outputs are available: IF, AM and FM. These outputs operate only above 30 MHz, and as noted in 3.1.2, these wideband outputs are normally useable only in the SCAN and VAR SCAN tuning modes. In the SYNTHesize tuning mode, the first local oscillator is not continuously tuned, but stepped in 10 MHz increments, so the incoming signal may not be centered in the wideband channel. It may be as much as 5 MHz off center. All three wideband outputs are simultaneously available. However, the wideband AM and FM are not available at the front panel AUDIO jack. The wideband

AM output is displayed on the CRT when turned on. No audio is present in this mode, and the IF gain is controlled by the wideband IF GAIN control.

3.2.2 NARROWBAND

The narrowband AM and FM detector outputs are simultaneously available at the NBAM and NBFM connectores respectively. The predetection bandwidth of these outputs is selected by the front panel BANDWIDTH switch. The adjacent DEMODulator switch does not affect these outputs except when it is in its USB or LSB position. When the DEMOD switch is in its USB position, the IF passband is shifted 1.8 kHz above its normal center frequency. When the DEMOD switch is in its LSB position, the IF passband is shifted 1.8 kHz below its normal center frequency. The post-detection AM and FM outputs are about one-half the IF bandwidths.

3.2.3 AUDIO

The DEMODulator switch connects the audio amplifier to the designated demodulator. The audio output is available at the front panel phone jack, and its level is adjustable by the adjacent AUDIO control. Bandwidth selection is independent of the demodulator selected, but as the front panel markings indicate, the 3 kHz bandwidth is normally used for LSB and USB. As noted in 3.2.2, the final If passband is shifted by plus or minus 1.8 kHz when the DEMOD switch is in its USB position or its LSB position respectively. The audio passband is approximately 300 to 6000 Hz.

3.3 PANORAMIC DISPLAY

The operation of the cathode ray tube (CRT) display depends upon the selected tuning mode: i.e. SCAN, VAR SCAN or SYNTHesize. It displays frequency along the horizontal axis and signal amplitude along the vertical axis except when the SCAN WIDTH control is fully counterclockwise in its OFF position; then the horizontal axis is a time base.

The FOCUS, INTensity, Horizonal POSition, and Vertical POSition controls affect the CRT display only and may be adjusted to the operator's preference in any operating mode.

3.3.1 HORIZONTAL

The horizontal CRT sweep is driven by the same sawtooth signal that sweeps the internal tuning ossillqtors, and the sweep speed for both the display and the oscillators are adjustable from 0.1 to 30 sweeps per second by the SCAN RATE control.

The SCANWIDTH control varies the frequency dispersion of the panoramic display. In the SCAN tuning mode, this control is inoperative because the receiver scans the entire band selected. In the VAR SCAN tuning mode, the VAR SCAN control varies the frequency dispersion from zero (OFF position) to a value of at least ten percent of the receiver center frequency. With the VAR SCAN in its OFF position, the frequency dispersion is zero, so the CRT displays amplitude versus time, with the horizontal sweep time adjustable by the SCAN RATE control. This time base display has limited use because of the restricted sweep rate range and lack of synchronization, but it permits operation of the demodulators in the VAR SCAN mode without interference from the sweeping oscillators. Often the time base display aids in signal identification. In the SYNTHesize tuning mode, the SCANWIDTH control varies the frequency dispersion from zero (OFF position) to 2.5 MHz. With the SCANWIDTH control in its OFF position the CRT displays amplitude versus time with the sweep time adjustable by the SCAN RATE

control. In the SYNTHesize tuning mode, the demodulators operate independently of the panoramic display. Therefore the time base display in the SYNTHesize mode is useful only as an aid to identifying signals.

3.3.2 VERTICAL

The vertical deflection of the CRT display is always proportional to signal amplitude. The LOG/LIN switch changes the vertical scale from a logarithmic one to a linear one. The logarithmic presentation is normally used for wide scans of signals having great differences in signal level. The linear presentation is normally used for detection of weak signals. The GAIN control varies the gain of both the panoramic and demodulator channels. It has no effect when the SCOPE INPUT is external.

3.3.3 MARKER

The MARKER control operates only in the SYNTHESIZE tuning mode.

The marker is a signal at the IF center frequency and injected in the IF amplifier along with any incoming signals. It appears on the CRT display and in the demodulators as a signal at the receiver center frequency. The CENTER control aligns the panoramic display channel within the receiver to center the marker signal on the display, and therefore assures the operator that the signal in the center of the display is the one in the demodulator channel. The marker should be centered at the minimum scanwidth used, and then turned OFF.

3.4 AGC/IF GAIN

The automatic gain control (AGC) circuits and the IF GAIN control adjusts the gain of the audio demodulator channels. With the AGC activated (up position), the IF GAIN control is inoperative, and the receiver gain is automatically held to a level compatible with the selected demodulator. The AGC time constant is selected by the DEMODulator switch. In the AGC OFF position, receiver gain is adjusted only by the adjacent IF GAIN control.

3.5 SUBCARRIER RECEIVER

The subcarrier receiver switch must be kept in its OFF position until the main receiver is tuned to the carrier of the received signal. Otherwise the AUDIO output will be connected to the subcarrier receiver, and the main receiver will appear to be inoperative. When the subcarrier switch is in its SCAN position, the CRT display is disconnected from the main receiver and connected to the subcarrier receiver output.

The DEMODulator switch of the main receiver must be set to AM or FM, depending on the type of complex modulation expected. This connects the input of the subcarrier receiver to the corresponding narrowband demodulator.

When the subcarrier mode switch is in its AM, CW/SSB or FM position, the corresponding subcarrier receiver demodulator is connected to the AUDIO output, and the adjacent TUNE control varies the subcarrier center frequency from 10 to 200 kHz. In its SCAN position, the CRT display is connected to the subcarrier receiver to scan its entire range of 10 to 200 kHz. In the SCAN position, there is no audio output, and the TUNE control varies a video marker below the baseline of the display. Once the marker is placed under a subcarrier signal, this subcarrier can be demodulated by switching to the correct demodulation mode.

A lamp indicates that the subcarrier receiver is turned on.

3.6 EXTERNAL CONTROL

In addition to all the features previously described, the PR-700B has provisions for remote control of the following functions via a TTL level parallel input connector on the rear panel.

3.6.1 EXTERNAL FREQUENCY INPUT

Pins 1 through 35 of the 50 pin rear panel connector provides for external input of frequency. These inputs are BCD positive true logic. The frequency of the receiver is controlled by these inputs when pin 35 (External Frequency Enable) is in a low TTL level. Band selection is automatic when the External Frequency input is enabled. When pin 35 is in a high TTL state, frequency control is via the front panel controls.

Pin assignments for these inputs are shown in Figure 3.1.

3.6.2 EXTERNAL MODE CONTROL

Pins 36 through 38 provide for external mode control. These inputs are also TTL level positive true. The BCD number required for various modes is shown in Table I.

3.6.3 EXTERNAL BANDWIDTH CONTROL

Pins 39 through 42 provide for EXTERNAL bandwidth control. Input requirements for various bandwidths are shown in Table II.

3.6.4 EXTERNAL DE-MOD CONTROL

Pins 43 through 46 provide for External De-Mod control. Input logic for these inputs are shown in Table III.

3.6.5 EXTERNAL ATTENUATION INPUT

Pin 47 provides for external input of approximately 10 dB of attenuation of the input signal. This input is useful for determining if a received signal is due to an intermodulation product in the PR-700B receiver. Input levels for this function is shown in Table IV.

3.6.6. EXTERNAL SUBCARRIER RECEIVER CONTROL

The 25 pin connector on the rear panel labeled "REMOTE B" provides for external control of the subcarrier receiver per Table V. In addition to pins in Table V, when the Remote S.C. MODE is enabled <u>all</u> S.C. tuning is done by inserting -5V to +5V corresponding to 0-200 kHz into pin 5. Also the S.C. Video Level from the S.C. is available at pin 7.

FIGURE 3.1

PIN No.	BCD No.	
1	1	BCD Input 10 Hz Digit
2	2	
3	4	
4	8	
5	1	BCD Input 100 Hz Digit
6	2	
7	4	
8	8	
9	1	BCD Input 1 kHz Digit
10	2	
11	4	
12	8	
13	1	BCD Input 10 kHz Digit
14	2	
15	4	
16	8	
17	1	BCD Input 100 kHz Digit
18	2	
19	4	
20	8	

PIN No.	BCD No.	
21	1	BCD Input 1 MHz Digit
22	2	
23	4	
24	8	
25	1	BCD Input 10 MHz Digit
26	2	
27	4	
28	8	
29	1	BCD Input 100 MHz Digit
30	2	
31	4	
32	8	
33	1	1 GHz Digit
34	2	
35		External Frequency Enable (Low = Enable)

50 pin connector Rear Panel

TABLE I

REMOTE INPUTS	Pin 38	Pin 37	Pin 36
Front Panel Control	High	X	X
SYNTHesize	Low	Low	High
VARI SCAN	Low	High	Low
SCAN	Low	High	High

TABLE II

REMOTE INPUTS	Pin 42	Pin 41	Pin 40	Pin 39
Front Panel Control	High	X	X	X
3 kHz	Low	Low	Low	High
15 kHz	Low	Low	High	Low
150 kHz	Low	High	High	High
2 MHz	Low	High	Low	Low

TABLE III

REMOTE INPUTS	Pin 46	Pin 45	Pin 44	Pin 43
Front Panel Control	High	X	X	X
AM	Low	Low	Low	High
FM	Low	Low	High	Low
CW	Low	Low	High	High
LSB	Low	High	Low	Low
USB	Low	High	Low	High

4.0 THEORY OF OPERATION

This section explains in detail the operation of circuits and components of the PR-700 receiver. Reference should be made to the corresponding schematics in section 7.0 when reading the following paragraphs. It is recommended that the general description and principles of operation contained in section 1.0 be read beforehand. Signal paths through the PR-700 RF section have been described previously in section 1.2 and are shown in schematic drawings 81B10-005 and 81B10-006. The wiring diagram, 81R10-1002, shows interconnections between the functional modules, boards and sub-assemblies which are described herein. Front, Top and Rear panel controls, indicators and connectors are included in this drawing.

4.1 ANTENNA PREAMP (A8B14)

Refer to schematics drawings 81B814-024 and 81A814-353. Input signals in the range of 3 kHz to 50 MHz enter the receiver through antenna input connector J1 of antenna preamp assembly A8B14. With the antenna preamp switch in the off position the signal path is routed directly out of (A8B14) via connector J2. If the antenna preamp switch is in the "on" position the signal is routed to the gate of Q1. The output of Q1 is then connected to output connector J2 via switch (S1). The antenna preamp module (A8B14) is a low noise amplifier with approximately 13 dB of gain. (Note: the preamp is designed for the whip antenna, or a high impedance input, therefore if the preamp is turned on with a 50 ohm input such as a signal generator connected to the antenna input the preamp will appear inoperative). The signal then proceeds to the low frequency preselector module (A8B1 J1).

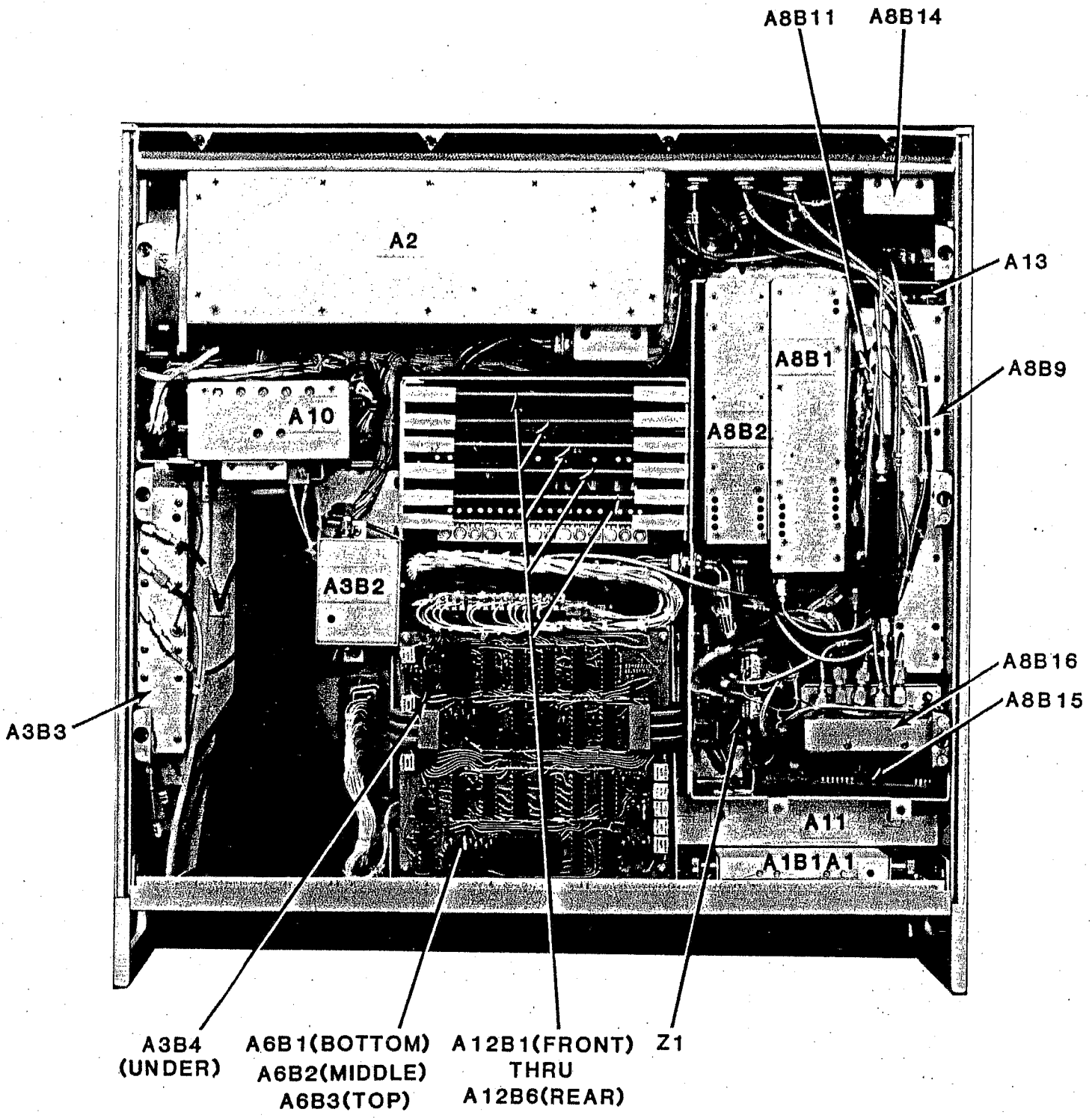
4.2 LOW FREQUENCY PRESELECTOR (A8B1)

Refer to schematic diagram 81R81-048. This module contains 11 switched low pass or bandpass filters which cover the range of 3 kHz to 50 MHz in approximately 1/2 octave ranges. The output for frequencies below 30 MHz is J4. For frequencies above 30 MHz the output is J3.

The filters are selected by relays K1-K3, pin diodes switches D1 thru D35 and transistor switches Q1 and Q2. All the switching logic necessary to select the proper filter is generated on the preselector-filter switch PC board (A12B1) whose operation will be discussed later. (See section 4.4). The 3 kHz to 30 MHz output from J4 is fed to the 45 MHz mixer amplifier module.

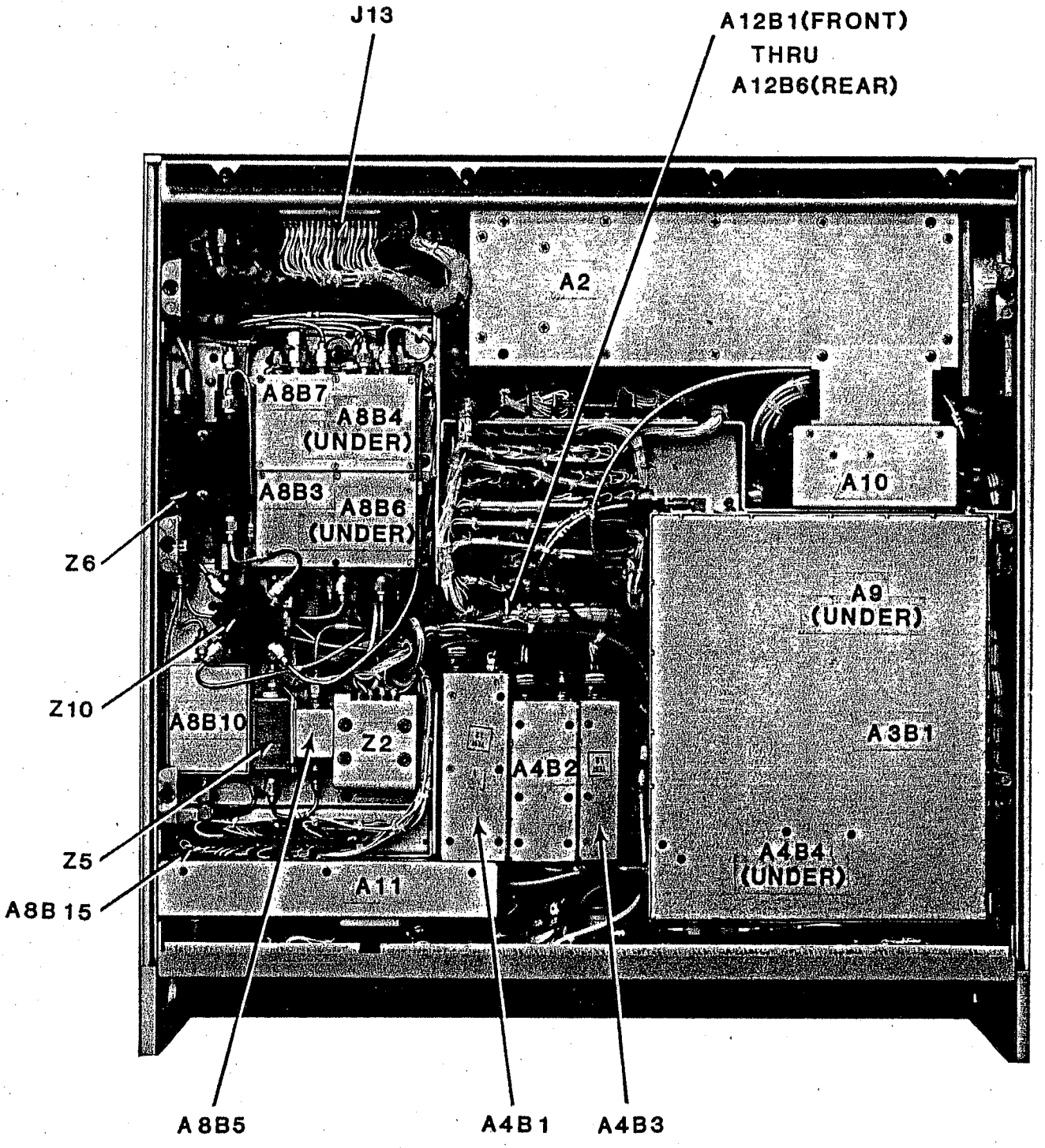
4.3 45 MHz MIXER AMPLIFIER (A3B3)

Refer to schematic diagram 81R33-043. The signal enters the A3B3 module via J1 where it first passes through a 45 MHz low pass filter (A3B3A2) and into Q1 which is an RF amplifier with approximately 10 dB of gain. After an impedance conversion in T2, it is fed to U1 which is a QUAD FET integrated circuit used as an active mixer stage. The Local Oscillator for the mixer enters J2 in the frequency range of 45 MHz to 75 MHz, 45 MHz above the desired signal frequency. The output of this mixer at 45 MHz is passed on to a bandpass filter and then split into 2 separate identical channels. Q2 and Q4 are FET RF amplifiers with approximately 10 dB of gain. The outputs of these two amplifiers are fed to A3B3A6 and A7 which are 45 MHz bandpass filters with a 2 MHz 3 dB bandwidth. A 45 MHz marker signal can be inserted into both the audio and video channels via J5 and R41.



PR-700B RECEIVER, TOP VIEW

MODULE LOCATIONS



PR-700B RECEIVER, BOTTOM VIEW

MODULE LOCATIONS

4.4 PRESELECTOR FILTER SWITCH (A12B1)

Refer to schematic diagram 81R121-039. The preselector filter switch PC board is the first board (from the front of the unit) in the card bucket. Its purpose is to provide all of the control logic necessary to switch the preselection filters located in the A8B1 and A8B2 modules. The band 1 filters (filters A thru F) are enabled in the following manner: A 0 to 10 VDC per band voltage enters on pin U and is buffered by operational amplifier U5. This output then drives one input of voltage comparators U6A, U6B, U6C, U6D, U7-A. The other input to the voltage comparators is an adjustable DC reference voltage centered at approximately the proper voltage for each filter switch point. As the tuning voltage increases from 0 VDC the outputs of each of the comparators switches to a "high" level as its reference voltage is exceeded. The outputs of each of these comparators then go to the inputs of exclusive OR gates which provide for a single output of only the highest voltage comparator output. These exclusive OR outputs are then fed to one input of a NAND gate. The other inputs of the NAND gates are connected to a 1 of 7 decoder output which decodes the BCD band information into a single line output for each band. The output line for band 1, for instance, connects to U15A,U15B,U15C,U15D,U14A, and U14B. These NAND gates then provide an enable function which allows their outputs to switch only in band 1.

The band 2 filters function in approximately the same manner with the following differences: The 0-10V tuning voltage from Pin U is converted to .48V to 3.48V by R90,R91 and R92. In band 2 FET switch (U4) is connected to pin 1, this output (U4 pin3) then is buffered by U5 and then goes to voltage comparators U7B,U7C, and U7D. These outputs then go to the excluive OR gates and the NAND gates as in band 1. The "Enable" line for band 2 comes from U1 Pin 2. The output from the RF unit (A8) is fed back into the low frequency receiver in the range of 10 to 20 MHz and filters H, J and K are used to provide additional preselection. When in bands 3 thru 7 the tuning voltage fed to the "Band " voltage comparators come from Pin T which is a .48 to 3.48 voltage that repeats every 10 MHz in tuning.

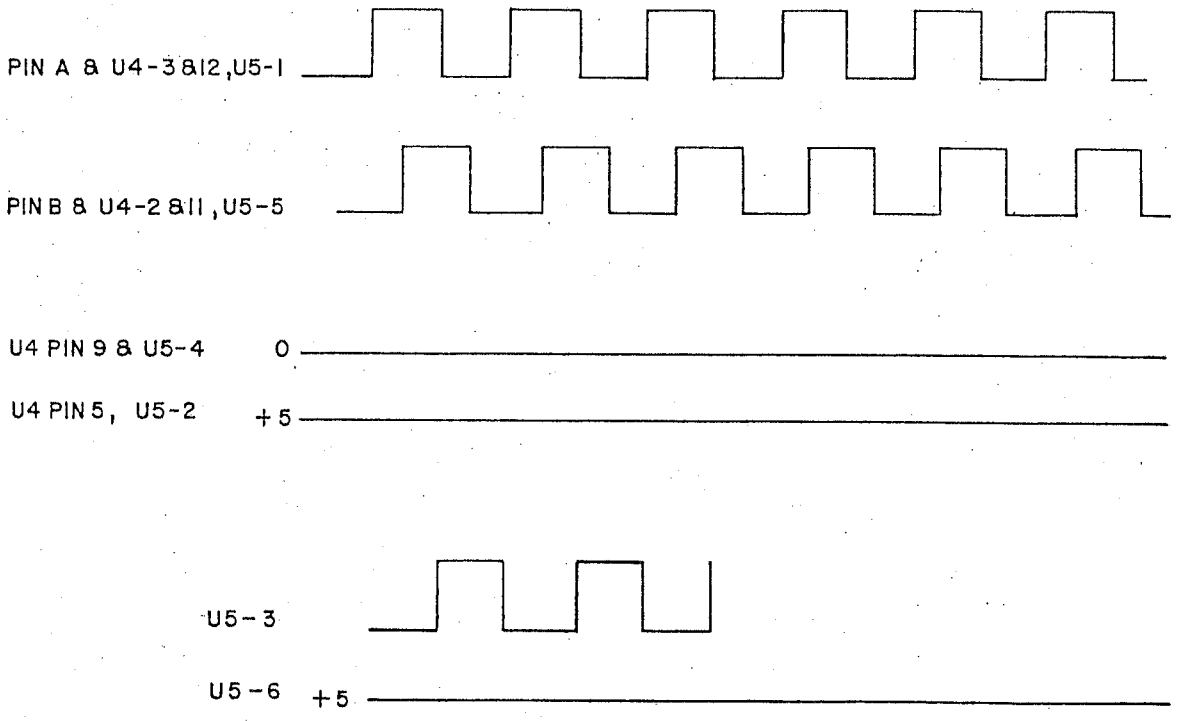
Band 3 uses a single 28-52 MHz filter (filter M) which is enabled directly by the band decoder U1 pin 4 thru buffer/inverters U2C, U2E and output on pin 14. Bands 4 (filters N,P,R,S) and Band 5 (filters T,U,V,W) are switched in the same manner as band 1 filters.

4.5 TUNING LOGIC (A1B1A2)

Refer to schematic diagram 81D112-027 and Figure A on page 4-5. The tuning logic assembly provides the decoding logic necessary for the front panel tuning buttons and the front panel optical encoder "FINE TUNE". It also provides the digital AFC Logic and tuning output.

4.5.1 TUNING (A1B1A2A2)

The pushbutton tuning works in the following manner: The front panel pushbutton switch logic enters on points E12 thru E19, with E12 being the fastest tuning rate up and E15 being the slowest tuning rate up. E16 is the fastest rate down and E19 the slowest rate down. The clock pulses to be output by A1B1A2 are generated by an LM566 (U3) VCO. When the AFC switch is in its off position a constant voltage is applied to U3 Pin 5, therefore the clock rate is determined by resistor R15 and capacitors C4, C5, C6 or C7. The capacitor is selected in the following manner. If no front panel pushbuttons or either of the slow buttons (E15 and E19)



AIB2A2, TUNING UP WAVEFORMS

FIGURE A

are depressed capacitor C4 is connected to ground via Q5. When any of the faster buttons are pressed C4 is removed from ground via either D4, D5 or D6 and transistor Q4. At the same time one of the other three capacitors (C5, 6 or 7) is enabled by Q6, Q7 or Q8, each step being approximately 10 times faster than the previous one. The tuning direction (up or down) is determined by quad AND gates U8A and U8B. Normally all four inputs to both quad NAND gates are high, therefore, their outputs are high. These connect to a pair of two input AND gates (U6C and U6D). With the AFC switch off the second input is always high therefore its output follows the input from U8. These outputs connect to a pair of two input OR gates. With no front panel pushbuttons depressed the output from these OR gates (U7A and U7B) is always high, therefore the VCO output which is connected or the second input of U7A and U7B never goes any futher.

When any of the front panel pushbuttons are pressed, the output of U8A (up) or U8B (down) goes low, causing the output of U6D or U6C to go low, thus allowing the oscillator output on U7A or U7B to pass on to U5C and U5D. U5C and U5D are two input NAND gates. The other input to U5C and U5D provides for the optical encoder (FINE TUNE control) tuning; however, if the fine tune control is not being tuned these inputs are always high. Therefore the oututs from U5C and U5D are the tuning pulses coming from U7A and U7B, but inverted. These go into one input of a pair of two input OR gates, U7C and U7D. The second input of these OR gates are the Hi (stop up, pin D) or Hi (stop down pin E) and go to a Hi state to prevent any pulses from going to their outputs when the top or bottom of a band is reached. Refer to Figure A for a description of the "FINE TUNE" optical encoder operation. Pin A is one input from the optical encoder on the front panel and pin B is the second input from the encoder. The input at pin A leads the input at pin B by 90° when tuning in the down direction. (see Figure A) These inputs go to the clock and D inputs of a dual D type positive edge triggered flip-flop. When the clock input of U4 sees a positive going edge of an input pulse it transfers the information on its D input to the "Q" output. The output of U4 associated with input pins 3 and 12 is U4 pin 9. The output associated with input pins 2 and 11 is U4 pin 5. Thus, when tuning in the up direction, a low level is always transferred to U4-9 and a high level is always transferred to U9-9. These outputs are NAND with the pulses coming out of the optical encoder in U5A and U5B which provide output pulses on the correct side for up or down tuning to transistors Q9 and Q10. The emitters of Q9 and Q10 are low if no front panel pushbuttons are pressed. Therefore, the outputs (collectors of Q9 and Q10) are the inverted inputs on the base. These outputs then become 1 input to U6A and U6B AND gates with the other input being always high as long as no front panel pushbutton is pressed and then continue out to pins C (up) or 2 (down) in the same manner as did the pulses from the pushbutton logic.

4.5.2 AFC (A1B1A2A1)

The AFC voltage from the main IF module (A3B1) enters on Pin 4 and goes to AFC inverting amplifier U1A whose output is fed to another inverting amplifier U1B. When the incoming AFC voltage is approximately 0 VDC (center frequency) the outputs of U1A and U1B are also at 0 VDC. Therefore, no AFC action takes place. As the AFC voltage changes (negative for example) the output of U1A goes to a positive voltage which has two

paths. One is through diode D1 to amplifier U2A which is an inverting amplifier that has a fixed positive DC offset that generates a voltage to feed the voltage controlled oscillator tuning input. The greater the AFC voltage is from 0 VDC the higher the output frequency becomes in U3. If the AFC voltage goes positive instead of negative the output from inverting amplifier U1B is then connected to U2A via diode D2. As the output of U1A or U1B goes positive, it provides a gating voltage to transistor Q1 or Q2, turning one or the other "on". This causes one input of either U6C or U6D to go low and its output to go low. With one input to OR gates U7A or U7B in its low state, the output from U7A or U7B will follow the VCO output on U7A pin 2 or U7B pin 5 and then provide an output on pin C (up) or pin 2 (down) in the same manner as the front panel pushbuttons.

4.6 45 MHz MARKER GENERATOR (A3B2)

Refer to schematic diagram 81B32-014. The first part of A3B2 consists of the following major parts: Q1, Y1, L1 is a simple crystal oscillator circuit with L1, C2 and C3 resonant at 45 MHz and feedback provided by C2. The output is very lightly coupled via capacitor C4 and 270K resistor R5. This output is coupled into a Pi network pin diode attenuator consisting of diodes D2, D3 and D4. The variable bias for the attenuator enters via FL2 through R12, is offset by resistor R7 and proceeds thru R8 and L2 to diode D3. Resistors R4, R6 and zener diode D1 bias the anode of D2 at approximately 5.1 VDC. When the marker is turned on and set for maximum amplitude, +15V is applied at FL2. After passing through resistor network R12, R9, R7 and R8 it provides forward bias to PIN diode D3 and applies reverse bias to diodes D4 and D2. This allows the signal to pass through to capacitor C9 and resistor R14 to the output of J1. As the marker amplitude control is decreased on the front panel (voltage at FL2 decreases from +15V to +4VDC) the forward bias on diode D3 is decreased and a forward bias begins on diodes D2 and D4 thus shunting a portion of the RF signal to ground and decreasing the output amplitude at J1. The output varies from a maximum of approximately -40 dBm to a minimum of approximately -60 dBm and is connected to the 45 MHz amplifier module A3B3 by input jack J5.

4.7 DISPLAY BOARD (A6B1)

Refer to schematic diagram 81R61-1008. The A6B1 PC board is the board which contains the LED frequency display and the up/down counters for tuning. The up/down counters function in the following manner: The pulses from the tuning logic board enter on pin F (up) or pin L (down) and are fed directly to the up and down clock inputs of U1 which is the counter for the least significant (10 Hz) digit. The borrow and carry outputs connect to U2 which is an FET switch used to route the signal to more significant digits during the faster tuning rates. For the slower rates those signals go straight thru U2 to the 100 Hz counter U4, thru U5 to 1 kHz counter U7 and so on up to the most significant digit (1 GHz on U19). The BCD outputs (pins 3, 2, 6, 7) of all of these (except U1) then connect to a BCD-to-seven segment decoder driver IC (U6, U8 etc.). These outputs (pins 9 thru 15) connect to the LED front panel displays via resistor arrays (RA1 thru RA8). The outputs of the 10 MHz to 1 GHz digits are connected to the decoders via the A6B2 board and will be explained later. All the BCD output

lines from the up/down counters are connected through diodes (D1 to D24) to the base of Q2, forming a large (24 input) OR gate used to detect all zero's on the 1 MHz and lower digits. This output is then connected via D34 to another diode OR gate consisting of diodes D25 thru D32. These are all connected to the base of Q1 and its output creates the Hi Stop down output on J1 pin N. The output of the counters are also connected to J1 or J2 for outputs to other logic boards.

J1 pin 10 provides for a parallel load input on pins 9, 10, 1 and 15 of the BCD counters (U1, U4, etc.). This input is only used on the PR-700B receivers which have external frequency control input capability.

4.8 CONTROL BOARD (A6B2)

Refer to schematic diagram 81R62-1009. The A6B2 module provides the frequency offset information for each band for the 10 MHz to 1 GHz digits that go to the A6B1 frequency display board. It also provides the digital output information for divide-by-N number 4 which is the frequency divide number for the phase locking circuitry of the YIG oscillator. The A6B2 board provides the frequency offset information for the 10 MHz to 1 GHz digits in the following manner: the output of the up/down counters on A6B1 enter on J2 pins 4, 3, 5, and 6 (10 MHz), J2 pins 11, 10, 9, 8 (100 MHz), and J3 Pin 7 (1 GHz). These are connected to one input of BCD adder integrated circuits U17 (10 MHz), U18 (10 MHz) and U19 (1 GHz). The other input to these adders is the outputs of a programable read only memory IC (U1). The PROM has as it address input (pins 10, 11, 12) the BCD band information, therefore the output from the PROM is dependent upon which band the receiver is in. When in band 1, for instance, the output from U1 to the second adder input of U17 is a BCD 0. To U18 and U19 it is also a 0, (band 1 starts at 0 MHz) therefore, the output of U17 is the same as its input from the up/down counters (any number + 0 = the number). The same is true for the 100 MHz and 1 GHz outputs from U18 and U19. In band 2, the output of the PROM supplies a BCD "1" to the input of U17. The inputs to the 100 MHz (U18) and U19 (1 GHz) digits are still 0. (band 2 starts at 10 MHz) Therefore, when the up/down counters which start at 0 for all bands are at 0, the frequency display reads 10 MHz. The same is true for all bands with the numbers in Table 4.8.1 being added to the up/down counter input for each band.

The "Hi - Stop Up" output command (the output which stops the tuning at the top end of each band) is also generated on the A6B2 board in the following manner: The inputs from the up/down counters go to one inputs of 4 bit magnitude comparators U3 (10 MHz), U4 (100 MHz), U5 (1 GHz). The other inputs to the 4 bit magnitude comparators comes from a second prom (U2) which also has the BCD band information as its address inputs. Its output information is shown in Table 4.8.2.

The 4 bit magnitude comparators are cascaded via pins 2, 3, and 4 and pins 5, 6, and 7 so that when the BCD information from the up/down counters is the same as the information from the proms, the output of U5 pin 6 goes high, generating the "Hi - Stop Up" command.

The divide-by-N #4 output which provides the input for the programmable divider in the YIG oscillator phase lock loop circuitry is generated by U6 thru U16 in the following manner: U6 thru U8 are BCD adder IC's which have as one input the output of the up/down counters

TABLE 4.8.1

	INPUT TO BCD ADDERS		
BAND	U17 10 MHz	U18 100 MHz	U19 1 GHz
1	0	0	0
2	2	0	0
3	3	0	0
4	5	0	0
5	5	1	0
6	7	4	0
7	0	0	1

TABLE 4.8.2

	INPUT TO 4 BIT MAGNITUDE		
BAND	U3 10 MHz	U4 100 MHz	U5 1 GHz
1	1	0	0
2	2	0	0
3	2	0	0
4	0	1	0
5	2	3	0
6	7	1	0
7	0	0	1

TABLE 4.8.3

BAND	U8 10 MHz	U7 100 MHz	U6 1 GHz
1	0	7	6
2	0	7	6
3	0	7	2
4	0	7	4
5	0	8	4
6	0	6	4
7	0	0	0

from the A6B1 PC board. The second input to these adders is an output from the PROM IC U1 and U2. These inputs are as shown in Table 4.8.3.

The output from these adders then goes to one input of a second set of adders, U12, U13, U14. The second input to these adders comes from a set of data selectors, U9, U10, U11. The select line for these data selectors comes from prom U1 pin 5. This output is low for all but band 7; therefore, the data selector for bands 1 to 6 puts the "A" inputs to the "Z" outputs. This puts the same data on the "B" inputs to the adders (U12, U13, U14) as is on the "A" inputs, therefore, the adder performs a "times two" multiplication of the output of the first set of adders. In band 7 the data selector selects the "B" inputs on U9, U10 and U11 which is a fixed number of 116. U15 and U16 are used as buffers on the outputs of the BCD adders. The divide-by-N #4 output is therefore a BCD number as shown in Table 4.8.4.

4.9 D/A CONVERTER REFERENCE BOARD (A6B3)

Refer to schematic diagram 81R63-038. The A6B3 board contains two D/A converters for generating the 0 to 10 volts per band tuning voltage, the .48V to 3.48V tuning voltage, and the "coarse tune out" voltage. It also contains the digital circuitry to generate two "divide-by-N" numbers for other phase locked loop circuitry.

The 0 to 10V per band output from J1 pin A is generated in the following manner: The A6B1 board up/down counter output enters on J2 pins 1 thru 16 and J3 pins 3 to 6 and 8 to 11. These inputs then connect to data selector IC's U12, 13, 14, and 15. In bands 1 through 4 the select line (pin 1 of U12, 13, 14, and 15) is high; thereby connecting the "A" inputs (pins 3, 6, 13, and 10) to the "Z" outputs (pins 4, 7, 12, and 9). This output then connects to the D/A inputs of DAC 2. (U11 and U16 are bus driver IC's whose function will be described later). With the BCD inputs to DAC 2 starting at 0 and counting up, (the maximum number is a function of which band the receiver is in) the output voltage at DAC 2 pin 14 starts at 0 and increases to a maximum value at the end of each band. Figure 4.9 lists the digital input numbers to DAC 2 and the corresponding output voltage from DAC 2 pin 14.

The analog output voltage connects to U18A pin 2 which serves as an inverter/buffer samplifier. Resistors R40 and R41 divide this voltage by two. U18B serves as an amplifier with its gain controlled by resistor feedback networks consisting of variable resistors R43 thru R47. The analog switch U19 selects a feedback network for each band to adjust the gain such that 0 to +10 volts is generated for each band.

4.10 DVM METER AMPLIFIER (A1B1A1)

Refer to schematic diagram 81D111-011. The heart of the digital signal level/SC frequency display module is a 3 digit A/D converter IC (U4) which measures a DC voltage in the range of 0 to 999 mv. The voltage to be measured is the input on U4 pin 17. The BCD output information is on pins 10 thru 13 in a multiplexed fashion Pins 7, 8 and 9 are the enable lines for each of the 3 digits. Integrated circuit U3 is a CMOS BCD to seven segment decoder which decodes the BCD information of U4 pins 10 to 13 and outputs the proper logic to the

TABLE 4.8.4

BAND	LOW END OF BAND	HIGH END OF BAND
1	152	154
2	152	154
3	144	148
4	148	168
5	168	232
6	128	234
7	116	216

TABLE 4.9

BAND	TOP OF BAND BCD NUMBER	TOP OF BAND DAC 2 OUTPUT VOLTS
1	1000	-1V
2	2000	-2V
3	2000	-2V
4	9999	-10V
5	3200	-3.2V
6	5300	-5.3V
7	9999	-10V

LED displays (DS 1 thru 3). Transistors Q1, Q2, Q3 provide for the multiplexing and decoding by turning on only when the proper information is present for each digit. The input to U4 pin 17 comes from a CD 4052 analog switch, U2. If U2 pin 10 is high (sub-carrier receiver on) the input from U2 pin 5 is connected to U4 pin 17, otherwise the input is connected to U2 pin 1. The "S" meter output from the main IF is to U1B pin 5. U1B is an operational amplifier which provides a DC offset via R8 and R9. U1A provides the same function for the sub-carrier tuning voltage entering on Pin 4.

4.11 AUDIO ASSEMBLY (A1B1A3)

Refer to schematic diagram (81A113-026-1. The audio assembly consists of one audio amplifier IC U1. The selected audio output from the main IF is input from the front panel audio level control to point E1. The amplified audio output (pin 6) is de-coupled via C3 and fed to the front panel phone jack via E4.

4.12 POWER SUPPLY (A2)

Refer to schematic diagram 81R20-042.

The power supply uses a switching regulator to maintain high efficiency over the specified range of input voltages. Series voltage regulators are used for some regulated outputs in order to improve regulation and reduce source impedance.

In the AC mode, the line voltage connects through isolation transformer T1 to rectifier DA1. The primary windings of T1 are switched in parallel for 115V operation and in series for 230V operation. The rectified output from DA1 is filtered by capacitor C1 and switched by transistors Q7 and Q9.

In the DC mode, the DC input voltage connects through diode D21 to the DC switching transistors Q11 and Q12. D21 protects the power supply against reverse polarity.

For both DC and AC operation, regulation is achieved by varying the duty cycle, i.e. on-time, of the switching transistors.

4.12.1 CONTROL CIRCUITS (A2B1)

The control circuits generate the driving waveform to the switching transistors. This waveform connects to the switching transistors through transformer T2. Separate windings drive the AC switching transistors and the DC switching transistors in assembly A2B4 In both cases the on-time of this signal varies inversely as the sample voltage applied to pin 11 of A2B1. When operating from AC, the control circuits are powered by the low voltage winding of T1, rectifier DA2 and filter capacitor C2. For DC operation the control circuits are powered directly from the input voltage, through L1 and D5.

The basic switching waveform is generated by integrated circuit U1 which is a switch-mode regulator designed specifically for this purpose. It generates two out-of-phase switching signals at pins 11 and 13. The on-time of these switching signals varies inversely as the input voltage to pin 6. The switching frequency is determined by resistor R4 and capacitor C4. The maximum on-time is set by the voltage applied to pin 7, and this voltage is adjusted to

allow sufficient off time for the ringing and switching transients to decay. U1 contains an internal voltage reference which is available at Pin 9. This voltage is the source for the dead time adjustment through trimmer R15 and also supplies the reference voltage for the comparator U2B. The output switching signals at pins 11 and 13 drive transistor switches Q2 and Q3 which switch the primary transformer T2. Integrated circuit U1 does not have the power capability to drive the transformer directly. Diodes D6 and D7 and transistor Q6 comprise an AND circuit to turn on transistors Q4 and Q5 when both Q2 and Q3 are in their off states. During this time, Q4 and Q5 short the primary winding of T2 connected to their collector and thus dampen any ringing or transient during the off-time of the switching transistors.

A sample of the power supply output voltage connects through pin 11 of A2B1 to U2B where it is compared to the reference source from U1. Comparator U2B amplifies any error voltage in the correct polarity to drive the regulator input to U1 to reduce the error signal at pin 11 of A2B1 to zero. Operational amplifier U2A adds a positive offset voltage as required by the input at Pin 6 to U1. Trimmer R22 adjusts the power supply output voltage to exactly 12 volts.

4.12.2 SWITCHING (A2B4)

In the DC mode, transistors Q11 and Q12 switch the low voltage DC input alternately to each side of the center tap primary winding of T3. Q11 and Q12 are driven directly from T2.

In the AC mode, transistors Q7 and Q9 switch the voltage rectified from the AC line alternately to each side of the center tap primary winding of T3. In order to insure minimum turn-off time for each of these high voltage switches, a turn-off circuit is included in A2B1. For example when Q7 is on, its base current is limited by R25, and the potential across R25 charges C6. Q8 does not conduct because it is biased off by the drop across D11. When the drive winding goes to zero to turn Q7 off, Q8 is forward biased by R24 and conducts to force a reverse current through the emitter-base junction of Q8.

4.12.3 RECTIFIERS/FILTERS (A2B2)

The secondaries of the power transformer T3 each connect to full wave rectifiers, DA3, D17 and D18. The outputs of these rectifiers are constant amplitude pulses with varying duty cycle. It is necessary to use inductor input filters if the filtered DC output is to be proportional to the duty cycle. Output voltages are $\pm$18V at pins 5 and 6, and +6V at pin 3.

4.12.4 REGULATORS (A2B3)

Series integrated circuit regulators provide additional filtering, as well as regulation of individual outputs and a low source impedance. Dissipation in these regulators is minimized because the input voltages to the regulators are held essentially constant by the switching regulator.

4.13 A10, OSCILLOSCOPE

Refer to schematic diagram 81R100-015. The oscilloscope consists of three PC board assemblies and contains its own power supply.

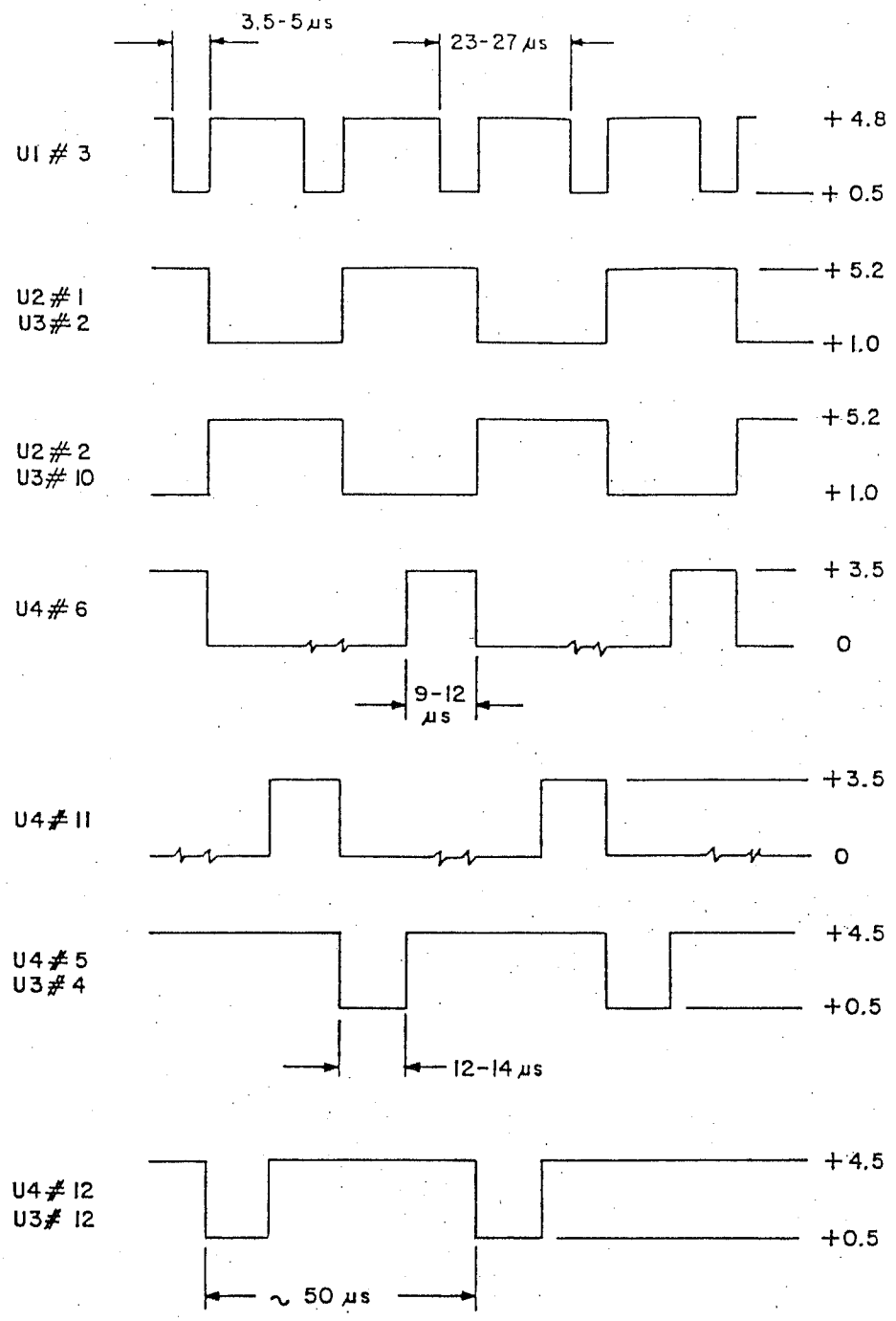


FIGURE 4.13.1

HIGH VOLTAGE POWER SUPPLY, A10B2

4.13.1 HORIZONTAL AND VERTICAL AMPLIFIERS (A10B1)

The A10B1 PC board contains horizontal and vertical differential amplifiers to drive the deflection plates of CRT V1.

Each differential amplifier consists of a differential pair (Q12, 14 for the vertical), driven by emitter followers, Q11, 15 and a current source,Q13.

Vertical and horizontal positioning are front panel controlled by means of potentiometers. These inputs enter on pins M, L, N (vert) or 8, 9, 10 (horiz).

4.13.2 A10B2, HIGH VOLTAGE POWER SUPPLY

Refer to the waveform diagram Figure 4.13.1.

Clock U1 generates negative-going pulses at a rate of approximately 40 kHz. These pulses are fed to "D" flip-flop U2 which generates two out-of-phase square waves at a rate of 20 kHz, at output pins #1 and #2.

The two outputs of U2 are fed to dual one-shot U3 which generates a negative-going pulse (output pins #4 and #12) every time the input waveform switches from low to high.

The two outputs of U3 are fed to "AND" gates U4, as well as the outputs of U2, thus generating positive going pulses, at a 20 kHz rate, out-of-phase by approximately half-period. The outputs of U4, pins #6 and #11, drive transistors Q1 through Q4, which in turn drive transformer T1.

The alternating voltage supplied to transformer T1 is rectified and filtered at two of the secondaries to provide -1000 VDC to the CRT and +100V to the collectors of the vertical and horizontal differential amplifiers in assembly A10B1.

The blanking signal generated by the receiver turns "on" phototransistor U5. 0 VDC turns U5 "on" and unblanks the CRT by applying the high votlage between cathode and grid.

Focus and intensity controls are front panel controlled. Astigmatism and trace rotation are adjusted by R16 and R48 in this PC board.

4.13.3 EXTERNAL INPUT BUFFER (A10B3)

The A10B3 chassis is a dual op-amp IC (U7) which provides for input buffering of the external blanking (input on Pin 5, outut on Pin 7) and the EXT HORIZ (input on Pin 3, output on Pin 1).

4.14 45/13.5 MHz CONVERTER (A3B4)

Refer to schematic diagram 81C34-035.

The 45/13.5 MHz converter takes the 45 MHz output from the A3B3 video channel and converts it to a 13.5 MHz swept output.

The 45 MHz signal enters transformer T1 via J1. The secondary of T1 provides 2 outputs 180° out of phase to QUAD FET mixer IC (U1). The local oscillator for the conversion is generated by integrated circuit U2. The frequency at which U2 oscillates is determined primarily by coil L2 and varactor diode CR1. A small variable DC voltage is applied to the cathode side of this varactor diode via FL-4 to provide centering control. The receiver's sweep voltage is applied to the anode side of the varactor via FL-5. The output of the oscillator is therefore a swept frequency that is centered at 58.5 MHz. This output is then connected to the active mixer IC U1 via amplifier transistor Q1 and transformer T3. The 13.5 MHz output from U1 is then connected to J2 via transformer T2.

4.15 HIGH FREQUENCY PRESELECTOR (A8B2)

Refer to schematic diagram 81D82-016.

The A8B2 module provides the preselection filtering for the receiver in the frequency range of 50 MHz to 470 MHz. The 8 filters in the A8B2 module are all switched via PIN diode switches in the following manner. Pins 5 thru 8 and 12 thru 15 are the select lines for each of the filters. A low level signal applied to these input enables the filter for that line by providing a current path thru the PIN diode switches. For example, if a low level is applied to J3 pin 5 it provides a current path thru R54, LED D53, FL-52, R52, pins diodes D52 and D4, R2, FL-2, FL-3 to +12 VDC at J3 pin 4. At the same time it provides a second current path for the other side of the filter via R54 and LED D53, FL-51, R51, PIN diodes D51 amnd D2, R1, FL-1, to +12V at J3-pin 4. All the other filters are selected in a similar manner.

4.16 470/2000 MHz AMPLIFIER/SWITCH (A8B3)

Refer to schematic diagram 81B83-030.

The A8B3 module provides gain in the 470/2000 MHz range when in bands 6 and 7 and also provides gain for the 685 MHz IF when it is used (bands 3, 4, 5). When in bands 3, 4 or 5 +15 VDC is applied to FL-2 supplying power to amplifiers Z2 and Z3 via diode D2. It also selects a signal path from J2 to C5 by providing current through R2, L3, thru Z1 and L2 to ground. When in bands 6 and 7 +15V is applied to FL-1 supplying power to Z2 and Z3 via D1 and creating a signal path from J1 to C5 by current path through R1, L1, Z1, L2. Amplifiers Z2 and Z3 have approximately 9 dB gain each and PIN diode switch Z1 has approximately 3 dB loss, therefore the overall gain of A8B3 is be approximately 15 dB.

4.17 30/470 MHz AMPLIFIER/SWITCH/MIXER (A8B4)

Refer to schematic diagram 81B84-031.

The A8B4 module provides conversion to a 685 MHz intermediate frequency in the following manner. When in bands 4 or 5 +15V is applied to FL-1 supplying power to Z1 via diode D3 and turning on PIN diode switch D1 via current through R1, L1, D1, L3, R3 thus connecting J1 to the input of amplifier Z1. The output of Z1 is connected to the RF input of mixer Z3. The local oscillator is input via J3 and is always tuned 685 MHz above the desired receive frequency thus generating a 685 MHz IF. The 30-50 MHz (band 3) is done in a similar manner by applying +15V to FL-2 therefore supplying power to Z1 via diode D4 and turning on diode D2 via R2, L2, D2, L3, R3.

4.18 YIG OSCILLATOR (A8B8)

Refer to schematic diagram 81B88-023.

The A8B8 module provides the tuning voltage and current necessary to drive the tuning coils for both the YIG oscillator and the YIG preselector.

Operation for both the filter and oscillator is identical, therefore only the oscillator section will be described.

The tuning voltage enters on E1 and is connected to one input of

comparator U1 pin 3. The second input of the comparator (U1 pin 2) is the voltage across the sense resistor (R6). This sense voltage is directly proportional to the current through the YIG oscillator tuning coil. The output of the comparator drives the power amplifier (U2) with the correct polarity to equalize the voltage across the sense resistor, and the current through the YIG directly follows the tuning voltage.

4.19 YIG TRACKING (A12B2)

The YIG tracking circuits modify the 0 to +10V tuning signal from the tuning generator to match the tuning function of the YIG oscillator and the YIG preselector.

The 0-10V input (pin 3) connects to the 5 "HI" networks associated with bands 3 to 7 of the YIG oscillator and to the 2 "HI" networks associated with bands 6 and 7 for the YIG preselector. These networks allow for individual adjustment of the "HI" tuning voltage for each band. The "LO" networks all connect to the precision 11.00 VDC supply and allow individual DC offset adjustments for each band. These two voltages are then resistively summed together and passed on to programmable operational amplifiers U6 or U7 for YIG oscillator or U2 for the YIG preselector. Network selection ia made by the BCD input information on pins 14, 15 and 16. The output for the oscillator is pin E and for the YIG preselector is pin 2.

The coarse tune voltage for the 45-75 MHz synthesizer is also generated on this board in a similar manner using U1 and resistor networks consisting of R16, R17, R8 (Scan 1 HI), R1, R2, R3 (Scan 1 LO) R19, R20, R21 (Scan 2 HI), R4, R5, R6 (Scan 2 LO), R13, R145, R15 (Man 1 LO), R42, R43 (Man 2 HI). The output of U1 (pin 10) then connects to U3 which performs as a buffer. This output at pin 7 connects to Q1 which is used as an amplifier which allows the output to go to a maximum output of -20VDC.

4.20 REFERENCE OSCILLATOR (A9)

Refer to schematic diagram 81R90-013-1.

The A9 module contains the 5 MHz temperature compensated crystal oscillator (TCXO) which generates the reference frequencies for all of the phase locked oscillators within the PR-700 receiver.

The A9B1 board contains the 5 MHz TCXO (Z1) whose buffer output is on pin 3. U2 is an AND gate used as a data selector. The 5 MHz output on U2 pin 6 connects to a counter IC U3 which performs a frequency division function to supply the output frequencies of 500 kHz to J2, 200 kHz to J4, 100 kHz to J1. These outputs are used for reference frequencies for various phase lock loop oscillators in the receiver.

The A9B2 board is a 10.7 MHz phase locked oscillator and functions as follows: U1 is the phase detector which has a 100 kHz reference signal on pin 1. Pin 3 is connected to a divide by 107 circuit consisting of integrated circuits U2, U3 and U4. Transistor Q3 is the oscillator with its center frequency at approximately 10.7 MHz. This center is controllable by varactor diode D2. Transistors Q5 and Q4 are buffer/amplifiers for the 10.7 MHz oscillator output. The output of Q4 is connected to the divide by 107 circuitry yielding an output frequency of 100 kHz when the

oscillator is exactly at 10.7 MHz. This counter output is then connected to the phase detector input (U1 pin 3). As long as the frequencies on pins 1 and 3 of U1 are identical (100 kHz) there is no error correction voltage generated at the junction of E1 and R7, however if the 10.7 MHz oscillator tries to drift in frequency the output of the divider integrated circuits will not be exactly 100 kHz causing an error voltage to be generated and applied to varactor diode D2 to tune the oscillator back to exactly 10.7 MHz.

The A9B3 board is another phase locked oscillator which generates a final output frequency of 55.7 MHz. U1 is the phase detector integrated circuit which has a 200 kHz signal on pin 1 as a reference input. The output of the divide by 557 circuitry consisting of integrated circuits U3, U4, U5, U6 and U7, is connected to the second input of the phase detector. Transistor Q1 is the oscillator operating at approximately 111.4 MHz. Transistor Q2 is a buffer amplifier which has 2 outputs, one off of its emitter which connects to a divide by 2 integrated circut U8 (pin 2) to supply the 55.7 MHz (111.4 -2 = 55') output to J7. The other output from Q2 (collector) connects to a divide by 55.7 counters to generate 200 kHz at U1 pin 3 (the phase detector) when the oscillator is exactly at 111.4 MHz. Again as long as the frequencies on pins 1 and 3 of U1 are identical (200 kHz) there is no error correction voltage generated on U2 pin 6, however, if the 111.4 MHz oscillator drifts in frequency the output of the divide by 55.7 counters will not be exactly 200 kHz and the phase detector (U1) and operational amplifier (U2) will generate an error votlage to varactor diode D3 to bring the frequency of oscillator Q1 back to 111.4 MHz.

4.21 SUB-CARRIER RECEIVER (A11)

Refer to schematic diagram 81R110-012.

The A11 sub-carrier receiver provides a second demodulated output for reception of sub-carrier transmissions in the frequency range of 0-200 kHz. The signal enters via J1 pin L. Coils L1, L2 and L3 and capacitors C1 and C2 form a 400 kHz low pass filter to provide some preselection filtering, and the signal then connects to the RF port (pins 3 and 4) of mixer Z1. The local oscillator section consisting of U5, Q1 and T1 provides the local oscillator input to Z1 pin 8 in the frequency range of 455 to 655 kHz. The tuning of this oscillator will be discussed later in this section. The 455 kHz intermediate frequency output of Z1 (pin 1) is then connected to a 6 kHz wide band pass filter Z2 and on to IF amplifiers U1, U2, U3. The FM demodulation is provided by integrated circuit U6 (output on pin 1), while U4 provides for AM, demodulation (at pin 1) and also provides the CW/SSB output (at pin 8). The BFO for SSB/CW detection is provided by U7. U4 also provides the AGC output for the sub-carrier receiver when in the AM mode (pin 4). When in CW/SSB the AGC is provided by U8 (pin 2).

The local oscillator (U5) is tuned as follows when in any of the DE-MOD modes (AM, FM, SSB/CW). The tuning voltage from the SC tuning control on the front panel enters on pin 7 and is buffered by U13. Its output (U13 pins 1 and 2) then proceeds through S1-B1 and R46 to the other half of U13 which is again a buffer amplifier. This output is then connected to the frequency tuning input of VTO U5, thus providing the manual tuning of the local oscillator. When in the "SCAN" mode the tuning

voltage to this oscillator is provided as follows; the receivers sweep voltage enters on pin 4 and is buffered by U10. This output (pins 6 and 7) is then connected via S1-B1 to U13 pin 6 and then on to the VTO (U5) from pin 7. Thus the output of the VTO will be a swept frequency starting at 455 kHz (R12 provides for fine adjustment of this frequency) and stopping at 655 kHz (R13 provides fine adjustment of this frequency).

The SC video is output as follows: the output from the AM detector (U4 pin 1) is connected to U10 pin 3 (via R34). This is an amplifier with an offset adjustment (R33) to allow the baseline of the video output to be adjusted to 0 VDC. When in the sub-carrier scan mode the sub-carrier video output is switched to the receiver's CRT display. This display is therefore a pan display showing 0-200 kHz due to the fact that as the display is swept the tuning voltage to the VTO is also swept from 455 kHz to 655 kHz.

4.22 LO SWITCH MIXER (A8B6)

Refer to schematic diagram 81D86-032.

The A8B6 module provides for switching the various local oscillators needed and the mixer for generating the 165 MHz intermediate frequency.

In bands 3, 4 and 5 +15V is applied to FL-3 thus turning on a signal path from J3 to C7 by providing a current through R3, L3, Z2 and L4 and turning on PINNdiode switch Z2, therefore applying 520 MHz to the LO port of mixer Z3. The RF signal entering on J5 is always 685 MHz $\pm$5 MHz therefore the IF output is 165 MHz $\pm$5 MHz.

In band 6, +15V is applied to FL-2. This connects the LO on J2 to the "L" port on Z3 by turning on PIN diode switches Z1 and Z2. This is done via current through R2, L2, Z1, Z2, L4. The LO on J2 is always 165 MHz $\pm$ 5 MHz above the signal on J5.

In band 7 +15V is applied to FL-1. This connects the LO on J1 to the "L" port of Z3 by turning on PIN diode switches Z1 and Z2 via current through R1, L1, Z1, Z2, L4. The LO on J1 is always 165 MHz $\pm$5 MHz above the signal on J5. The conversion loss of mixer Z3 is approximately 4 dB.

4.23 IF (A3B1)

4.23.1 45/10.7 MHz CONVERTER (A3B1A1)

Refer to schematic diagram 81R31-062 and Figure A on page 5-35.

The 45 MHz IF output from A3B3 enters on J1 and is coupled by transformer T1 to QUAD FET mixer IC (U1). The 55.7 MHz local oscillator signal generated in the A9 module enters on J2 and connects to the FET mixer (U1) via transformer T2. The 10.7 MHz thus generated exits the A3B1A1 section via T3 and C1. This output is connected to several separate 10.7 MHz IF strips (A3B1A2,3,4, 5) and to a 10.7 MHz video IF section.

4.23.2 2 MHz BANDWIDTH (A3B1A2)

When the 2 MHz bandwidth is selected by the front panel bandwidth switch, a ground is applied to FL-5, turning on transistor Q12 thus supplying 12 VDC to the A3B1A2 section and enabling the 2 MHz IF strip.

The 10.7 MHz signal from A3B1 connects to first IF amplifier (Q2 pin 3) via capacitor C204. The output of this amplifier then feeds two separate circuits. One via C23 which is for the FM circuitry and one via C7 which is for AM CW.

4.23.3 AM DEMODULATION (A3B1A2)

The AM signal path is as follows. Integrated circuit U2 is a gain controlled RF amplifier. Its output (pin 7) connects to AM/AGC detector integrated circuit U3. This IC performs the AM demodulation (output on pin 1) and also provides the AGC voltage (pin 4) for the 2 MHz bandwidth. Both of these outputs are fed to other amplifiers for further switching which will be discussed in detail later.

4.23.4 FM DEMODULATION (A3B1A2)

The FM signal path via C23 is connected to U6 pin 1. U6 is an amplifier and FM discriminator (output on pin 6) and also provides a tuning meter output (pin 13). Again these outputs are fed to other amplifiers or switches which will be discussed in detail later.

4.23.5 150 kHz BANDWIDTH (A3B1A5)

The 150 kHz bandwidth operates in a manner swimilar to A3B1A2, with the signal entering amplifier transistor Q3 via C206. This output then passes through ceramic filter Z1, amplifier Q4 and filter Z2. The filters Z1 annd Z2 limit the bandwidth to 150 kHz. The output of Z2 is then coupled to the CW and AM amplif er (U7) and detector (U9) which operates in the same manner as in the 2 MHz IF strip. The FM amplifier (U11) gets its input directly from the output of Z2.

4.23.6 3 and 15 kHz BANDWIDTHS (A3B1A3 & A3B1A4)

The 15 kHz IF bandwidth operates in a manner similar to A3B1A2: the signal enters via C205 into amplifier transistor Q6, passes through 15 kHz filter Z3 and on to Q7 which is an FET switch used to connect the 15 kHz channel into the AM, FM and CW demodulators.

The 3 kHz IF bandwidth signal path is as follows: the signal enters amplifier transistor Q9 via C203. Capacitor C103 connects this output to one of 3 filter switching networks: Q20, Z10 and Q21 for CW; Q22, Z11 and Q23 for upper sideband demodulation; and Q24, Z12 and Q25 for lower sideband. The outputs of all three of these networks are then connected to the "NB AM IF" via C83 and NB FM IF via C113.

4.23.7 FM DEMODULATION

The narrowband FM discriminator (U17) operates in the same manner as the 2 MHz and 150 kHz bandwidths.

4.23.8 AM/CW/SSB DEMODULATION

The narrowband AM detector (U14) operates in the same manner as the 2 MHz and 150 kHz bandwidths with the additional capability of SSB and CW demodulation. A 10.7 MHz signal is injected into pin 6 of U14 when in the CW or SSB de-mod modes which serves as the beat frequency oscillator. The CW or SSB audio exits on U14 pin 8 and goes to audio selector IC U24 and also to the SSB AGC generator IC (U16) via Q8.

4.23.9 AUDIO SWITCHING (A3B1A6)

The AM outputs of all three bandwidths are combined by a resistor network consisting of R118 (2 MHz AM), R119 (150 kHz AM) and R121 (3 and 15 kHz AM) and applied to one input of operational amplifier U23. The positive input

of U23 is connected to a variable DC voltage generated by R123, D17 and variable resistor R124 and provides for adjusting the no signal (noise input) to approximately 0 VDC.

In a similar manner the FM outputs are combined by resistors R108 (2 MHz), R111 (150 kHz) and R112 (3 and 15 kHz) and are applied to one input of operational amplifier U22. The second input of U22 is also a summing network (R113, 114, 116) and connects to a "REF" output from each of the FM discriminator IC's to center the FM output level at approximately 0 VDC.

Although all three bandwidths are combined in these resistive networks there is only one bandwidth present at any one time because the bandwidth selector on the front panel turns on only one IF bandwidth.

The AM output (U23 pin 6) and the FM output (U22 pin 6) then proceed to audio selector IC U24. The CW/SSB output from U14 pin 8 also connects to U24 at pin 4. U24 selects one of these three (AM/CW-SSB/FM) to feed multiplexer U27 which then outputs the audio on pin 18.

4.23.10 AGC

The AGC voltages from each IF bandwidth connect to AGC amplifier U19 via diodes D13, D14 or D16. The output of U19 (pin 7) then connects to gate #2 of RF amplifier transistors Q9, Q6, Q3, Q2 to provide some AGC control near the "front end" of each IF bandwidth strip (A1B2A2 through A5).

Additional AGC is provided by AGC detector/amplifier IC's U3 (2 MHz), U9 (150 kHz) or U14 (3 and 15 kHz). The outputs of each of these IC's (pin 4) is connected to MAN/AGC switch selector IC U18. This switch connects either the front panel (MANUAL) gain control or the output of the AGC generators to Gain controlled amplifier IC's U2 (2 MHz), U7 (150 kHz) or U12 (3 and 15 kHz).

4.23.11 10 kHz BANDWIDTH VIDEO (A3B1A7)

The swept 13.5 MHz from the A3B4 module enters via J6. Transistors Q20, Q100, Q101, Q18 and integrated circuits U28 and U29 are amplifiers. Z13 is a 10 kHz bandwidth filter. The output of U29 (pin 3) is fed to log amplifier IC U33 and to a video detector circuit (D23 and D24). The log output from U33 (pin 10) also goes to a video detector consisting of D22 and D26. The output of both of these videos then proceeds to IC U34 which is an analog switch used to select the video output (U34 pin 14). This output then goes through video amplifier U35 and out at J7.

4.23.12 200 kHz BANDWIDTH VIDEO (A3B1A7)

The input to amplifier transistor Q19 comes directly from the 45/10.7 MHz converter (A3B1A1). This input is amplified by Q19, U31 and U32, and filtered by 200 kHz bandwidth filters Z7 and Z8. The output then goes to log amplifier U33 and to a video detector consisting of D29 and D28. The log output from U33 (pin 6) also goes to a video detector consisting of D31 and D27. This output then proceeds to video selector IC (U34) and again to video amplifier U35 and out J7.

4.24 260/520 MHz MULTIPLIER (A8B11)

Refer to schematic diagram 81B11-034-1.

The A8B11 module takes the 260 MHz output from A8B16 and frequency doubles this to 520 MHz in the following manner.

The 260 MHz input enters J1 at approximately 0 dBm. Transistor Q1 and tuned circuit consisting of C4, L1, C5, C6 and L2 perform the frequency doubling. Transistors Q2 and Q3 are amplifiers which amplify this 520 MHz output to approximately a +7 dBm level.

4.25 1-2 GHz AMPLIFIER (A8B5)

Refer to schematic diagram 81A85-050.

The 1-2 GHz amplifier module takes the 1160 MHz to 2160 MHz output from the YIG oscillator (via Z6, Z10, and Z5) and amplifies this signal to approximately a +10 dBm level. Integrated circuit U1 is a thin film modular amplifier with a 50 ohms input and output impedance and a 1000 to 2200 MHz bandwidth.

4.26 160 MHz DIVIDER/MIXER/LPF (A8B7)

Refer to schematic diagram 81B87-028.

The 160 MHz IF input on J2 first enters power splitter Z1 which provides a 160 MHz output for the wideband amplifier A8B9. The other output of power divider Z1 goes to RF amplifier U1 which has approximately 20 dB of gain. This output then goes to the RF input of mixer Z2. The LO input of Z2 is a 180 MHz signal from A8B16. The 10-20 MHz output from Z2 then passes through a LPF consisting of C1, C2, L1, L2, and L3 and exit at J4.

4.27 IF AMPLIFIER (A8B9)

Refer to schematic diagram 81R89-017.

The IF amplifier consists of a 160 MHz center frequency 20 MHz wide amplifier and contains its own AM and FM detectors and video amplifiers.

The 160 MHz signal out of the A8B7 module is fed to the first amplifier stage (Q1) through the impedance matching network L1, L2 and C1, C2. This matching network, together with the low-noise input transistor Q1, assures a low noise figure for the IF amplifier.

The first five stages (Q1,2 3, 4, 5) provide the gain and selectivity (20 MHz at 6 dB) for the auxiliary output J3. The overall gain from J2 to J3, including the loss at the resistive pad R14, R15, R16 is approximately 40 dB.

The remaining stage (Q6), with a gain of approximately 13 dB, provides additional gain and selectivity before the AM detector (D6). Diodes D1 through D4 provide some limiting action at high input levels and FM operation. They do not affect the AM performance.

Transistors Q2, 3, 4 are gain controlled by the IF GAIN potentiometer (R21 on assembly A1B4), which reduces their base voltages from -8 to -12 VDC to reduce the gain.

The AM video amplifier consists of U1, Q7 and Q1. It is DC coupled from detector to output, has a voltage gain of about 60 and a 6 dB bandwidth in excess of 10 MHz, so that the determining factor in video sensitivity is the selectivity prior to the AM detector. Potentiometer R55 adjusts the display baseline around 0 VDC. Diode D7 provides temperature compensating to U101, balancing out the junction variation of the AM detector D6. The output of the video amplifier is fed to J4.

Transistors Q12 and Q13 further amplify the 160 MHz signal, which is then limited by D11 and D12 and fed to amplifier Q14 and a Travis discriminator (L13, L14, L15, D13, D14 and associated circuitry). The discriminator has a 6

MHz video bandwidth at 6 dB. Its output is fed to the video amplifier (U2 and Q15), which has unity gain and provides a low output impedance at J5. Potentiometer R85 adjusts the DC level at center frequency around 0 VDC.

4.28 580-1170 MHz DIVIDE BY 10 (A8B10)

Refer to schematic diagram 81B810-033.

The 580 MHz to 1170 MHz signal from the YIG oscillator (via Z6, Z7) enters on J1. Integrated circuit U1 is an amplifier with approximately 10 dB of gain. Its output is fed to integrated circuit U2 which divides the frequency by 10. Its output exits through J2. Diode D1 is a 5.1 volt zener diode to supply U2 with approximately a 6.8 volt supply voltage.

4.29 RF SWITCHING (A8B15)

Refer to schematic diagram 81D815-1010.

The heart of the A8B15 module is U1 which is a ROM that provides the output logic shown in the table on the above referenced schematic for the BCD band input on pins J, H, F, K. These outputs then proceed to provide the following switched outputs.

1. Output pins C, D, E produce $\pm$15V as follows: output Y1 from ROM U1 is high in bands 3, 4, 5. This high level ($\approx$ +4.5V) is connected to operational amplifier U2A (non-inverting input pin 3); because pin 2 voltage is lower than pin 3 the output of U2A (pin 1) switches to approximately +14 VDC causing buffer amplifier U4 to do the same. This output goes to pin C via R7. Operational amplifier U3B inverts this level (-14 VDC) and U5 buffers this signal and is output on Pins D and E. In bands 6 and 7 the output from PROM U1 pin 6 is high, therefore causing the output from U2A to be -14 VDC.

2. Using the logic levels in the U1 PROM table on the schematic, the outputs for pins A and B are generated in a similar manner.

3. The positive switched voltages (Q1 thru Q8) are generated in the following manner: (using U8B and Q2 as an example) the input to U8B comes from PROM U1 pin 4. From the PROM program table, note that Y4 is high in band 6, therefore with U8B pin 3 high, U8B pin 4 is low, causing Q2 to turn on supplying +15 VDC out pin 13 in band 6.

4. The negative switched output voltages work in a similar manner. (using Q10 and Q14 as an example). Q14 emitter connects to PROM U1 pin 1 via R47. U1 pin 1 is high in bands 3, 4, and 5. With a high level on Q14 emitter Q14 turns on, applying a positive voltage to the base of Q10 thus turning it on and supplying -12V out of pin T in bands 3, 4 and 5.

5. Transistors Q17 and Q18 are turned on when pin 5 (Attenuator Enable) is low. This in thurn lowers the bias to the antenna select Pin Diode Switch. Resistor R60 is adjusted so that this decrease in bias provides approximately 10 dB of attenuation.

4.30 180-260 MHz PHASE LOCK LOOP (A8B16)

Refer to schematic diagram 81R816-059.

The A8B16 module generates the 180 MHz and 260 MHz phase locked signals for use as local oscillators in the receiver. These 2 signals are generated in a similar manner as described in the following section.

4.30.1 180 MHz PHASE LOCKED SOURCE

Transistor Q3 is a voltage controlled oscillator with its frequency being approximately 180 MHz when the voltage on varactor diode D2 is at 3 VDC. This oscillator output is connected to buffer amplifier Q5. The signal at the emitter of Q5 is amplified Q6 and exits at J2. The collector of Q5 provides the input via C13 to a divide by 36 divider chain consisting of U9 (divide by 9), Q4 and U2 (divide by 4). The 5 MHz output is applied on to phase detector IC U1. The reference input (pin 1) of U1 is at 5 MHz. The output of the phase detector then generates a DC voltage at U1 pin 8 which keeps the voltage tuned oscillator (Q3) at exactly 180 MHz.

4.30.2 260 MHz PHASE LOCKED SOURCE

The 260 MHz loop works in a similar manner. The voltage tuned oscillator Q2 operates at 260 MHz when the voltage at D2 (cathode side) is at 7 VDC. This output connects to amplifier Q3. Q3 collector provides the 260 MHz output to J4 while its emitter provides the input to a divide by 104 divider chain consisting of U8, U7, U4, U5 and U6. The output of this divider (U4 pin 9) is a 2.5 MHz signal and provides one input to phase detector U2. The reference input to the phase detector is provided by the 5 MHz signal input at J3, divided by two at U1 pin 12. The phase detector outputs (U2 pin 2 and 15) are summed in operational amplifier Q3 and applied to the varactor diode D2 via R11 and R32, thus keeping the oscillator tuned to 260 MHz.

4.31 YIG PHASE LOCK LOOP/FILTER (A8B17)

Refer to schematic diagram 81R817-060.

The A8B17 module takes a sample of the YIG oscillator output which is divided by 10 in the A8B10 module and uses this input on J2 to phase lock the YIG oscillator in 10 MHz steps via the output on pins 12 and 13 which goes to the YIG oscillators FM coil inputs.

The input at J2 goes to a divide by N circuit consisting of U5, U1, U2, U3 and U4. The divide number (N) is entered on J1 pins 1 thru 10 and is generated by assembly A6B2. This divide by N circuit divides the YIG oscillator output by the correct number to generate a 500 kHz output from U1 pin 9 when the loop is phase locked.

The 500 kHz signal then proceeds to the A8B17A2 PC board and becomes one input to phase detector IC U1 (pin 3). The reference input to U1 (pin 1) is a 500 kHz signal from J3. The output of the phase detector (pins 2 and 13) are summed by operational amplifier U2. This output then goes on to buffer amplifier U3 and then on to the YIG oscillator FM coil via pin 12.

4.32 SWITCHING LOGIC (A12B3)

Refer to schematic diagram 81D123-040.

The heart of the A12B3 switching logic PC board is the programmable read-only-memory IC U2. The PROM generates the output logic shown in the truth table on the schematic depending on the inputs on pins B, C, D, E, J, and K. (Band and Mode Input). The outputs from this PROM then connect to transistor switching circuits identical to those describe in section 4.29.

4.33 SWEEP MARKER GENERATOR (A12B4)

Refer to schematic diagram 81D124-041.

The sweep generator section consists of transistor Q1, operational amplifiers U2 and U3A and U3B and associated components. These components generate a sawtooth waveform of -5V (adjusted by R21) to +5V (adjusted by R23). The sweep rate is varied by the front panel sweep rate control adjusting the bias on gate of Q1 thus controlling the charge current to C1. The sweep output is taken from U2 pin 6. This drives the input to U1A pin 3 (via R17) which provides the -5 to +5V sweep to A3B4 pin 4. It also provides the input to U1B (via R25) which generates the outputs for the sub-carrier sweep at pin C and the CRT display "Horiz" sweep at pin D. This -5 to +5V also generates the "Vari Scan" sweep voltage by sending this -5V to +5V sweep out to the front panel sweep width control via R1. The attenuated sweep voltage then returns on pin F, is bufered by U4A, summed with a DC voltage (from pin E and U5) at R53 and R54, buffered by U8A, U8B and U9 and exits on pin M.

The blanking and the sub-carrier marker is generated by integrated circuits U6, U3C and U3D, U7A and U7B and output on pin 2.

The +11.00 volt precision reference is generated by diode D7, operational amplifier U13 and transistor Q2 and output on pin S.

4.34 +5 VOLT REGULATOR (A13)

Refer to schematic diagram 81B30-046.

A 2.4V reference voltage is generated at the cathode of zener diode D1. This voltage is one input to operational amplifier U2 which is used as a voltage comparator. The other input to the comparator is a sample of the +5V output (via resistive divider network R7, R8 and R9). If the voltage at pin 6 of U2 falls below the reference voltage. Operational amplifier U2 increases its voltage to transistor Q2 causing an increase in base current to Q1 and raising the +5V output voltage until the voltage at pins 5 and 6 of U2 are equal. If the voltage at pin 6 of U2 is higher than the reference then the voltage out of U2 goes lower thus providing less base current to Q1 via Q2 and lowering the output voltage.

4.35 LOW FREQUENCY SYNTHESIZER

The low frequency synthesizer (LFS) consists of four modules which generate an output of 45-75 MHz. The LFS frequency is referenced to 100 kHz and 200 kHz signals derived from the 5 MHz oven-controlled crystal oscillator within the A9 assembly. The output frequency is programmed by the A6 Display boards.

4.35.1 20.0-29.9 MHz DIVIDE BY N SYNTHESIZER A4B1 (100 Hz + 1 kHz Resolution)

A4B1 provides the 100 Hz and 1 kHz resolution components of the programmed frequency. To accomplish this it generates a frequency of 20 MHz to 29.9 MHz in response to a digital input. The 20-29.9 MHz signal is translated and divided to provide the .1 kHz resolution described.

The heart of the loop is the divide-by-N circuitry consisting of pre-settable down counnters U5, U6 and U7; controller U3; and variable modulus pre-scalar U4. This group of circuits has two inputs and one output. The first input signal is the buffered output of VCO U1, into the variable modulus prescalar U4 which performs a series of divide-by-ten and divide-by-eleven operations on the frequency output of U1. The second input is the two least significant digits of the number N, corresponding to the 100 Hz and 1 kHz BCD

words of the frequency input command, into U5 and U6 respectively. The most significant digit of N(2) is a constant, and is hard-wired high through pin 1 of U7. The single output is a digital signal which is a 100 kHz pulse to the phase detector.

Controller U3 receives the digital input (N) of pre-settable down counters U5, U6 and U7 and operates on this information to provide the proper mix of divide-by-ten and divide-by-eleven commands to the variable modulus pre-scalar so that the following relationship is true:

$F/(10m + 11n) = 100$ kHz

F = Corrected frequency of VCO #1 corresponding to the selected input N.

m = Number of divide-by-10 commands to U7

n = Number of divide-by-11 commands to U7

Where m and n are derived values from N such that the relationship is true.

In the active loop, F is the independent variable and the nominal 100 kHz error signal is the dependent variable which tracks any error in F. The purpose of the closed loop is, of course, to drive F so that the error tends toward zero (precisely 100 kHz out).

With the loop closed and operating with some input N, the controller U3 outputs a series of commands from pin 7 to the variable modulus prescalar U4. Depending on the state of pin 7 of U3, U4 outputs a pulse on pin 11 for each ten or eleven cycles of VCO 1. This pulse is coupled to the clock inputs of U5 and U6, (pin 14) and of U3 (pin 1) to reduce the inserted N number by one for each clock pulse received. This process continues until N has been reduced to zero, at which time controller U3 outputs a pulse from pin 9 to reset N into U5, U6 and U7 and to provide the phase error signal to phase detector U1. This cycle repeats continuously resulting in an output from pin 9 of U3 at a rate of 100 kHz plus or minus the factored short-term stability of the VCO.

The phase error signal enters the phase detector on pin 3 of U1. The 100 kHz reference signal is outputted on pin 10 of U2, and the nominally 100 kHz error signal on pin 5. They are summed at the common node of R3 and R4. This node also includes the base of Q1 and dampening filter R5, R6, and C1. The emitter of Q1 is coupled to a Darlington series in U2 through which the error signal is amplified and outputted on pin 8 of U1. This level is applied to Varactor Diode D1 which, in conjunction with L1, forms a parallel resonant circuit for VCO U1. L1 is adjusted so that resonance from 20 to 29.9 MHz is attainable through the controlled range of Varactor Diode D1.

The loop is closed by the output of U2 through buffer U8, one output (pin 14) of which is the input to variable modulus pre-scalar U7. The second output of buffer U8 is the input to the divide-by-100 combination, Q2 and U9.

4.35.2 20-29.9 MHz SYNTHESIZER, A4B2 (10 kHz and 100 kHz Resolution)

This unit is very similar to the previously described A4B1 module to the extent that sub-module A4B2A1 is an exact copy of A4B1 with the exception of the frequency control input. Whereas the 200 off-set in the divide-by-N of A15 was hard-wired, the 198 off-set for the divide-by-T of A4B2 is arithmietically added to the input frequency control word.

4.35.2.1 SUMMINNG LOOP, A4B2A1

For a discussion of the operation of A4B2A1 refer to 4.35.1. The differences on this board, as compared to the

A4B1, are that the divide number is 198-297 rather than 200-299; also, the divide-by-100 circuitry of A4B1 is not used on A4B2A1.

4.35.2.1 DIVIDE-BY N, A4B2A2

Inputs to this board are the 19.8-29.7 MHz output of A4B2A1 (T loop) and 200-299 kHz output of A4B1 (N loop divided-by-100).

The description of operation will use the following designations:

F_T = 19.8-29.7 MHz output of A4B2A1 (T loop)

F_N = 200-299 kHz input from A4B1 (N loop)

F_{NT} = 20-29.999 MHz sum of F_T + F_N

U3 is a D flip-flop and U4 a phase detector. Each of these circuits have inputs of F_T and F_N. The purpose of U3 is to detect any error in the loop summation so that a correction signal may be derived by phase detector U1. U4 is the first stage of a feed-back path to U1 output summing node which assures that U2 sums F_T and F_N rather than differencing them.

F_T is the "D" input to U3 at pin 6, and F_{NT} the clock input at pin 7. The resultant output at pin 2 is F_{NT} - F_T which is F_N plus or minus any short-term instability of VCO V1. This output is an ECL level signal which is converted to TTL by Q2 and applied as the "variable" input to pin 3 of phase detector U1. The "reference" input at pin 1 is F_N, the N loop frequency divided by 100.

The phase detected outputs are summed at the common node of R4 and R6. The common node of R5 and R6 is a correction node to which is coupled the processed output of phase detector U4 to assure that F_{NT} is greater than F_T. So long as the F_{NT} input to pin 6 of U6 is higher in frequency than the F_T input at pin 9, differential amplifier U5 will have a positive output. In this case diodes D2 and D3 are back-biased and will produce no effect at the correction node junction of R5 and R6. Should the frequencies become inverted during turn-on or due to a switching transient such that F_T is greater than F_{NT}, diodes D3 and D4 are forward biased to raise the potential at the summing node R4-R6. This level is amplified by a Darlington series consisting of Q1 and part of U1 which is outputted at pin 8 of U1 and applied to varactor diode, D1, raising the frequency of VCO V1. Once the sense is settled, the effect of U4 and U5 back biases D2 and D3 and phase detector U1 reverts to correcting the minor deviations of U2.

The output of U6 is applied to Q3 which amplifies the signal to meet TTL logic levels and drives U7. U7 divides the signal by 100 and thus provides a TTL output signal which is the summation of A4B1 and A4B2A1 divided by 100 (200 to 299.99 kHz).

4.35.3 45-75 MHz SYNTHESIZER A4B3

This is the final loop of the low frequency synthesizer (LFS) and adds the 1 MHz BCD, 10 MHz BCD, and 100 MHz digit of the frequency select word.

4.35.3.1 44.8-74.8 MHz SYNTHESIZER A4B3A1

The inputs to A4B3A1 are the crystal derived 200 kHz reference and an divide-by-M inputs have digital values of 448-748.

The phase detector (U1) compares the phase of the trailing edges of the signals on input pins 1 and 3. To be in a phase-locked condition, the frequency

of the two signals must be exactly equal. The U1 outputs on pins 13 and 2 have switching outputs which vary dependent upon the phase of the signals on pins 1 and 3. The outputs from pins 13 and 2 feed into the U3 filter circuit and are integrated to produce an analog voltage out on pin 6 of U3. The U3 output is connected to a twin-T filter used to reduce the 200 kHz spurious signals. The Q2, R18, R12, R14, R15 and C13 circuit is a passive filter to lower the loop bandwidth, thus reducing phase noise and spurious signal levels. The passive filter cannot be in the circuit at all times, however, because it severely slows the lock time of the loop. U2, Q1 and Q2 are used to switch the filter out of the circuit when not phase locked and not switch the filter back in until a phaselocked condition has been obtained ffor a short period of time. U1 detects a phase-locked condition and controls U2.

The voltage at L1 controls the Q4 oscillator frequency. The tuning on the oscillator ranges from 3-9 volts. Tuning is accomplished by varying the capacitance of varactors D5 and D6. The capacitance decreases as the voltage across the varactors increases.

Q5 is a buffer amplifier which supplies the oscillator frequency to the A4B3A2 board and the divide by M pre-scalar (U5).

The programmable divide-by-M circuitry consists of U4-U8 of which U6-U8 are presettable down counters. U5 is a variable ratio divider (divided by 10/divided by 11), and U4 is the controller which controls the U5 divide ratio, presets the counters and monitors the counter outputs. When pin 2 of U5 is held low (ECL) the division ratio of U5 is 11, and when held high by U4 the ratio changes to divide-by-10.

The controller monitors the down counters' status to determine divide ratio requirements and to determine when the counter is down to a count of two. A look-ahead technique employed by the controller enables the circuitry to operate at a higher frequency than would be typically possible. The pin 9 output of the controller presets the counters to the divide-by-M ratio present at the J1 connector input and drives the phase detector variable input upon receiving a zero count from all of the down counters.

4.35.3.2 SUMMING LOOP, A4B3A2

Operation of the A4B3A2 board is basically the same as A4B1 and A4B2A1 with the exceptionns of the reference frequency, divide ratio, and the switchable passive filter.

4.35.4 45-75 MHz BUFFER PLL A4B4

A4B4 is a buffer phase-locked loop used to reduce the sample rate spurious from the A4B3 module. This PLL is different from the other PLL units in the PR-700 in that there is no divider circuit included and the output frequency is identical to the input frequency.

U1 is an ECL phase detector which compares the incoming reference frequency on pin 9 to a sample of the VCO signal on pin 6. The two outputs from pins 3 and 12 drive the U2 active filter, which integrates the signals and results in a DC voltage to drive the Q1 oscillator. Tuning is accomplished by varying the voltage across varactors D1 and D2. L1 is a RF choke used to isolate the driver from oscillator circuit but retain a low impedance source voltage. D6 and D7 are diodes used to decrease switching time by lowering the time constant R12, R13 and C8.

Q2 is a buffer amplifier stage and Q3 is a low impedance amplifier to drive the coax cable and phase detector.

5.0 MAINTENANCE

This section contains instructions for limited corrective maintenance of the PR-700 Receiver.

The Procedures and diagrams contained in this manual are considered adequate to enable a qualified technician to maintain the receiver in normal operating condition.

Actual location of malfunctions, replacement of components, and subsequent re-alignment is beyond the scope of this handbook.

Maintenance personnel should be familiar with the material contained in other sections of this manual prior to attempting repair or adjustment.

A good understanding of the system block diagram, wiring diagram, and control functions will aid in localizing faults to particular modules.

Reference is made to schematic diagrams found in section 7.0 of the manual. Component layouts are included where applicable.

Voltage measurements are made using a digital voltmeter with a minimum input impedance of 100K ohms. Waveforms are observed using an oscilloscope with a minimum probe impedance of 1 Megohm and a capacitance of 47pf or less.

Any failure in the receiver may be the cause or effect of improper power supply performance, therefore, the power supply should be checked prior to and following any other procedure.

It is suggested that the theory of operation section be read for the module in which the fault is suspected before proceeding with the maintenance of the module.

5.1 POWER SUPPLY, ADJUSTMENT AND MAINTENANCE, A2

5.1.1 POWER SUPPLY PRELIMINARY CHECK

a. Check fuses F_1 and F_2.

b. Check position of the 115/230V switch.

c. Check position of the AC/DC switch.

d. Remove the top and bottom covers.

e. Connect a voltmeter between the chassis and the following terminals with wire colors as indicated. Refer to Figure 5.1 for terminal locations. Turn the receiver POWER ON.

WIRE	READ VOLTAGE
Green	+5 VDC ±2%
Rd/Wht	+15 VDC ±2%
Red	+12 VDC ±2%
Orange	+6 VDC ±2%
Yel/Wht	-15 VDC ±2%
Yellow	-12 VDC ±2%
Blue	-6 VDC ±2%
Violet	-20 VDC ±2%

5.1.2 POWER SUPPLY MAINTENANCE

5.1.2.1 PRELIMINARY SETTINGS

If an abnormal voltage was measured by procedure 5.1.1, a fault probably exists in the power supply. Proceed as follows:

a. Turn power OFF and remove all external power.

b. Check all power connectors for tightness.

c. Remove the 25 pin power connector from the power supply.

d. Connect a jumper between pin 12 of the power supply chassis connector and ground.

NOTE: When performing the following step the power supply should be left on no longer than necessary to make the measurements and then turned off.

e. Reconnect power to the receiver and measure the voltages at all of the test points listed on 5.1.1 (e). If all voltages are normal, with the exception of the +5 VDC which will be higher, an excessive load is probably being applied by circuits external to the power supply. If an abnormal voltage still exists, however, proceed with the following steps.

f. Remove the power supply from the receiver, and remove the power supply covers.

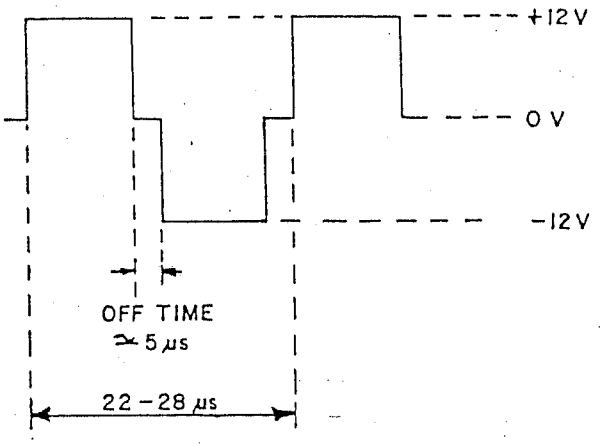
g. Remove the jumper from pin 12 to ground and reconnect the power supply to the receiving cabling.

h. Switch the following controls to the settings shown:

BAND	Band 2
IF BANDWIDTH	15 kHz
MODE	SYNTH
TUNING	10 MHz (approx.)

5.1.2.2 FAULT ISOLATION

a. If the pre-regulated +6 VDC, measured at pins 5, 6, 7 or 8 is not within specifications (+6 VDC ±5%) check the waveform at assembly A2B1 (control). The correct waveform between pins 1 or 3 of transformer T2 and ground is shown in the following diagram.



b. If one of the regulated voltages, as measured in 5.1.2.1 (e) preceeding, is not within specifications, check assembly A2B3 (Regulators). The input voltage at pin #18 of A2B3 is +18 VDC minimum; at pin #19, -18 VDC minimum. If these voltages are correct a problem exists in one of the four-pin regulators (U4 through U10).

c. If the voltages at pins 18 and 19 of A2B3 are incorrect a problem exists in assembly A2B2, which comprises the high voltage switching transistors Q7 and Q9 (AC operation); high current switching transistors Q11 and Q12 (DC operation); bridge rectifiers and filters to generate the pre-regulated +6 VDC and ±18V minimum to assembly A2B3.

5.2 ANTENNA PREAMP, A8B14

Refer to schematic diagram 81B814-024 and component layout 81A814-353.

NOTE: The antenna pre-amp is designed for the high impedance whip antenna supplied with the PR-700 Receiver. If the antennna pre-amp is switched on with a 50 ohm antenna input connected, there will be no increase in receiver performance. Additionally, the antenna pre-amp has no significant gain above 30 MHz.

If the antenna pre-amp appears inoperative (no increase in signal or noise level when the pre-amp is switched to ON) the following checks should be made.

a. Remove A8B14 assembly.

b. Check DC voltage on input filter (10 ohms resistor): -8.1V ±.3V.

c. Remove the cover from module and inspect for broken wires.

d. Measure the DC voltage from the case of FET (Q1) to ground (-4.3 VDC ±.3). If this voltage is incorrect replace Q1.

e. Check continuity from input connector to Q1 Pin 3 and E2 to output connector.

5.3 PRESELECTOR/LOW FREQUENCY, A8B1

Refer to schematic diagram 81R81-048 and component layouts 81B81-316, 81B81-317 and 81A81-318.

The most obvious receiver fault that would indicate a problem in the A8B1 module would be a large decrease in receiver sensitivity over a small portion of the frequency range that closely matches one of the ranges indicated in Table 5.3.1.

If this is true then remove the top cover of the receiver and check to see that the LED for that frequency range is on. If it is on, then the fault probably is not in the A8B1 module. If it is not on, first check the logic on A12B1 PC board (section 5.4) before proceeding as follows:.

a. Remove A8B1 module from A8 RF assembly and remove the top and bottom covers.

b. Reconnect the input power plug to A8B1 and turn the receiver on.

c. Select the proper band and frequency to switch the suspected bad filter on.

d. Check for voltages as listed in Table 5.3.2.

e. If these DC voltages appear correct the next step is to input a signal into J1 at approximately 0 dBm (.6 V p-p) and check the output at J4 using an oscilloscope. (Note: J4 must be terminated with 50 ohms). This output should be no less than .2 V p-p if the filter is working. If it is less than .2 V p-p it will be necessary to trace this signal through the A8B1 module to determine where the problem exists. Using Filter "C" as an example proceed as follows:

Determine from Table 5.3.1 that filter "C" must be "on" from 2 MHz to 2.75 MHz. Tune the

TABLE 5.3.1

	A8B1 PRESELECTOR FILTER RANGES	
BAND	FILTER DESIGNATION	FREQUENCY RANGE (APPROXIMATE)
1	A	0-5000 kHz
1	B	500 kHz - 2 MHz
1	C	2 MHz - 2.75 MHz
1	D	2.75 MHz - 4.15 MHz
1	E	4.15 MHz - 6.7 MHz
1	F	6.7 MHz - 10 MHz
2	H	10 MHz - 12 MHz
2	J	12 MHz - 15 MHz
2	K	15 MHz - 19 MHz
2	L	19 MHz - 30 MHz
3	M	30 MHz - 50 MHz

TABLE 5.3.2

FILTER ON	
A	R58, FL14 side ≈ 0 VDC, cathode D38 ≈ .42 VDC Anode D38 ≈ .2 VDC, Q3 base -.74 VDC Q3 collector ≈ 0 VDC
B	R49, FL13 side ≈ 0 VDC, cathode D36 ± .4 VDC Anode D36 + 2 VDC, D35 cathode, D34 Anode -5.4 VDC
C thru L	Check to see that the pin diodes at the input and output of filter are biased on (cathode ≈.7 VDC lower than anode. If they are not, check equivalent points using filter "B" as an example.

receiver and the generator to 2.4 MHz. If there is no output at J4 follow the signal path from J1 thru K1 (in pin 2 and out pin 4) and thru K2 (in pin 2 and output pin 4) to C51 which connects the signal to the input of filter "C" via PIN diode D30. Continue following the signal through the filter, PIN diode D31 and on thru to the output via C99 and K3 or until the signal level drops below approximately .2 V-p-p. All of the other filters can be checked in the same manner.

5.4 PRE-SELECTOR FILTER SWITCH, A12B1

Refer to schematic diagram 81R121-039 and component location 81A121-375.

If a problem is suspected on the A12B1 board first check the logic or voltage levels at the points specified in Table 5.4.

The voltage comparators can be checked in the following manner using band 1 as an example.

With the receiver in band 1, mode in Synthesize, and tuned to 0000.0000 MHz, the output from U6-1 should be low and the input to U10-1 high; the output at U10-3 is high, causing U15-3 to go low enabling filter "A".

As the receiver is tuned up in frequency the 0-10V per band at pin U increases and the voltage at U5-1 follows. The output of U5-1 connects to one input of voltage comparators U6 and U7. The other input of the voltage comparators is an adjustable voltage from a resistive voltage divider. As the tuning voltage on U6-7 exceeds the voltage on U6-6 ($\approx$.5V) the comparator output (U6-1) goes high. This makes both inputs on "exclusive or" gate U10 (pins 1 and 2) high causing its output to go low thus turning off filter "A". The output of U6-1 also connects to U10-4 thus causing U10-6 to go high and U15-6 to go low, enabling filter "B". This same procedure occurs thru to the end of band 1 and also applies for bands 2, 4 and 5.

5.5 45 MHz MIXER AMPLIFIER, A3B3

Refer to schematic diagram 81R33-043 and component layout 81B33-311.

The procedure to determine if a problem exists in A3B3 is as follows:

Tune the receiver to 16 MHz and input a signal at 16 MHz (-30 dBm) into J1 on A3B3 module. With an oscilloscope (terminate input of scope with 50 ohms) check the outputs from J3 and J4. Both should be greater than 180 mV-p-p. If they are, then the A3B3 module is operating properly. If not proceed as follows:

a. Remove A3B3 module from the unit and remove the top and bottom covers.

b. Check DC voltage levels per Table 5.5.

c. Using oscilloscope check for approximately .1 V-p-p on Q1 Pin 3 and 1.2 V-p-p on Q1 pin 1.

d. Check the following points on U1.

PINS 3 & 5	$\approx$3 V-p-p
PINS 1 & 7	3 V-p-p
PINS 2 & 6	40 mV-p-p

TABLE 5.4

MODE	BAND	FREQ	J1 Pin 15	J1 Pin 16	J1 Pin 17	J1 Pin N	J1 Pin 14	J1 Pin S	U15 Pin 1	U16 Pin 12	U17 Pin 12	U18 Pin 12	U14 Pin 10	U5 Pin 1	U5 Pin 7
SYNTH	1	0	H	L	L	H	H	H	H	L	L	L	H	0	-
SYNTH	2	10	L	H	L	L	H	H	L	H	L	L	H	0	1.5
SYNTH	3	30	H	H	L	L	L	L	L	H	L	L	H	0	1.5
SYNTH	4	50	L	L	H	L	H	L	L	H	H	L	H	0	1.5
SYNTH	5	150	H	L	H	L	H	L	L	H	L	H	H	0	1.5
SYNTH	6	470	L	H	H	L	H	L	L	H	L	L	H	0	1.5
SYNTH	7	1000	H	H	H	L	H	L	L	H	L	L	H	0	1.5
SYNTH	2	10	-	-	-	-	-	-	-	-	-	-	L	-	-
SYNTH	1	10	-	-	-	-	-	-	-	-	-	-	-	10	3.5
SYNTH	2	30	-	-	-	-	-	-	-	-	-	-	-	10	3.5
SYNTH	3	50	-	-	-	-	-	-	-	-	-	-	-	10	3.5
SYNTH	4	150	-	-	-	-	-	-	-	-	-	-	-	10	3.5
SYNTH	5	470	-	-	-	-	-	-	-	-	-	-	-	10	3.5
SYNTH	6	470	-	-	-	-	-	-	-	-	-	-	-	-	1.5
SYNTH	6	479.99	-	-	-	-	-	-	-	-	-	-	-	-	2.5

TABLE 5.5

PIN	Q1	Q2, Q4	Q3
1	11.63	11.79	.63
2	7.68	4.05	1.23
3	3.57	2.62	11.62
4	1.34	0	-

TABLE 5.6

DEVICE DESIGNATION	PIN NUMBER													
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
U1	0	14.28	3.13	0	3.13	0	0	0	-	-	-	-	-	-
U2	4.89	0	3.72	0	1.41	0	0	0	-	1.62	-	1.61	-	4.89

TABLE 5.7

TEST POINT	VOLTAGE
FL-1	+15 VDC
FL-2	*15.06
FL-2	**2.90
Q1-E	1.63
Q1-B	2.28
Q1-C	15.06

TEST POINT	VOLTAGE
D2 Anode	*4.8
D2 Anode	**2.72
D1 Cathode	*4.83
D3 Cathode	*4.04
D3 Cathode	**1.45
D2 Cathode	*4.44
D2 Cathode	**2.12

* Marker at Max
** Marker at Min

e. Check peak to peak voltage at Q3. Collector should be approximately 3 V-p-p.

f. Check peak to peak voltage on Q2 pin 3 (.5 V-p-p) and Q4 pin 3 (.5 V-p-p.

5.6 45/13.5 MHz CONVERTER, A3B4

Refer to schematic diagram 81C34-025 and component layout 81A34-330.

The A3B4 module is the first module of several for generating the pan video output in the SYNTHESIZE mode. Therefore if there is a problem with the pan video in the synthesize mode a possible source is A3B4.

To determine if the 45/13.5 MHz converter is operating properly, proceed as follows:

Remove the A6 assembly to access the A3B4 module under it. Remove the connector on J1 and input a 45 MHz, -20 dBm signal into J1. Remove connector on J2 and connect this output to the oscilloscope. Set the front panel SCANWIDTH control to "OFF" and the center ing control to midrange. There should be a 13.5 MHz signal on the oscilloscope at approximately .1 V-p-p. If this signal is present at the above level the module is operating correctly.

If the above signal is not present it will be necessary to remove the top cover of the A3B4 module and proceed as follows:.

a. Check DC voltages per Table 5.6.

b. Check the signal levels at the following points with an oscilloscope.

U1 pins 3 & 5	.75 V-p-p
U1 pins 1 & 7	5 V-p-p
U1 pins 2 & 6	.75 V-p-p
U2 pins 3	1.5 V-p-p

c. Set the front panel scanwidth control to maximum and check for sweep voltage on FL-5 (1 V-p-p).

d. Check DC voltage on FL-4 (6.39 VDC).

5.7 45 MHz MARKER GENERATOR, A3B2

Refer to schematic diagram 81B32-014 and component layout 81A32-331.

A problem exists in the A3B2 module if a marker is not present in the synthesized mode but a signal is received and displayed normally.

The first step in checking this module is to remove the cable from the A3B3 J5. Turn the marker on and set to maximum amplitude. With the spectrum analyzer and a 10X scope probe check for the presence of 45 MHz at approximately -66 dBm on the cable removed above.

If the signal is present then the module is working properly. If it is not it is necessary to remove the top cover of the module and proceed as follows.

a. Check DC voltages per Table 5.7.

b. Check for the following with an oscilloscope.

TEST POINT	VOLTAGE
R5 & C4	2.0 V-p-p

TABLE 5.8.1

E12	E13	E14	E15	E16	E17	E18	E19
Fast Up			Slow Up	Fast Down			Slow Down

TABLE 5.8.2

TEST POINT	LOGIC LEVEL WITH "FAST UP" BUTTON PRESSED
E16	L
U9C-3	H
U8A-8	L
U6C-11	L
U6C-12	H
U7A-12	PULSE
U7A-11	PULSE
U5C-13	H
E4	H
E2	H
U5C-11	PULSE
U7C-6	PULSE*
U7C-5	H End of Band

* when not at end of band

TABLE 5.8.3

TEST POINT	LOGIC LEVEL WITH "FAST UP" BUTTON PRESSED
E16	L
U9C-3	H
U8B-6	L
U6D-8	L
U6D-9	H
U7B-10	PULSE
U7B-8	PULSE
U5D-8	L
U5D-10	L
U7D-3	PULSE *
U7D-2	H **
E4	H
E2	H

* when not at end of band
** when at end of band

TABLE 5.8.4

TEST POINT	LOGIC LEVEL WHILE TUNINNG IN "UP" DIRECTION	LOGIC LEVEL WHILE TUNING IN "DOWN" DIRECTION
Pin A	PULSE	PULSE*
Pin B	PULSE	PULSE**
U4-5	PULSE	PULSE
U4-9	L	H
U5A-6	PULSE	H
U5B-3	H	PULSE
U5D-8	H	PULSE
U5C-11	PULSE	H
U7C-6	PULSE	H
U7D-3	H	PULSE

* normally high
** normally low

5.8 TUNING LOGIC, A1B1A2

Refer to schematic diagram 81D112-027 and component location drawings 81A112-382 and 81A111-383 for unit serial numbers up to 174 or schematic diagram 81D112-027-1 and component layouts 81A112-183 and 81A112-182 for serial numbers 175 and up.

Before proceeding, please read Theory of Operation section 4.5.

A problem probably exists on the tuning logic assembly if the receiver will not tune up or down in frequency via the front panel pushbuttons or the optical encoder "FINE TUNE" knob.

1. If the front panel pushbuttons are inoperative proceed by checking for a low logic level (less than .8 VDC) on points E12 thru E19 (see Table 5.8.1) when the associated front panel pushbutton is depressed and a high logic level (greater than 3 VDC) when not depressed.

2. While pressing the "FAST UP" button check for the logic levels listed in Table 5.8.2 and 5.8.3 using an oscilloscope.

3. If the "FINE TUNE" is inoperative check the logic levels per Table 5.8.4.

5.9 SCOPE ASSEMBLY (A10)

Refer to schematic diagram 81R100-015 and componenty layouts 81A101-354, 81A102-355 and 81A103-398.

The Scope Assembly is located on the left side of the receiver, directly behind the CRT.

CAUTION

DANGEROUS HIGH VOLTAGES ARE PRESENT IN THIS MODULE AND ON THE SOCKET OF THE CRT.

5.9.1 MEASUREMENTS

Voltage measurements can be made by removing the A10 module from the chassis in the following manner:

1. Disconnect the line cord, remove the four screws securing the CRT bezel to the front panel and remove the bezel.

2. Unplug the small connector on the front side of the module and carefully remove the CRT.

3. Unplug the PC edge connector at the right side of the A10 module.

4. Remove the two screws that secure the A10 module to the chassis and remove the module.

5. Place the PR-700 receiver on its left side and bring the PC edge connector out through the bottom of the receiver.

6. Remove the screws securing the module cover and remove the cover.

7. Plug the CRT into the module, connect the small (2) pin connector and PC edge connector.

8. Connect the line cord and turn the receiver on.

Set the front panel VERT GAIN control fully CCW. Adjust INTEN, FOCUS, VERT POS, HORIZ POS, for a sharp, sharp, clear, medium to low intensity

TABLE 5.9.1

The following voltages are taken with no signal input.

CRT - CAUTION - HIGH VOLTAGE

Pin	V1
1	0
2	-665 to -780
3	-685 to -800
4	-640 to -730
5	* 0 to +95
6	** +30 to +95
7	** +30 to +95

Pin	V1
8	---
9	0
10	---
11	*** +30 to +95
12	0
13	*** +30 to +95
14	0

* - varies with ASTIGMATISM control
** - varies with HORIZONTAL position control
*** - varies with VERTICAL position control

	E	B	C
Q6	-0.3	. 0.4	15
Q7	-0.7	.-0.3	30 to 95
Q8	-10.3	-9.73	-.7
Q9	-.7	-.3	30 to 95
Q10	-0.3	.0.3	15.0

	E	B	C
Q11	0	.50	15.0
Q12	-0.6	0	*** 30 to 95
Q13	-10.4	-9.77	-0.6
Q14	-0.6	0	*** 30 to 95
Q15	0	.0.6	12

*** - varies with VERTICAL position control

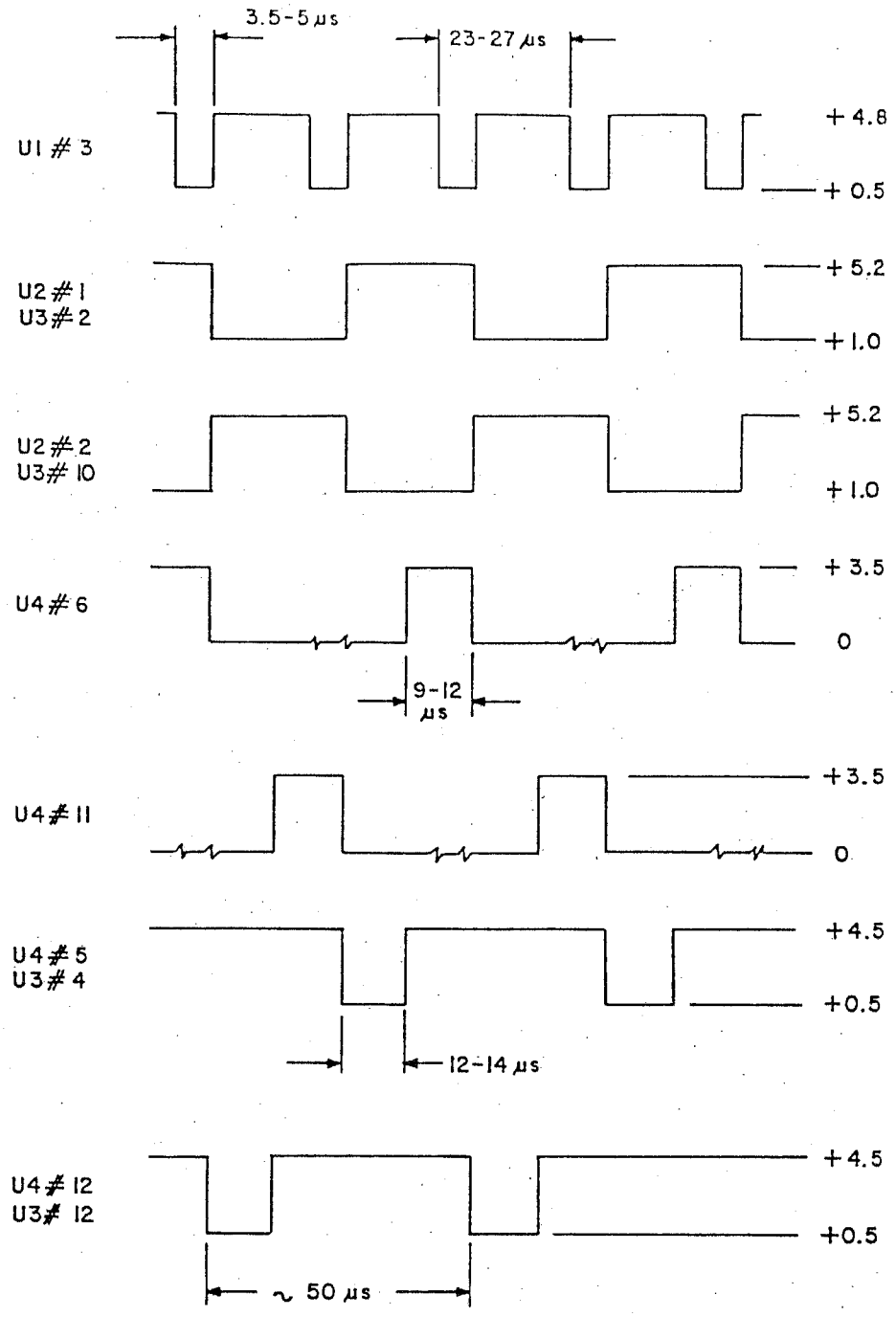


FIGURE 5.13

HIGH VOLTAGE POWER SUPPLY, A10B2

trace. Center the trace about 1/8 inch above the lower gradicule reference line.

Adjust R48 (TRACE ROTATION) for a trace parallel to the gradicule reference line. If the trace rotates in the wrong direction, reverse the two pin plug at the front of A10. Check the voltages per Table 5.9.1.

Inject a RF signal to the receiver to obtain a normal signal presentation on the scope. Adjust the FOCUS and ASTIG (R16) controls for a well defined display.

5.10 IF AMPLIFIER MAINTENANCE, A8B9

5.10.1 IF AMPLIFIER PRELIMINARY CHECK

If a problem is suspected in the IF amplifier chassis the following preliminary checks should be performed:

a. Connect a 160 MHz, 1000 Hz AM modulated signal source to the IF input J2.

b. Put the receiver in the V.S.mode, with IF GAIN control maximum, and then IF BW control at 20 MHz. A signal should be discernible at the W.B. AM output with an input level of approximately -80 dBm.

If the IF amplifier operates normally under the preceding conditions, a problem exists elsewhere in the receiver.

If the preceding test indicates a problem exists , align the IF amplifier as described in section 5.10.2.

5.10.2 IF AMPLIFIER ALIGNMENT

5.10.2.1 BLOCK DIAGRAM

Connect a sweep generator and step attenuator to the input of A8B1 as shown in Figure 5.10.2.1.

5.10.2.2 PRELIMINARY SETTINGS

1. IF GAIN ..... Fully CW
   MODE ..... V.S. (Scanwidth at 0)

2. Test Equipment Needed:

RF Detector (8471A, HP)
Sweep Generator (VS50, Texscan)
Signal Generator (608, HP)
Scope, Single Channel (544, Tektronix)
AC VTVM (400EL, HP)
Step Attenuator (0-50 dB Minimum)
Power Meter (460B, General Microwave)
Counter

3. The IF's bottom cover must be removed to perform test 5.10.2.4. It must be in place for the remainder of the test. The top cover is removed for alignment.

4. Refer to Schematic diagram 81R89-017 and component layout 81B89-304 for location of tuning and alignment controls.

5.10.2.3 AUXILIARY OUTPUT (J3)

1. Disconnect the RG-188 cable from J3 in the IF amplifier, connect a 50 ohms detector to it, and the detector output to the video input of the sweep generator.

2. Tune C1, C3, C6 and C16 for maximum symmetrical display around 160 MHz. Keep scope display below the equivalent of 0 dBm input to the detector being used. C1 and C3 should be trimmed for maximum bandwidth without reducing the level at center frequency.

3. Check 6 dB bandwidth; 24 MHz minimum.

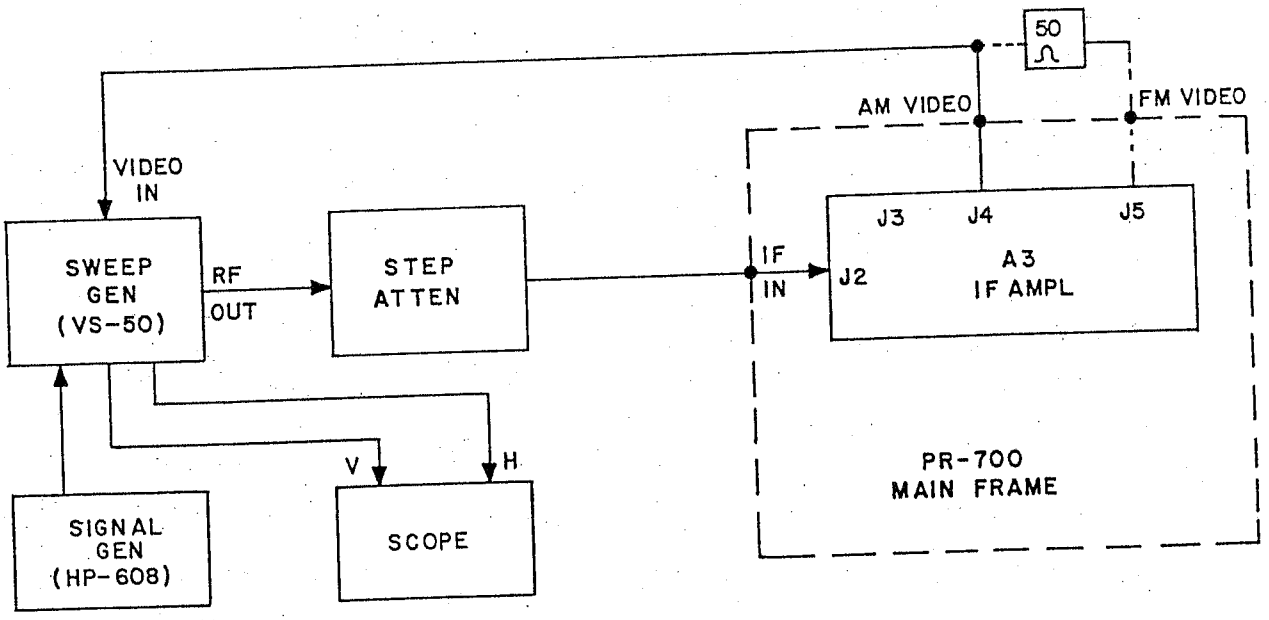

50
AM VIDEO
FM VIDEO
VIDEO
IN
SWEEP
GEN
(VS-50)
RF
OUT
STEP
ATTEN
IF
IN
J2
J3
J4
J5
A3
IF AMPL
PR-700
MAIN FRAME
V
H
SIGNAL
GEN
(HP-608)
SCOPE

FIG. 5.10.2.1

4. Check gain: 35 to 40 dB, by connecting the detector input directly to the step attenuator and measuring the increase in sweep level necessary to obtain in the scope the same DC level as the peak of the bandpass display.

5. Return all connections to the form shown in the block diagram, and reconnect the RG-188 cable to J3.

5.10.2.4 20 MHz AM VIDEO

1. Tune C26, C35, C42 and C46 for maximum symmetrical display around 160 MHz. A slight retune of C6 and C16 might be necessary. During this alignment adjust the sweep level as necessary to obtain a display of 4V peak; also adjust R155 as necessary to keep the display's baseline at or around 0 VDC.

2. Check 6 dB bandwidth: 16 to 24 MHz.

3. Connect the WB AM video output directly to the vertical input of the scope, and set the display's baseline to 0 VDC by adjusting R155.

4. Measure the input level necessary to obtain a 4V peak display: Limit: -80 to -84 dBm.

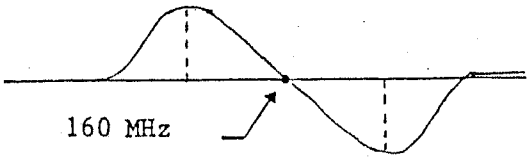
5. Return all connections to the form shown in the block diagram (Figure 5.10.2.1).

5.10.2.5 20 MHz FM VIDEO

1. Switch IF bandwidth to 20 MHz.

2. Connect the sweep's video input to the FM video output of the receiver, through a 50 ohms feedthrough termination.

3. With -80 dBm input, tune C163 and C167 for maximum symmetrical (S-curve) display around 160 MHz and 0 VDC. Adjust R185 as necessary to keep sweep's baseline at 0 VDC, as shown below:



FM DISPLAY

4. With -70 dBm input, tune C73 and C74 for maximum peak spacing, keeping the S-curve crossover with the baseline at 160 MHz. A slight retune of C67 might be necessary to make the display as linear as possible between peaks.

5. Check: (a) at -60 dBm, peak separation is 20 MHz minimum. (b) at -70 dBm, slope is 0.1V/MHz minimum. (c) at -80 dBm, peak-to-peak amplitude is 80 mv minimum.

5.10.3 IF AMPLIFIER MAINTENANCE

a. Check all interconnecting cables for tightness.

b. Remove the IF amplifier covers and measure the voltages under conditions described in Table 5.10.3.

c. Replace the faulty component. NO RE-ALIGNMENT SHOULD BE ATTEMPTED.

d. Replace the cover.

TABLE 5.10.3

IF AMPLIFIER DC VOLTAGES AT TRANSISTOR AND INTEGRATED CIRCUIT PINS

Preliminary Settings:

IF GAIN - FULLY CW
MODE - V.S. (VS Width at 0)
NO SIGNAL INPUT

PIN	Q1	Q2	Q3	Q4	Q5	Q6
E	-8.9	-8.5	-8.2	-8.6	-8.7	-8.8
B	-8.2	-7.8	-7.5	-7.9	-8.0	-8.1
C	0*	0*	0*	0*	0*	0*

PIN	Q7	Q11	Q12	Q13	Q14	Q15
E	+12	0	-8.8	-8.8	-8.9	+12
B	+11.3	+0.6	-8.1	-8.1	-8.1	+11.4
C	+0.6	+12	-4.3	0*	0*	0

PIN	#1	#2	#3	#4	#5	#6
U1	-0.3	-9.3	-12	-10	-0.3	+12
U2	-1.4	-0.7	-0.6	-1.4	+12	0

PIN	#7	#8	#9	#10	#11	#12
U1	-4.1	+11.4	---	---	---	---
U2	-0.6	+12	0	0*	+11.4	+11.4

NOTE: Tolerance: $\pm$5% or $\pm$0.2V DC, whichever is greater
(*) No Tolerance

5.11 DVM/METER AMPLIFIER, A1B1A1

Refer to schematic diagram 81D111-011 and component layout 81A111-364.

The A1B1A1 module can be broken down into 2 major sections. The first consisting of U1 and U2 which take the subcarrier tuning voltage or the S meter voltage and convert it to a 0-999 mV voltage for the second section which is a 0-1 volt A/D converter.

If neither the "S meter" or the SC tune affect the digital display a problem probably exists in the A/D converter section. Checkout can be accomplished per section 5.11.3. If only the SC receiver section appears inoperative checkout should proceed per section 5.11.1. If only the "S meter" appears inoperative proceed with section 5.11.2.

5.11.1 SC RECEIVER CHECKOUT

Set the receiver to the SC FM Mode and the SC tuning to approximately the center of its range. Check the voltages per Table 5.11.1.

5.11.2 S METER CHECKOUT

Set the receiver to SC Off, Band to Band 1 (0-10 MHz) and tune the receiver to 0000.0000 MHz. Check the voltages per Table 5.11.2.

5.11.3 A/D CONVERTER CHECKOUT

Set the receiver to SC FM Mode and tune SC TUNE control to approximately midrange.

The voltage at pin 3 of U2 should be approximately 200 mVDC, and the Front Panel display should read 200. If it does not, proceed as follows.

1. Check for -5V at U4 pins 15 and 3.
2. Check for 20 VDC at U4 Pin 2.
3. Check U4 pin 4 for -.26 VDC and U4 pin 16 for -.96 VDC.
4. Check U8-17 for 200 mVDC.
5. With an oscilloscope check waveforms per Figure 5.11.3 on page 5-19.

5.12 AUDIO ASSEMBLY, A1B1A3

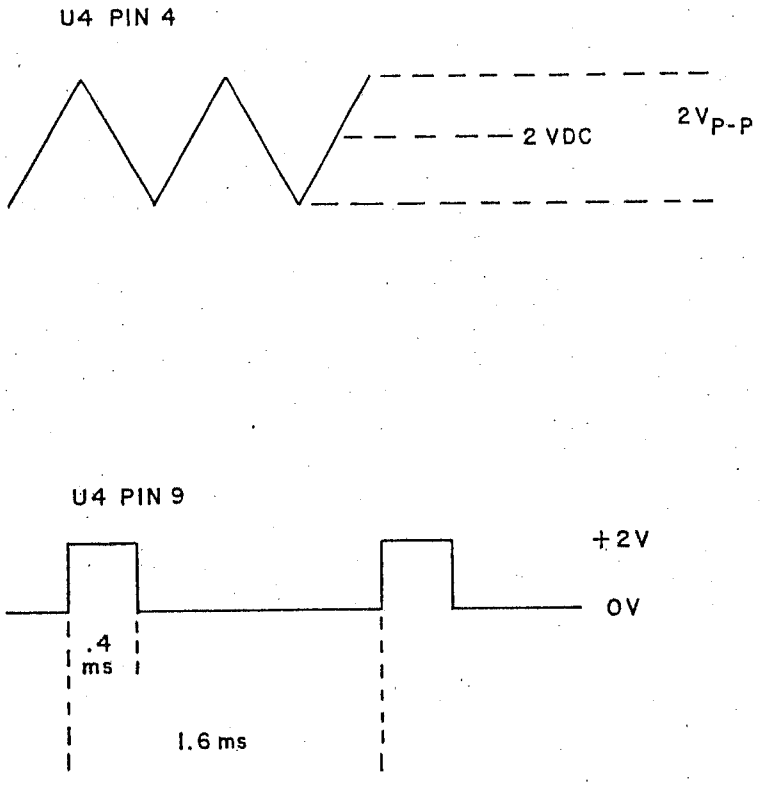
Refer to schematic diagram 81A113-026-1 and component layout 81A113-359.

The A1B1A3 module is a single chip Audio Amplifier circuit which takes the chosen audio and amplifies it to the proper levels to drive a 600 ohms headset.

A problem probably exists in this module if there is no audio output in any demodulation mode but there is audio present on any of the narrowband (BNC) outputs when viewed with an oscilloscope. The audio amplifier can be checked by tuning the receiver to a known signal (using the proper de-mod) and checking the signal on E1 (with the front panel audio control at midrange) for approximately .075 V-p-p. The output (E4) should approximately 2 V-p-p with a 600 ohms headset connected to the audio output jack.

5.13 LOW FREQUENCY SYNTHESIZER A4

Refer to Figure 5.13. The Low Frequency Synthesizer consists of a



AIBIAI, A/D CONVERTER WAVEFORMS

FIGURE 5.11.3

TABLE 5.11.1

J1 Pin 1	11.99 VDC
J1 Pin 2	-5 VDC
J1 Pin 4	200 mVDC
U2 Pin 3	200 mVDC

TABLE 5.11.2

J1 Pin 5	+5 VDC
J1 Pin 6	2.1 VDC
U2 Pin 1	.61
U2 Pin 10	-.26
U2 Pin 30	* .61

* NOTE: If this voltage is correct proceed to section 5.11.3.

TABLE 5.13

PR-700	OUTPUT FREQUENCY			
FREQUENCY (MHz)	A4B1	A4B2	A4B3	A4B4
0000.0000	200.00 kHz	200.00 kHz	45.00000 MHz	45.00000 MHz
10.000	200 kHz	200 kHz	55.000 MHz	55.000 MHz

series of phase locked loops which are summed to obtain the desired frequency resolution. Each phase locked loop functions basically in the same manner. Primarily the operation is a series of independent functions operated in such a manner as to form a closed loop system. Table 5.13 identifies the basic blocks and operating frequencies.

5.13.1 OSCILLATOR

Two techniques of repairing such a system are:

1. Opening the loop and monitoring the operation of the independent sections.

2. Monitoring signals at certain points within the loop while operating in a closed-loop mode.

Normally the loop would be evaluated in the closed loop configuration and the loop would be opened and tested as a last resort.

The following procedure will cover repair of a low frequency synthesizer using the monitoring of specific test points in a closed loop system.

5.13.2 DIVIDE BY N PLL (A4B1)

The block diagram in Figure 5.13.2 shows the basic functions contained in the A4B1 Module.

The first step in repairing A4B1 is to verify that the power and input signals are correct. Reference schematic diagram 81R41-020-1 for the following discussion.

Remove the 15 pin D connector and verify +5 VDC on pin 13. Measure the voltages on pins 1-8, and verify that all voltages meet the level requirements of TTL signals. Insure that a 100 kHz TTL level signal is present at A4B1-J2.

Open the A4B1 module.

Utilizing an oscilloscope, monitor the signal on pin 3 of U2 (MC4044). A 100 kHz signal should be present if the loop is operating correctly. If no signal is present a problem probably exists within the divide-by-N-circuitry or the signal source to the divide-by-N.

If a signal is present at the correct frequency and the signal is stable, the loop is probably phase locked. This can be verified by measuring the frequency of the signal at pin 3 of U8 (MC 10116).

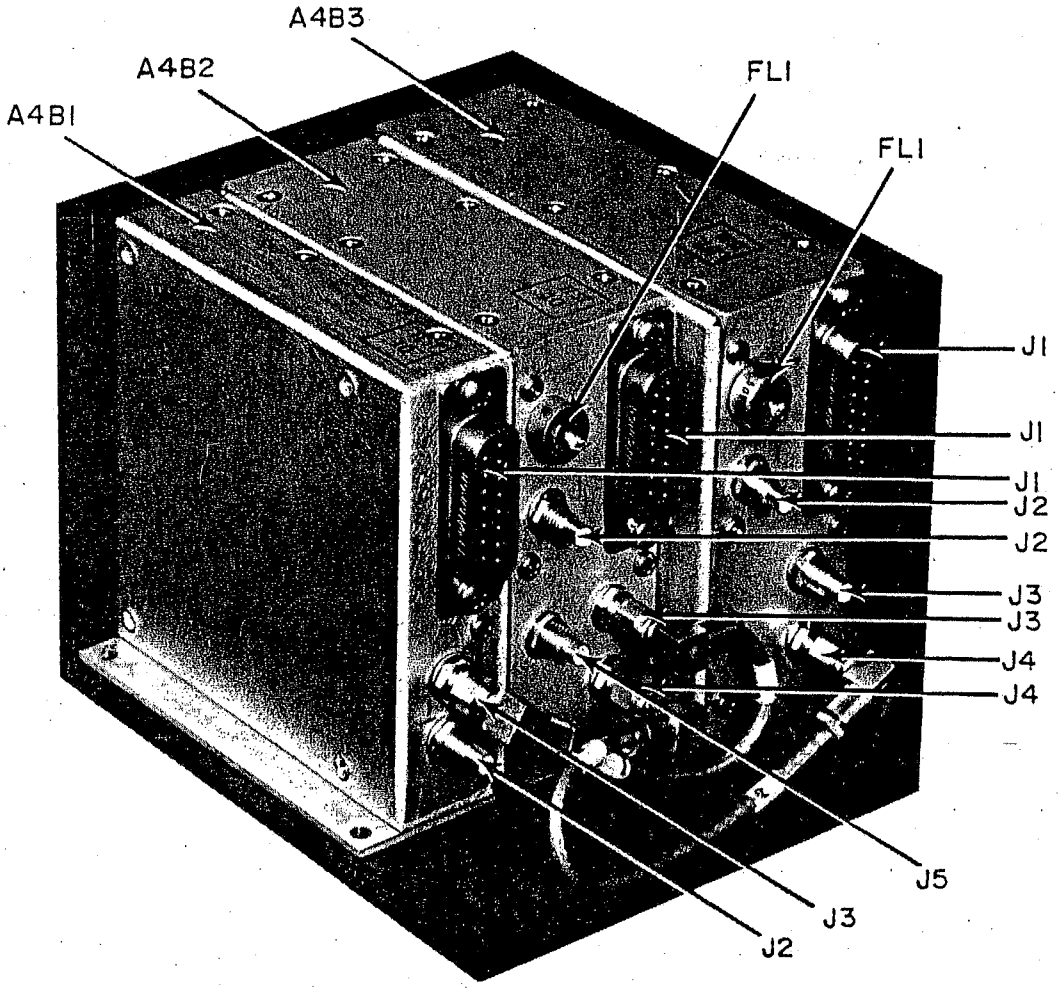
If the signal at pin 3 of U2 (MC4044) is not 100 kHz, measure the DC voltage at pin 8 of U2. If the frequency at pin 3 of U2 was higher than 100 kHz the voltage should be $\leq$2.0V. If the frequency was lower than 100 kHz the voltage should be $\geq$4V. If these conditions exist the phase detector circuitry is probably functioning correctly and the problem is after the phase detector.

Proper VCO operation can be verified easily by measuring the voltage across the tuning varactor and comparing the actual frequency of the oscillator vs the approximate frequency at which the VCO should be operating.

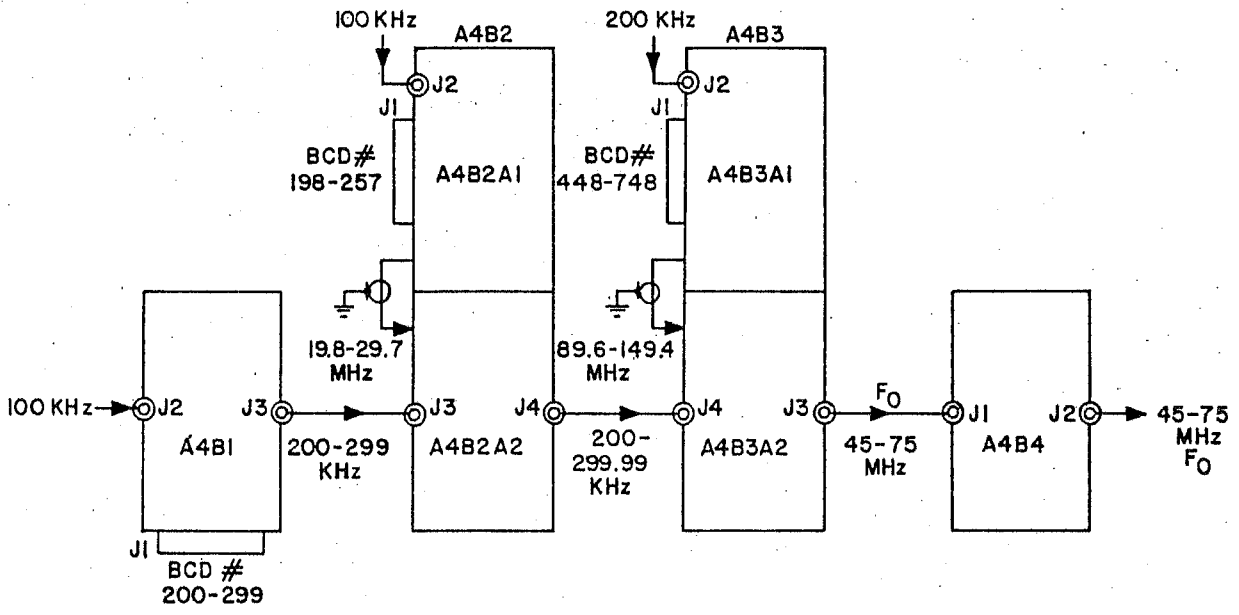
The remaining independent function within the loop is the divide-by-N circuitry. This block consists of U3, U4, U5, U6 and U7. To isolate a loop problem to the divide by-N circuitry, monitor the frequency at the input to the divide-by-N and the output. The frequencies are related as follows:

$$f\ out = \frac{fin}{200+N}$$

If the divide-by-N has failed, determine that the digital signal



A4B1, A4B2, A4B3



$$10\,N + 1000\,T + 1 \times 10^5\,M = F_O$$

N = 200-299
T = 198-297
M = 448-748

A4, INTERCONNECTION DIAGRAM
LOW FREQUENCY SYNTHESIZER

FIGURE 5.13

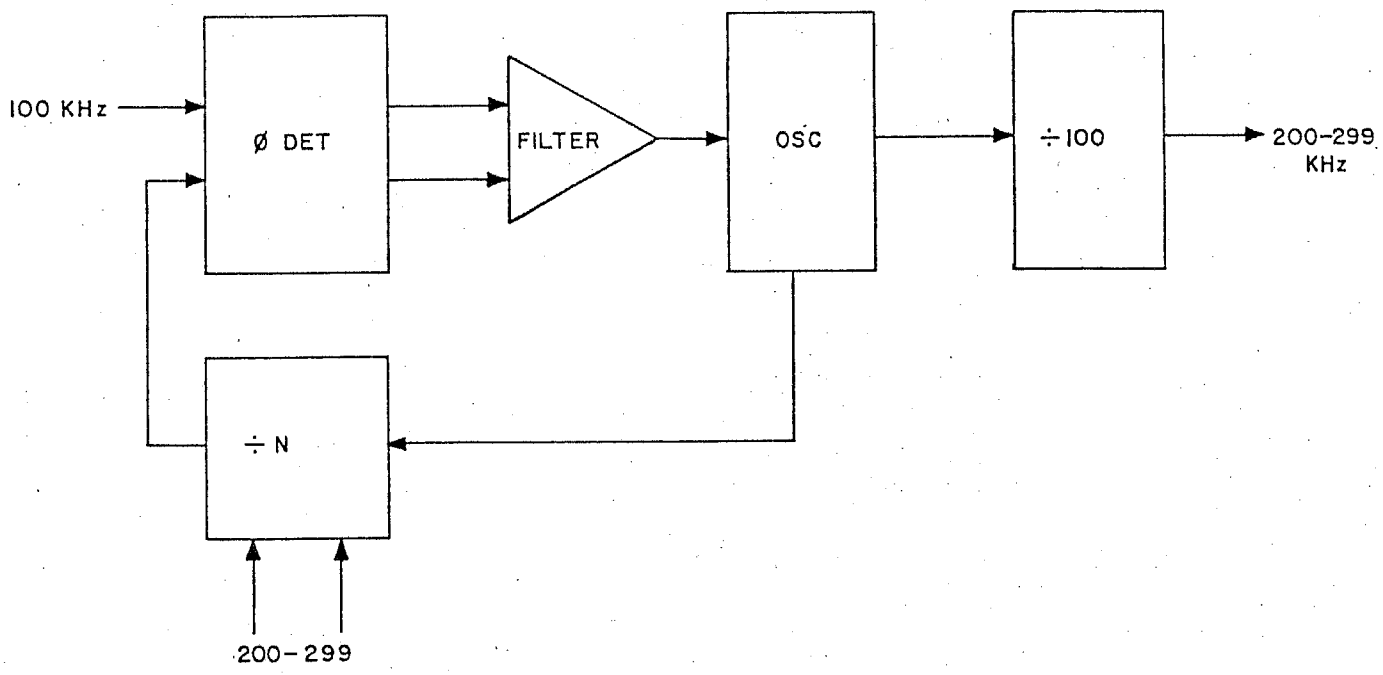


FIGURE 5.13.2 – A4B1 BLOCK DIAGRAM

N= 200 + (0 TO 99)

F_O = FREQUENCY OUTPUT

R= REFERENCE FREQUENCY

$F_O = \frac{NR}{100}$ Hz

levels are correct at the various points within the divide-by-N. The input to the divide-by-N is an ECL signal (≃.8V peak-to-peak) at pin 16 of U4 (SP8690). The SP8690 is a variable modulus prescaler which divides by either 10 or 11 dependent upon the TTL signal present at pin 7 of U3. The U4 output is a TTL level present at pin 11.

U5, U6 and U7 are presettable down counters (TTL) with BCD outputs. These devices are preset by pulling pin 11 low. This preset pulse is also the output from the divide-by-N and thus it is a short negative going signal ideally at a 100 kHz repetition rate when the loop is "locked".

U9 is a divide-by-100 Counter. Measure the TTL level signal at pin 1 of U9. The signal at pin 1 of U9 is a 20-29.9 MHz TTL level signal. The output signal on pin 13 of U9 is 200-299 kHz.

5.13.3 DIVIDE BY T & SUMMING LOOP A4B2

This module has two printed circuit boards. The first (A4B2A1) accepts digital data representing the 10 kHz and 100 kHz digit and a 100 kHz reference to generate a signal ranging from 19.8 to 29.7 MHz. The second board (A4B2A2) sums the 200-299 kHz from A4B1 and the signal generated on the A4B2A1 board. Once summed, the resulting 20.0 to 29.999 MHz is divided by 100 to result in a 200 to 299.99 kHz signal.

5.13.4 DIVIDE BY T PLL A4B2A1

This printed circuit board is identical to A4B1 with the exception that the output is not divided as in the A4B1 module. Refer to 5.13.2 to test and repair A4B2A1.

5.13.5 SUMMING LOOP A4B2A2

The function of the summing loop is to add the 200-299 kHz signal from A4B1 to the 19.8-29.7 MHz signal from A4B2A1. The signal is then divided by 100 to obtain a signal from 200.00 kHz to 299.99 kHz.

U4, U5, Q3 and U7 are not in the phase locked loop. U4 and U5 are used to guarantee that the oscillator will never be lower in frequency than the frequency originating on A4B2A1 and connecting to A4B2A2 at pin 6 of U3 and pin 9 of U4.

The reference frequency for the phase locked loop is a TTL signal from the A4B1 module (200-299 kHz). When the loop is locked, the TTL signal on pin 3 of U1 will be the same frequency as the signal on pin 1.

After verifying that the power supply voltages are correct, use an oscilloscope to monitor the signal on pin 3 of U1. The signal must be a TTL level signal. If the frequency on pin 3 is greater than the reference frequency on pin 1, the voltage on pin 8 should be less than 2 volts. Conversely, if the pin 3 signal frequency is lower than the reference frequency, the pin 8 voltage should be greater than 4 volts.

The oscillator can be tested simply by measuring the voltage on pin 8 of U1 and monitoring the frequency of the oscillator (U2). The oscillator should be relatively linear from ≃ 20.0 MHz at 2 VDC to 29.9 MHz at 4 VDC.

U6 is a buffer and signal splitter. Pin 14 of U6 should be an ECL signal at the same frequency as the oscillator. Q3 is an amplifier to interface the ECL output from U6 to the TTL signal required at pin 1 of U7.

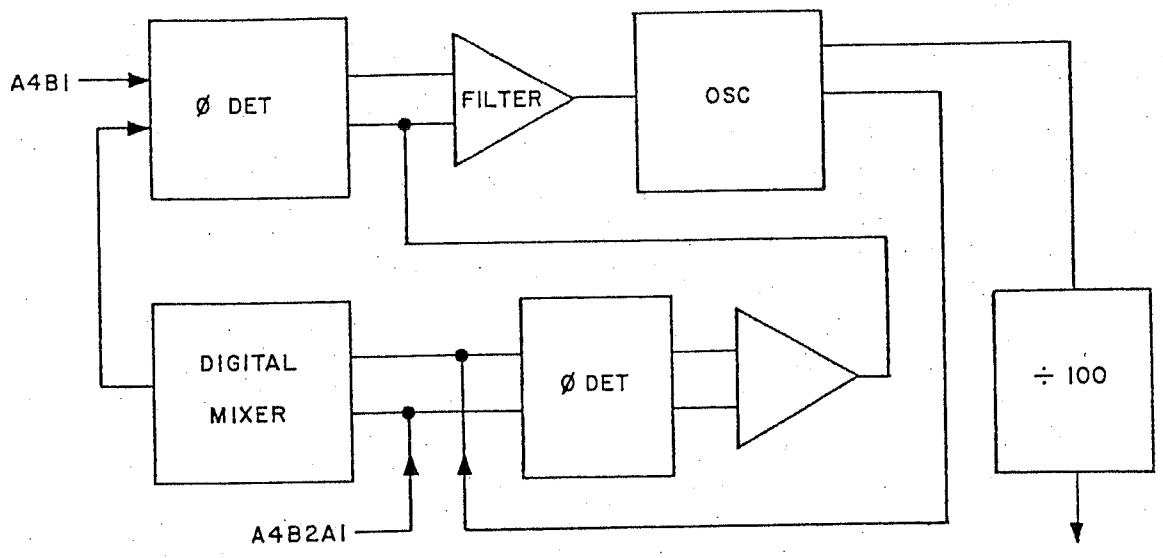


FIGURE 5.13.5-A4B2A2 BLOCK DIAGRAM

U3 pin 6 and 7 should each have an ECL signal present with the signal on pin 7 higher in frequency than pin 6 of U3. The signal on the collector of Q2 is a TTL signal equivalent to the difference between pin 7 and pin 6.

The U5 output is low only when the oscillator is lower in frequency than the output from A4B2A1. When U5 goes low it forces the voltage on pin 8 of U1 to go high, Which forces the oscillator frequency to go higher in frequency than A4B2A1. The U5 output should then go to a high voltage, which back biases D2 and D3.

5.13.6 DIVIDE BY M & SUMMING LOOP (A4B3)

The A4B3 module contains two printed circuit boards. The A4B3A1 multiplies the reference frequency by using a programmable divider in the feedback loop.

The A4B3A2 module sums the A4B2 output signal and the A4B3A1 signal divided by two, in order to obtain the resulting 45-75 MHz signal.

The technique described in this section is to monitor certain points within the active phase locked loop to identify the problem to a specific section.

5.13.7 DIVIDE BY M PLL (A4B3A1)

Refer to schematic diagram 81R43-019-1 for the following discussion.

Verify that the +5V, +15V, and -15V supply voltages are present on the PC board.

Verify a 200 kHz TTL signal on pin 1 of U1, the phase detector. This signal is the reference frequency and should never change or vary. Use an oscilloscope to monitor the signal on pin 3 of U1. If the TTL signal on pin 3 is higher in frequency than 200 kHz, pin 12 of U1 will be low, pin 13 will be high and pin 2 will be a switching signal. Pin 6 of U3 should be less than 2 volts. If the frequency of the signal on pin 3 of the phase detector is less than 200 kHz, the conditions on pin 6 of U3 and pins 13 and 2 of U1 will reverse, while pin 12 will still be low. As soon as pin 12 goes to a low state, U2, Q1, and Q2 change state, which in turn switches out the passive filter consisting of R12, R14, R15, C13 and R18. The passive filter circuit can be disabled while repairing the remainder of the phase locked loop.

Again, if the frequency on pin 3 of U1 is higher than pin 1, the active filter output (pin 6 of U3) will be low. Pin 6 of U3 should be greater than 10 volts if pin 3 of U1 is higher in frequency than 200 kHz.

The oscillator frequency should follow the voltage on the output of U3, with the oscillator varying from 89.6 MHz to 149.4 MHz for voltages of ≈2.5 to 9 VDC. Q5 is a buffer and signal splitter.

The remaining circuitry consisting of U4, U5, U6, U7 and U8 make up the divide by M circuit. U5 is a variable ratio prescaler (divide by 10/divide by 11) with an ECL input on pin 16 and a TTL output on pin 11. The divide by M controller integrated circuit (U4) controls the ratio by controlling pin 2 of U5 which determines if U5 divides by 10 or 11. U6, U7, and U8 are presettable down counters. The counters are preset to a pre-determined number from the J1 connector when pin 11 goes to a low state. The signal from U5 is used as the clock and the counters count down to

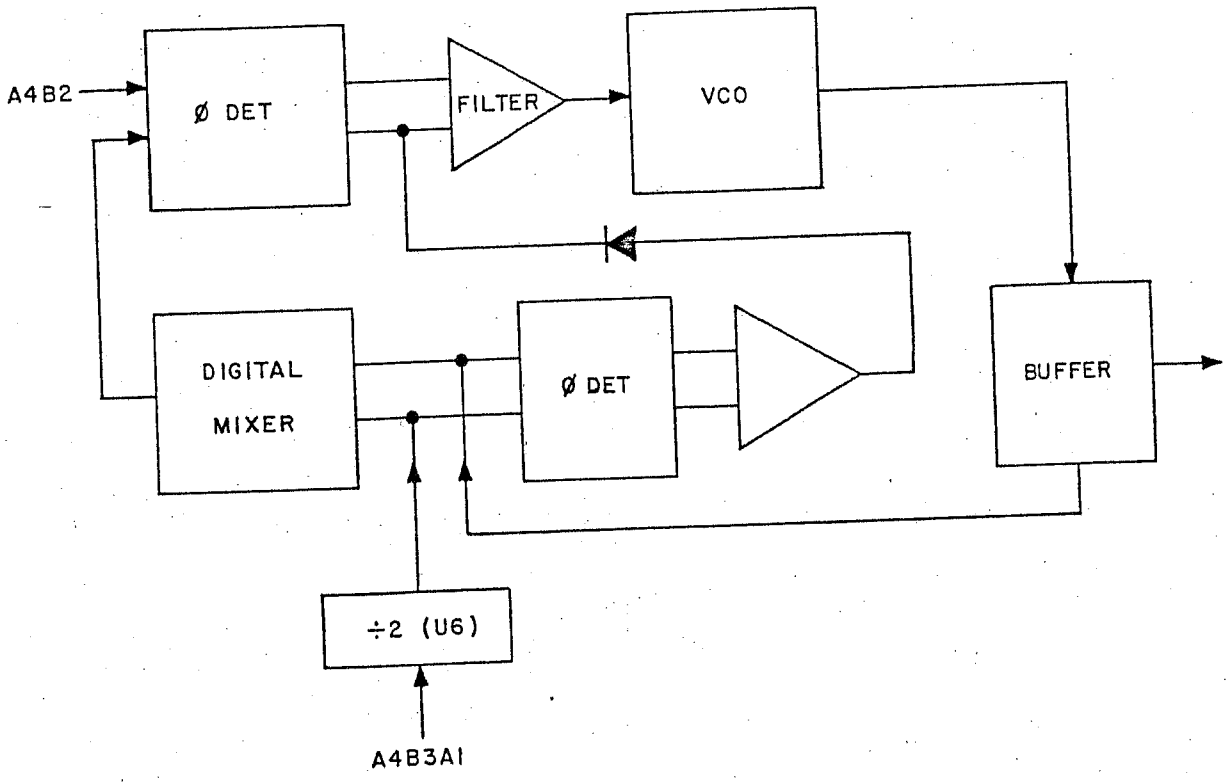


FIGURE 5.13.7-A4B3A2 BLOCK DIAGRAM

zero. U4 senses when the counters get to zero and provides a pulse to preset the counters again. This pulse is also the pulse to pin 3 of U1. U6, U7 and U8 can be tested by monitoring the 1, 2, 4, 8 time ratio as in any BCD counter. The data from J1 to the counters can vary from 398 to 597. The data signal levels should meet the requirements of a TTL level signal (Low $\leq$ .8 volts, High $\geq$ 2.4 volts.

5.13.8 SUMMING LOOP A4B3A2

The function of the summing loop is to add the output from the A4B2 module and the A4B3A1 board.

Repair of the module can be completed by testing individual sections within the closed loop.

First, verify that the power supply voltages are correct. Next, test the two input signals to the A4B3A2 printed circuit board. Verify a TTL signal on pin 1 of U1 between 200 kHz and 299.99 kHz. Next, monitor the ECL signal on pin 7 of U3, which is the signal from A4B3A1 divided by two. If this signal is correct, U6 is functioning correctly.

Once it has been established that all externally generated voltages and signals are present and correct, the various sections can be tested by observing the circuit response to the existing stimuli.

Observe the signal on pin 1 of U1 to insure the presence of the A4B2 TTL signal (200 kHz - 299.99 kHz). Measure the frequency of the TTL signal on pin 3 of U1 and compare it to the signal on pin 1 of U1. When the loop is phase locked, the two frequencies will be equal, and the phase detector and filter (U1 and U2) produce an output voltage on pin 6 of U2 between +2 volts and +10 volts. If the pin 3 frequency exceeds the pin 1 frequency, the voltage on pin 6 of U3 should be less than 2 volts. Conversely, the pin 6 voltage should be higher than 10 volts if the pin 3 frequency is lower than the pin 1 frequency.

The next stage to test is the oscillator Q2, which has relatively linear characteristics from 45-75 MHz for an approximate 3 to 11.75 volt input voltage. If the oscillator is not functioning, measure the voltage across R19 which is in the DUAL GATE MOS-FET Source. The voltage should be between .7 and 1.5 volts, dependent upon the individual FET characteristics. The Gate 2 voltage should be approximately 4 volts and the DRAIN should be approximately 13 volts.

The output from the A4B3 module at J3 should be approximately -5 dBm.

In the event that the output frequency is less than the frequency of the U6 output, check the U4, U5 and D7 circuitry. It is the function of this circuit to insure that the output of the A4B3A2 printed circuit board is higher than the U6 output. The U5 output goes to a high state only when the output frequency is too low. Thus the U5 output will normally be $\simeq$ -7.5 VDC.

U3 and Q3 mix the frequencies available on pins 6 and 7 of U3 and provide a TTL difference signal to pin 3 of U1. If this is not the case, test pin 2 of U3 and verify an ECL output to Q3.

5.13.9 45-75 MHz BUFFER PLL A4B4

The A4B4 module is a buffer phase locked loop used to eliminate unwanted spurious signals. Since there are only two integrated circuits and three transistors, operation and repair is relatively simple.

The unit can be tested very quickly by connecting a 0 dBm, 45-75 MHz signal to the J1 input and monitoring the output. The output should be exactly the same frequency as the input signal. Refer to schematic diagram 81C44-021 to assist in the following discussion.

To repair the unit, check the +5V, +15V and -15V inputs to the printed circuit board. Next, measure the ECL signals (≃ .8V peak-to-peak) on pins 6 and 9 of U1. When phase locked the frequencies will be equal. When the frequency on pin 9 of U1 exceeds the frequency of the pin 6 signal the filter output (U6) should be greater than 10 volts. The U6 output should be less than 2 volts if the opposite condition exists.

The voltage controlled oscillator (VCO) can be tested simply by measuring the frequency and comparing it to the voltage on pin 6 of U2. The frequency should vary from 45-75 MHz for a 3-12V potential on pin 6 of U2. The loop can be opened and the VCO tested independently by lifting the U2 side of L1 and applying a positive potential to the open end of the inductor. The VCO should be approximately linear.

If the VCO is not operating, check Q1 source current by measuring a .7 to 1.5 volt potential across R17. Gate 2 voltage should be approximately 4 volts.

Q2 and Q3 are buffer amplifiers and can be tested as simple amplifiers.

5.14 470-2000 MHz AMP/SWITCH, A8B3

Refer to schematic diagram 81B83-030 and component layout 81A83-346.

The A8B3 module contains a PIN diode switch (Z1), which selects between inputs J1 and J2, plus two modular amplifiers (Z2 & Z3).

The module can be checked for proper operation in the following manner:

1. Set the receiver to band 6 (470-1000 MHz).
2. Check if +15 VDC is present on FL-1.
3. Disconnect the coax on input Jack J1 and inject a 470 MHz signal at -50 dBm into J1.
4. With a spectrum analyzer check that the output at J3 at 470 MHz is approximately -30 dBm.
5. Set the receiver to BAND 3 (30-50 MHz).
6. Check to if +15 VDC is present on FL-2.
7. Disconnect the coax cable at J2 and inject a 30 MHz signal at -50 dBm into J2.
8. Check the output at J3 for a -30 dB signal at 685 MHz.

5.15 30-470 MHz AMP/SWITCH/MIXER, A8B4

Refer to schematic diagram 81B84-031 and component layout 81A84-347.

The A8B4 module contains a modular amplifier and a mixer and can be checked in the following manner:

1. Set the receiver front panel controls as follows:

BAND	50-150 MHz
MODE	Synthesize
FREQ	85 MHz

2. Check for the following voltages:

FL-1	+15 VDc
FL-2	+1.52 VDC

3. Disconnect hard coax on J1 and connect a signal generator set at 80 MHz, -30 dBm to J1.

4. Check the output at J4 with a spectrum analyzer for 685 MHz at -22 dBm.

5. Set the receiver front panel controls as follows:

BAND	30-50 MHz
MODE	Synthesize
FREQ	35 MHz

6. Check the voltages on:

FL-1	.17 VDC
FL-2	15 VDC

7. Check for 685 MHz with spectrum analyzer at J4 at -28 dBm.

8. If the 685 MHz is not present first check to see that 720 MHz at +14 dBm is present at the input to J3. If it is, the problem is in A8B4. If not, check the YIG oscillator output and pin diode switch Z10.

5.16 1-2 GHz AMPLIFIER, A8B5

Refer to schematic diagram 81A85-050 and component layout 81A85-348.

The A8B5 module is a modular amplifier (U1) with approximately 9 dB of gain from 1 to 2.1 GHz.

The A8B5 module can be checked in the following manner:

1. Remove coax on J1 and insert a signal in the range of 1-2.1 GHz into J1 at -40 dBm.

2. Set the receiver to band 7 (1-2 GHz) and check for +15 VDC on FL-1.

3. Remove the coax on J2 and connect the spectrum analyzer to J2.

4. Check for a signal at the same frequency as the input frequency above and at a level of -31 dBm $\pm$2 dB.

5.17 LO SWITCH/MIXER, A8B6

Refer to schematic diagram 81B86-032 and component layout 81A86-349.

The A8B6 module consists of two pin diode switch modules (Z1 and Z2) to select between the 3 inputs (J1, J2 and J3) and a double balanced mixer (Z3) for conversion to the 165 MHz center frequency IF output.

This module can be checked in the following manner:

1. Set the receiver to band 3 (30-50 MHz), tune to 30 MHz in the synthesize mode and check for +15 VDC at FL-3.

2. Inject a -30 dBm 685 MHz signal into J5.

3. With a spectrum analyzer check for a -40 dBm signal at 165 MHz out of J4.

4. If this signal is not present, check for a +7 dBm $\pm$3 dB signal at 520 MHz on the cable that connects to J3. If this signal is present, the problem is in the A8B6 module. If it is not, check the A8B16 and A8B11 modules.

5. Set the receiver to band 6 (470-1000 MHz),tune to 470 MHz and check for +15 VDC at FL-2.

6. Inject a -30 dBm 475 MHz signal into J5.

7. With a spectrum analyzer check for a 165 MHz signal at -38 dBm at J4.

8. If the signal is not present check for a +14 dBm signal at 640 MHz going into J2. If this 640 MHz signal is present the problem is in the A8B6 module. If it is not, check Z2, Z10 and A8B17.

9. Set the receiver to band 7 (1-2 GHz),tune to 1000 MHz and check for -15 VDC at FL-1.

10. Inject a -30 dBm 1005 MHz signal into J5.

11. Check for a -40 dBm signal at 165 MHz out of J4.

12. If the signal is not present check for a +10 dBm 1170 MHz signal at J1. If this signal is present the problem is in the A8B6 module, if it is not check Z2, Z10, Z5 and A8B17.

5.18 160 MHz DIVIDER/MIXER/LPF, A8B7

Refer to schematic diagram 81B86-032 and component layout 81A86-349.

The A8B7 module consists of a power divider (Z1), a 1-500 MHz amplifier (U1) and a mixer (Z2).

The module can be checked in the following manner:

a. Set the receiver to SYNTH mode, Band 3 (30-50 MHz).

b. Check for +15 VDC at FL-1.

c. Inject a 165 MHz -30 dBm signal into J2.

d. Check for a 15 MHz signal out of J4 at approximately -25 dBm. If this signal is present the module is operating correctly. If it is not check for the 180 MHz local oscillator at approximately +7 dBm at J1.

e. Check the 165 MHz output from J3 at approximately -33 dBm.

5.19 YIG CONTROLLER, A8B8

Refer to schematic diagram 81B88-023 and component layout 81A88-351.

The YIG controller PC board has 2 separate YIG driver circuits (U1 and U2 for the YIG oscillator) and (U3 and U4 for the YIG preselector).

The easiest method to determine if the oscillator YIG driver circuit is operating correctly is to measure the voltages at E1 and E3. E1 should be equal to E3 and between 2 (band 7 low end) and 7 volts (band 6 high end).

For the YIG preselector measure the voltages at E4 and E8. E4 should be equal to E8 and be between .02 (band 6 low end) and 11 volts (band 7 high end). If these voltages are correct the YIG controller is operating correctly.

If the oscillator section is incorrect proceed by measuring the voltage at U1 pin 6. It should be approximately .25-.5 volts higher than the voltage at E1. Then check the voltage at U2 pin 11 which should be the same as U1 pin 6.

The preselector section can be

checked in the same manner by measuring the voltage at U3 pin 6 which should be between .2 and .7 volts higher than E4. The voltage at U4 pin 11 should be equal to U3 pin 6.

5.20 REFERENCE OSCILLATOR, A9

Refer to schematic diagram 81R90-013-1 and component layouts 81A91-158, 81A92-159, 81A93-160.

5.20.1 TCXO, A9B1

The A9B1 section consists of a 5 MHz temperature compensated crystal oscillator (Z1), a 5 volt regulator (U1), a data selector integrated circuit (U2) and a dual divide by ten integrated circuit (U3). The 5 volt regulator can be checked in the following manner:

1. Check for +12 VDC at E1.
2. Check for approximately 9.3 VDC at U1 pin 1.
3. Check for 5 VDC at U1 pin 2.

The 5 MHz TCXO can be checked by checking the output (Z1 pin 3) for a TTL level 5 MHz signal.

The data selector can be checked by checking for a 5 MHz TTL level signal at U2 pin 6 or J3.

The divide by 100 integrated circuit U3 can be checked by looking for TTL level outputs at the locations specified in Table 5.20.1.

5.20.1 10.7 MHz PHASE LOCK LOOP, A9B2

The first step in repairing A9B2 is to verify that the power and input signals are correct. Verify +5 VDC on U1 pin 14. Insure that a 100 kHz TTL level signal is present at U1 Pin 1.

Utilizing an oscilloscope, monitor the signal on pin 3 of U1 (MC4044). A 100 kHz signal should be present if the loop is operating correctly. If no signal is present a problem probably exists within the divide-by-107-circuitry or the signal source to the divide-by-107, as described below.

If a signal is present at the correct freqency and the signal is stable, the loop is probably phase locked. This can be verified by measuring the frequency of the signal at J6.

If the signal at pin 3 of U1 (MC4044) is not 100 kHz, measure the DC voltage at pin 8. If the frequency at pin 3 of U1 was higher than 100 kHz the voltage should be $\leq$2.0V. If the frequency was lower than 100 kHz the voltage should be $\geq$4V. If these conditions tions exist the phase detector circuitry is probably functioning correctly and the problem is after the phase detector.

Proper VCO operation can be verified by measuring the voltage across the tuning varactor D2 (between 3 and 4 VDC) and checking for a 10.7 MHz signal at to be collector of Q5.

The remaining independent function within the loop is the divide-by-107 circuitry. This block consists of U2, U3, and U4. Testing to isolate the loop problem to the divide-by-107 is done by monitoring the frequency at the input to the divide-by-107 and the output.

If the divide-by-107 has failed, determine that the digital signal

TABLE 5.20.1

OUTPUT JACK	OUTPUT FREQUENCY
J3	5 MHz
J4	200 kHz
J1	100 kHz
J2	500 kHz

levels are correct at the various points within the divide-by-107. The input to the divide-by-107 is a TTL signal at pin 1 of U2, at a frequency of 10.7 MHz.

U3 and U4 are presettable down counters (TTL) with BCD outputs. These devices are preset by pulling pin 11 low. This preset pulse is also the output from the divide-by-107 and thus it is a short negative going signal ideally at a 100 kHz repetition rate when the loop is "locked".

5.20.3 55.7 MHz PLL (A9B3)

Verify that the +5V, +15V, and -15V supply voltages are present on the PC board.

Verify a 200 kHz TTL signal on pin 1 of U1, the phase detector. This signal is the reference frequency and should never change or vary. Use an oscilloscope to monitor the signal on pin 3 of U1. If the TTL signal on pin 3 is higher in frequency than 200 kHz, pin 13 of U1 will be high and pin 2 will be a switching signal. Pin 6 of U2 should be less than 2 volts. If the frequency of the signal on pin 3 of the phase detector is less than 200 kHz, the conditions on pin 6 of U2 and pins 13 and 2 of U1 will reverse.

The oscillator frequency as measured at the collector of Q2 should follow the voltage on the output of U2, with the oscillator frequency being 111.4 MHz when in Lock. Q2 is a buffer and signal splitter.

The remaining circuitry consisting of U3, U4, U5, U6 and U7 make up the divide-by-557 circuit. U4 is a variable ratio prescaler (divide by 10/divide by 11) with an ECL input on pin 16 and a TTL output on pin 11. The divide-by-557 controller integrated circuit (U3) controls the ratio by controlling pin 2 of U4 which determines if ;U4 divides by 10 or 11. U5, U6, and U7 are presettable down counters. The counters are preset to a pre-determined number by pins 1,9,10 and 15, when pin 11 goes to a low state. The signal from U4 is used as the clock and the counters count down to zero. U3 senses when the counters get to zero and provides a pulse to preset the counters again. This pulse is also the pulse to pin 3 of U1. U5, U6 and U7 can be tested by monitoring the 1, 2, 4, and 8 time ratio as in any BCD counter. The data signal levels should meet the requirements of a TTL level signal (Low $\leq$.8 volts, High $\geq$2.4 volts).

5.21 IF (A3B1)

Refer to schematic diagram 81R31-047 for S/N's below 175 or 81R31-047-1 for S/N's 175 and up.

The A3B1 IF provides for all the demodulation outputs (AM, FM, CW, SSB) in 4 selectable bandwidths (3, 15, 150 kHz and 2 MHz). The IF can be divided into distinct sections as in simplified block diagram Figure A. Check out of the IF requires carefully removing the IF from the receiver and reconnecting the IF to the receiver with extender cables and removing the IF top and bottom covers.

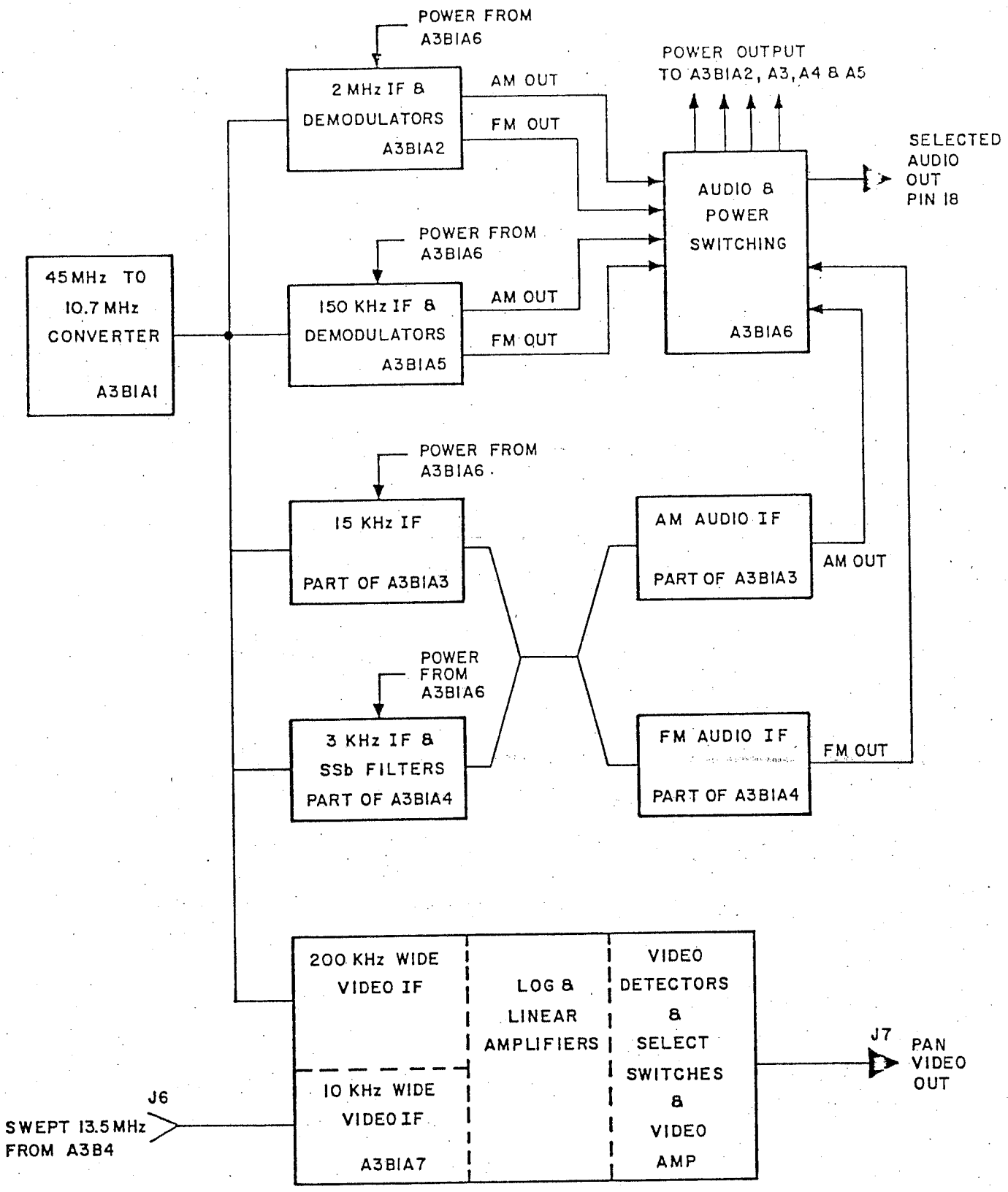
5.21.1 45 MHz to 10.7 MHz COVERTER, (A3B1A1)

Refer to component layout 81A311-332.

This section of the IF can be checked as follows:

a. with an oscilloscope check for the presence of 55.7 MHz at the base and collector of Q1, with levels of 0.2 and 1.25 V-p-p respectively.

b. Remove the cable connected to J1



PR700
FIGURE A
A3BI IF SIMPLIFIED BLOCK DIAGRAM

and inject a 45 MHz CW signal at -20 dBm and measure the 45 MHz peak to peak voltage at T1 pin 1 (.13 V-p-p).

c. Check voltage at C1, .15 V-p-p. If this voltage is correct then A3B1A1 is operating properly, if not check U1 as listed in Table 5.21.1.

5.21.2 2 MHz IF, A3B1A2

Refer to component layout 81A312-333.

Set the receiver front panel controls as follows:

Mode - SYNTH
Demod - AM
Bandwidth - 2 MHz

Section A3B1A2 can be checked as follows:

a. With the 45 MHz still connected to J1 and modulated with 50% AM and -40 dBm level, check with an oscilloscope the AM output at U3 pin 1 for .2 V-p-p.

b. Turn AM modulation off and FM modulate the 45 MHz signal with close to 500 kHz deviation. Check the FM output at U6 pin 6 with the oscilloscope for 1.5 V-p-p.

If both of the above are correct the A3B1A2 section is operation correctly. If not proceed as follows:

a. Measure the DC voltages on Q2:

Pin 1	+11.2 $\pm$ .3 VDC
Pin 2	+9.2 $\pm$ .3 VDC
Pin 3	+2.5 $\pm$ .3 VDC
Pin 4	+.4 $\pm$ .2 VDC

b. Check with an oscilloscope the points as listed in Table 5.21.2.

5.21.3 150 kHz IF, A3B1A5

Refer to component layout 81B315-336.

Set the receiver front panel controls as follows:

Mode - SYNTH
Demod - AM
Bandwidth - 150 kHz

Section A3B1A5 can be checked as follows:

a. With a 45 MHz signal input to J1,50% AM modulated and -40 dBm level, check the AM output at U9 pin 4 for approximately .2 V-p-p.

b. Change the modulation to FM, with 50 kHz deviation, and check the FM output at U11 pin 6 for approximately .4 V-p-p.

If both of the above are correct the A3B1A5 section is operating correctly. If not proceed as follows:

a. Measure the DC voltages on Q3 and Q4 per Table 5.21.3.

b. Check with an oscilloscope the points as listed in Table 5.21.3. A.

5.21.4 15 kHz IF, A3B1A3 & A3B1A4

Refer to component layout 81A313-334 and 81B314-335.

Set the receiver front panel controls as follows:

Mode - SYNTH
Demod - AM
Bandwidth - 15 kHz

TABLE 5.21.1

U1 PIN	WAVEFORM PEAK TO PEAK VOLTS	DC VOLTS
1,7	1.5 V-p-p 57 MHz	0
2,6	1.5 V-p-p 57 MHz	0
3,5	1.7 V-p-p 57 MHz	+12V
4,8		GND

TABLE 5.21.2

INPUT LEVEL AT J1	MODULATION	TEST POINT	VOLTS P-P
-20	Off	Q2 Pin 3	.15
-30	Off	Q2 Pin 1	.1
-40	Off	U2 Pin 7	1.25 *
-50	50% AM	U3 Pin 9	1.5
-50	50% AM	U3 Pin 1	.2 **
-50	500 kHz FM Deviation	U6 Pin 1	0
-60	500 kHz FM Deviation	U6 Pin 6	1.5

* Note: If incorrect check DC volts on U2 pins 3 and 4.for 1.11 VDC
** Note: If incorrect check AGC voltage on U3 pin 4 for 4.50 VPC

TABLE 5.21.3

PIN	Q3	Q4
1	11.24 VDC	0 VDC
2	5.44 VDC	10.84 VDC
3	2.46 VDC	2.98 VDC
4	.24 VDC	0 VDC

TABLE 5.21.3.A

INPUT LEVEL AT J1	MODULATION	TEST POINT	VOLTS P-P
-20	Off	Q3 Pin 3	.15
-30	Off	Q3 Pin 1	.1
-30	Off	Q4 Pin 3	.04
-40	Off	Q4 Pin 2	.1
-40	Off	U7 Pin 14	.04
-50	Off	U7 Pin 7	1 *
-50	50% AM	U9 Pin 9	1.25
-50	50% AM	U9 Pin 1	.2 **
-50	500 kHz FM Deviation	U11 Pin 1	-
-60	500 kHz FM Deviation	U11 Pinn 6	.5

* Note: If incorrect check DC volts on U7 pins 3 and 4.for 1.55 VDC
** Note: If incorrect check AGC voltage on U9 pin 4 for 2.95 VDC

Sections A3B1A3 and A4 can be checked as follows:

a. With a 45 MHz signal input to J1, 50% AM modulated and -40 dBm level, check the AM output at U14 pin 4 for approximately .15 V-p-p.

b. Change the modulation to FM, with 50 kHz deviation, and check the FM output at U17 pin 6 for approximately 1.5 V-p-p.

If both of the above are correct the A3B1A3 and A3B1A4 sections are operating correctly. If not proceed as follows:

a. Measure the DC voltages on Q6 and Q7 per Table 5.21.4.

b. Check with an oscilloscope th points as listed in Table 5.21.4.A.

5.21.5 3 kHz IF, A3B1A4 and A3B1A3

Refer to component layout 81A313-334 and 81B314-335.

Set the receiver front panel controls as follows:

Mode - SYNTH
Demod - AM
Bandwidth - 3 kHz

Sections A3B1A3 and A3B1A4 can be checked as follows:

a. With a 45 MHz signal input to J1, 50% AM modulated and -40 dBm level check the AM output at U14 pin 4 for approximately .1 V-p-p.

b. Change the modulation to FM, with 50 kHz deviation, and check the FM output at U17 pin 6 for approximately .3 V-p-p.

If both of the above are correct the A3B1A4 and A3B1A3 sections are operating correctly. If not proceed as follows:

a. Measure the DC voltages on Q9 and Q20 and Q21 per Table 5.21.5.

b. Check with an oscilloscope the points as listed in Table 5.21.5.A.

5.21.6 AUDIO AND POWER SWITCHING, A3B1A6

Refer to component layout 81A316-337.

5.21.6.1 POWER SWITCHING

The power switching section of this board can be checked by using Table 5.21.6.1.

5.21.6.2 AUDIO SELECTION

The selected Audio is processed by U22 (FM) or U23 (AM) and U24 and U27. It can be checked as follows:

AM AUDIO:

The AM Audio of the selected bandwidth should be present at R118 (2 MHz) or R119 (150 kHz) or R121 (3 and 15 kHz). This Audio is amplified by U23 (X10). The output of U23 (pin 6) is then fed to the Audio Selector/Amp U24 via C138 and R129.

FM AUDIO:

The FM Audio of the selected bandwidth should be present on R118 (2 MHz) or R119 (150 kHz) or R121 (3 and 15 kHz). This audio is amplified by U23

TABLE 5.21.4

PIN	Q6	Q7
1	11.89 VDC	0 VDC
2	4.9 VDC	10.85 VDC
3	2.53 VDC	2.77 VDC
4	.21 VDC	0 VDC

TABLE 5.21.4

INPUT LEVEL AT J1	MODULATION	TEST POINT	VOLTS P-P
-20	Off	Q6 Pin 3	.15
-30	Off	Q6 Pin 1	.15
-30	Off	Q7 Pin 3	.05
-40	Off	Q7 Pin 2	.15
-40	Off	U12 Pin 14	.15
-50	Off	U12 Pin 7	.6 *
-50	50% AM	U14 Pin 9	1.0
-50	50% AM	U14 Pin 1	.12 **
-50	500 kHz FM Deviation	U17 Pin 1	.06
-60	500 kHz FM Deviation	U17 Pin 6	1.5

* Note: If incorrect check DC volts on U12 pins 3 and 4.for 1.66 VDC
** Note: If incorrect check AGC voltage on U14 pin 4 for 3.08 VDC

TABLE 5.21.5

PIN	Q9	Q20	Q21
1	11.81 VDC	0 VDC	0 VDC
2	4.97 VDC	.68 VDC	11.5 VDC
3	2.50 VDC	2.83 VDC	2.42 VDC
4	.44 VDC	0 VDC	0 VDC

TABLE 5.21.5.A

INPUT LEVEL AT J1	MODULATION	TEST POINT	VOLTS P-P
-20	Off	Q9 Pin 3	.2
-30	Off	Q9 Pin 1	.3
-30	Off	Q20 Pin 3	.3
-40	Off	Q20 Pin 2	.06
-40	Off	Q21 Pin 3	.02
-40	Off	Q21 Pin 2	.1
-40	Off	U12 Pin 14	.1
-50	Off	U12 Pin 7	.6 *
-50	50% AM	U14 Pin 9	.75
-50	50% AM	U14 Pin 1	.1 **
-50	500 kHz FM Deviation	U17 Pin 1	.04
-60	500 kHz FM Deviation	U17 Pin 6	.3

* Note: If incorrect check DC volts on U7 pins 3 and 4.for 0 VDC
** Note: If incorrect check AGC voltage on U9 pin 4 for 0 VDC

TABLE 5.21.6.1

FRONT PANEL BANDWIDTH	Q12 BASE	Q12 COLLECTOR	Q13 BAES	Q13 COLLECTOR	Q14 BASE	Q14 COLLECTOR	Q16 BASE	Q16 COLLECTOR	Q7 BASE	Q7 COLLECTOR
2 MHz	11.17	11.81	11.94	0	11.95	0	11.93	0	11.94	0
150 kHz	11.94	0	11.16	11.53	11.94	0	11.93	0	11.94	0
15 kHz	11.94	0	11.93	0	11.23	11.96	11.93	0	11.18	11.98
3 kHz	11.94	0	11.94	0	11.94	0	11.21	11.94	11.18	11.98

(X10) and fed to the Audio Selector switch U24 via C139 and R149.

CW/SSB AUDIO:

The CW/SSB Audio is present in the 3 and 15 kHz bandwidths only and is generated by U14. The output of U14 (pin 8) is then coupled via C137 and R128 to Audio Selector switch U24.

AUDIO SWITCHING:

U24 is an FET switch used to select the desired audio to be connected to U27 pin 5. The desired audio is selected by applying a "low" level to input pins 5 (CW) or 12 (FM) or 13 (AM). When this low level is applied to one of these inputs, the selected audio should be present on U27 pin 5. U27 is another FET switch which is used to select either the subcarrier audio or one of the above audio signals and switch it to pin 18 of A1B3A6. This switch also determines whether the FM or AM output is sent out to the subcarrier receiver for the second demodulation. The AM signal is entered on U27 pin 1 and the FM on U27 pin 13. One of these 2 inputs is selected by a low level on pin 11 (for FM) or pin 10 (for AM). This input also connects the SC audio to the audio output at pin 18 of A1B3A6.

5.21.7 200 kHz VIDEO IF, A3B1A7

Refer to component layout 81A317-338.

The 10.7 MHz output from A3B1A1 enters A3B1A7 at Q19 pin 3. This section can be checked in the following manner:

Set the mode switch to VARI-SCAN and the receiver scanwidth to "OFF". Inject a 45 MHz -20 dBm signal into J1 and check the points as listed in Table 5.21.7.

The 13.5 MHz Video IF can be checked by injecting a 13.5 MHz signal into J6 and taking measurements per Table 5.21.7A (with the receiver in SYNTH mode).

5.22 580-1170 MHz DIVIDE BY 10, A8B10

Refer to schematic diagram 81B810-033 and component layout 81A810-352.

The A8B10 module takes the 580 MHz to 1170 MHz signal from the YIG oscillator (via Z6, Z7) and divides this frequency by 10. It can be checked by injecting a signal into J1 at -3 dBm in the 580 to 1170 MHz frequency range and counting the output from J2. The output at J2 should be the input frequency divided by 10.

5.23 RF SWITCHING, A8B15

Refer to schematic diagram 81D815-035 and component layout 81A815-388.

All of the output logic on A8B15 is generated by U1, therefore if a problem is suspected on this board the BCD band input logic on input pins K, F and H should be checked per Table 5.23.

If this input is correct next check the outputs of U1 per the Table on the schematic diagram. If these outputs are correct the next step is to check the switched outputs per Table 5.23.A.

TABLE 5.21.7

INPUT LEVEL	TEST POINT	VOLTS DC	V-p-p
-20	Q19-3	4.35	.15
-30	Q19-2	13.83	.15
-30	U31-1	1.25	.04
-40	U31-5	2.50	.3
-40	U32-6	.78	.15
-50	U32-3	2.11	1.5
-50	U34-3	1.25	.02
-50	U33-4	0	.09
-50	U33-10	4.66	-
-50	U34-2	0	-
-50	J7 (LOG)	4.79	-
-50	J7 (LIN)	11.23	-

TABLE 5.21.7A

INPUT LEVEL	TEST POINT	VOLTS DC	V-p-p
-20	Q20-3	2.17	.14
-20	Q20-2	4.35	.5
-30	Q100-2	* 3.6	* .6
-30	Q101-3	* 1.8	* .15
-30	Q101-2	* 3.5	* .08
-40	Q18-3	2.13	.04
-40	Q18-2	4.29	.2
-50	U28-6	.92	.1

INPUT LEVEL	TEST POINT	VOLTS DC	V-p-p
-50	U28-3	2.57	.1
-50	U33-12	0	.1
-60	U34-2	.03	.02
-60	U29-6	.84	.02
-60	U29-3	1.5	.35
-60	U34-1	.19	.02
-60	J7 (LOG)	1.49	-
-60	J7 (LIN)	.56	-

*Serial Number 175 and up only

TABLE 5.23

	PIN		
BAND	H	F	K
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L
5	H	L	H
6	H	H	L
7	H	H	H

TABLE 5.23.A

MODE	BAND	OUTPUT	
		PIN No.	VDC
X	3,4,5,7	A	+ .73
X	6	A	- .93
X	3,4,5,6	B	+ .72
X	7	B	- .93
X	3,4,5	C	+ 2.26
X	6,7	C	- 5.33
X	6,7	D	+ .78
X	3,4,5	D	- .91
X	6,7	E	+ 4.24
X	3,4,5	E	- 5.27
SYN	3,4,5,6,7	11	+12
SYN	1,2	11	0
X	6	13	+15
X	5	13	+ .14
X	6,7	N	+15
X	5	N	0
X	3	P	+15
X	4	P	+ .24
X	4,5	R	+15
X	6	R	+ .13
X	3,4,5	S	+15
X	6	S	+14.81
X	3,4,5	8	+ .12
X	6	8	+14.91
X	7	16	+15
X	6	16	0
X	3,4,5,6,7	15	+15
X	2	15	0
X	3,4,5,6,7	17	+ .14
X	2	17	+14.93
X	3,4,5	T	-12
X	6	T	0
X	3,4,5,6,7	18	+ 3.51
X	2	18	+ .2
X	3,4,5,6,7	U	-12
X	2	U	0
ATTENUATOR IN	3	5	0
ATTENUATOR OUT	3	5	5

X = Don't care

5.24 SUBCARRIER RECEIVER, A11

Refer to schematic diagram 81R110-012 and component layout 81B811-245.

In order to test the subcarrier receiver it is necessary to remove the unit from the receiver. Then remove the top cover and the coax cable attached to pin L. Another cable should be soldered to pin L to allow connection to a signal generator.

5.24.1 SC AUDIO

The first item to check in the SC Receiver is the Local Oscillator (U5). Set the SC Mode switch to AM and the tuning control fully CCW. With a scope probe connected to a frequency counter check the frequency at U5 pin 13. It should be 455 kHz $\pm$20 kHz. Repeat the above but checking at T1 pin 2. If this is operating normally adjust the SC tuning control to get a 555 kHz output. Inject a 100 kHz signal at -20 dBm into pin L. Check for the signal levels listed in Table 5.24.1.

5.24.2 SC VIDEO

Set the SC Mode switch to SCAN. Externally sweep an oscilloscope using the PR-700 Receiver's Horizontal output. Inject a 100 kHz signal into pin L and with a scope probe check the points as shown in Table 5.24.2.

5.25 260-520 MHz MULTIPLIER, A8B11

Refer to schematic diagram 81B811-034-1 and component layout 81A811-151.

The A8B11 module can be checked for proper operation by checking for a 520 MHz +3 dBm or larger signal at output jack J2 with a spectrum analyzer. The receiver band select switch must be set to Band 3 (30-50 MHz). If this signal is not present remove the 260 MHz input into J1 and inject a 260 MHz CW signal into J1 from a signal generator and again check the output for +3 dBm at 520 MHz. If the 520 MHz is present there is no problem in the A8B11 module; if not, remove A8B11 module from the receiver and check the DC voltages per Table 5.25 with no signal input.

5.26 YIG TRACKING, A12B2

Refer to schematic diagram 81R122-022 and component layout 81B1222-360.

5.26.1 MAINTENANCE

If a problem is suspected on the YIG tracking board, check levels at points listed in Tables 5.26.A, 5.26.B, 5.26.C and 5.26.D. Check also the 11.00 VDC reference on pin A.

TABLE 5.24.1

GENERATOR INPUT LEVEL	MODULATION	TEST POINT	VOLTAGE PEAK-TO-PEAK
-20 dBm	OFF	J1-L	.13
-30 dBm	OFF	U2-3	.020
-40 dBm	OFF	U3-3	.8
-40 dBm	50% AM	U4-1	.2
-30 dBm	OFF	U6-4	.02
-30 dBm	3 kHz FM	U6-1	2.5

TABLE 5.24.2

GENERATOR INPUT LEVEL	TEST POINT	WAVEFORM
-30 dBm	U4-1	.5 V-p-p on A .6 VDC baseline
-30 dBm	U10-3	.2 V-p-p on A .3 VDC baseline
-30 dBm	Pin C	3V-p-p on A 0 VCD baseline

TABLE 5.25

	E	B	C
Q1	-11.61	-10.87	0
Q2	-9.03	-8.28	0
Q3	-8.76	-8.06	0

TABLE 5.26.A

FRONT PANEL CONTROL	TEST POINT PIN	
	H	F
SYNTH	+5	0
VARI-SCAN	0	+5
SCAN	+5	+5

TABLE 5.26.B

FRONT PANEL BAND	TEST POINT PIN		
	M	J	N
1	0	0	5
2	0	5	0
3	0	5	5
4	4.07	0	0
5	4.07	0	5
6	4.07	5	0
7	4.07	5	5

TABLE 5.26.C

FRONT PANEL FREQUENCY	BAND	MODE	TEST PIN NO.	OUTPUT VDC	TEST PIN NO.	OUTPUT VDC
0	1	SYNTH	B	.51	E	
0	1	SYNTH	7	-.04	E	
10	1	SYNTH	B	1.51	E	
10	1	SYNTH	7	-4.0	E	
10	2	SYNTH	B	1.51	E	
10	2	SYNTH	7	-4.01	E	
30	2	SYNTH	B	3.52	E	
30	3	SYNTH	7	-12.05	E	
30	3	SYNTH	3	0	E	4.68
50	4	SYNTH	3	10.03	E	4.82
50	4	SYNTH	3	.002	E	4.81
150	5	SYNTH	3	10.03	E	5.51
150	5	SYNTH	3	.001	E	5.50
470	6	SYNTH	3	10.03	E	7.73
170	6	SYNTH	3	.002	E	4.12
1000	7	SYNTH	3	10.03	E	7.80
1000	7	SYNTH	3	.002	E	3.76
2000	7	SYNTH	3	10.03	E	7.22

NOTE: Voltages on Pin E are approximate and will vary from unit to unit.

If any of the above voltages are incorrect proceed to Table 5.26.D for the Band or Bands involved.

TABLE 5.26.D

BAND	FREQUENCY	TEST POINTS	OUTPUT
1	0000	U1-10	0
		U3-1	0
		U3-7	-.85
		Q1-C	-.04
1	10 MHz	U1-10	2.20
		U3-1	-2.19
		U3-7	.18
		Q1-C	-4.00
2	10 MHz	U1-10	2.20
		U3-1	-2.19
		U3-7	6.22
		Q1-C	-4.01
2	30 MHz	U1-10	6.60
		U3-1	-6.58
		U3-7	-.65
		Q1-C	-12.04
3	30 MHz	U6-3	2.38
		U6-10	4.68
3	50 MHz	U6-3	2.45
		U6-10	4.82
4	50 MHz	U7-6	2.44
		U7-12	5.48
		U6-10	4.81
4	150 MHz	U7-6	2.79
		U7-12	6.17
		U6-10	5.51
5	150 MHz	U7-8	2.79
		U7-12	6.19
		U6-10	5.50
5	470 MHz	U7-8	3.90
		U7-12	8.43
		U6-10	7.73
6	470 MHz	U7-1	2.10
		U7-12	4.81
		U6-10	4.12
		U2-6	.82
		U2-10	1.66
6	1000 MHz	U7-1	3.93
		U7-12	8.48
		U6-10	7.73
		U2-6	1.79
		U2-10	3.61
7	1000 MHz	U7-3	1.92
		U7-12	4.45
		U6-10	3.76
		U2-8	1.78
		U2-10	3.57
7	2000 MHz	U7-3	3.65
		U7-12	7.97
		U6-10	7.23
		U2-8	3.58
		U2-10	7.19

5.27 180/260 MHz PHASE LOCK LOOP, A8B16

Refer to schematic diagram 81R816-059 and component layouts 81A816-164 and 81A816-165.

5.27.1 180 MHz LOOP, A8B16A1

Check the output power and frequency at J2 with a spectrum analyzer. If this output is 0 dBm ±2 dBm at exactly 180 MHz then the A8B16A1 assembly is operating properly. If it is not first check to see that the 5 MHz reference signal is present at J1. If this signal is present then it will be necessary to remove the A8B16 module from the receiver remove the top and bottom covers and check for signals as listed in Table 5.27.1.

5.27.2 260 MHz PLL, A8B16A2

The 260 MHz PLL can also be checked very easily by selecting band 3 and checking for a 260 MHz output at J4 at approximately 0 dBm ± 2 dBm. If this signal is not present first check for a low level (less than 15V) on the 260 MHz enable input FL-5, then proceed to check the outputs as listed in Table 5.27.2.

5.28 YIG PHASE LOCK LOOP, A8B17

Refer to schematic diagram 81R817-060 and component layouts 81A817-167 and 81A817-168.

Proper operation of the A8B17 module can be checked by monitoring the YIG oscillator output frequency by removing the 50 ohm load on Z6 (bottom of A8 RF Head) and connecting this output to a frequency counter. This output can then be checked using Table 5.28.A.

If the readings on Table 5.28 are correct then the A8B17 module is functioning properly; if not, proceed by checking those points per Table 5.28.A with the receiver in the Synthesize mode.

If the logic levels in Table 5.28.B are correct the entire A8B17A1 Divide by N board can be checked as follows:

1. Set the receiver to band 3 and tune to 30 MHz.
2. Remove the input to J2 and inject a 72 MHz signal at 0 dBm into J2.
3. Check the output at U1-9. If it is 500 kHz the A8B17A1 board is functioning properly.

The A8B17A2 board can be checked by monitoring the "+FM OUT" on pin 12 while varying the 72 MHz input. If the 72 MHz input is lowered in frequency (71.9 MHz) the FM output should go to approximately +.064 VDC. If the input is above 72 MHz the "+FM OUT" should be approximately -.053 VDC.

5.29 SWITCHING LOGIC, A12B3

Refer to schematic diagram 81D123-040 and component layout 81B123-361.

All of the output logic on A12B3 is generated through U2 therefore if a problem is suspected on this board the input and output logic to U2 should be checked per the truth table on the schematic.

If these outputs are correct the next step is to check the switched outputs per Table 5.29.

TABLE 5.27.1

TEST POINT	FREQUENCY	OUTPUT
FL-2	-	<1.5 VDC
U1-1	5 MHz	TTL Level
Q2-C	180 MHz	+14 VDC
Q5-C	180 MHz	+3 dBm
Q6-C	20.000 MHz	-10 dBm
U3-8	5.00 MHz	1 V-p-p
U2-9	-	4 V-p-p
Q1-C	-	2.97 VDC

TABLE 5.27.2

TEST POINT	FREQUENCY	OUTPUT
FL-4	-	+5 VDC
FL-6	-	+15 VDC
Q1-C	-	+14 VDC
U1-1	5 MHz	TTL Level
U2-1	2.5 MHz	TTL Level
Q3-B	260 MHz	-4 dBm
U8-2	260 MHz	-4 dBm
U8-6	130 MHz	-4 dBm
U4-1	12.5 MHz	TTL Level
U4-9	2.5 MHz	TTL Level
U3-6	-	6.87 VDC

TABLE 5.28

MODE	BAND	FRONT PANEL FREQUENCY	YIG OSCILLATOR OUTPUT FREQUENCY (MHz)
VS	3	30 MHz	*715
SYNTH	3	30 MHz	720
VS	3	50 MHz	*735
SYNTH	3	50 MHz	740
VS	4	50 MHz	*735
SYNTH	4	50 MHz	740
VS	4	150 MHz	*835
SYNTH	4	150 MHz	840
VS	5	150 MHz	*835
SYNTH	5	150 MHz	840
VS	5	470 MHz	*1155
SYNTH	5	470 MHz	1160
VS	6	470 MHz	*635
SYNTH	6	470 MHz	640
VS	6	1000 MHz	*1165
SYNTH	6	1000 MHz	1170
VS	7	1000 MHz	*528.5
SYNTH	7	1000 MHz	585
VS	7	2000 MHz	*1082.5
SYNTH	7	2000 MHz	1085

* If incorrect proceed to alignment section of A12B2 for adjustment

TABLE 5.28.A

BAND	RECEIVER FREQUENCY	PIN J1 10	9	8	7	6	5	4	3	2	1
3	30 MHz	L	H	L	H	L	L	L	H	L	L
3	50 MHz	L	H	L	H	L	L	H	L	L	L
4	50 MHz	L	H	L	H	L	L	H	L	L	L
4	150 MHz	L	H	L	H	H	L	H	L	L	L
5	150 MHz	L	H	L	H	H	L	H	L	L	L
5	470 MHz	H	L	L	L	H	H	L	L	H	L
6	470 MHz	L	H	L	L	H	L	H	L	L	L
6	1000 MHz	H	L	L	L	H	H	H	L	L	L
7	1000 MHz	L	H	L	L	L	H	L	H	H	L
7	2000 MHz	H	L	L	L	L	H	L	H	H	L

TABLE 5.29

MODE	BAND	POINT	OUTPUT
X	X	T	+6 VDC
SCAN	X	U	+6 V
SCAN or VAR-SCAN	3-7	V	+6 V
SCAN or VARI-SCAN	1&2	R,N	+6 V
SYNTH	X	R,N	+6V
SCAN	1&2	L	+6V
SYNTH, SCAN and VARI-SCAN	3-7	1	+15 V
SYNTH, SCAN and VARI-SCAN	3-7	6	TTL Low
S	X	H	+15 VDC
SCAN, VARI-SCAN	3-7	S	+15 VDC
SCAN, VARI-SCAN	1&2	P,M	+15 VDC
SYNTH	X	P,M	+15 VDC

X = Don't Care

5.30 +5 VOLT REGULATOR BOARD, A13

Refer to schematic diagram 81B130-046 and component layout 81A130-399.

The A13 board is operating properly if there is +5 VDC ±.2 VDC present on E4. If it is not, the problem can be isolated by taking DC measurements per Table 5.30.

5.31 SWEEP/MARKER GENERATOR, A12B4

Refer to schematic diagram 81D124-041 and component layout 81B124-362.

5.31.1 SWEEP GENERATOR

The sweep generator consists of the following major components: U2, U3 and Q1. The waveforms for proper operation in the SCAN mode are shown in Table 5.31.1 and 5.31.1 A.

5.31.2 SYNTHESIZE TUNING VOLTAGE

The 0 to 10V output per band on pin M in the SYNTHesize mode is generated from the D/A voltage input on pin E, and can be checked as listed on Table 5.31.2.

5.31.3 +11.00 VDC REFERENCE

The precision 11.00 V reference is generated by diode D7, Op Amp U10 and transistor Q2. Table 5.31.3 shows the correct operating voltages.

5.32 ASSEMBLY A6

Due to the necessity for all three (A6B1, A6B2 & A6B3) boards to be interconnected to test their operation and the need for special extender cables to allow access to all of these boards, the following maintenance section is written to allow the most complete checkout of the three A6 PC boards as a unit. If a problem is discovered with the A6 assembly using this checkout it is recommended that the receiver be returned to the factory for repair.

5.32.1 DISPLAY BOARD, A6B1

1. Check for +5V on J1 pins 18 and V.
2. Check for Gnd on J1 Pins 1 and A.
3. Check for TTL level pulses on pin F when tuning in the up direction.
4. Check to see that pin N goes to a TTL level high when the top on any band is reached.

5.32.2 CONTROL BOARD, A6B2

1. Check the BCD band input on pins 10, J and K of J1 per Table 5.32.2.
2. Check for +5V on pins 18 and V.
3. Check for Gnd on pins A and 1.
4. Check the "Divide by N #4" output per Table 5.32.2.A.

TABLE 5.30

TEST POINT	VOLTS DC
E3	-6V $\pm$.3V
E2	+6V $\pm$.3V
D1 Cathode	2.4 VDC $\pm$.3
U2-7	1.12 VDC $\pm$.3
Q2-C	4.81 VDC $\pm$.3
Q1-C	+5 VDC $\pm$.2

TABLE 5.31.1A

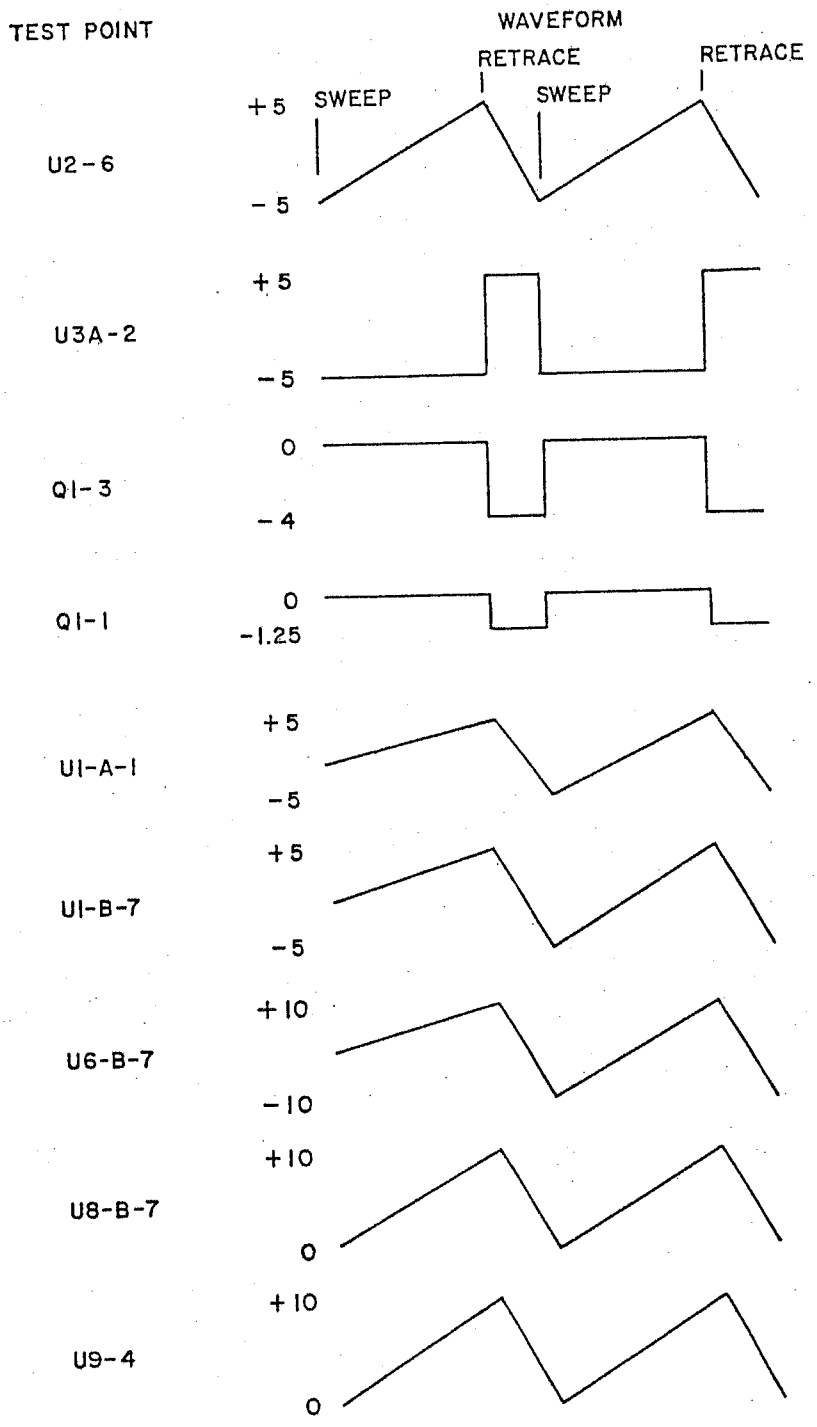

TEST POINT
WAVEFORM
RETRACE
RETRACE
SWEEP
SWEEP
U2-6
+5
-5
U3A-2
+5
-5
Q1-3
0
-4
Q1-1
0
-1.25
U1-A-1
+5
-5
U1-B-7
+5
-5
U6-B-7
+10
-10
U8-B-7
+10
0
U9-4
+10
0

TABLE 5.31.1B

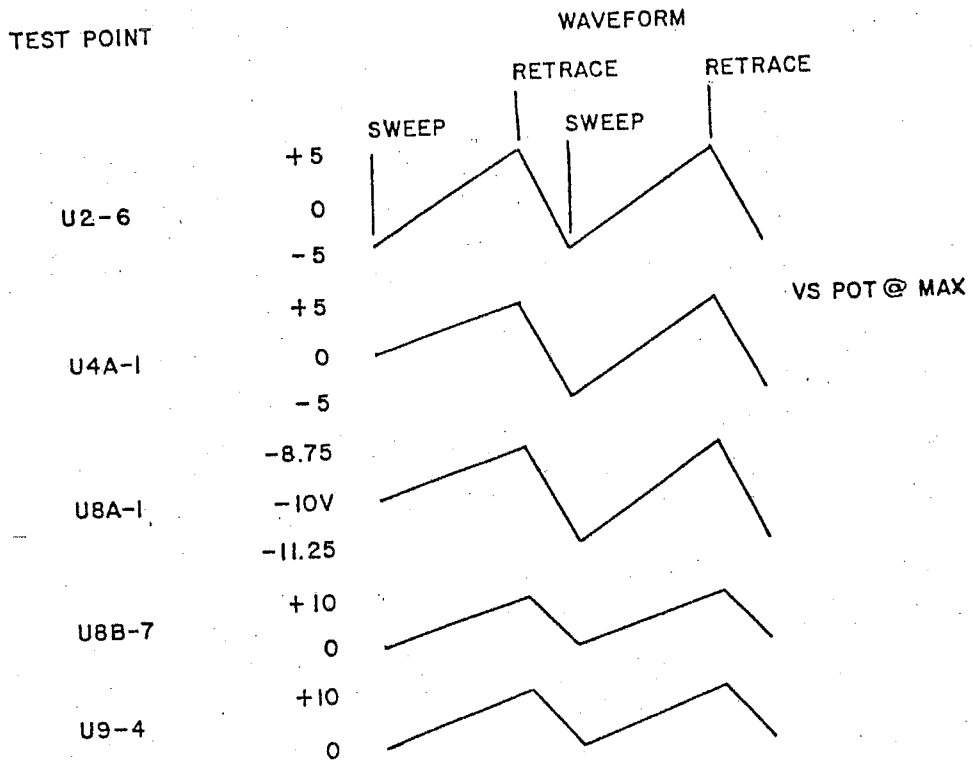

TEST POINT
WAVEFORM
RETRACE
RETRACE
SWEEP
SWEEP
+5
0
-5
U2-6
+5
0
-5
U4A-1
VS POT @ MAX
-8.75
-10V
-11.25
U8A-1
+10
0
U8B-7
+10
0
U9-4

TABLE 5.31.2

BAND	FREQUENCY (MHz)	PIN E VOLTS	U5B-7 VOLTS	U8B-7 VOLTS	PIN M VOLTS
1	0	-0.3	-10.02	-.03	-.02
1	5	5.00	.02	5.11	5.01
1	10	10.02	10.05	10.25	10.03
2	10	-.01	-9.98	0	0
2	20	5.01	.05	5.13	5.02
2	30	10.02	10.06	10.25	10.03
3	30	-.01	-9.98	0	0
3	40	5.01	.05	5.13	5.02
3	50	10.03	10.07	10.25	10.04
4	50	.01	-9.95	0	.47
4	100	5.02	.06	5.13	5.03
4	150	10.03	10.05	10.26	10.04
5	150	0	-9.96	0	0
5	310	5.01	.06	5.13	5.02
5	470	10.03	10.07	10.25	10.04
6	470	0	-9.95	0	0
6	735	5.02	0	5.13	5.03
6	1000	10.03	10.07	10.26	10.04
7	1000	0	-9.95	0	0
7	1500	5.02	.06	5.13	5.03
7	2000	10.03	10.06	10.25	10.04

TABLE 5.31.3

TEST POINT	VDC
D7 Cathode	+6.35
U10-3	6.34
U10-6	11.71
Q2-C	14.94
Q2-E	11.01

TABLE 5.32.2

	J1 PIN #		
BAND	K	J	10
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L
5	H	L	H
6	H	H	L
7	H	H	H

TABLE 5.32.2.A

BAND	FREQUENCY (MHz)	J1 PIN # C	3	4	5	9	8	E	6	7	D
3	30	L	H	L	H	L	L	L	H	L	L
3	41	L	H	L	H	L	L	L	H	H	L
3	50	L	H	L	H	L	L	H	L	L	L
4	50	L	H	L	H	L	L	H	L	L	L
4	62	L	H	L	H	L	H	L	L	L	L
4	150	L	H	L	H	H	L	H	L	L	L
5	150	L	H	L	H	H	L	H	L	L	L
5	274	L	H	H	L	L	H	H	L	H	L
5	470	H	L	L	L	H	H	L	L	H	L
6	470	L	H	L	L	H	L	H	L	L	L
6	788	L	H	H	L	L	H	L	L	L	L
6	1000	H	L	L	L	H	H	H	L	L	L
7	1000	L	H	L	L	L	H	L	H	H	L
7	1700	L	H	H	L	L	L	L	H	H	L
7	2000	H	L	L	L	L	H	L	H	H	L

TABLE 5.32.3

BAND	PIN E	D	C
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L
5	H	L	H
6	H	H	L
7	H	H	H

5.32.3 D/A CONVERTER REFERENCE BOARD, A6B3

1. Check for -20 VDC at pin V.
2. Check for Gnd at pin 1.
3. Check for +5 VDC at pin P.
4. Deck for +15 VDC at pin 17.
5. Check for -15 VDC at pin U.
6. Check for a high TTL level on pin H in the SCAN and VARI-SCAN modes.
7. Check the BCD band input on pins C, D and E per Table 5.32.3.
8. Check the 0 to 10V D/A output at pin A and the .48 to 3.48V output at pin 16 and the "COARSE TUNE OUT" at pin 18 per Table 5.32.3.A.
9. Check the Divide by N #2 and 3 per Table 5.32.3.B with the receiver in the SYNTHesize mode.

TABLE 5.32.3.A

BAND	FREQUENCY (MHz)	OUTPUT		
		PIN 4	PIN 16	PIN 18
1	0	0 VDC	.51	-.4
1	5		1.01	-2.11
1	10	10 VDC	1.51	-4.10
2	10	0 VDC	2.52	-4.09
2	20		3.52	-8.06
2	30	10 VDC	1.51	-12.00
3	30	0 VDC	1.51	-4.10
3	40		1.51	-4.10
3	50	10 VDC	1.51	-4.10
4	50	0 VDC	1.51	-4.09
4	100		1.51	-4.10
4	150	10 VDC	1.51	-4.10
5	150	0 VDC	1.51	-4.10
5	250		1.51	-4.10
5	470	10 VDC	1.51	-8.03
6	470	0 VDC	1.51	-4.10
6	600		1.51	-4.10
6	1000	10 VDC	1.51	-4.10
7	1000	0 VDC	1.51	-4.10
7	1500		1.51	-4.10
7	2000	10 VDC	1.51	-4.10

TABLE 5.32.3.B

BAND	FREQUENCY	DIVIDE BY N #2										DIVIDE BY N #3									
		R	N	F	7	4	8	3	6	2	5	M	L	14	S	J	K	9	15	T	10
1	0	L	H	H	L	L	H	H	L	L	L	L	L	L	H	L	L	H	L	L	L
1	10	H	L	H	L	L	H	L	H	H	H	L	H	L	H	L	L	H	L	L	L
2	10	L	H	H	L	L	H	H	L	L	L	L	H	L	H	L	L	H	L	L	L
2	30	H	L	H	L	L	H	L	H	H	H	H	H	L	H	L	L	H	L	L	L
3	30	L	H	H	L	L	H	H	L	L	L	L	H	L	H	L	L	H	L	L	L
3	50	H	L	H	L	L	H	L	H	H	H	H	L	L	H	L	L	H	L	L	L
4	50	L	H	H	L	L	H	H	L	L	L	L	H	L	H	L	L				
4	150	H	L	H	L	L	H	L	H	H	H	H	L	L	H	L	L				
5	150	L	H	H	L	L	H	H	L	L	L	L	H	L	H	L	L				
5	470	H	L	H	L	L	H	L	H	H	H	H	L	L	H	L	L				
6	470	L	H	H	L	L	H	H	L	L	L	L	H	L	H	L	L				
6	1000	H	L	H	L	L	H	L	H	H	H	H	L	L	H	L	L				
7	1000	L	H	H	L	L	H	H	L	L	L	L	H	L	H	L	L				
8	2000	H	L	H	L	L	H	L	H	H	H	H	L	L	H	L	L	H	L	L	L

MICRO-TEL CORPORATION
an Adams-Russell Company
10713 Gilroy Road
Hunt Valley, MD 21230

OPERATING & MAINTENANCE

MANUAL

FOR

PR-700 RECEIVERS

OPTIONS

March 1982

ADDENDUM II

This addendum provides a description and the theory of operation and maintenance information for various options available in the PR-700 Receivers. These options are listed along with a brief description on page ii. Additionally, the PR-707C Receivers are provided for in this addendum by considering a PR-707C Receiver as a PR-700B receiver with options 3, 4, 5, 6, 8 and 9.

OPTION LIST

OPTION 1 - Selectable Pan Video Bandwidths of 3, 10 or 35 kHz by front panel switch.

OPTION 2 - Not Assigned

* OPTION 3 - Moves all Rear Panel BNC connectors and the antenna inputs ot the top panel and extends depth of receiver approximately 3 inches to provide for additional options.

OPTION 4 - Provides for 5 Audio Bandwidths (normally 4). These bandwidths are 3, 15, 75, 300 kHz and 2 MHz.

** OPTION 5 - Provides a 21.4 MHz IF Output.

** OPTION 6 - Provides a 1.65 MHz IF Output.

** OPTION 7 - Remote Control of sub-carrier receiver.

OPTION 8 - Selectable sub-carrier bandwidths of 6 and 35 kHz.

OPTION 9 - Front Panel Threshold and squelch.

* For PR-700B only
** For PR-700B with Option 3 only

SCHEMATIC AND COMPONENT LAYOUTS

Assembly Ref. No.	Schematic Dwg. No.	Component Layout Dwg. No.	Title
A3B1	81R31-062		IF (Option 1)
A3B1A7		81A317-184	Video IF (Option 1)
A3B5	81B35-064	81A35-1368	Selected IF Bandwidth (Option 4)
A5	81B50-1034	81A50-1320	Audio Squelch (Option 9)
A7	81D70-1035	81B70-1321	Tape Converter (Option 6)
A11	81R110-063(2)	81A110-1370	Sub Carrier (Option 7)
A11	81R110-1038	81B110-1369(2)	Sub Carrier (Option 8)
A11B1	81A111-1039	81B110-1369(2)	Sub Carrier (Option 8)
A11B2	81A112-1040	81B110-1369(2)	Sub Carrier (Option 8)
A17	81B170-1033	81A170-1328	21.4 MHz Converter (Option 5)

OPTION 1

Option 1 provides for 3 selectable Pan Video Bandwidths of 3, 10 and 35 kHz via a front panel slide switch located on the left side of the receiver under the CRT and video centering control.

Refer to schematic diagram 81R31-062 and component layout 81A317-184.

The only difference for an Option 1 Receiver is the switch mentioned above and the addition of 2 more filters (Z13 and Z15) in the main IF (A3B1A7) and 6 field effect transistors used to select these filters depending upon the logic present at IF pins 17 (+12 = 3 kHz), 33 (+12 = 10 kHz), or 34 (+12 = 35 kHz) which connect directly to the front panel switch. This +12 VDC input supplies the bias necessary to turn the 2 FET's associated with each filter on connecting the proper filter into the 13.5 MHz video IF channel. These "switches" can be checked for proper operation by injecting a 13.5 MHz CW signal at -20 dBm into J6 and checking with an oscilloscope to see that this signal is present at pin 2 of Q100 (3 kHz selected) or Q102 (10 kHz selected) or Q104 (35 kHz selected) and also at Q101 (3 kHz) or Q103 (10 kHz) or Q105 (35 kHz).

The remainder of the A3B1A7 IF maintenance can be performed using the standard maintenance procedures in the PR-700A or PR-700B maintenance section 5.21.7.

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
OPTION 1, SELECTABLE PIN VIDEO BANDWIDTHS			
A1B1, FRONT PANEL			
	Add the following components		
	SWITCH, 2P3T Slide	Switchcraft	46313LDR
A3B1A7, 200/10 kHz VIDEO IF			
	Add the following components		
C196,286,288, 291,294	CAPACITOR, Ceramic, .1uf, 20%, 50V	Erie	8121-050-651-104M
C285,290	CAPACITOR, Ceramic, .01uf, 20%, 50V	Erie	8121-050-651-103M
C302,305	CAPACITOR, Mica, 47pf, 5%, 50V	Elmenco	
C303,306	CAPACITOR, Mica, 27pf, 5%, 50V	Elmenco	DM-5FY-270J
L302,305	TOROID, 3.1uh	MTC	T25-2
L303,306	INDUCTOR TOROID, 5.2uh	MTC	T25-2 39T #30
L308,309	INDUCTOR, 100uh	Delevan	1025-100uh
Q102,103,104, 105	TRANSISTOR, FET	Signetics	SD201
R197	RESISTOR, Composition, 33K, 5%, 1/4W		RC07GF333J
R285,290	RESISTOR, Composition, 100K, 5%, 1/4W		RC07GF104J
R286,291	RESISTOR, Composition, 68K, 5%, 1/4W		RC07GF673J
R287,292	RESISTOR, Composition, 51 ohms, 5%, 1/4W		RC07GF510J

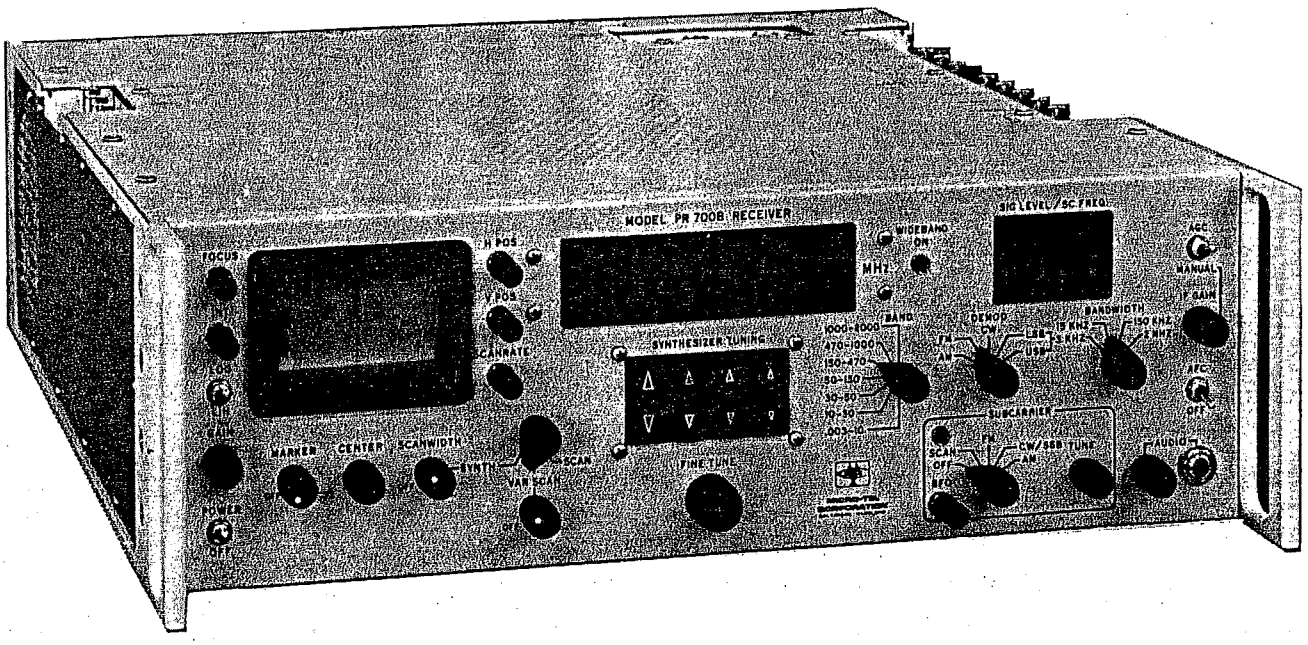
REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
R288,293	RESISTOR, Composition, 220 ohms, 5%, 1/4W		RC07GF221J
R289,294	RESISTOR, Composition, 120 ohms, 5%, 1/4W		RC07GF121J

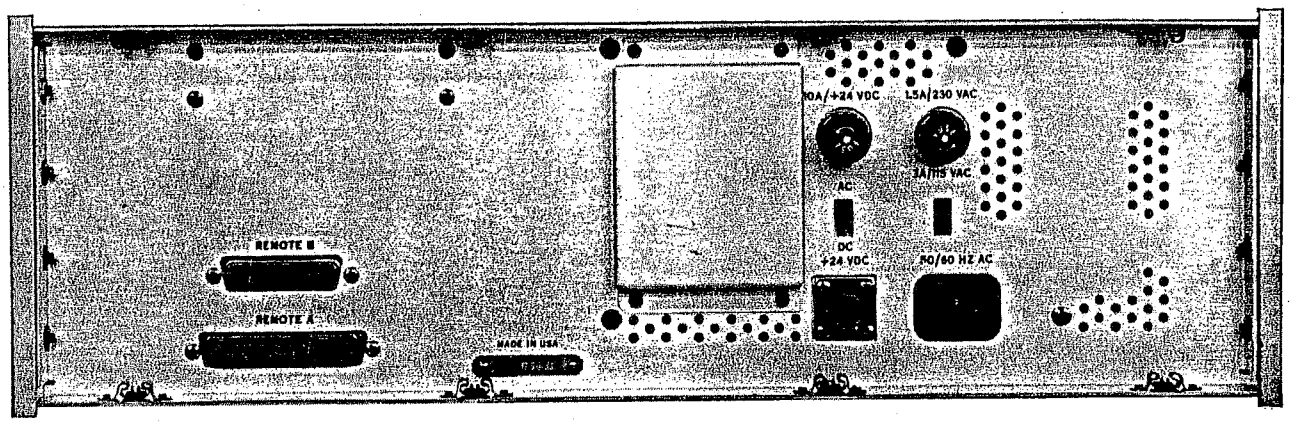
The following components are changed for Option 1

R282	RESISTOR, Composition, 51 ohms, 5%, 1/4W		RC07GF510J
R283	RESISTOR, Composition, 120 ohms, 5%, 1/4W		RC07GF121J
R284	RESISTOR, Composition, 220 ohms, 5%, 1/4W		RC07GF221J

OPTION 3

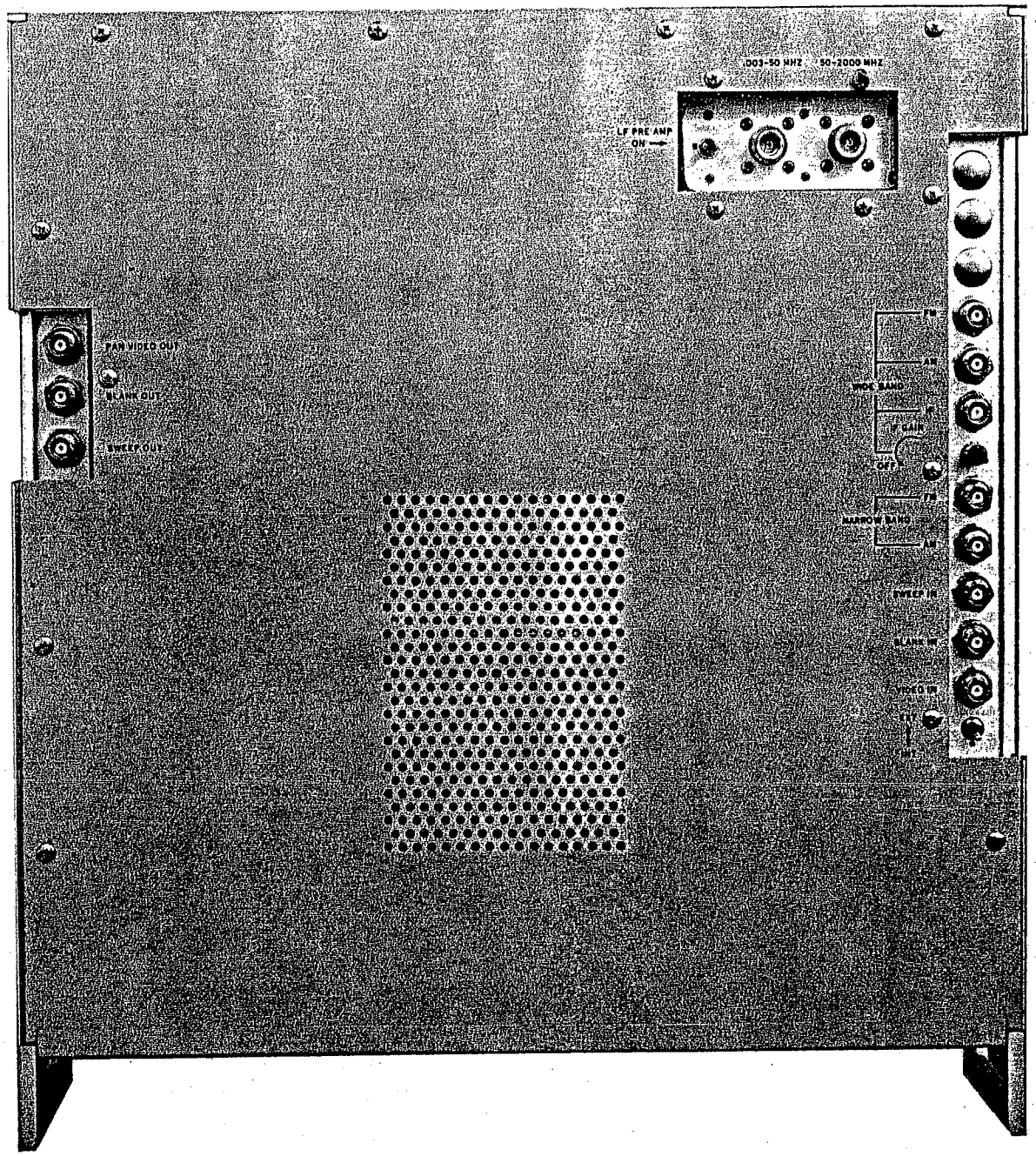
Option 3 is mainly a physical change in moving the BNC input connectors and the antenna inputs from the rear panel of the PR-700B Receiver to the top side-rails. The receiver is also approximately 3 inches deeper to provide the additional room needed for other options. See enclosed photographs showing PR-700B unit with option 3 and internal views showing module locations.





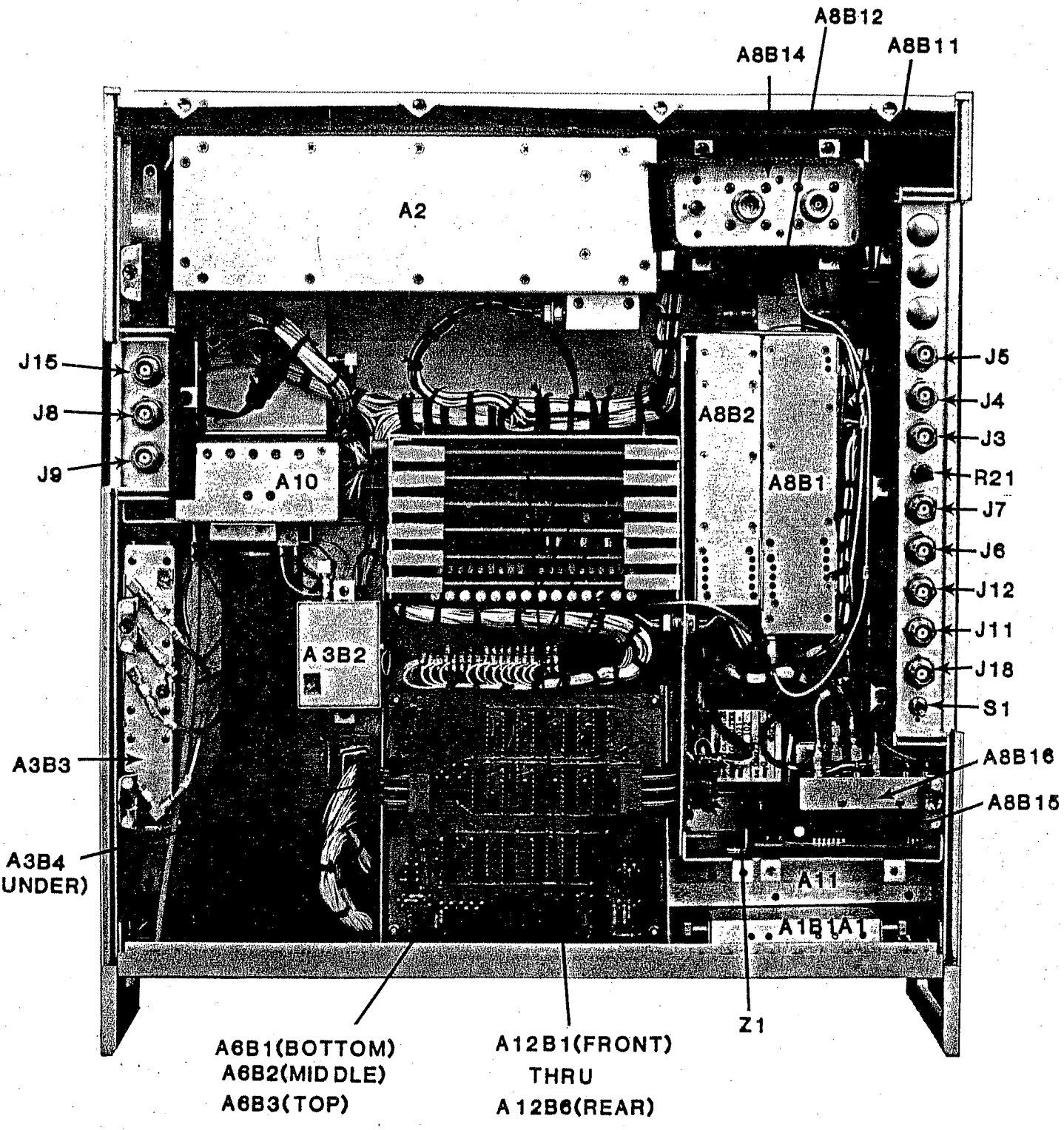
FRONT AND REAR VIEWS

PR-700B OPTION 3



TOP VIEW

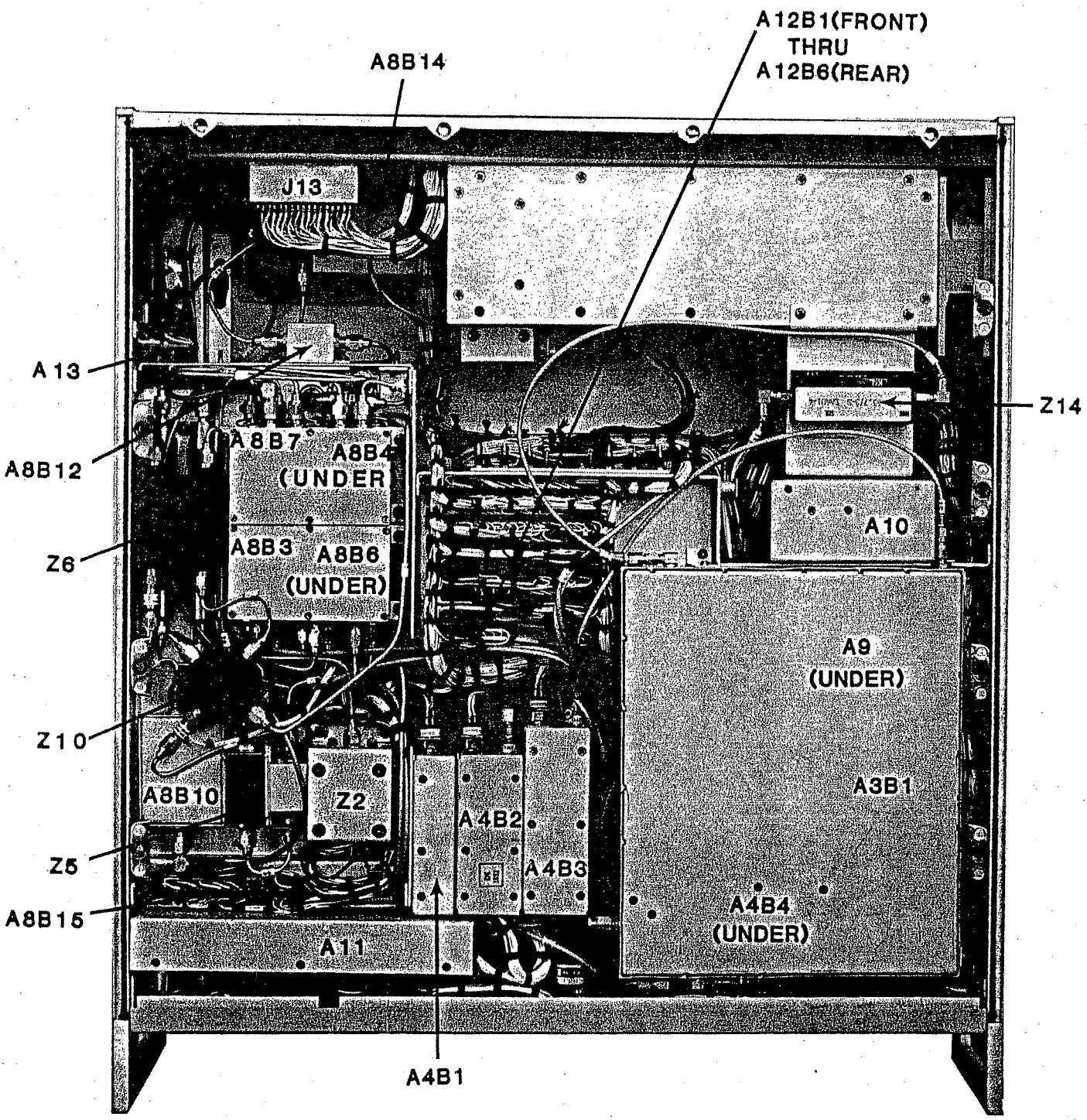
PR-700B OPTION 3



TOP VIEW

PR-700B OPTION 3

MODULE LOCATIONS



BOTTOM VIEW

PR-700B OPTION 3

MODULE LOCATIONS

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
OPTION 3			
A1B1, FRONT PANEL			
	Add the following components		
D2	LED & SOCKET	IEE	1901R
A1B2, REAR PANEL			
	Delete the following components		
C6	CAPACITOR, Tantalum, 10uf, 20V	Kemet	T310B106K020AS
J1	CONNECTOR		OSM 21011
R5	RESISTOR, Composition, 100 ohms, 5%, 1/4W		RC07GF101J
S1	SWITCH		JMT-223
A1B4			
	Add the following components		
J8,9,10,11, 12,13,14	CONNECTOR		8248
J1	CONNECTOR, 9 Pin with Hood/Lock Ring		M9PH10LRN
R1	RESISTOR, Variable with Switch, 2.5k, 10%, 1/W		GS1G040P252UA
S1	SWITCH, Toggle	JBT	JMT223 or SF22SCW191
A1B6			
	Delete the following components		
J13	CONNECTOR		8248

OPTION 4

Option 4 provides 5 audio bandwidths of 3, 15, 75, 300 kHz and 2 MHz. This is accomplished by adding an additional module, A3B5, which provides for the selection of 2 bandwidths (75 and 300 kHz). The A3B1A5 IF strip in the A3B1 main IF is modified per Figure A and 2 jacks (J8, J9) are added to the main IF to provide the input/output connectors required for the A3B5 module.

When either the 75 or 300 kHz bandwidth is enabled by the front panel selector switch or the remote input the A3B1A5 IF strip is enabled. The 45 MHz input enters at Q3 pin 3 and is amplified and passed on to Z1 which is changed to a 280 kHz wide filter for option 4. This signal then proceeds to amplifier Q4 and is then output via J8 to the A3B5 module. Refer to schematic diagram 81B35-064 and component layout 81A35-1368. The 45 MHz signal enters A3B5 on J1 and is coupled to both the 300 kHz channel (Q1 and Q2) and the 75 kHz channel (Q3 thru Q5). Only one of these two channels has power applied. The channel that is enabled depends upon the logic level present at FL-2.

IF FL-2 is a high TTL level (front panel bandwidth switch set to 300 kHz) then transistor Q6 is turned on pulling the base of transistor Q7 low thus turning it on and supplying +12 VDC to transistor Q1 and Q2 (300 kHz channel).

If FL-2 is a low TTL level (front panel switch set to 75 kHz) then transistor Q6 is off but transistor Q8 is turned on supplying +12 VDC to Q3, Q4 and Q5 (75 kHz channel). Each of the FET stages in the A3B5 module are identical and can be checked by injecting a 45 MHz signal into J1 at approximately -25 dBm and checking for approximately 8 dB of gain in each stage.

The 300 kHz bandwidth is determined in the main IF by filter Z1 (A3B1A7). Filter Z1 in the A3B5 module is replaced by a capacitor for a 300 kHz bandwidth. The 75 kHz bandwidth is determined by the 3 cascaded filters (Z2, Z3 and Z4) in the A3B5 module.

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
OPTION 4, SELECTED IF BANDWIDTHS			
A3B5			
C1,2,3,4, 5,6,7,8,9	CAPACITOR, Ceramic, .01uf, 20%, 100V	Erie	8121-100-651-103M
FL1,2	FILTERCON		859640-1
J1,2	CONNECTOR		UG1619/U
L1,2,3	INDUCTOR, 100uh	Delevan	1025-100uh
Q1,2,3,4,5	TRANSISTOR		SD201
Q6	TRANSISTOR		2N3904
Q7,8	TRANSISTOR		2N5193
R1,4,7,10,13	RESISTOR, 100K, 5%, 1/8W		RC05GF104J
R2,5,8,11,14	RESISTOR, 33K, 5%, 1/4W		RC05GF333J
R3,6,9,12,15	RESISTOR, Composition, 330 ohms, 5%, 1/4W		RC07GF331J
R16	RESISTOR, 10K, 5%, 1/8W		RC05GF103J
R17,19	RESISTOR, 1K, 5%, 1/8W		RC05GF102J
R18	RESISTOR, 100 ohms, 5%, 1/8W		RC05GF101J
R20	RESISTOR, Composition, 560 ohms,, 5%, 1/4W		RC07GF561J
R21	RESISTOR, 300 ohms, 5%, 1/8W		RC05GF301J
Z1	CAPACITOR, 15pf	Elmenco	M15-150J
Z2,3,4	FILTER, Ceramic	Murata	SFE 10.7 MH-A
XQ7,8	INSULATOR PAD		7403-09-FR-54

OPTION 5

Option 5 provides a 21.4 MHz IF output with a 3 dB bandwidth = 2 MHz and the output nominally at -70 dBm into 50 ohms.

Refer to schematic diagramm 81B170-1033 and component layout 81A170-1328.

The 21.4 MHz converter takes the PR-700 Receivers 45 MHz IF and converts this output to a 21.4 MHz IF in the following manner.

The 45 MHz IF from the A3B3 module enters on J1. This input is amplified by U1 (~12 dB) and buffered by Op Amp (U3) and fed to a double balanced mixer Z1. The local oscillator to the mixer comes from a crystal oscillator circuit (Q1) and amplifier (Q2) at 21.4 MHz above the incoming 45 MHz (66.4 MHz) and therefore generates a 21.4 MHz output at Z1-B. This output then passes through a 2 MHz wide band pass filter and on to the output buffer Op Amp U4 and proceeds out J4.

The maintenance of the A17 21.4 MHz converter is relatively simple as follows.

1. Check for +12 VDC on FL-1.
2. Check for -12 VDC on FL-2.
3. Check for a 66.4 MHz signal on Z1-W at approximately +7 dBm $\pm$3 dB.
4. Input a 45 MHz signal into J1 at -25 dBm and check for a 45 MHz signal on U1 pin 3 and U3 pin 11 at approximately -15 dBm.
5. Check for a 21.4 MHz signal at Z1-B amd U4-5 at approximately -20 dBm.
6. Check for a 21.4 MHz output at J4 at approximately -20 dBm.

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
OPTION 5			
A1B6, SIDE RAIL ASSEMBLY			
	Add the following components		
J17	CONNECTOR		8248Z
A17, 21.4 MHz CONVERTER			
C1,3,9,10, 16,18,22	CAPACITOR, Ceramic, .1uf, 20%, 100V	Erie	8121-100-651-104M
C2,4,11,13,17	CAPACITOR, .01uf, 20%, 100V	Erie	8121-100-651-103M
C5	CAPACITOR, Mica, 200pf, ±1%, 50V	Elmenco	DM5FY201J
C6,8	CAPACITOR, Mica, 390pf, ±1%, 50V	Elmenco	DM10FY391J
C7	CAPACITOR, Mica, 100pf, ±1%, 50V	Elmenco	DM5FY101J
C12,20	CAPACITOR, Mica 7 pf, ±1%, 50V	Elmenco	DM5FY7R0J
C14	CAPACITOR, Mica, 62Pf ±1 50V	Elmenco	DM5FY620J
C15	CAPACITOR, Mica, 22pf, ±1%, 50V	Elmenco	DM5FY220J
C19	CAPACITOR, Mica, 10pf, ±1%, 50V	Elmenco	DM5FY100J
C21	CAPACITOR, Mica, 200pf, ±1%, 50V	Elmenco	DM5FY201J
FL1,2	FILTERCONN		859640-1
J1 - 4	CONNECTOR		UG1619/U
L1,2	COIL, Variable, .15uh	Cambion	558-71-7-03

PR-700 RECEIVER Option 5

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
L3	COIL, luh	Delevan	1025-20
L4,5	COIL, Variable, 47uh	Cambion	558-71-7-09
Q1	TRANSISTOR, NPN		2N3478
Q2	TRANSISTOR, NPN		2N2857
R1	RESISTOR, Variable		62PR-10K
R2,3,6,7	RESISTOR, Composition, 1M ohm, 5%, 1/4W		RC07GF105J
R4,11,14	RESISTOR, Composition, 12 ohms, 5%, 1/4W		RC07GF120J
R5,12	RESISTOR, Composition, 51 ohms, 5%, 1/4W		RC07GF510J
R8	RESISTOR, Composition, 12K, 5%, 1/4W		RC07GF123J
R9	RESISTOR, Composition, 2.2K, 5%, 1/4W		RC07GF222J
R10	RESISTOR, Composition, 750 ohms, 5%, 1/4W		RC07GF751J
R13	RESISTOR, Composition, 1K, 5%, 1/4W		RC07GF102J
R15	RESISTOR, Composition, 47 ohms, 5%, 1/4W		RC07GF470J
U1	INTEGRATED CIRCUIT, Amp	Plessey	SL-611
XU1	INTEGRATED CIRCUIT, Pad		RCT05030-2A
U2	INTEGRATED CIRCUIT, Regulator		UA78L06
U3,4	INTEGRATED CIRCUIT, Buffer	National	LH0033CG
Y1	CRYSTAL, HC-18u, 66.4 MHz, .001% 32pf Load		
Z1	MIXER	Lorch	FC-200Y

OPTION 6

Option 6 provides a 1.65 MHz center frequency IF output with a 2.7 MHz bandwidth. Its output is AGC controlled and maintains a ±3 dB output over a greater than 60 dB input range. This output is adjustable up to 1V-p-p into a 75 ohms load.

Refer to schematic diagram 81D70-1035 and component layout 81B70-1321.

The 45 MHz If enters on J1 and is amplified by Q1 and Q2 (~ 20 dB) and passed on to double balanced mixer Z1 via T1. The 55.7 MHz phase lock source from the receiver enters on J2 and is amplified and buffered by Q5 and becomes the local oscillator for mixer Z1. The resulting 10.7 MHz center frequency is output on J3 and is filtered by an external 2.7 MHz wide filter. This filtered output then re-enters the A7 module on J4 and is amplified by U1 which is an IC AGC controlled amplifier with approximately 40 dB of gain. This output (U1 Pin 7) then proceeds to another double balanced mixer Z2 via T3. The local oscillator for this mixer is generated by crystal oscillator circuit Q4 and amplifier Q3, and input to Z2 by T4 and C27. The resulting 1.65 MHz (12.35-10.7) passes through a 2.7 MHz wide band pass filter consisting of L5, 6, 7 and C38 and 39. Variable resistor R33 sets the output level (adjustable up to 1 V-p-p into 75 ohms). The signal then proceeds to another integrated circuit amplifier U4 which has approximately 25 dB of gain. This output (U4 pin 7) then proceeds to output buffer U5 and out J5.

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
OPTION 6			
A1B4			
	Add the following components		
J17	CONNECTOR		8248
	SMC TEE CONNECTOR	Sealectro	50-085-0000
A7, TAPE CONVERTER			
C1,3,11,13,17 20,21,22,24, 25,27,29,40, 41,42,43,44, 45,47,52,53, 55	CAPACITOR, Ceramic, .01uf, 20%, 50V	Erie	8121-050-651-103M
C4,9	CAPACITOR, Mica 130pf	Elmenco	DM15-131J
C5,15,51	CAPACITOR, Ceramic .001pf	Sprague	5GAD10
C6,14,35	CAPACITOR, Tantalum, 6.8uf, 20%, 16V	Kemet	T390B685M016AS
C7,18,26,28, 31,34,46, 49,50,54	CAPACITOR, Ceramic, .1uf, 20%, 50V	Erie	8131-050-651-104M
C8	CAPACITOR, Mica 8.2pf, 5%, 500V	Stackpole	C80-51
C10	CAPACITOR, Mica, 100pf	Elmenco	DM15-101J
C12,23	CAPACITOR, Mica, 30pf	Elmenco	DM15-300J
C16,19,30	CAPACITOR, Mica, 20pf	Elmenco	DM15-200J
C32	CAPACITOR, Mica, 22pf	Elmenco	DM15-220J

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
C33	CAPACITOR, Variable, 6-25pf	Erie	10ST22-6/25
C36	CAPACITOR, Tantalum, 47uh,6V	Kemet	T310B476K006AS
C37	CAPACITOR, Tantalum, 2.2uf, 25V	Kemet	T390B225M025AS
C38,39	CAPACITOR, Ceramic, 1800 pf, 5%, 500V	Elmenco	CM06FD182J03
C48	CAPACITOR, Mica, 200pf, 55, 500V	Elmenco	DM15-201J
J1,2,5	CONNECTOR, Straight		UG1619/U
J3,4	CONNECTOR, Right Angle		AEP112
L1,4	INDUCTOR, Fixed, 100uh	Delevan	1025-68
L2,3	INDUCTOR, Fixed. 12uh	M-T	8 Turns #26
L5,7	INDUCTOR, Fixed, 2.7uh		1025-30
L6,8	INDUCTOR, Fixed, 4.7uih		1025-36
Q1,2	TRANSISTOR, FET		SD306
Q3,5	TRANSISTOR,		2N5109
Q4	TRANSISTOR		2N3904
R1	RESISTOR, Composition, 130K, 5%, 1/4W		RC07GF134J
R2,9	RESISTOR, Composition, 43K, 5%, 1/4W		RC07GF433J
R3,10	RESISTOR, Composition, 75K, 5%, 1/4W		RC07GF753J
R4,11	RESISTOR, Composition, 50K, 5%, 1/4W		RC07GF503J
R5,22,27	RESISTOR, Composition, 5.6K, 5%, 1/4W		RC07GF562J

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
R6,12,13,25, 30,37,41,42	RESISTOR, Composition, 10 ohms, 5%, 1/4W		RC07GF100J
R7	RESISTOR, Composition, 560 ohms, 5%, 1/4W		RC07GF561J
R8	RESISTOR, Composition, 150K, 5%, 1/4W		RC07GF154J
R14	RESISTOR, Composition, 10K, 5%, 1/4W		RC07GF103J
R15,28	RESISTOR, Composition, 1K, 5%, 1/4W		RC07GF102J
R16,20,36	RESISTOR, Composition, 1.2K, 5%, 1/4W		RC07GF122J
R17,18,21,34	RESISTOR, Composition, 51 ohms, 5%, 1/4W		RC07GF510J
R19,35,38	RESISTOR, Composition, 33K, 5%, 1/4W		RC07GF333J
R23	RESISTOR, Composition, 33 ohms, 5%, 1/4W		RC07GF330J
R24	RESISTOR, Composition, 2.4K, 5%, 1/4W		RC07GF242J
R26	RESISTOR, Composition, 180 ohms, 5%, 1/4W		RC07GF181J
R29	RESISTOR, Composition, 330 ohms, 5%, 1/4W		RC07GF331J
R31	RESISTOR, Variable, 20K		62PR-20K
R32	RESISTOR, Composition, 100 ohms, 5%, 1/4W		RC07G101J
R33	RESISTOR, Variable, 100 ohms,		62PR-100 ohms
R39	RESISTOR, Composition, 1 Meg ohm, 5%, 1/4W		RC07GF105J

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
T1	TRANSFORMER Core	MT	8 Turns on 57-3596-24
T2,3,4	TRANSFORMER Core	MT	17 Turns on 266CT12S/4C4
U1,4	INTEGRATED CIRCUIT		UA757
U2	INTEGRATED CIRCUIT, Regulator	Fairchild	78L06AWC
U3	INTEGRATED CIRCUIT	Plessey	SL623
U5	INTEGRATED CIRCUIT Buffer	NS	LH0033CG
Y1	CRYSTAL	International	12.35 MHz XTAL
Z1,2	MIXER, Double Balancedq	Lorch	FC-200Y
Z3	FILTER, Bandpass	K&L	8B51-107/2.7S

OPTION 7

Option 7 provides the necessary logic necessary to provide for remote control of the sub carrier receiver. The basic sub carrier receiver remains essentially unchanged and therefore the basic maintenance section in the standard manual can be used for maintenance of the signal section of the sub carrier receiver. The main difference in this sub carrier receiver is that the routing of signals within the sub carrier receiver is done via FET switches or solid-state logic instead of the wafer switch used in the standard units. This logic is shown on schematic diagram 81R110-063. Refer to this schematic and component layout 81A110-1370 for the following discussion.

Control of the sub carrier functions in a PR-700 Receiver with option 7 is done via a 3 bit BCD input number generated either by the front panel sub carrier switch or by the remote sub carrier input connector J18. (see 81R10-1002 sheet 4 of 4 in the standard PR-700B manual for wiring information of front panel switch S12 and rear panel connector J18). See Table B for the proper input logic. U19 serves as a level translator taking the TTL level inputs and translating them into a 0 = LO to +12V = HI to drive U18 which is a data selector used to select between the external or "LOCAL" (front panel) logic inputs depending on the state of U18 pin 1. (LO = Remote). The chosen input data is then routed to the 3 CMOS analog switches U15, U16 and U17 via U18 pins 4 and 7.

U17 is a dual 4 input analog switch used to select the audio output via the inputs at pins 1, 5, 2, 4. U17 also turns on the BFO in the CW/SSB mode by grounding the base of Q2 in the CW/SSB mode via U17 pin 15.

U15 is another dual 4 input analog switch used to turn the SC video on by applying +12V to R62 via U15 pin 1 in the scan mode, which turns transistor Q6 on thus grounding pin L. The second section of U15 provides for connecting the proper AGC voltage out to E1 for the AM and SSB modes. These AGC voltages are present on U15 pins 11 and 15.

U16 is an 8 input switch used to select the proper voltage out to the voltage tuned oscillator (E11). In the local scan mode the sweep voltages at U16 pin 1 is connected to E11.

In the local AM, FM and SSB sub carrier modes the voltage from the front panel tuning control is present at E9 (U16 pins 5, 2, 4) and is connected to E11. In any of the remote modes the sub carrier tuning voltage is generated externally and is input via pin H and connected to E11 via U16 pins 13, 14, 15, 12.

OPTION 7

TABLE B

		All PIN NUMBER					
	SUB CARRIER MODE	13	M	N	P	14	R
LOCAL	OFF	X	X	X	X	X	X
	SCAN	L	L	L	H	X	X
	FM	L	H	H	H	X	X
	CW/SSB	H	L	L	H	X	X
	AM	H	H	H	H	X	X
REMOTE	SCAN	X	X	X	L	L	L
	FM	X	X	X	L	L	H
	CW/SSB	X	X	X	L	H	L
	AM	X	X	X	L	H	H

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
OPTION 7, REMOTE SUB CARRIER			
A1B1, FRONT PANEL			
	Add the following components		
S12	SWITCH		71AD30-02-2-AJN
A1B2, REAR PANEL			
	Add the following components		
J16	CONNECTOR, BNC		8248
J18	FILTERED CONNECTOR, 25 Pin, Female	Erie	1255-130-0017
A11, SUB CARRIER RECEIVER			
	The following A11 module replaces the A11 module in the standard manual		
C1,2	CAPACITOR, Film, .0082, 10%, 100V	Spr	225P82291
C3	CAPACITOR, Mica, 910pf, 5%, 500V		DM15-911J
C4,8,12,13, 16,26,34	CAPACITOR, Tantalum, 1.0uf, 10%, 15V	Kemet	T310A105K015
C5,9	CAPACITOR, Mica, 4300pf, 5%, 300V		DM15-432J
C6,10	CAPACITOR, Film, .027uf, 20%, 100V	Erie	8121-100-651-273M
C7,11,14,17, 18,23,27,28, 32,33,37,38, 39,40,51,52, 56	CAPACITOR, Ceramic, .1uf, 10%	Erie	8121-100-651-104M
C15,41	CAPACITOR, Tantalum, 47uf, 10%, 6.3V	Kemet	T390D476K006AS

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
C19,20,21,25, 46,48,49	CAPACITOR, Ceramic, .01uf, 10%, 100V	Erie	8121-100-651-103M
C22,36	CAPACITOR, Mica, 390pf, 5%, 500V		DM15-391J
C24	CAPACITOR, Ceramic, .001		8121-050-651-104M
C29	CAPACITOR, Mica, 820pf, 5%, 500V		DM15-821J
C30	CAPACITOR, Mica, 100pf, 5%, 500V		DM15-101J
C31	CAPACITOR, Film, 3300pf, 10%, 100V	Erie	8121-100-X7R0332K
C35,45,57	CAPACITOR, Tantalum, 15uf, 10%, 16V	Kemet	T390C156K016AS
C42,43	CAPACITOR, Tantalum, 100uf, 10%, 6.3V	Kemet	T390D107K006AS
C44,64	CAPACITOR, Tantalum, 4.7uf, 10%, 16V	Kemet	T390B475K016AS
C50	CAPACITOR, Ceramic, .047uf, 10%, 100V	Erie	8121-100-651-473
C53,54,55,57, 58,59,60,61, 62,63	CAPACITOR, Ceramic, .1uf	Erie	8121-100-651-104M
D1	DIODE, Silicon		1N4148
L1,3	INDUCTOR, Fixed, 27uh, 10%	Delevan	1025-54
L2	INDUCTOR, Fixed, 47uh, 10%	Delevan	1025-60
L4	INDUCTOR, Fixed, 150uh, 10%	Delevan	1025-72
L5,6	INDUCTOR, Variable, 33uh	Cambion	7107-31

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
L7	INDUCTOR, Variable, 150uh	Cambion	7107-39
L8,9	INDUCTOR, Fixed, 1000uh, 10%	Delevan	2307-105
Q1	TRANSISTOR, Silicon		2N3904
Q2,3	TRANSISTOR, Silicon		2N2905
Q4,5,6	TRANSISTOR, Silicon		2N3904
R1	RESISTOR, Fixed, 51 ohms, 5%, 1/4W		RC07GF510J
R2,6,8	RESISTOR, Fixed, 330 ohms, 5%, 1/4W		RC07GF331J
R3,4,7	RESISTOR, Fixed, 47 ohms, 5%, 1/4W		RC07GF470J
R5,25,53	RESISTOR, Fixed, 1K, 5%, 1/4W		RC07GF102J
R9	RESISTOR, Fixed, 10K, 5%, 1/4W		62PR10K
R10	RESISTOR, Fixed, 4.64K, 5%, 1/4W		RN55D4641D
R11	RESISTOR, Fixed, 13.7K, 5%, 1/4W		RN55D1372D
R12	RESISTOR, Variable, 1K	Beckman	62PR1K
R13	RESISTOR, Variable, 5K	Beckman	62PR5K
R14,40	RESISTOR, Film, 4.75K, 1%, 1/4W		RN55D4751D
R15,26	RESISTOR, Fixed, 5110 ohms, 1%		RN55D5111D
R16,27	RESISTOR, Fixed, 3920 ohms, 1%		RN55D3921D

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
R17,45	RESISTOR, Fixed, 47K, 5%		RC07GF473J
R18	RESISTOR, Fixed 390 ohms, 5%		RC07GF391J
R19	RESITOR, Fixed, 820 ohms, 5%, 1/4W		RC07GF821J
R20,23	RESISTOR, Fixed, 4.7K, 5%, 1/4W		RC07GF472J
R21	RESISTOR, Fixed, 4640 ohms, 5%, 1/4W		RN55D4641D
R22	RESISTOR, Variable, 500 ohms, 1%, 1/4W	Beckman	62PR500
R24	RESISTOR, Fixed, 15K, 5%, 1/4W		RC07GF153J
R28	RESISTOR, Fixed, 82K		RC07GF823J
R29	RESISTOR, Variable, 100K	Beckman	62PR100K
R30	RESISTOR, Fixed, 1.3K, 5%, 1/4W		RC07GF132J
R31,34,36,39, 43,48,49	RESISTOR, Fixed, 10K, 5%, 1/4W		RC07GF103J
R32	RESISTOR, Fixed, 1000 ohms, 5%, 1/4W		RC07GF102J
R33	RESISTOR, Variable, 20K	Beckman	62PR20K
R35,59,60,62, 71	RESISTOR, Fixed, 10K, 5%, 1/4W		RC07GF103J
R37,38,41,42, 50	RESISTOR, Fixed, 22K, 5%, 1/4W		RC07GF223J
R44	RESISTOR, Fixed, 270K, 5%, 1/4W		RC07GF273J

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
R46,51,56	RESISTOR, Fixed, 10K ohms, 5%, 1/4W		RC07GF103J
R47	RESISTOR, Fixed, 12K, 5%, 1/4W		RC07GF123J
R52	RESISTOR, Fixed, 13K, 5%, 1/4W		RC07GF132J
R54	RESISTOR, Fixed, 10 ohms, 5%, 1/4W		RC07GF100J
R55	RESISTOR, Composition, 2.7 ohms, 5%, 1/4W		RC07GF2R7J
R57,61,64,67, 68,69,70,72, 73	RESISTOR, Composition, 100K, 5%,, 1/4W		RC07GF104J
R58,63	RESISTOR, Composition, 6.8K ohms, 5%, 1/4W		RC07GF682J
R65	RESISTOR, Composition, 12K, 5%, 1/4W		RC07GF123J
R66	RESISTOR, Composition, 470 ohms, 5%, 1/4W		RC07GF471J
T1	TRANSFORMER	Alladin	65-139
U1,2,3	INTEGRATED CIRCUIT, IF Amp	Plessey	SL612C
U4	INTEGRATED CIRCUIT, Detector	Plessey	SL623C
U5,7	INTEGRATED CIRCUIT, VCO	Rohm	XR-2207
U6	INTEGRATED CIRCUIT, IF Detector	RCA	CA2111AE
U8	INTEGRATED CIRCUIT, AGC	Plessey	SL621C
U9	INTEGRATED CIRCUIT, Voltage Regulator	Fairchild	78L06AWC

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
U10,11,12,13	INTEGRATED CIRCUIT, Dual Op/Amp		1458
U14	INTEGRATED CIRCUIT, 1 Shot	Mot	MC851P
U15,17	INTEGRATED CIRCUIT		CD4052
U16	INTEGRATED CIRCUIT		CD4051B
U18	INTEGRATED CIRCUIT		74C157
U19	INTGRATED CIRCUIT		7407
U20	INTEGRATED CIRCUIT		LM380-N-8
U21	INTEGRATED CIRCUIT		79M05AHC
Z1	MIXER	Mini-Ckt	SRA-8
Z2	FILTER	Vernitron	TL6D11-12A

OPTION 8

Option 8 provides for the selection of 2 bandwidths (6 kHz and 35 kHz) in the sub carrier receiver via a front panel switch. Option 8 also provides a sub carrier audio output via a BNC connector. This is accomplished by adding two sub assemblies to the standard sub carrier receiver module. (A11B1 and A11B2).

Refer to schematic diagrams 81A111-1039 and 81R110-1038 and component layout 81B110-1369.

The A11B1 sub assembly provides an audio amplifier which gets its input from switch S1 in the sub carrier receiver module and outputs this audio via pin 6. This pin 6 then connects to the BNC connector on the PR-700 Receiver's side rail assembly. This audio assembly is identical to the A1B1A3 module inn the PR-700A or B receiver therefore refer to that assembly for maintenance information.

The A11B2 assembly provides for the selection of 2 differenct audio bandwidths by selecting between 2 ceramic filters FL-1 or FL-2 using PIN diode switches. If -12V is applied to pin 8 via the front panel bandwidth select switch then FL-1 filter (6 kHz) is connected in the sub carrier module by forward biasing diodes D1 and D2.

If +12V is applied to pin 8 via the front bandwidth selector switch then FL-2 (35 kHz) is connected in the sub carrier module by forward biasing diodes D3 and D4.

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
OPTION 8, SELECTABLE SC BANDWIDTH			
A1B1			
	Add the following components		
S11	SWITCH		SF-22-SCW-191 or JMT 2223
A11			
	Add the following components		
Z2	FILTER	Vernitron	TL6D11-12A
A11B1			
C1,2	CAPACITOR, Ceramic, .1uf, 20%, 100V	Erie	8121-100-651-104M
C3,4	CAPACITOR, Tantalum, 6.8uf, 10%, 16V	Kemet	T310B226K0-15AS
D1,2,3,4	DIODE		MPN 3402
FL-1	FILTER, Ceramic,	Vernitron	TL6D11-12A
FL-2	FILTER, Ceramic,	Vernitron	
R1,2,3,4,5,6	RESISTOR, Composition, 3K ohms, 5%, 1/4W		RC07Gf302J
A11B2			
C1	CAPACITOR, .001uf, 20%, 100V	Erie	8121-100-651-105
C2	CAPACITOR, 22uf, 15V	Kemet	T310B226KL015AS
C3	CAPACITOR, 4.7uf, 1%v	Kemet	T310B475K015AS
R1	RESISTOR, Composition, 2.7K, 5%, 1/4W		RC07GF272J
R2	RESISTOR, Composition, 470 ohms, 5%, 1/4W		RC07GF471J
U1	INTEGRATED CIRCUIT		LM380N-8

OPTION 9

Option 9 provides a front panel audio squelch or threshold control. This is accomplished by replacing the normal audio board (A1B1A3) withh an A5 PC board which provides both an audio amplifier and an audio threshold circuit.

Refer to schematic diagram 81B50-1034 and component layout 81A50-1320.

The audio from the front panel audio control enters on J1 pin 1 and is applied to the gate of FET amplifier Q2.

The NB AM output is connected to buffer amplifier U1 Pin 3 and then rectified by diode D1 and filtered by R2 and C3. The resulting DC voltage is then applied to the noninverting input of U1 (pin 6). A variable DC voltage from the front panel threshold control enters on pin 4 and is applied to the other input of U1 (pin 5). As long as the DC voltage generated by the NB AM input is larger than the DC voltage set by the threshold control the output of U1 at pin 7 is positive and FED switch Q1 is turned off, and the audio present at the gate of Q2 passes on to audio amplifier U2 and out J1. If the threshold voltage on U1 pin 5 is greater than the voltage on pin 6 then the output at U1 pin 7 is approximately -12V and Q1 is turned on thus shorting the audio present at Q2 gate to ground. This prevents the audio from getting to audio amplifier U2 thus providing an audio squelch.

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
OPTION 9			
A1B1			
	Add the following components		
R23	RESISTOR, Variable,	RV6NAYSD103A	
A5, Audio/Squelch			
A5J1	CONNECTOR	Cinnch	DEM9P
C2,3	CAPACITOR, Tantalum, 1uf, 35V	Kemet	T310A-106-K-035AS
C4	CAPACITOR, Ceramic, .1uf, 20%, 50V	Erie	8121-M050-651-104M
C5,7,9,10,11	CAPACITOR, Tantalum, 22uf, 15V	Kemt	T310B226K015AS
C6	CAPACITOR, Ceramic, .001uf, 100V	Spr	5GA-D10
C8	CAPACITOR, Tantalum, 4.7uf, 15V	Kemet	T310B475015AS
D1,2	DIODE		1N4148
E1 thru E8	TERMINALS		2520-B-1
Q1,2	TRANSISTOR	Motorola	2N5459
R1	RESISTOR, Composition, 220K, 5%, 1/4W		RC07GF224J
R2	RESISTOR, Composition, 10K, 5%, 1/4W		RC07GF103J
R3	RESISTOR, Composition, 750K, 5%, 1/4W		RC07GF754J
R4	RESISTOR, Composition, 100K, 5%, 1/4W		RC07GF104J

REF. DESIGN.	DESCRIPTION	MFR.	DRAWING/ PART NO.
R5	RESISTOR, Composition, 10M, 5%, 1/4W		RC07GF106J
R6	RESISTOR, Composition, 1M,5%, 1/4W		RC07GF105J
R7	RESISTOR, Composition, 1K, 5%, 1/4W		RC07GF102J
R8	RESISTOR, Composition, 680 ohms, 5%, 1/4W		RC07GF681J
R9	RESISTOR, Composition, 51K, 5%, 1/4W		RC07GF513J
U1	INTEGRATED CIRCUIT		1458
U2	INTEGRATED CIRCUIT		LM380N-8

40 MHz IN

55.7 MHz IN

A3DIA1
40/10.7 MHz
CONVERTER

+12V

A3DIA2
10.7 MHz (2 MHz BW) IF
IF AMP

2 MHz AM

2 MHz FM

A3DIA3
10.7 MHz (150 KHz BW) IF
IF AMP

150 KHz AM

150 KHz FM

A3DIA4
10.7 MHz (15 KHz BW) IF
IF AMP

A3DIA5
10.7 MHz (5 KHz BW) IF
IF AMP

AGC

25

24

25
+12 CW

L3
RCT
LO IN

TUNING METER

AGC ON/OFF

-12VDC

+12VDC

5W SELECT

2 MHz

150 KHz

15 KHz

2 KHz

FM PRE-D OUT

SC PRE-D ON

AM PRE-D ON

SC AUDIO IN

J9
MS FM VIDEO OUT

CH QUAD

SC SELECTOR

AM

FM

D37
1N4148
R222
150K

+12 (2 MHz)

+12 (150 KHz)

+12 (15 KHz)

+12 (2 KHz)

D36
1N4148
R221
75K

D35
1N4148
R220
91K

FM SUM AMP

AM SUM AMP

AUDIO SELECTOR/AMP

R223
5.1K
1/4W

FM VIDEO

AFC

938 AGC DET/AMP

3/15 KHz AM

10.7 OSC

MAN/AGC SWITCH

GAIN

NB AGC

NB GAIN

150 KHz GAIN

2 MHz GAIN

150 KHz AGC

2 MHz AGC

AGC AMP

MUTE

3/15 KHz FM

REF

FM

A- REV PER CO NO'S 562, 563 & 569 WM 5/2/85 LF
B- REV PER CO NO'S 567, 570, 571, 572, 573 7/23/85 WM

PAN VIDEO IF
A3BIA7

SC AUDIO IN 12 | AFC OUT 14 | AUDIO OUT 16 | IF GAIN ARM 15 | IF GAIN HI 14 | IF GAIN LO 17 | AUDIO SELECT: AM 19, FM 20, SC 21, CW/SSB 22

J6 VID FM VIDEO OUT

J6 13.5 MHz IN

13.5 MHz (10 KHz BW) IF FILTER

+5V R300 1.2K

FL17 17 | FL33 33 | FL34 34

L307, 100μh

R280 100K, R282 51, C281 .1, C283 .1, R284 220
C301 27pf, Z13 3KHz, C304 22pf
Q100 SD201, Q101 SD201
L301 4.7μh, L304 4.7μh
R281 67K, R283 120
C280 .01

L308, 100μh

C196 .1, R195 150K, L200 5.2μh, C307 27pf
C195 .001, C203 .01, C285 .01, C290 .01
Q20 SD201
R196 150K
R285 100K, R287 51, C286 .1, C288 .1, R288 220
C302 47pf, Z14 10KHz, C305 47pf
Q102 SD201, Q103 SD201
L302 3.1μh, L305 3.1μh
R286 67K, R289 120

L309, 100μh

R290 100K, R292 51, C291 .1, C294 .1, R293 220
C303 33pf, Z15 35KHz, C306 22pf
Q104 SD201, Q105 SD201
L303 5.2μh, L306 5.2μh
R291 67K, R294 120

C295 .01

IF AMP | FILTER | IF AMP

C197 .1, R164 10, +5, R167 10
FL27, FL28, FL29
R179 10, C179 .01, L201 WBC, C151 .1
R161 150K, C149 100pf, Q18 SD201, R163 150K
R181 10, R182 10
C157 180pf, C181 .01, C182 .01
U28 SL612, U29 SL611
C152 .001, R166 100, L29, C154 9pf, C156 3.5/20pf
C153 180pf

R199 1K, R200 1K

R207, 10K

FL23 29
FL14 14 VIDEO GAIN CONTROL
FL28 28 -12V S,V5 3-7
FL26 26 +5V SYN 1-7, 3, V5 1-2
FL27 27 +5V S,V5 3-7
FL30 30 +5V
FL31 31 LOG/LIN
J7 PAN VIDEO
FL46 FL32 32 -6V

10.7 MHz (200 KHz BW) IF
IF AMP | FILTER | IF AMP | FILTER | IF AMP | LOG AMP | VIDEO DET | VIDEO SELECT SWITCH

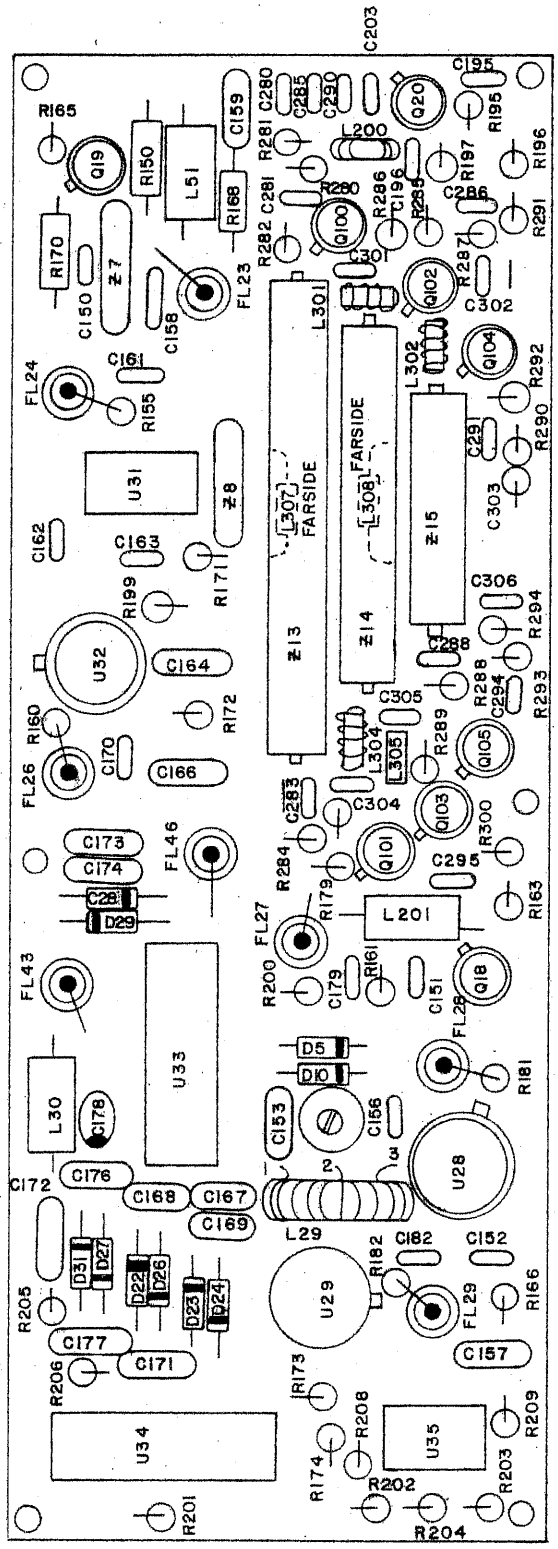
R169 12, +12
FL23, FL24, FL26
C158 .1, L81 WDL, Q19 SD201H
R150 150K, R168 330, C150 .01, R170 220, C159 10pf
27 CERAMIC FIL, 28 CERAMIC FIL
R224 15K, R155 10
U31 UA753, C161 .01, C162 .01
R171 1.2K
C164 180pf, U32 SL612, R160 10, C170 .01, R172, 100, C166, 180pf
U33 SN76502
C147 180pf, C168 180pf, D26 IN270, D22 IN270, D24 IN270, C169 180pf, D23 IN270, C171 180pf, C172 180pf
C176, 180pf, D27 IN270, D31 IN270, C177 180pf
C173, 180pf, D28, IN270, D29 IN270, C174 180pf
L30, 47μh, C178 56, R173 47K
U34 CD4053AD
R205 4.7K, R206 10K, R204 1K, R208 10K, R209 10K, R202 47K, R203 47K
FL55, R174 5W

NOTES:
1. ALL RESISTORS 1/4W UNLESS OTHERWISE SPECIFIED.
2. ALL RESISTANCES IN OHMS.
3. ALL CAPACITANCES IN μF UNLESS OTHERWISE SPECIFIED.

(OPT. 1)

PR-700A
A3BI - SCHEMATIC,
IF

81B31-082 B



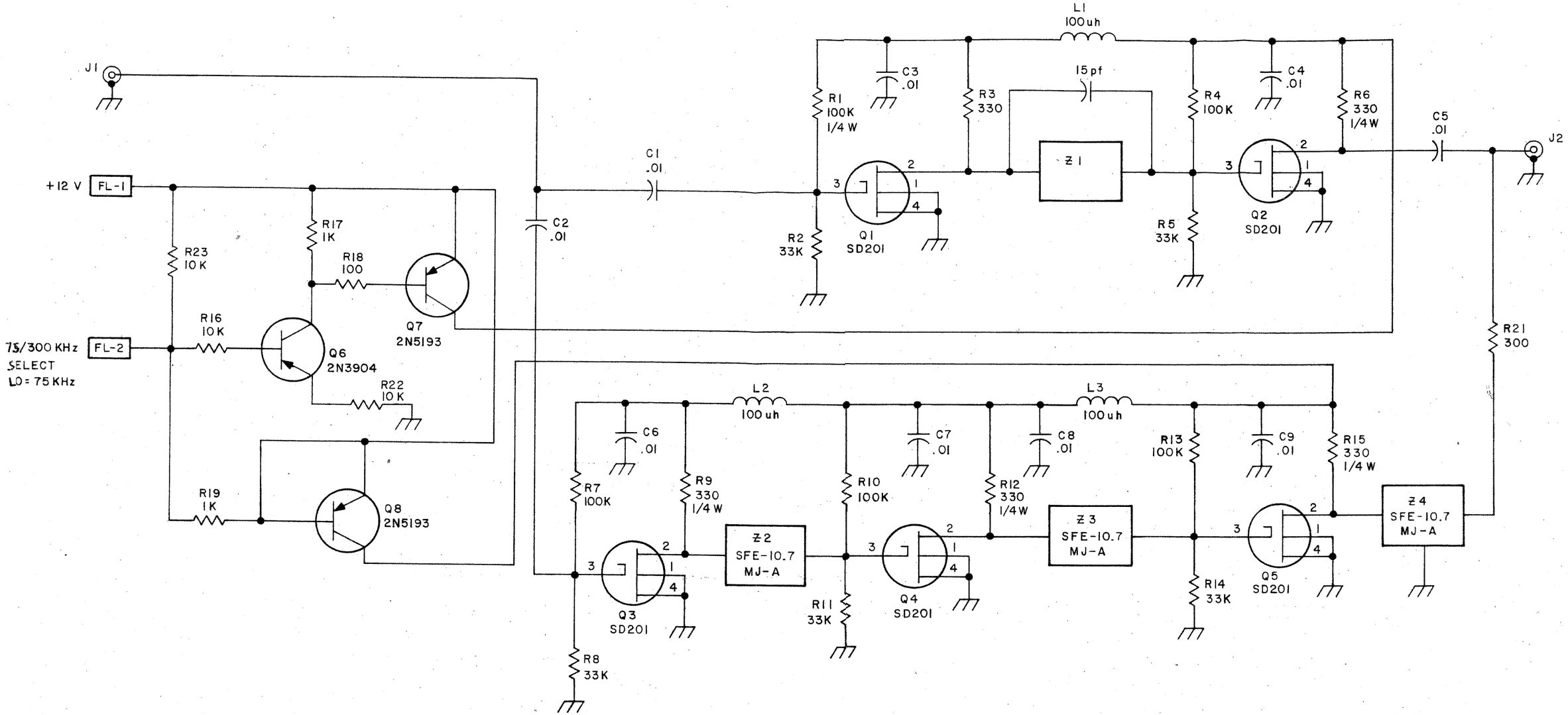
(OPTION I)

PR7.00A

A3B1A7-COMPONENT LOCATION

VIDEO I.F.

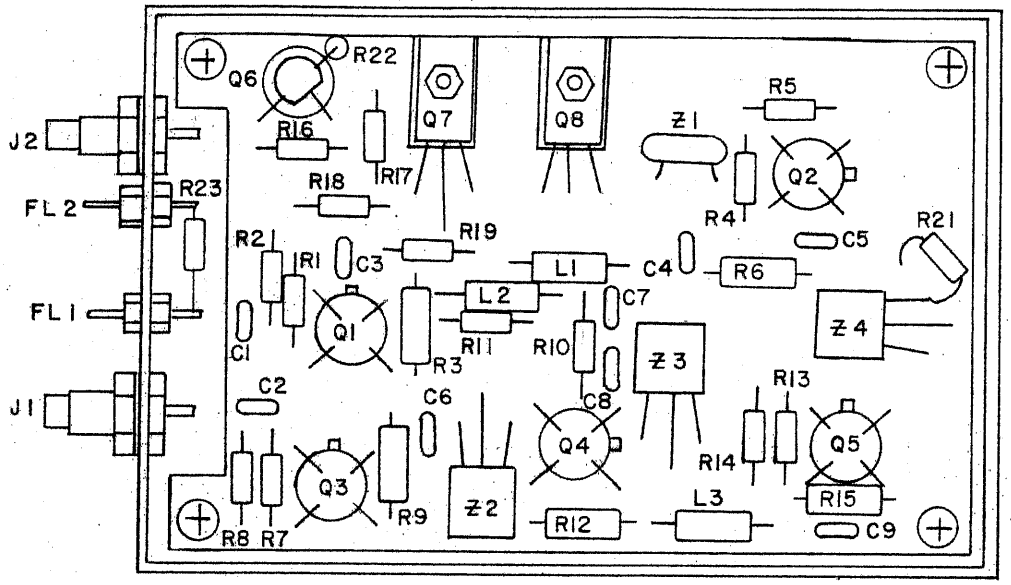
81A317-184



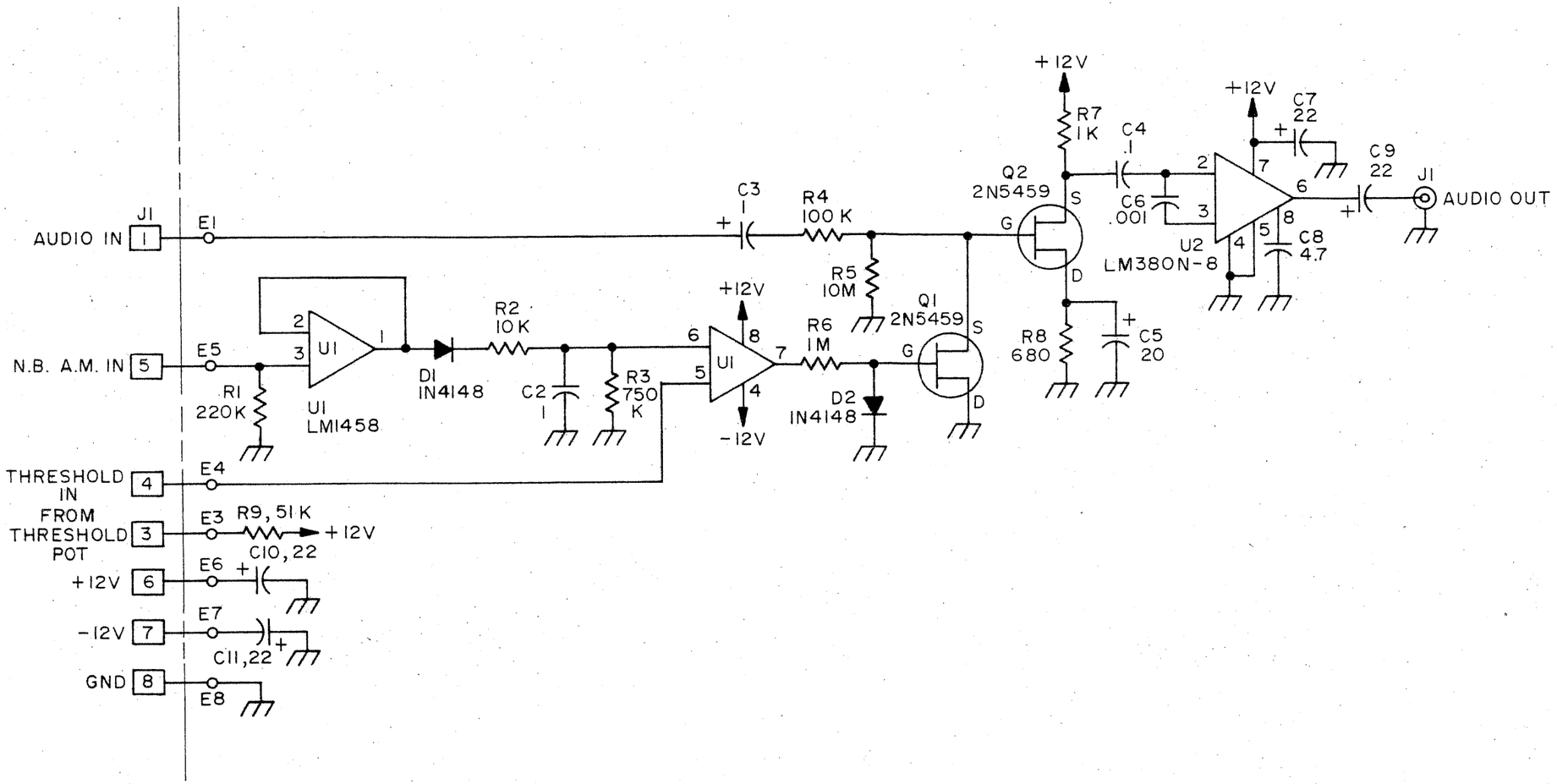
REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C9 FL-2 J2 L3 Q8 R23 Z4	R20

UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE IN OHMS, AND ARE 1/8 W
ALL CAPACITORS ARE IN MICRO-FARADS

PR-700(OPT.4)
A3B5 - SCHEMATIC
SEL IF BW
81B35-064



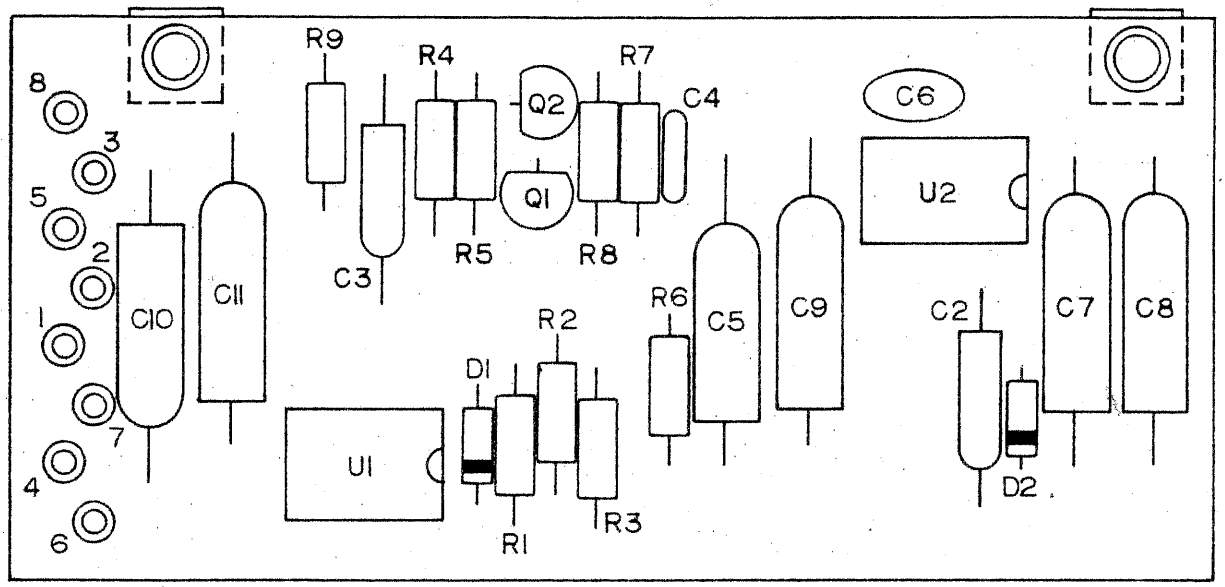
PR 700 (OPT. 4)
A3B5- COMPONENT LOCATION
SEL IF BW
81A35-1368



REF DESIGNATIONS	
LAST USED	NOT USED
C11 D2 E8 J1 Q2 R9 U2	C1 E2

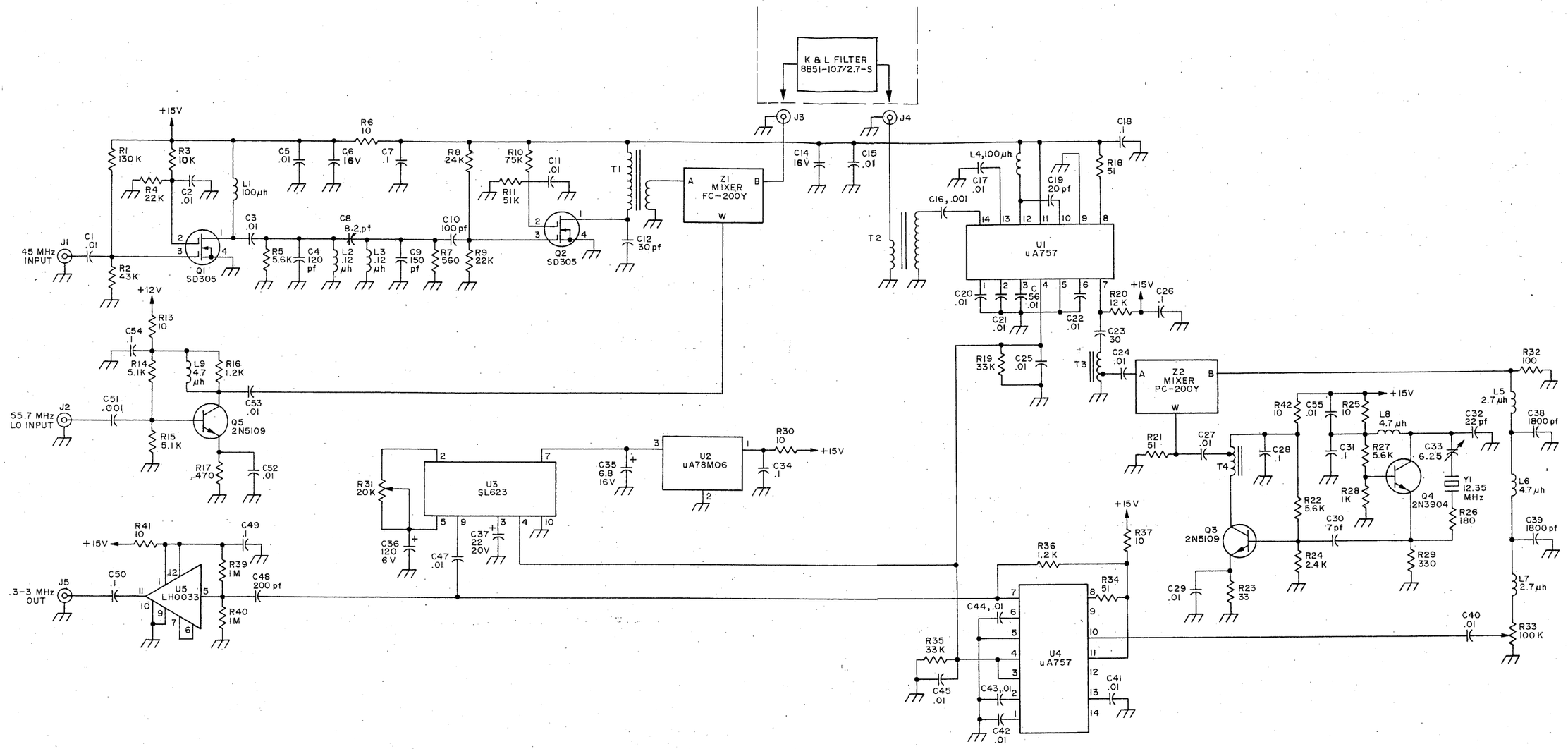
UNLESS OTHERWISE SPECIFIED:
ALL RESISTOR VALUES ARE IN OHMS AND 1/4 W.
ALL CAPACITOR VALUES ARE IN MICROFARADS.

PR-700 (OPT. 9), PR-707
A5 – SCHEMATIC,
AUDIO/SQUELCH
81B50-1034



PR-700 (OPT. 9), PR-707
A5-COMPONENT LOCATIONS,
AUDIO/SQUELCH

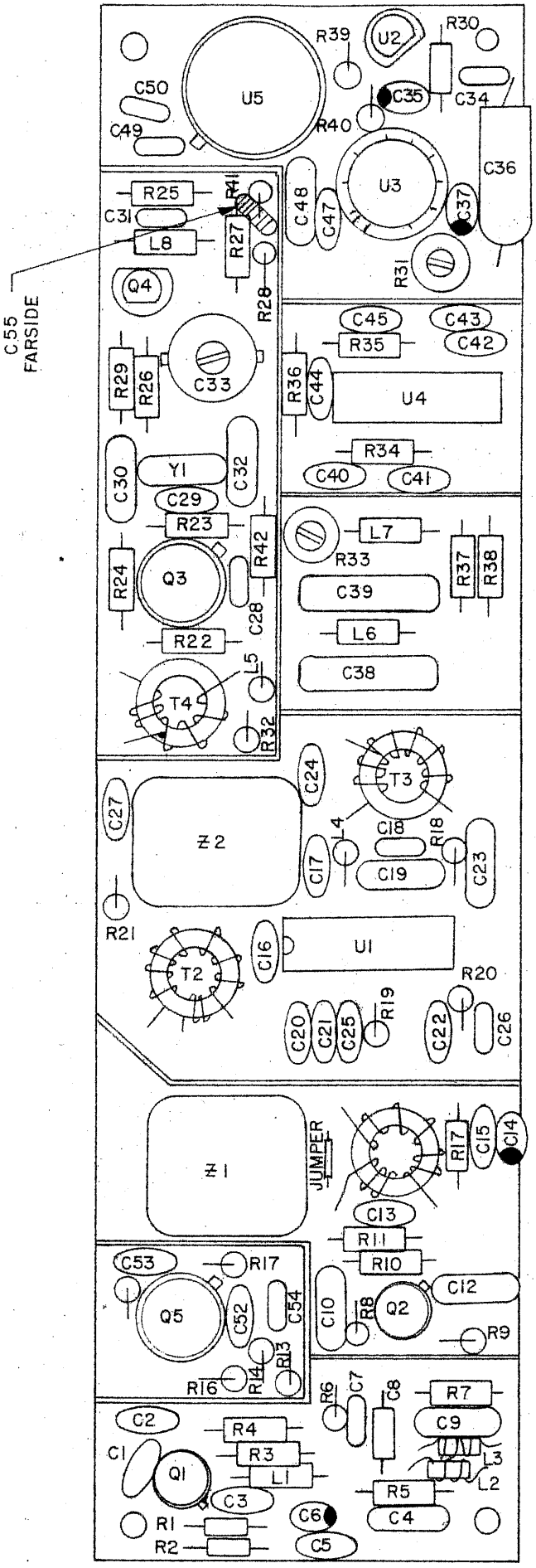
81A50-1320



REF DESIGNATIONS	
LAST USED	NOT USED
C56	C13, 46
J5	
L9	
Q5	
R42	R12, 38
T4	
U5	
Y1	
Z2	

UNLESS OTHERWISE SPECIFIED:
ALL RESISTOR VALUES ARE IN OHMS & 1/4 W.
ALL CAPACITOR VALUES ARE IN MICROFARADS.

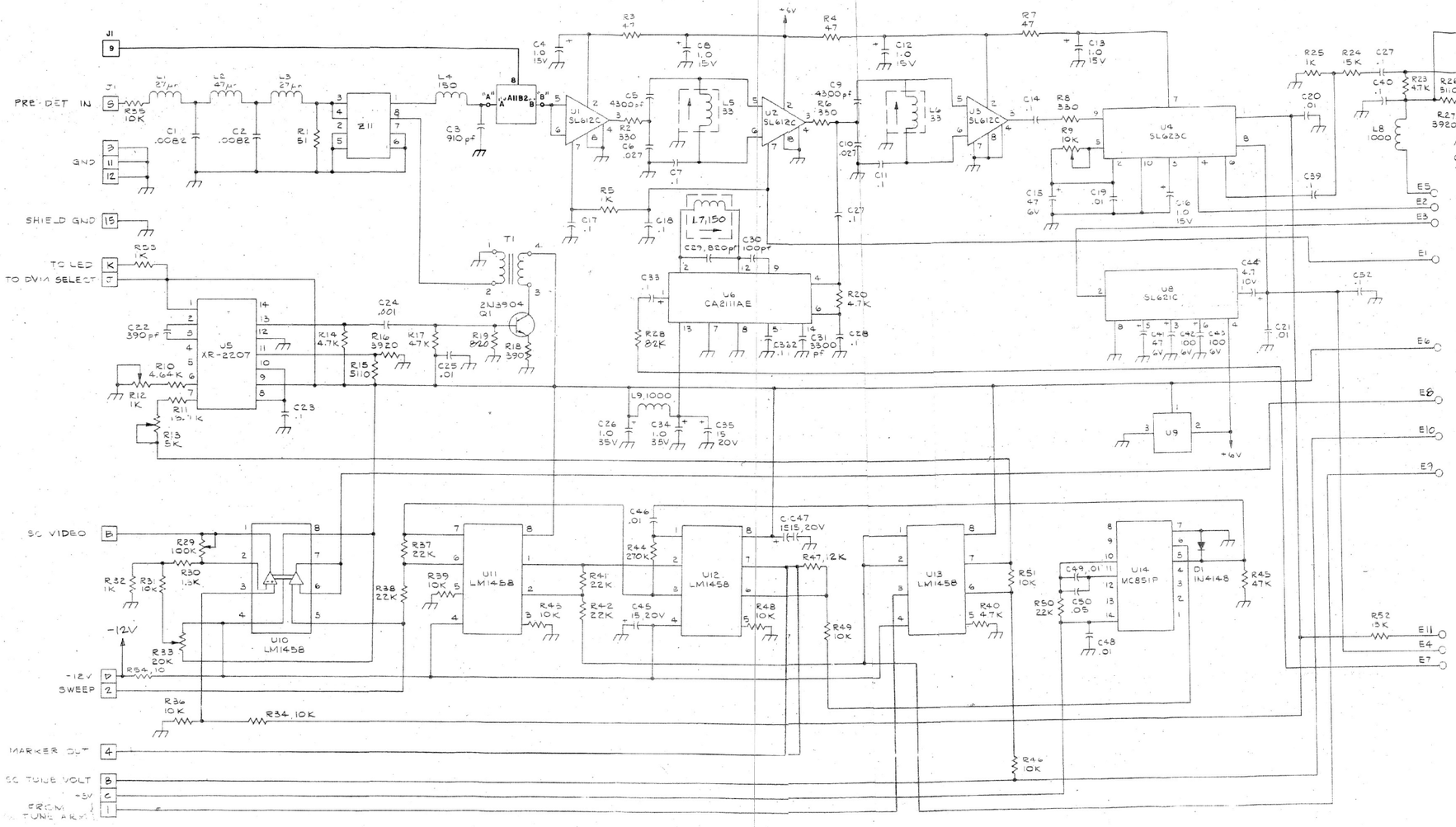
PR-700(OPT. 6), PR-707
A7 – SCHEMATIC,
TAPE CONVERTER
81D70-1035



PR-700(OPT.6), PR-707
A7-COMPONENT LOCATION,
TAPE CONVERTER
81B70-1321

C.O. 314 2/11/82 JFF

CO 432 6-23-83 W.B.



REF DESIGNATIONS	
LAST	NOT USED
L9	
Z2	
U21	
S	
T1	
Q2	
R73	
C65	
E	

UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCES ARE IN OHMS
ALL RESISTORS ARE 1/4 W
ALL CAPACITORS ARE IN MICROFARADS

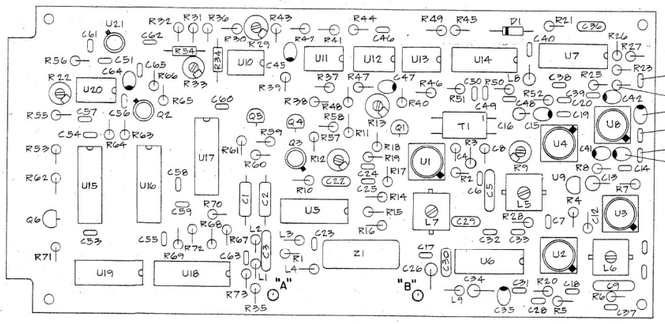
(OPT 7 & 8)

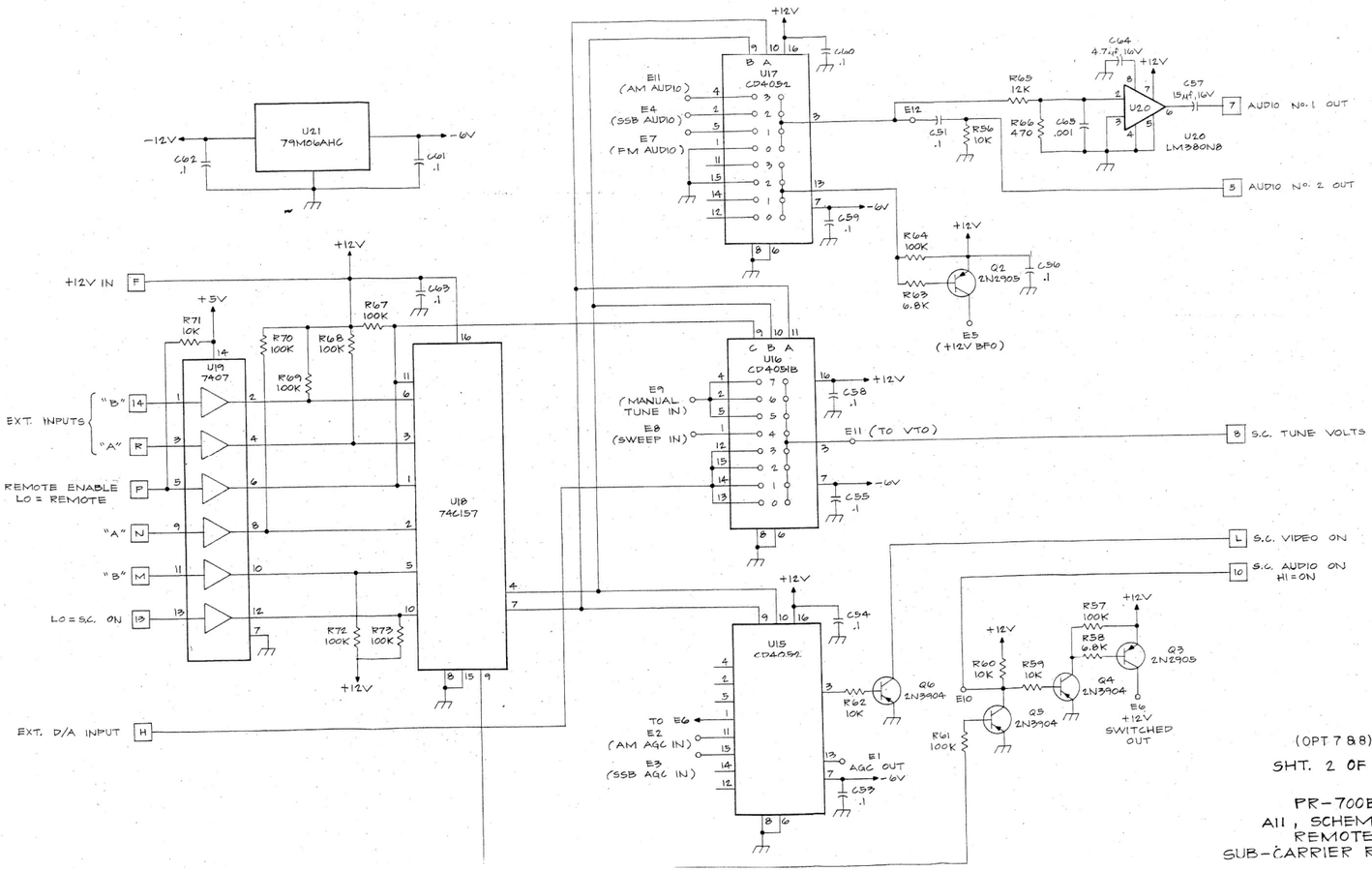
SHT. 1 OF 2

PR-700B
A11, SCHEMATIC
REMOTE
SUB-CARRIER RECEIVER

81R110-063

C.O. 237 1/11/82 MF
C.O. 301 2/11/83 MF
C.O. 432 6-23-83 G.B.

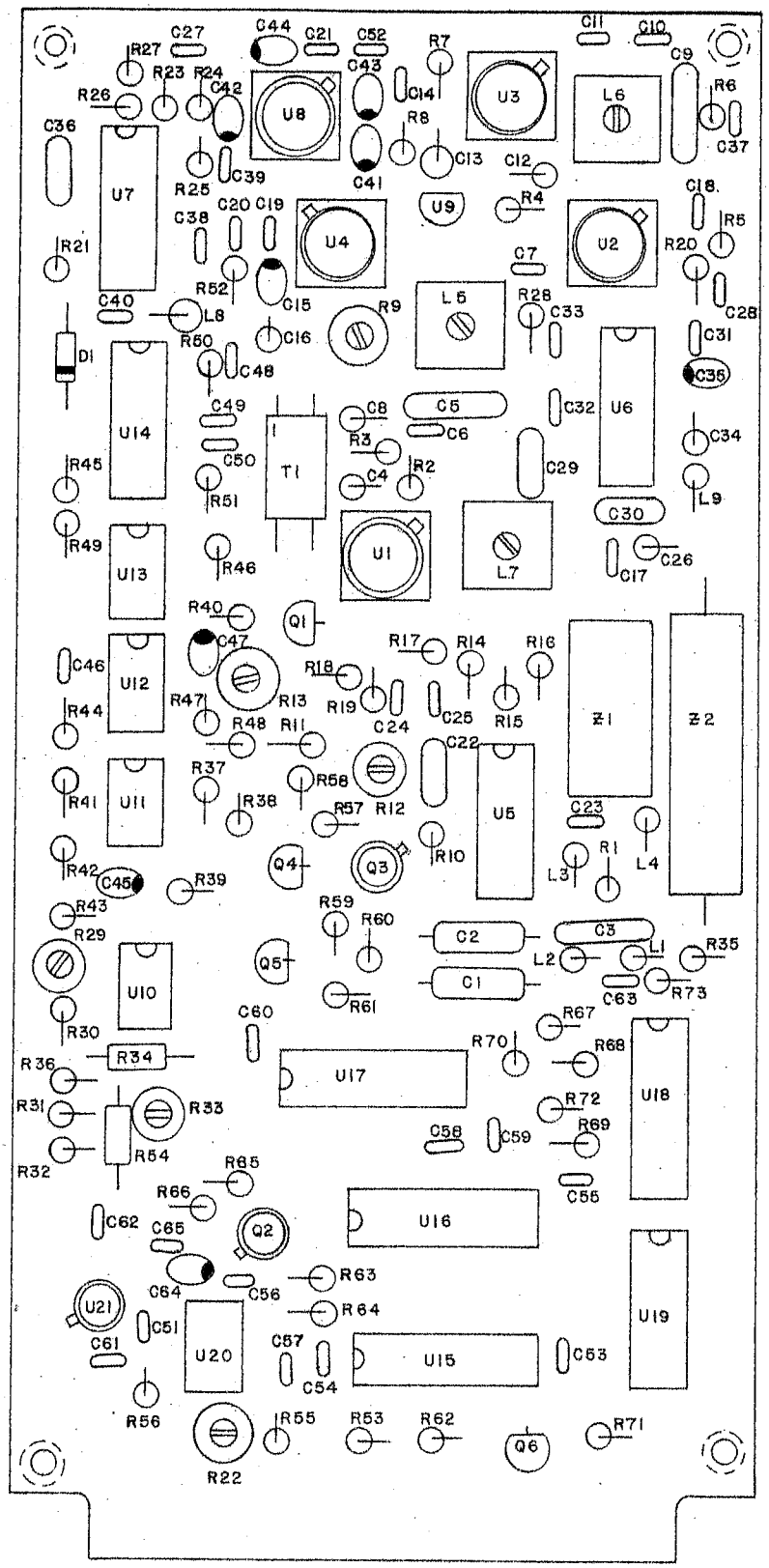




(OPT 7 & 8)

SHT. 2 OF 2

PR-700B
A11, SCHEMATIC
REMOTE
SUB-CARRIER RECEIVER



PR700 (OPT. 7)
ALL-COMPONENT LOCATION
SUB-CARRIER. RCV'R ASS'Y
81A110-1370

REV. A PER. CO. NO. 428 4/14/83 WMW

PRE-DET IN J1 L
GND 5
SHIELD GND 10
TO LED H
TO DVM SELECT 4
SC VIDEO C
-12V SWEEP E 4
MARKER OUT K
SC TUNE VOLT 9
+5V D
7

L1 27μH
L2 47μH
L3 27μH
L4 150
R35 10K
C1 .0082
C2 .0082
R1 51
Z1
C3 910pf
B1A112-1040
A1182
C4 1.0 15V
C8 1.0 15V
C12 1.0 15V
C13 1.0 15V
+6V
R4 4.7
R7 47
U1 SL612C
U2 SL612C
U3 SL612C
C5 4300pf
L5 33
C6 .027
C7 .1
C9 4300 pf
R6 330
L6 33
C10 .027
C11 .1
R2 330
R3 330
C14 .1
R8 330
R9 10K
U4 SL623C
C15 47 6V
C19 .01
C16 1.0 15V
R5 K
C17 .1
C18 .1
L7 150
C29 820pf
C30 100pf
T1
2N3904 Q1
U6 CA2111AE
C33 .1
R28 82K
C52 .1 pf
C31 3300
C28 .1
R20 4.7K
U8 SL621C
C44 4.7 10V
C52 .1
C41 47 6V
C42 .100 6V
C43 .100 6V
C21 .01
C24 .1
C22 390pf
U5 XR-2207
R14 4.7K
R16 3920
R17 47K
R19 15K
R18 390
R10 4.7K
R12 1K
R11 10.1K
R15 5K
C25 .01
C23 .1
L9 1000
C26 1.0 35V
C34 1.0 35V
C35 15 20V
U9
+6V
R25 1K
R24 15K
C27 .1
C40 .1
R23 4.7K
R26 5110
R27 3920
C38 .1
L8 1000
C20 .01
C39 .1
U7 XR-2207
C36 390pf
R21 4640
B TO SC BFO CONTROL
E FROM SC BFO CONTROL
R22 500

UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCES ARE IN OHMS
ALL RESISTORS ARE 1/4 W
ALL CAPACITORS ARE IN MICROFARADS

REF DESIGNATIONS	
LAST	NOT USED
L9	
Z1	
U14	
S1	
T1	
D1	
R56	
C52	
E16	

E5
E2
E3
E1
E8
E6
E9
E11
E10
E12
E13
E14
E4
E7
E15

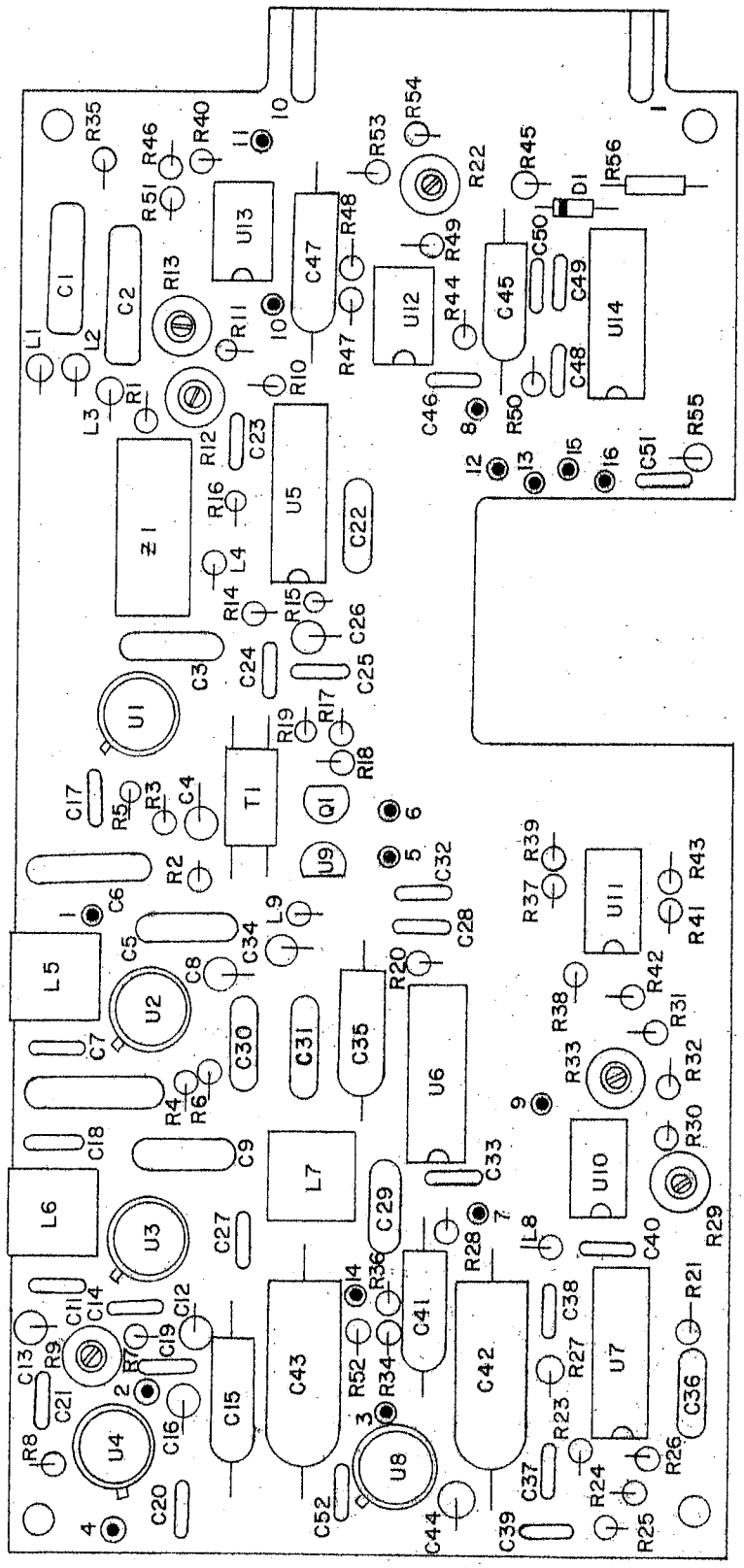
S1-A1 OFF 1 SCAN 2 FM 3 CW/SSB 4 AM 5
S1-A2 OFF 7 SCAN 8 FM 9 CW/SSB 10 AM 11
S1-B1 A 1 2 3 4 5
S1-B2 7 8 9 10 11
S1-C1 A 1 2 3 4 5
S1-C2 7 8 9 10 11

J SC AUDIO ON
2 SC VIDEO OUT
A AUDIO OUT
6
1 +12V

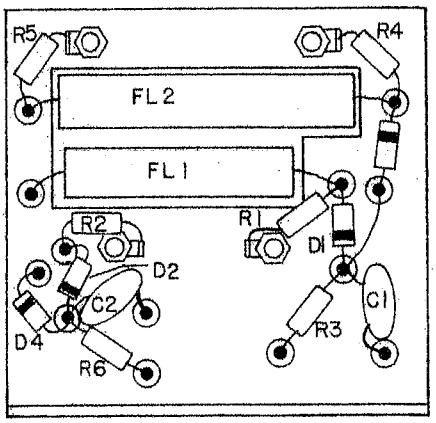
R52 15K
C51 .1
R56 10K
R55 2.7
81A111-1039
A11B1

U10 LM1458
R29 100K
R30 1.3K
R32 1K
R31 10K
R33 20K
R54, 10
R36 10K
R34, 10K
U11 LM1458
R37 22K
R38 22K
R39 10K
R43 10K
U12 LM1458
R41 22K
R44 270K
R42 22K
C45 15, 20V
C46 .01
C47 15, 20V
R47, 12K
R48 10K
R49 10K
U13 LM1458
R51 10K
R40 5 4.7K
R46 10K
U14 MC851P
C49, .01
C50 .05
C48 .01
R50 22K
D1 IN4148
R45 4.7K

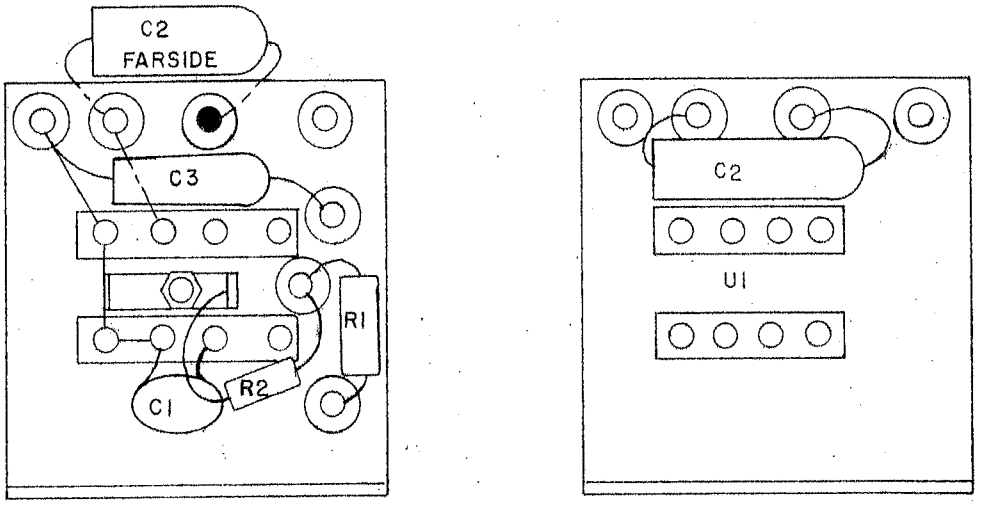
PR700 OPT. 8
A11 - SCHEMATIC,
SUB-CARRIER RECEIVER
81R110-1038



PR700 (OPT. 8)
A1 B1-COMPONENT LOCATION
SUB-CARRIER RCV'R ASS'Y
81B110-1369 SHT 1 OF 2

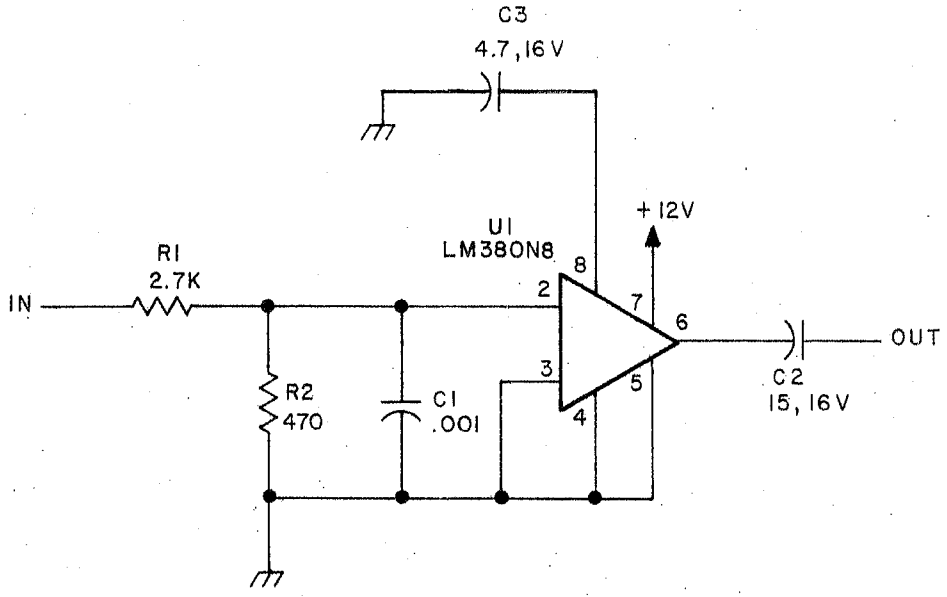


A11B2



A11B1

PR700 (OPT. 8)
A11-COMPONENT LOCATION
SUB-CARRIER RCV'R ASS'Y
81B110-1369 SHT 2 OF 2



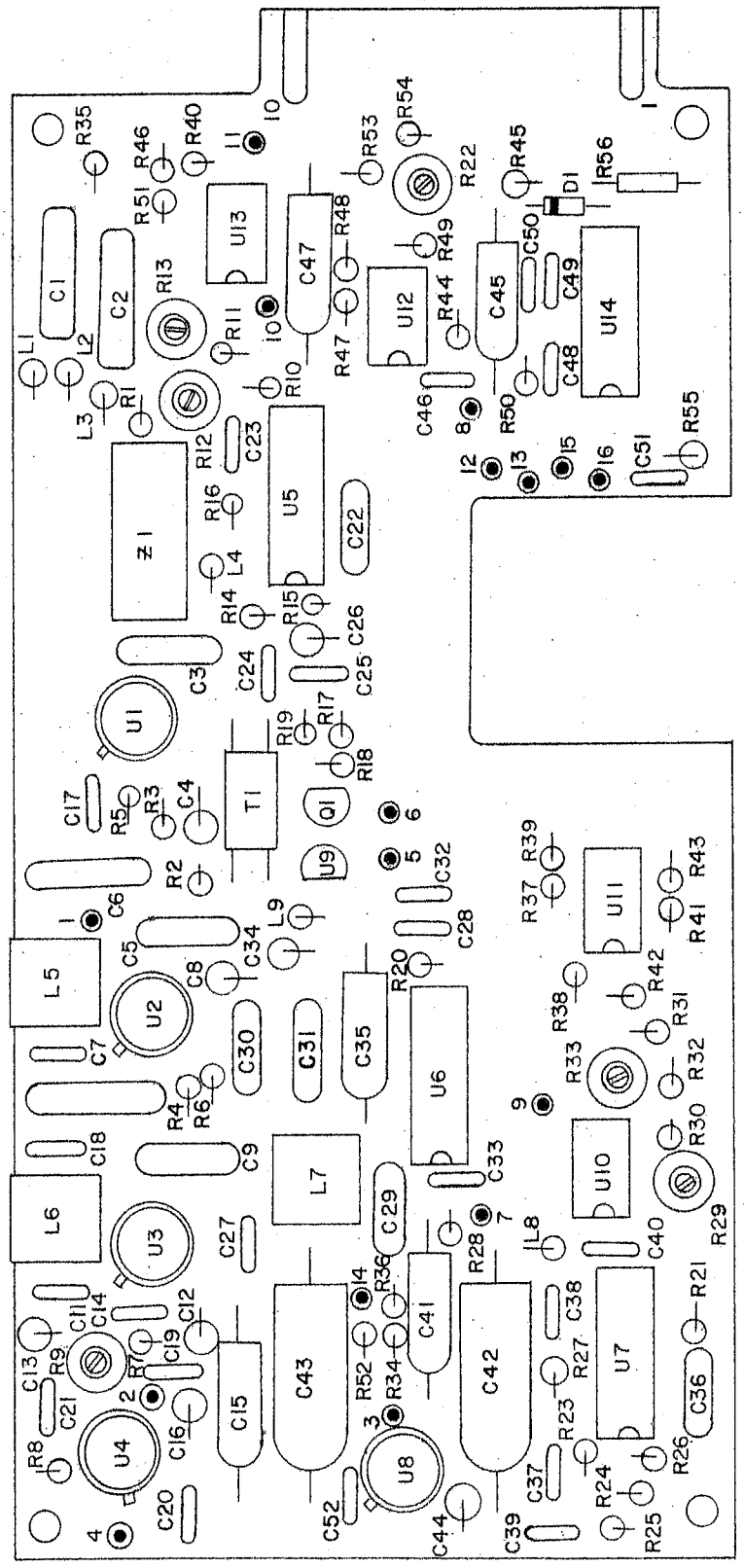
UNLESS OTHERWISE SPECIFIED:

ALL RESISTANCES ARE IN OHMS
ALL RESISTORS 1/4W
ALL CAPACITORS ARE IN MICROFARADS

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C3 R2 U1	

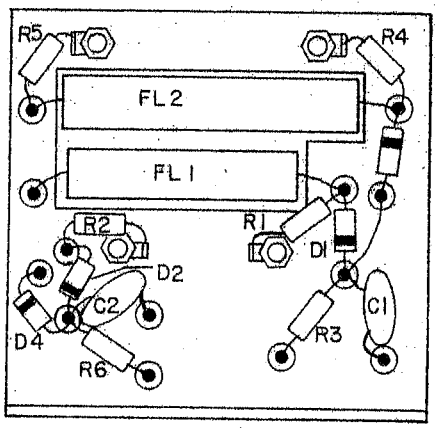
PR-700 (OPT. 8), PR-707
A11B1-SCHEMATIC
SUBCARRIER SUB ASS'Y #1

81A11-1039

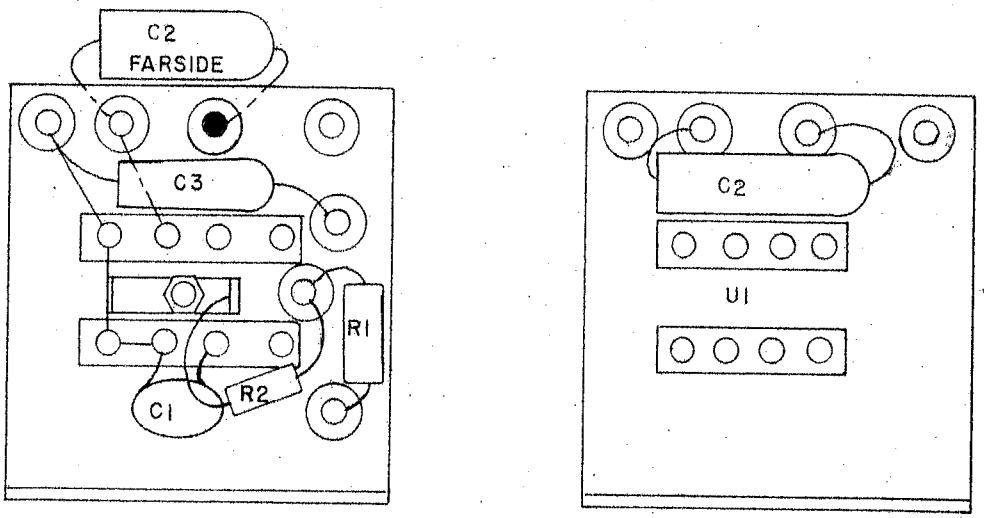


PR700 (OPT. 8)
A11B1-COMPONENT LOCATION
SUB-CARRIER RCV'R ASS'Y

81B110-1369 SHT 1 OF 2

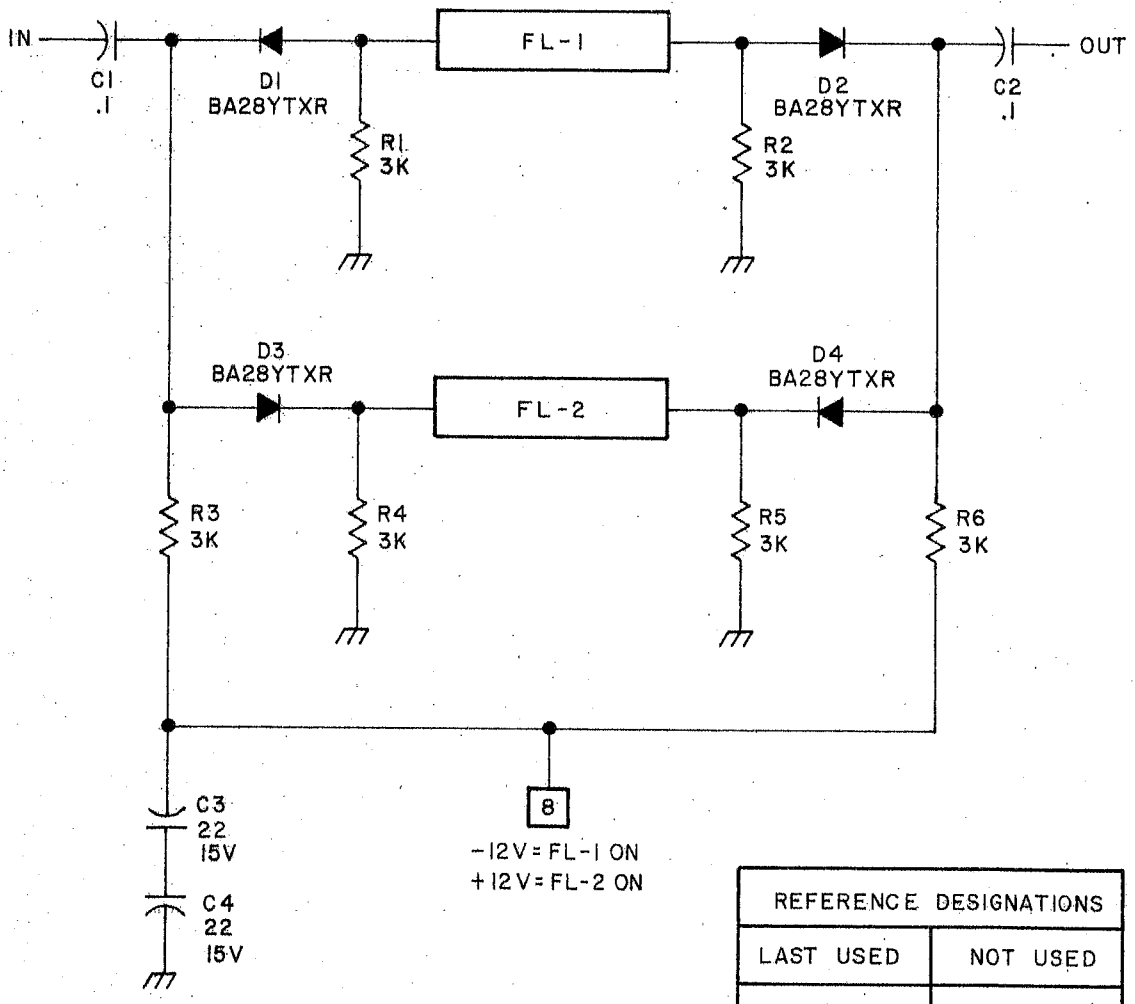


A11B2



A11B1

PR700 (OPT. 8)
A11-COMPONENT LOCATION
SUB-CARRIER RCV'R ASS'Y
81B110-1369 SHT 2 OF 2

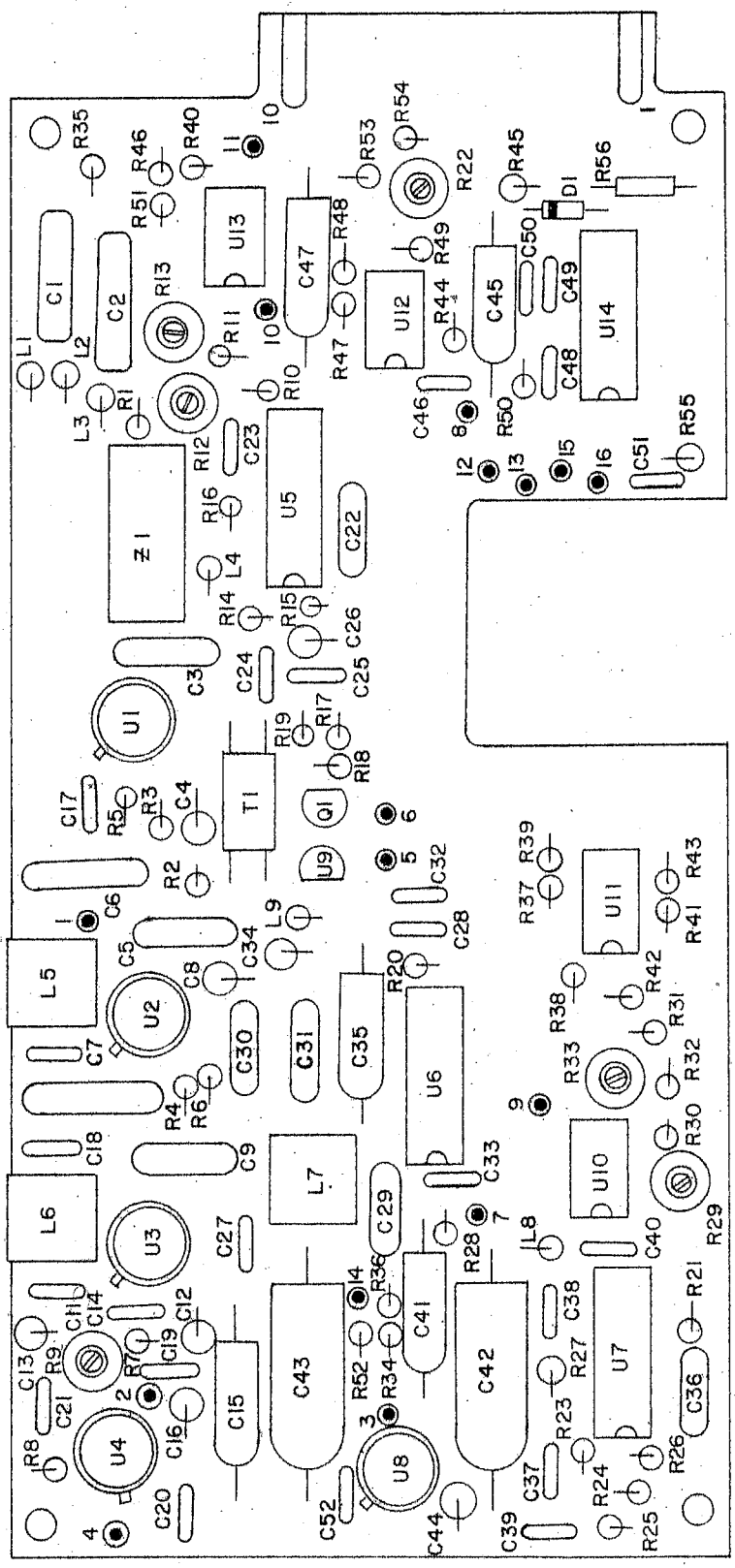


REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C4 D4 FL-2 R6	

UNLESS OTHERWISE SPECIFIED:

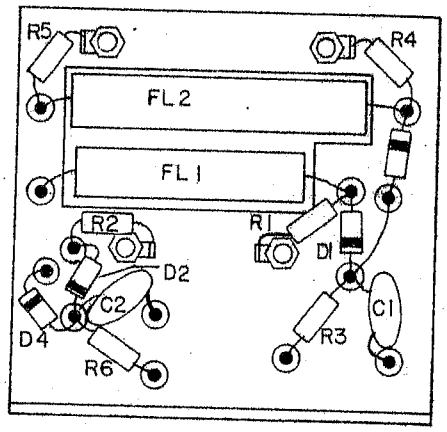
ALL RESISTANCES ARE IN OHMS
ALL RESISTORS ARE 1/4 W
ALL CAPACITORS ARE IN MICROFARADS

PR-700 (OPT. 8), PR-707
A11B2-SCHEMATIC
SUBCARRIER SUB ASS'Y #2
81A112-1040

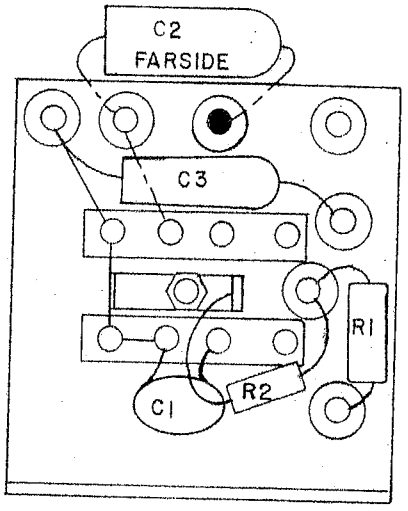


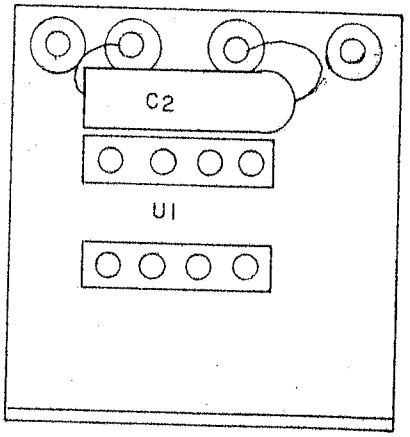
PR700 (OPT. 8)
A1|B1-COMPONENT LOCATION
SUB-CARRIER RCV'R ASS'Y

81B110-1369 SHT 1 OF 2



A11B2

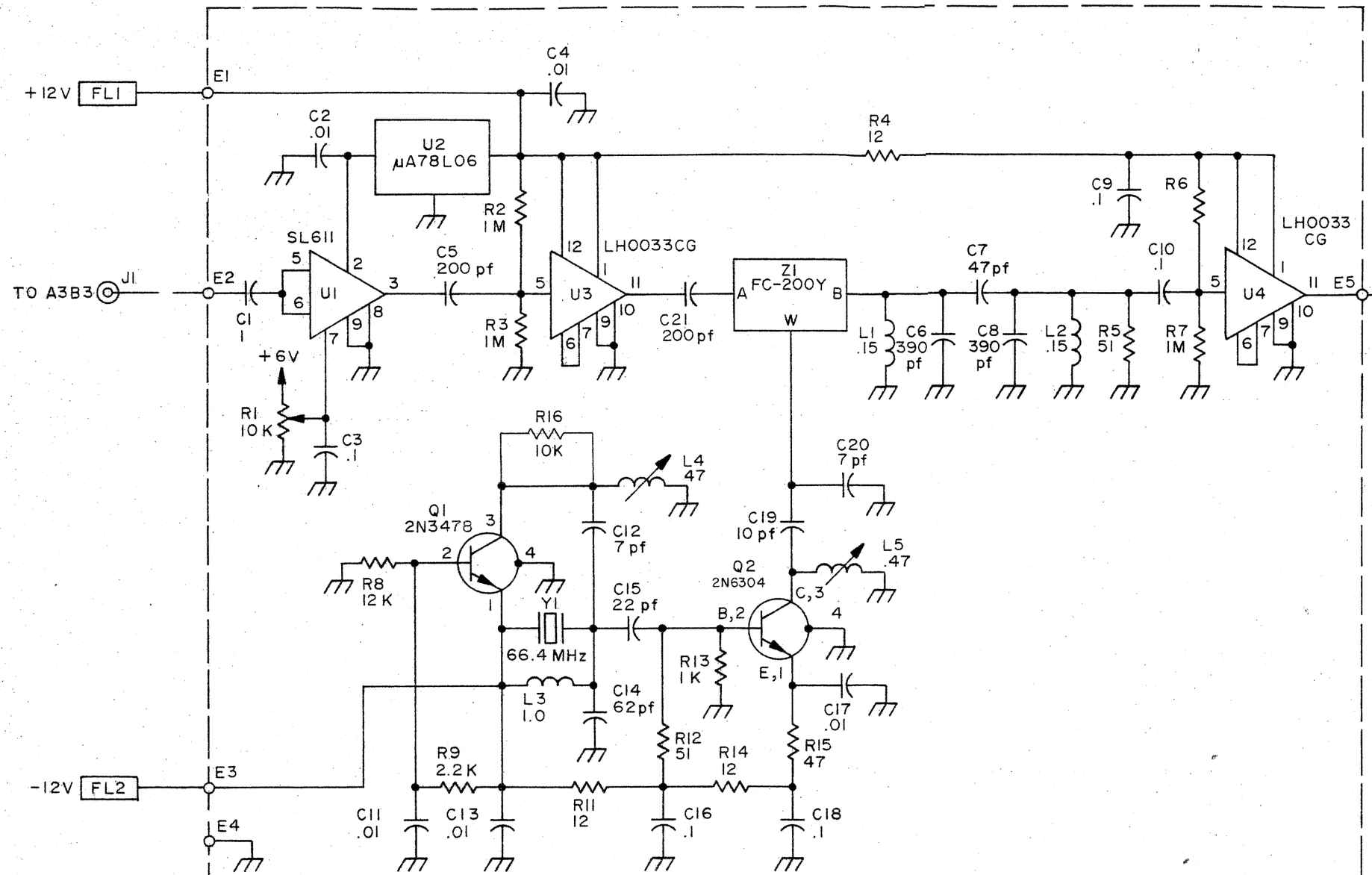




A11B1

PR700 (OPT. 8)
A11-COMPONENT LOCATION
SUB-CARRIER RCV'R ASS'Y
81B110-1369 SHT 2 OF 2

A – EFF. PER	C.O. 215	6·2·80	PS
B –	C.O. 286	6·19·81	L.W. Kraus
C –	C.O. 468	1·24·84	WMW
D –	C.O. 16	9·17·84	WMW
E –	C.O. 579	7·23·85	WMW

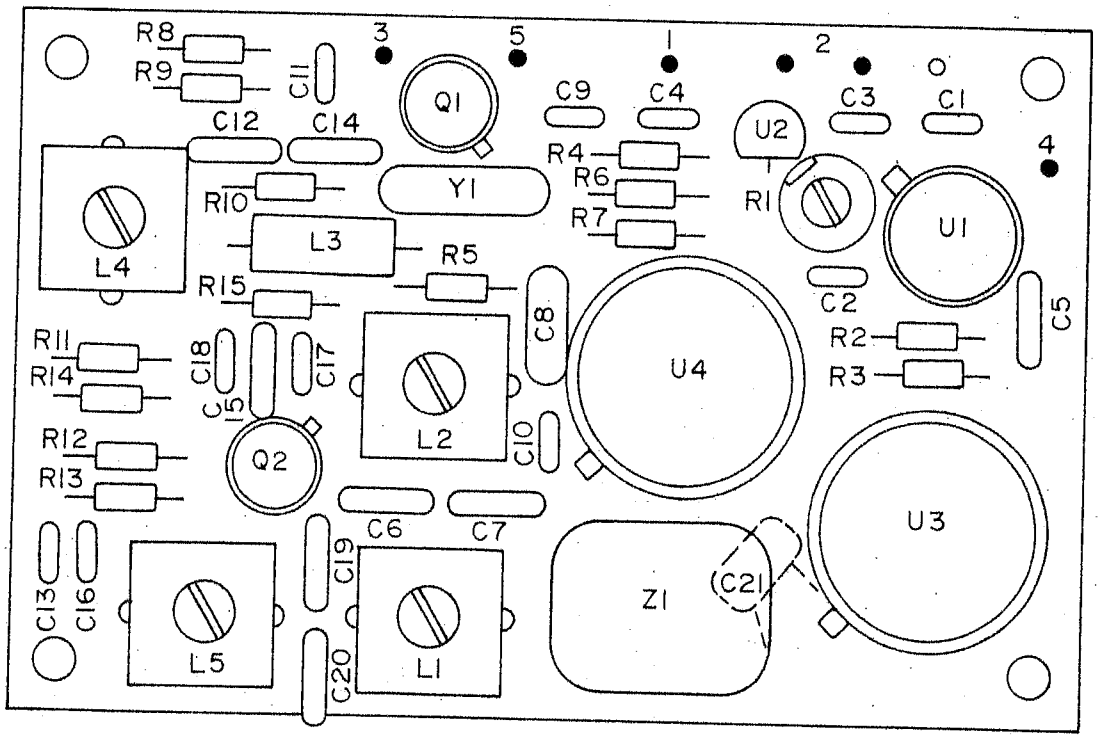


REF DESIGNATIONS	
LAST USED	NOT USED
C22 E5 FL2 J4 L5 Q2 U4 Y1 Z1	

UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE IN OHMS & 1/4 W
ALL CAPACITORS ARE IN MICROFARADS
ALL INDUCTORS ARE IN MICROHENRYS

PR-700 (OPT. 5), PR-707
A17 – SCHEMATIC,
21.4 MHz CONVERTER

81B170-1033E



PR-700 (OPT. 5)
A17-COMPONENT LOCATION,
21.4 MHz CONVERTER

81A170-1328

MANUFACTURER'S FSC CODE

ABB.	FULL NAME	ADDRESS	CODE
AB	Allen-Bradley Co.	1201 South 2nd St. Milwaukee, WI 53204	01121
AEC	Applied Engineering Consultants	10237 Southard Dr. Beltsville, MD 20705	58168
Add.	Addington Laboratories, Inc Microwave Components Div.	785 Palomar Ave. Sunnyvale, CA 94086	51859
AEP	Applied Engineerings Products	2600 State St. P.O. Box 6071 Hamden, CT 06517	19505
ALCO	Alco Electronic Products, Inc. Div. Augat, Inc.	1551 Osgood St. North Andover, MA 01845	95146
ALGO	Hamilton Electronic Corp. Algo Div.	50 Schrieffer St. S. Hackensack, NJ 07606	29715
Amatom	Amatom Electronic Hardware Div. of Mite Corp.	446 Blake St. New Haven, CN 06515	06540
AMP	AMP Incorporated	Harrisburg, PA 17105	00779
Amph	Bunker Ramo, RF Div. Amphenol Connector System	33 E. Franklin St. Danbury, CT 06810	74868
Ampx	Amperex Electronic Corp. Electro-Optical Devices Div.	P.O. Box 278 Slatersville, RI 02876	25403
Anaren	Anaren Microwave Inc	6635 Kirkville Rd. E. Syracuse, NY 13057	31597
Ansley	Ansley Electronics Corp.	3208 Humboldt St. Los Angeles, CA 90031	15912
Anzac	Anzac Electronics Div. of Adams Russell	39 Green St. Waltham, MA 02154	21912
APC	Active & Passive Comp. Inc.	6 Aerial Way Syosset, NY 11791	50369
Arco	Arco Electronics Inc.	400 Moreland Rd. Commack, NY 11725	84171
Arnold	Arnold Magnetics Corp.	11520 Jefferson Blvd. Culver City, CA 90230	04879
Augat	Augat Inc. Interconnection Cmpnts Div.	33 Perry Ave. Attleboro, MA 02703	91506

MANUFACTURER'S FSC CODE

ABB.	FULL NAME	ADDRESS	CODE
Avantek	Avantek Inc.	3175 Bowers Ave. Santa Clara, CA 95051	24539
Beck	Beckman Instruments Inc. Helipot Div.	2500 Harbor Blvd. Fullerton, CA 92634	73138
Belden	Belden Corp.	P.O. Box 1327 Richmond, IN 47374	70903
Bendix	Bendix Corp Electrical Components Div. RF Connector Sales	Sherman Ave. Sidney, NY 13838	77820
Berg	Winfred M. Berg, Inc.	499 Ocean Ave. East Rockaway L.I., NY 11518	29440
Bergquist	Bergquist	5300 Edina Ind'l. Minneapolis, MN 55435	55285
Bourns	Bourns Inc. Trimpot Div.	1200 Columbia Ave. Riverside, CA 02138	32997
Buckeye	Buckeye Stamping Co.	555 Marion Rd. Columbus, OH 43207	21604
Cambion	Cambion	445 Concord Ave. Cambridge, MA 02138	71279
Camloc	Rex Chainbelt, Inc. Camloc Div.	22 Spring Valley Rd. Paramus, NJ 07652	71286
Cannon	ITT Cannon Electric	666 E Dyer Rd. Santa Ana, CA 92702	71468
CDE	Cornell-Dubilier Electronics	150 Avenue "L" Newark, NJ 17101	14655
Cen-Lab	Centralab Electronics Div.	Box 858, Hwy. 20W Fort Dodge, IA 50501	71590
C-H	Cutler-Hammer	Specialty Products Div. Milwaukee, WI 53201	81640
Cinch	TRW/Cinch Connectors Electronic Components Div.	1501 Morse Ave. Elk Grove Village, IL 60007	71785
C-L	Centralab Electronics Div.Globe Union, Inc.	5757 N. Green Bar Ave. Milwaukee, WI 53201	71590
Clrstat	Clarostat Mfg.	1 Washington St. Dover, NH 03820	12697

MANUFACTURER'S FSC CODE

ABB.	FULL NAME	ADDRESS	CODE
CML	Chicago Minature/Drake	4433 N. Ravenswood Chicago, IL 60640	71744
Corcom	Corcom Inc.	2635 N. Kildare Ave. Chicago, IL 60639	05245
CTS	CTS Knights, Inc.	400 Reimann Ave. Sandwich, IL 60548	75378
Dale	Dale Electronics	P.O. Box 609 Columbus, NB 68601	91637
Datel	Datel Intersil	11 Cabot Blvd. Mansfield, MA 02048	50721
Del	Delevan Div. of American Precision Ind., Inc	270 Quaker Rd. Aurora, NY 12052	99800
DEL-BLIN	Delbert Blinn Co.	Box 2007 Pomona,, CA 91766	08289
Delco	Delco Electronics Div. General Motors Corp.	700 Firmin St. Kokomo, IN 46901	16758
Dennison	Dennison Mfg. Co.	300 Howard St. Framingham, MA 01701	05975
Dim-Gry	Dimco-Gray Co.	8200 S. Suburbon Rd. Dayton, OH 45459	80813
EFJ	E F Johnson Co.	299 10th Ave., SW Waseca, MN 56093	74970
Electroid	Electroid Co.	95 Progress St. Union, NJ 07083	16554
Elmenco	El-Menco	P.O. Box 7600 Lauter Ave. Florence, SC 29501	72136
EMC	Electronic Molding Co.	88 Mill St. Woonsocket, RI 20895	17117
EMF	EMF Systems, Inc.	P.O. Box 1009 State College, PA 16801	52747
Erie	Erie Technological Prods. Inc.	644 W 12th St. Erie, PA 16512	72982
Fairchild	Fairchild Semiconductor	464 Ellis St. Mountain View, CA 94040	07263

MANUFACTURER'S FSC CODE

ABB.	FULL NAME	ADDRESS	CODE
F-Dyne	F-Dyne Electronics	449 Howard Ave. Bridgeport, CT 06605	27735
FED	Federal Screw Prods. Inc.	3917 N Kedzie Ave. Chicago, IL 60618	73734
Fen	Fenwall Electronics	63 Fountain St. Framingham, MA 01701	15801
Ferox	Ferroxcube	5083 Kings Hwy. Saugerties, NY 12477	02114
G-B	Gordos Corp.	250 Glenwood Ave. Bloomfield, NJ 07003	95348
	G-C Electronics		72653
GE	General Electric Co. Electronic Capacitor Dept.	P.O. Box 158 Irmo, SC 29063	06001
G-M/Gen Mic	General Microwave Corp.	155 Marine St. Farmingdale, NY 11735	11332
Gray	Grayhill Inc.	565 Hillgrove Ave. Lagrange, IL 60525	81073
Guardian	Guardian Electric Co.	1550 W Carrol Ave. Chicago, IL 60607	73949
Haydon	A.W. Haydon Co.	232 N. Elm St. Waterbury, CT 06720	82227
	Honeywell - Spacekom	214 E. Gutierrez St. Santa Barbara, CA 93101	50245
HHS	Smith Inc., Herman H.	812 Snediker Ave. Brooklyn, NY 11207	83330
H-P	Hewlett Packard Co.	1501 Page Mill Rd. Palo Alto, CA 94304	28480
IEE	Industrial Electronic Engineers, Inc.	7740 Lemona Ave. Van Nuys, CA 91405	05464
IERC	Internat'l. Electronic Research Corp.	135 West Magnolia Blvd. Burbank, CA 91502	98978
Intersil	Intersil, Inc.	10900 N Tantave Ave. Cupertino, CA 95014	32293

MANUFACTURER'S FSC CODE

ABB.	FULL NAME	ADDRESS	CODE
JBT	JBT Switches Div. of Cutler-Hammer	P.O. Box 1904 New Haven, CT 06509	55459
JFD	JFD Electronics Corp.	15th at 62nd St. Brooklyn, NY 11219	73889
JM Hart	Joseph M. Hart & Son Inc.	95 S Hoffman Ln. Central Islip, NY 11722	81245
Kemet	Union Carbide Corp. Material System Div. Components Dept.	Hwy 276 SE Greenville, SC 29606	31433
Keystone	Keystone Electronics Corp.	49 Bleeker St. New York, NY 10012	91833
Kings	Kings Electronics Co. Inc.	40 Marbledale Rd. Tuckahoe, NY 10707	91836
K&L	K & L Microwave, Inc.	408 Coles Circle Salisbury, MD 21801	50140
Kry	Krytar	574 Weddel Dr. Unit 5 Sunnyvale, CA 94086	2R550
Littelfuse	Littelfuse, Inc.	800 E Northwest Hwy. Des Plaines, IL 60016	75915
Magnetics	Magnetics, Div. of Industries, Inc.	Box 391 Butler, PA 16001	90797
Mallory	Mallory Capacitor Co.	3029 E Washington Box 372 Indianapolis, IN 46201	90201
Mepco	Mepco/Electra, Inc.	P.O. Box 82927 San Diego, CA 92138	30983
Mic-Lab	Microlab/FXR	Ten Microlab Rd. Livingston, NJ 07039	00929
Mil	Mil Electronics	176 Walker St. Lowell, MA 01854	07862
M-M	Micrometals	1190 N. Hawk Anaheim, CA 92807	12856
M-O	Marco-Oak Div. of Oak Electro/Netics	207 S Helena St. Anaheim, CA 92803	76854

MANUFACTURER'S FSC CODE

ABB.	FULL NAME	ADDRESS	CODE
Mot	Motorola, Inc. Semiconductor Products Div.	P.O. Box 20912 Phoenix, AZ 85036	04713
MTC	Micro-Tel Corp.	10713 Gilroy Road Hunt Valley, MD 21030	29644
Narda	Narda Microwave Corp.	Plainview, NY 11803	99899
Nat/NSC	National Semiconductor Corp.	2900 Semiconductor Dr. Santa Clara, CA 95051	27014
Nobex	Nobex/Div. Griffith Plastics Corp.	1027 California Dr. Box 4365 Burlingame, CA 94010	32767
Norsal	Norsal Inds.	85 Hoffman Lane S. Central Islip, NY 11722	19136
Ohmite	Ohmite Mfg. Co.	3601 W. Howard St. Skokie, IL 60076	44655
	Omni-Yig	3350 Scott Blvd. Bldg. 66 Santa Clara, CA 95051	55682
OSM	Omni Spectra Inc. Microwave Comp. Div.	21 Continental Blvd. Merrimack, NH 03054	16179
Piezo Tech	Piezo Technology, Inc.	2525 Shader Rd. Box 7877 Orlando, FL 32804	25120
Plessey	Plessey Semiconductor Prods. Div. of Plessey Microsystems	1674 McGaw Ave. Santa Ana CA 92705	52648
Promenco	Inductive Components Inc.	181 Bridge Rd. Hauppauge, NY 11787	25159
RCA	RCA Solid State Div.	Route 202 Sommerville, NJ 08875	02735
RFD	RFD, Inc.	5024 Nassau St. Tampa, FL 33607	21992
RHG	RHG Electronic Lab, Inc.	161 Industry Ct. Deer Park, NY 11729	15286
Richco	Richco Plastic Co.	5825 N. Tripp Ave. Chicago, IL 60646	06915

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ABB.	FULL NAME	ADDRESS	CODE
RMF	RMF Products, Inc.	1275 Paramount Pkwy. Batavia, IL 60510	60662
Robinson/ROB	Robinson-Nugent, Inc.	802 E 8th St. New Albany, IN 47150	06776
Rodan	Rodan Industries	2905 Blue Star St. Anaheim, CA 92806	15454
Rogan	Rogan Corp.	3455 Woodhead Dr. Northbrook, IL 60062	86797
Schadow	Schadow Inc./ITT	8081 Wallace Rd. Eden Prairie, MN 55344	31918
S-D	Systron-Donner Microwave Div.	14844 Oxnard St. Van Nuys, CA 91409	01220
	Semtech		14099
Signetics	Signetics Corp.	811 E Arques Ave. Sunnyvale, CA 94086	18324
Sol	Solitron/Microwave	Box 278 Port Salerno, FL 33492	95077
Sou-Co	Southco Inc.	Concordville, PA 19331	94222
Spec. Cont.	Spectrum Control, Inc.	8061 Avonia Rd. Fairview, PA 16415	33095
Spr	Sprague Electronic Corp.	North Adams, MA 01247	56289
Stackpole	Stackpole Carbon Electronic Comp. Div.	Stackpole St. St. Marys, PA 15857	78488
Stimpson	Stimpson Co. Inc.	Bayport, NY 11705	57771
Struth	Struthers Electronics Corp.	Railroad Place Mamaroneck, NY 10534	00341
Sunbank	Sunbank Electronics, Inc.	3110 Winona Ave. Burbank, CA 91504	
Swcr	Switchcraft, Inc.	5555 N Elston Chicago, IL 60630	82389
Tek	Tektronix	Box 500 Beaverton, OR 97077	80009

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ABB.	FULL NAME	ADDRESS	CODE
Tel	Teledyne Microwave	3155 W El Segundo Blvd. Hawthorne, CA 90250	11532
Therm	Thermalloy, Inc.	2021 W Valley View Dallas, TX 75222	13103
TI	Texas Instruments, Inc. Semiconductor Comp. Div.	Box 5012-MS84 Dallas, TX 75222	01295
Trio	Trio Metal Prod. Co. Inc.	Falls & Clarkview Rd. Baltimore, MD 21209	26430
Unirode	Unitrode Corp.	590 Pleasant St. Watertown, MA 02172	12969
Unif-Tub	Uniform Tubes Microdelay Div	Collegeville, PA, 19426	93306
USECO	Useco Div. Litton Industries	13536 Saticoy St. Van Nuys, CA 91409	88245
USM	USM Corp. Fastener Group	510 River Rd. Shelton, CN 06484	07707
UTC	United Transformer Div. of TRW	150 Varick St. New York, NY 10013	80223
Vari-L	Vari-L Co.	3883 Monaco Pkwy. Denver, CO 80207	05375
Varo	Varo Semiconductor, Inc.	1000 N. Shiloh Rd. Garland, TX 75040	30857
Vema	Vemaline Products, Co.	455 W. Main St. Wyckoff, NJ 07481	08730
Vernitron	Vernitron Corp.	300 Marcus Blvd. Deer Park, NY 11729	10651
Vik/Viking	Viking Industries, Inc.	9324 Topanga Canyon Blvd. Chatsworth, CA 91311	05574
	Wakefield	60 Audobon Road Wakefield, MA 01880	05820
Win	Winchester Electronics Div. of Litton Industries	Main St. & Hillside Ave. Oakville, CT 06779	81312
W-J	Watkins-Johnson Co.	3333 Hillview Ave. Palo Alto, CA 94304	14482

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W-M	Western Microwave Labs.	1260 Birchwood Sunnyvale, CA 94086	16453
YIG-Tek	Eaton Corp/YIG-Tek Plant	610 N. Mary Ave. Sunnyvale, CA 94086	34657
Zierick	Zierick Mfg. Corp.	44 Radio Circle Mt. Kisco, NY 10549	79963