TECHNICAL MANUAL

MAINTENANCE INSTRUCTIONS

TEST SET, RADAR, AN/UPM-145, 58139-40001

AAI Corporation
F33657-78-C-0394

Published under authority of the Secretary of the Air Force.

1 NOVEMBER 1979

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2-1. GENERAL. This section identifies and describes the recommended special tools and test equipment required for maintenance of the Test Set. When the recommended tools or test equipment are not available, equivalent items may be substituted.

2-2. SPECIAL TOOLS AND TEST EQUIPMENT. Table 2-1 lists the special tools and test equipment required to maintain the Test Set.

Table 2-1. Special Tools and Test Equipment

Tool/equipment number	Nomenclature	Use and application
American 2098-5065	Torque wrench	To tighten semi rigid cable connectors to 8 ±0.5 inch-pounds.
MIL-C-9988A	Frequency counter	To measure frequency.
MIL-M-38706	Multimeter	To test ac, and dc voltages, resistance, and current.
Model AS-4, Weinschel (NSN 6625-869-2394)	Attenuation standards	To provide precision attenuation standards when using attenuator and signal calibrator.
Model H01-H0A, Weinschel (NSN 6625-909-3084)	Heterodyne Mixer-oscillator	To be used with attenuator and signal calibrator.
Model VM-3, Weinschel (NSN 6625-909-3185)	Attenuator and signal calibrator	To provide accurate attenuator measurements.
Model X382A, Hewlett-Packard (NSN 6625-00-602-2089)	Variable attenuator	To attenuate rf signals.
Model 350C-1, Pace Inc. (NSN 4940-01-031-4541)	Benchtop repair center	General repair kit.

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Tool/equipment number	Nomenclature	Use and application
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Model 454A, Hewlett-Packard (NSN 6625-433-4282)	Logic probe	To troubleshoot logic circuits.
Model 475-4, Tektronix (NSN 6625-00-397-4179)	Oscilloscope	To provide visual display of electrical signals.
Model 5255A, Hewlett-Packard (NSN 6625-00-058-3042)	Frequency counter X-band plug-in	To extend range of frequency counter.
Model 779D, Hewlett-Packard (NSN 5895-490-2834)	Directional coupler	To couple X-band signals to the test equipment.
Model 8011A, Hewlett-Packard (NSN 6625-01-022-2247)	Pulse generator	To provide calibration and troubleshooting signals.
Model 8478B, Hewlett-Packard (NSN 6625-811-2435)	Thermistor mount	To provide X-band rf power measurement device for power meter.
Model 8690B, Hewlett-Packard (NSN 6625-00-442-3470)	Sweep generator	To provide X-band frequency source.

S/N 2573

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BASIC AND ALL CHANGES HAVE BEEN MERGED TO MAKE THIS A COMPLETE PUBLICATION.

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SECTION I

INTRODUCTION AND GENERAL INFORMATION

1-1. INTRODUCTION

a. Purpose. This Technical Order provides information to assist technicians at the field level Precision Measurements Equipment Laboratory (PMEL) in the maintenance of Test Set, Radar, AN/UPM-145, part number 58139-40001 (NSN 6625-01-074-4846) (figure 1-1), manufactured by AAI Corporation, Cockeysville, Maryland. Test Set, Radar, AN/UPM-145 is referred to as the Test Set throughout the manual.

b. Scope. This Technical Order provides Test Set theory of operation and maintenance procedures. The maintenance procedures include troubleshooting, repair, and calibration to be performed by the PMEL facility. Functional drawings, schematics, and wiring data are provided to complement the theory of operation and maintenance procedures. The Test Set operation instructions are provided in T.O. 33D7-44-225-1. The illustrated parts breakdown is provided in T.O. 33D7-44-225-4.

c. Arrangement. This Technical Order consists of eight sections as follows:

(1) Section I, Introduction and General Information, provides a brief description of the Test Set including physical makeup, capabilities, and operating characteristics.

(2) Section II, Special Tools and Test Equipment, provides a tabular list of special tools and test equipment used to maintain the Test Set.

(3) Section III, Preparation for Use and Shipment, provides a reference to the operation manual.

(4) Section IV, Operating Instructions, provides theory of operation for the Test Set.

(5) Section V, Maintenance Instructions, provides procedures for operational checkout, inspection, preventive maintenance, troubleshooting, repair, and calibration of the Test Set.

(6) Section VI, Diagrams, provides the block diagrams, functional diagrams, and subassembly schematics required to maintain the Test Set. The diagrams appear in the same order in which they are described or referenced in the preceding sections.

(7) Section VII, Illustrated Parts Breakdown, is provided in T.O. 33D7-44-225-4.

(8) Section VIII, Difference Data, is not required.

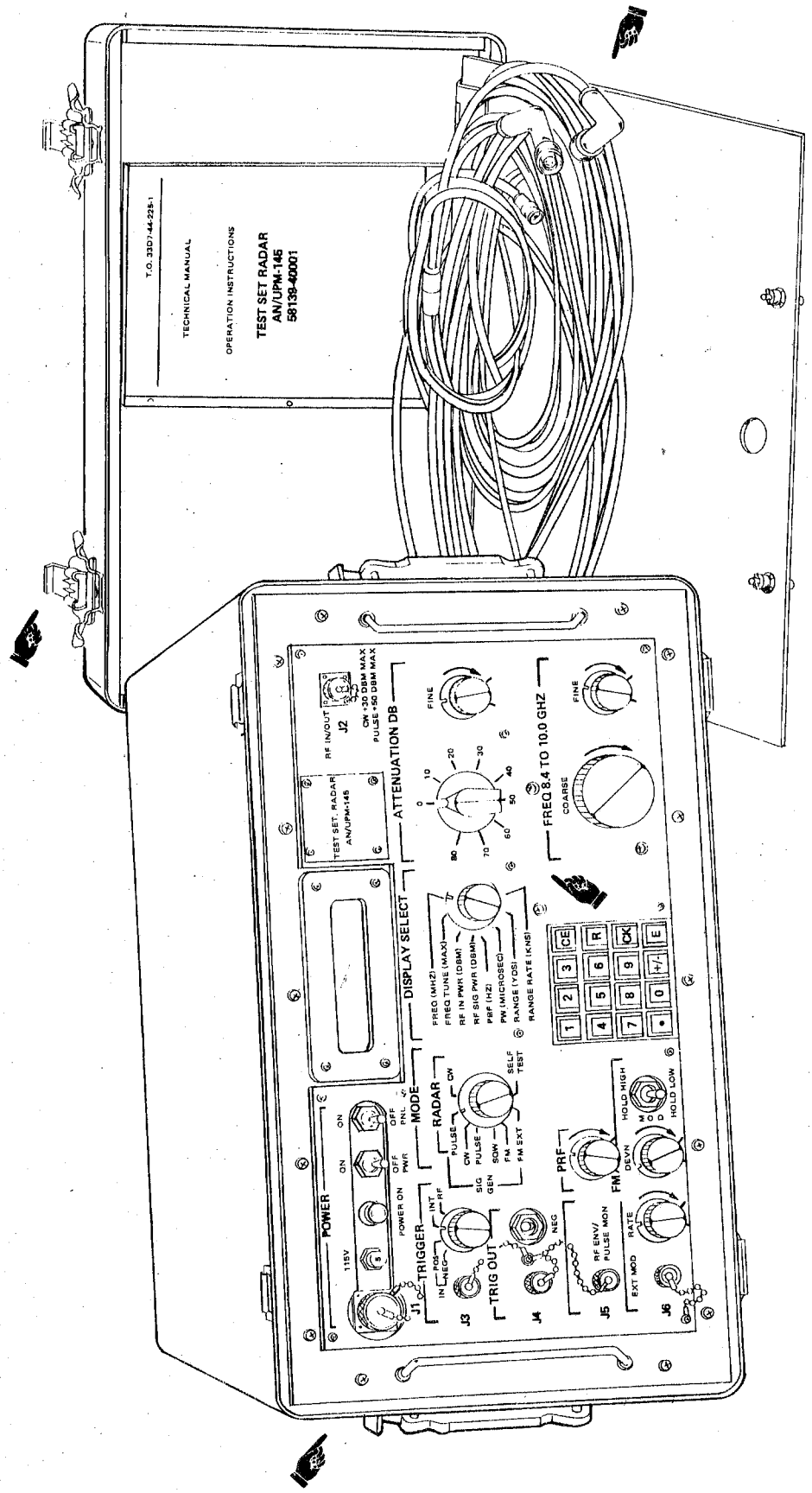

Figure 1-1. Test Set, Radar, AN/UPM-145

1-2. GENERAL INFORMATION

a. General. The Test Set is a portable X-band transponder/analyzer. The Test Set is used to test and adjust pulse radar, continuous wave (cw) radar, and beacon radar systems. The tests are initiated and controlled by controls and indicators provided on the front panel of the Test Set. The results of each test are displayed on a six-digit numeric display on the front panel.

b. Function of the Test Set. The function of the Test Set is to test radar power, frequency, pulse repetition frequency (prf), and range tracking capabilities; receiver bandwidth and minimum discernible signal; and beacon radar transmit response. The Test Set can be used as a signal generator with continuous wave (cw), pulse modulated (pulse), square wave (sqw), or frequency modulated outputs. These signals are controllable in frequency, power, prf, pulse width, range, and range rate. The radar tests can be performed in either a laboratory, flight line, or field shop environment.

c. Physical Description. The Test Set and all the cables necessary for operation of the Test Set are contained in a portable combination case. The lid contains the cables and the Test Set operation manual and is completely removable from the Test Set case. The Test Set case contains all the Test Set assemblies (table 1-1), which are mounted on Test Set (Electronics Assembly 1A1). Electronics Assembly 1A1 is removable for servicing, and is suitable for rack mounting. Table 1-1 lists the major assemblies and cables of the Test Set in reference designator order.

1-3. LEADING PARTICULARS

a. Testing Capabilities. The test capabilities of the Test Set are provided in T.O. 33D7-44-225-1.

b. Utilities Requirements. The Test Set requires a power source capable of supplying 115 volts ±10% ac rms, 60 ±10 Hz or 400 ±20 Hz, 5 amperes, single phase.

c. Power Supply Characteristics. The characteristics of Test Set Power Supply 1A1PS1 are provided in table 1-2.

d. Weights and Dimensions. The weights and dimensions of the Test Set and cables are provided in table 1-3.

Table 1-1. Major Components and Cables

Official name	Part number 58139-	Reference designator	T.O. nomenclature
Test Set, X-Band, AN/UPM-145	40001	Unit 1	Test Set
Test Set Electronics Assembly	40005	1A1	Electronics Assembly
Circuit Card Assembly, Front Panel Interface	40020	1A1A1	Front Panel Interface
Circuit Card Assembly, Digital	40015	1A1A2	Digital Assembly
Circuit Card Assembly, Microwave Interface	40010	1A1A3	Microwave Interface
Microwave Assembly	40060	1A1A4	Microwave Assembly
Modulator Mixer	90012	1A1A4A1	Modulator/Mixer
Coupler Module	90013	1A1A4A2	Coupler Module
VCO/Prescaler	90014	1A1A4A3	VCO/Prescaler
RF Detector	90007	1A1A4A4	RF Detector
Coaxial Switch	90003	1A1A4S1	Coaxial Switch
RF Oscillator Assembly	40030	1A1A5	RF Oscillator
Circuit Card Assembly, Gunn Oscillator Regulator	40050	1A1A5A1	Gunn Oscillator Regulator
Solid State Oscillator	90001	1A1A5Y1	Gunn Oscillator
Directional Detector	90015	1A1A6	Detector
Panel, Illuminated	90011	1A1A7	Illuminated Panel
Attenuator Assembly	40055	1A1A8	Attenuator Assembly
Step Attenuator	90002	1A1A8AT1 1A1A8S1	Step Attenuator Step Attenuator Switch
Multi-voltage Power Supply	90006	1A1PS1	Power Supply

Table 1-1. Major Components and Cables - Continued

Official name	Part number 58139-	Reference designator	T.O. nomenclature
Cable, Special Purpose Electrical (Power)	40035	W1	Power Cable W1
Cable, Special Purpose Electrical (RF)	40040	W2	RF Cable W2
Cable, Special Purpose Electrical (BNC)	40045	W3	BNC Cable W3

Table 1-2. Power Supply 1A1PS1 Characteristics

Input power requirements	Output ratings	
	Voltage	Current
115 volts ±10% at 50 through 70 Hz, or 380 through 420 Hz, single phase	+4.5 to +5.5 vdc, less than 150 mV peak to peak ripple	20.0 amperes (max)
	±14.0 to 16.0 vdc, less than 50 mV peak to peak ripple	3.0 amperes (max)

Table 1-3. Weights and Dimensions

Assembly	Overall dimensions			Cubage (cu ft)	Net weight (lb)
	Length (in.)	Width (in.)	Height (in.)		
Test Set Unit 1	20.75	20.04	12.78	3.0	50
Electronics Assembly 1A1	16.20	18.88	10.38	N/A	32
Power Cable W1	120	N/A	N/A	N/A	N/A
RF Cable W2	216	N/A	N/A	N/A	N/A
BNC Cable W3	72	N/A	N/A	N/A	N/A

Section II

SPECIAL TOOLS AND TEST EQUIPMENT

2-1. GENERAL. This section identifies and describes the recommended special tools and test equipment required for maintenance of the Test Set. When the recommended tools or test equipment are not available, equivalent items may be substituted.

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MIL-M-38706	Multimeter	To test ac, and dc voltages, resistance, and current.
Model AS-4, Weinschel (NSN 6625-869-2394)	Attenuation standards	To provide precision attenuation standards when using attenuator and signal calibrator.
Model H01-H0A, Weinschel (NSN 6625-909-3084)	Heterodyne Mixer-oscillator	To be used with attenuator and signal calibrator.
Model VM-3, Weinschel (NSN 6625-909-3185)	Attenuator and signal calibrator	To provide accurate attenuator measurements.
Model X382A, Hewlett-Packard (NSN 6625-00-602-2089)	Variable attenuator	To attenuate rf signals.
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Table 2-1. Special Tools and Test Equipment

Tool/equipment number	Nomenclature	Use and application
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MIL-C-9988A	Frequency counter	To measure frequency.
MIL-M-38706	Multimeter	To test ac, and dc voltages, resistance, and current.
Model AS-4, Weinschel (NSN 6625-869-2394)	Attenuation standards	To provide precision attenuation standards when using attenuator and signal calibrator.
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Model 8690B, Hewlett-Packard (NSN 6625-00-442-3470)	Sweep generator	To provide X-band frequency source.

Table 2-1. Special Tools and Test Equipment - Continued

Tool/equipment number	Nomenclature	Use and application
Model 8694B-001, Hewlett-Packard (NSN 6625-00-460-3304)	Sweep Generator X-band plug-in	To extend sweep generator frequency range.
Model 8734B, Hewlett-Packard (NSN 6625-113-6300YA)	Pin modulator	To pulse modulate X-band signals.
6625-70-163A Hewlett-Packard (NSN 6625-00-439-5154)	Digital multimeter	To make precision tests of ac and dc voltages, resistance, and current.
Model HP495A Hewlett-Packard (NSN 6625-00-084-1106	Traveling wave tube amplifier	To amplify pulse generator output.

SECTION III

PREPARATION FOR USE AND SHIPMENT

Instructions for preparation for use and shipment are provided in T.O. 33D7-44-225-1.

SECTION IV

OPERATION INSTRUCTIONS

4-1. GENERAL. This section provides Test Set theory of operation and operating instructions. The theory of operation is provided at two levels: overall theory of operation and subsystem theory of operation. The overall theory of operation describes Test Set operation at an overall block diagram level to define the functional areas of the Test Set and the relationship between each functional area. The subsystem theory of operation describes the operation of each Test Set subsystem at a functional diagram level. The related functional diagrams for each subsystem description are included in Section VI. The operating instructions are provided in T.O. 33D7-44-225-1.

4-2. OVERALL THEORY OF OPERATION (Figure 6-1). The Test Set is divided into eight subsystems: CPU and I/O, display, RF tune and frequency measurement, frequency modulation, target generation, power measurements, measurements, and power distribution. Although each subsystem performs a different function, the subsystems are interrelated to allow the Test Set to perform its overall functions of 1) measuring radar frequency, power, and prf; and 2) generating cw and pulsed rf returns. The subsystems also operate together to perform the self-test of the Test Set. A general description of the purpose of each subsystem is provided in the following order:

a. CPU and I/O subsystem

b. Display subsystem

c. RF tune and frequency measurement subsystem

d. Frequency modulation subsystem

e. Target generation subsystem

f. Power measurements subsystem

g. Measurements subsystem

h. Power distribution

a. CPU and I/O Subsystem. The CPU and I/O subsystem determines the type of test or operation to be performed, communicates with the other subsystems to control the selected testing sequence or operation, determines the results of the test or operation performed by the other subsystems, and generates the required display data. The CPU and I/O subsystem contains the random access memory (RAM), read only memory (ROM), microprocessor (CPU), and input/output (I/O) ports. The ROM contains the program instructions, which are executed by the CPU to control the selected test or operation. The execution of the program instructions results in

the transfer of data, via the I/O ports, to control the other subsystems and to determine the results of the test or operation. The RAM provides scratch pad memory used for temporary storage of data while the CPU is executing the program instructions. The CPU and I/O subsystem operates in the following manner:

(1) The CPU and I/O subsystem operation is started when the Test Set power is turned on, or when the R (reset) key is pressed on the keyboard. When the power is turned on or the reset key is pressed, the CPU starts execution of the program instructions in the ROM, which causes the CPU to set up the I/O to the proper input/output configuration, enabling the CPU to communicate with the other subsystems. The CPU then performs a CPU test, a ROM test, and a RAM test to verify operation of these areas. If the results of these tests indicate that these areas are operating properly, the CPU and I/O subsystem reads the MODE SELECT and DISPLAY SELECT data.

(2) After the MODE SELECT data and DISPLAY SELECT data are decoded by the CPU, the program instructions used to perform the selected test or operation are read from the ROM and executed by the CPU. The execution of the selected program instructions results in the data transfers, via the I/O to and from the other subsystems, to control the subsystems and to determine the results of each test or operation. The CPU then generates the display data which is used to provide the visual display of the results of the test or operation.

b. Display Subsystem. The display subsystem provides for the selection of the test or operation to be performed; entry of the pulse width, range, and range rate parameters for the Test Set generated target; and the display of the results of the selected test or operation. The display subsystem includes the front panel MODE switch, DISPLAY SELECT switch, keyboard, and six-digit numeric display. The MODE switch and DISPLAY SELECT switch provide for the selection of the test or operation to be performed by the Test Set. The keyboard provides the capability for the entry of the pulse width, range, and range rate data to control the parameters of the Test Set generated target. The six-digit numeric display provides a visual indication of the results of the selected test or operation. The display subsystem operates in the following manner:

(1) The MODE SELECT and DISPLAY SELECT data are read for the first time by the CPU and I/O subsystem when the Test Set power is turned on or when the R (reset key) is pressed on the keyboard. The CPU and I/O subsystem decodes the MODE SELECT data and DISPLAY SELECT data, and then performs the selected test or operation. When the selected test or operation has been completed and the required DISPLAY DATA has been output to the six-digit numeric display, the CPU and I/O subsystem reads the MODE SELECT and DISPLAY SELECT data again and compares this data with what was read before the test or operation was started. If the MODE SELECT and DISPLAY SELECT data read at this time are the same as the data read previously, the CPU and I/O subsystem repeats the same test or operation, and generates new DISPLAY DATA for output to the six-digit numeric display. If the MODE SELECT and DISPLAY SELECT data read at this time are not the same as the data read previously, the CPU and I/O subsystem decodes the new MODE SELECT and DISPLAY SELECT data, performs the selected test or operation, and generates the DISPLAY DATA required by the new switch settings.

(2) The KEYBOARD DATA data inputs to the CPU and I/O subsystem are read and decoded whenever a key is pressed. If the R (reset) key is pressed, the CPU and I/O subsystem proceeds to initialize the Test Set as if power was turned on (described in CPU and I/O subsystem description). If a data key (0 through 9, +/-, or .) is pressed, the CPU and I/O subsystem stores the decoded KEYBOARD DATA in scratch pad memory, and reads the MODE SELECT and DISPLAY SELECT data inputs. If the MODE switch is set to RADAR PULSE or SIG GEN PULSE, and the DISPLAY SELECT switch is set to PW (MICROSEC), RANGE (YDS), or RANGE RATE (KNS), the CPU and I/O subsystem displays the value stored in the scratch pad memory on the six-digit numeric display and causes a flashing 1 to appear. The flashing 1 indicates that a value is being entered on the keyboard. The next time a data key is pressed, the CPU and I/O subsystem adds the new key value to the value already stored in the scratch pad memory and displays this new value on the six-digit numeric display. Ths process continues until the E (enter) key is pressed. When the enter key is pressed, the CPU and I/O subsystem replaces the previous pulse width range or range rate value with the value that has just been entered.

c. RF Tune and Frequency Measurement Subsystem. The rf tune and frequency measurement subsystem provides for control of the Test Set oscillator frequency, generates a signal proportional to the oscillator frequency for measurement, and provides for tuning the Test Set oscillator frequency to the frequency of the rf input applied to the RF IN/OUT connector. The rf tune and frequency measurement subsystem includes the Test Set oscillator, afc circuits, frequency conditioning circuits, and rf tuning circuits. The Test Set oscillator provides the Test Set X-band rf source. The frequency conditioning circuits generate a signal proportional to the Test Set oscillator frequency, which can be measured directly by the Test Set. The rf tune circuits provide a signal to indicate when the Test Set oscillator frequency is tuned to the incoming rf frequency. The rf tune and frequency measurements subsystem operates in the following manner:

(1) The Test Set oscillator is mechanically tuned by the FREQ 8.4 TO 10.0 GHZ COARSE control, and electrically tuned by the OSC FINE TUNING input from the frequency modulation subsystem. The OSC OUTPUT signal is applied to the target generation subsystem, which provides the RF RETURN to RF IN/OUT connector J2 via the power measurements subsystem. When THE DISPLAY SELECT switch is set to FREQ (MHZ), the VCO ÷ 256 output of the frequency conditioning circuits is measured by the measurements subsystem digital measurements circuits. Next, the COARSE TUNE POSITION signal is measured by the measurements subsystem analog circuits. The result of this measurement is used by the CPU and I/O subsystem to determine the approximate oscillator frequency. The results of the VCO ÷ 256 measurement and the COARSE TUNE POSITION measurement are then compared; if the two values agree, the frequency is displayed on the six-digit numeric display.

(2) The rf tune circuits compare the frequency of the incoming rf input at RF IN/OUT connector J2 with the frequency of the Test Set oscillator to generate the TUNE FOR MAX output to the measurements subsystem analog circuits. The level of the TUNE FOR MAX output indicates the difference in frequency between the incoming rf and the Test Set oscillator. When the DISPLAY SELECT switch is set to FREQ TUNE (MAX), the CPU and I/O subsystem measures the TUNE FOR MAX signal

level and outputs a number between 0 and 255 to the six-digit numeric display. The level of the measured TUNE FOR MAX signal increases as the FREQ 8.4 TO 10.0 GHZ COARSE and FINE controls are adjusted, until the Test Set oscillator is tuned to the frequency of the incoming rf. This causes the displayed number to increase from 0 to approximately 100 for a pulsed rf input, or from 0 to approximately 170 for a CW rf input.

d. Frequency Modulation Subsystem. The frequency modulation subsystem provides for frequency modulation of the Test Set oscillator. The Test Set oscillator can be modulated, using the Test Set internal sweep generator or an external modulation source. The frequency modulation subsystem includes a sweep generator and oscillator fine tune circuits. When the Test Set is operating in signal generator mode, the sweep generator provides the sweep voltage which is applied to the oscillator fine tune circuits to sweep the OSC FINE TUNE output to the Test Set oscillator. When operation is in external mode, the external modulation (EXT MOD) input is applied directly to the oscillator fine tune circuits to sweep the OSC FINE TUNE output to the Test Set oscillator. The frequency modulation subsystem operates in the following manner:

(1) The internal fm signal generator is controlled by the DEVIATION, HOLD HIGH-MOD-HOLD LOW, and RATE signals supplied by the front panel FM controls. The internal fm signal generator mode is selected when the MODE switch is set to SIG GEN FM. The starting frequency is established by holding the FM HOLD HIGH-MOD-HOLD LOW switch to HOLD LOW. With HOLD LOW selected, the internal sweep generator output is removed from the oscillator fine tune circuits to stop the sweep of the OSC FINE TUNE output. With the sweep removed, the FINE FREQUENCY input to the fine tune circuits from the FREQ 8.4 TO 10.0 GHZ FINE control controls the OSC FINE TUNE output to the Test Set oscillator. The starting frequency is then adjusted by setting the DISPLAY SELECT switch to FREQ (MHZ) and adjusting the FREQ 8.4 TO 10.0 GHZ COARSE and FINE controls to the desired starting frequency.

(2) The deviation (upper frequency point) is established by setting the FM HOLD HIGH-MOD-HOLD LOW to HOLD HIGH. With HOLD HIGH selected, the fine tune circuits output is removed from the OSC FINE TUNE output, and the DEVIATION signal from the FM DEVN control is applied to the OSC FINE TUNE output. The FM DEVN control is then adjusted until the desired upper frequency point is displayed. The OSC FINE TUNE signal is modulated when the FM HOLD HIGH-MOD-HOLD LOW switch is released (returns to MOD position) and a SYSTEM TRIGGER pulse is received from the target generation subsystem. The SYSTEM TRIGGER pulse starts the sweep generator, modulating the OSC FINE TUNE output. The FM VALID output is then examined by the CPU and I/O subsystem. If the FM VALID signal is high (sweep is complete before next SYSTEM TRIGGER is applied), the CPU and I/O subsystem blanks the six-digit numeric display. If the FM VALID signal is low (SYSTEM TRIGGER applied before sweep is complete), the CPU and I/O subsystem generates a ␣103 display. When ␣103 is displayed on the six-digit display, the FM RATE control must be adjusted to the point where the sweep is completed before the next SYSTEM TRIGGER pulse is applied to the frequency modulation subsystem.

e. Target Generation Subsystem. The target generation subsystem provides for the selection of the Test Set triggering mode, and enables cw or pulsed rf returns at RF IN/OUT connector J2. The pulsed rf returns are controllable in pulse width, range, and range rate by keyboard entry. The target generation subsystem includes trigger selection circuits, range and pulse width counters, a range rate interrupt generator, and buffers to provide the TRIGGER OUT output at TRIG OUT connector J4 and the rf envelope at RF ENV/PULSE MON connector J5. The target generation subsystem operates in the following manner.

(1) A Gunn Oscillator in the rf tune and frequency measurement subsystem provides rf power as the GUNN OSC OUTPUT signal. The target generation subsystem switches this rf power, using a pin switch, to provide cw or pulse modulated rf as the RF RETURN signal. The RF RETURN signal passes through the power measurements subsystem to become the RF IN/OUT signal to RF IN/OUT connector J2.

(2) PULSE, CW MODE CONTROL signals from the CPU and I/O subsystem select either continuous wave or pulsed rf return from the target generation subsystem. Pulsed rf operation requires a trigger source to trigger a range counter and a pulse width counter to produce each rf return pulse. The range counter counts time from a trigger to the beginning of the return pulse and the pulse width counter counts time from the trigger to the end of the return pulse. RNG DATA (range) and PW DATA (pulse width) from the CPU and I/O subsystem determine the times counted by the range and pulse width counters and, therefore, determine the range delay and pulse width of the rf return pulse. For moving target simulation, the target generation subsystem produces periodic RANGE RATE INTERRUPT pulses to the CPU and I/O subsystem. For each pulse, the CPU and I/O subsystem increments or decrements the RNG DATA and PW DATA. This causes a constant increase or decrease in range delay, simulating an opening or closing target.

(3) Four trigger sources are applied to trigger select logic within the target generation subsystem. The TRIGGER SELECT signals from the TRIGGER IN POS/NEG-INT-RF switch cause the trigger select logic to select one source to trigger the range and pulse width counters. The first trigger source is from an internal pulse generator which is controlled by the PRF signal from the PRF control. The second trigger source is derived from the RF IN/OUT signal. This signal is detected and buffered to provide the RF ENVELOPE signal to RF ENV/PULSE MON connector J2. The RF ENVELOPE signal is converted to a logic level pulse to provide the second trigger source. The EXTERNAL TRIGGER signal from TRIGGER connector J3 provides the third trigger source. This signal is inverted and provides the fourth trigger source.

(4) The selected trigger is buffered by one-shots to provide three trigger outputs: the TRIGGER OUT signal, the SHAPED TRIGGER signal, and the SYSTEM TRIGGER signal. The TRIGGER OUT signal provides an output at the TRIG OUT connector. The SHAPED TRIGGER goes to the measurements subsystem for prf measurement, and the SYSTEM TRIGGER triggers the frequency modulation subsystem during FM operation.

f. Power Measurements Subsystem. The power measurements subsystem provides for rf power measurement of the radar input and the Test Set return. The power

measurements subsystem has directional couplers and detectors used for power measurement, and has attenuators used to control the return power level. The power measurements subsystem operates in the following manner:

(1) The radar input or Test Set return rf is sampled by a directional detector and is applied to an rf detector. The rf detector output is peak detected to produce the DETECTED POWER signal, a voltage proportional to the rf power being measured. This voltage is measured by the measurements subsystem to provide the CPU and I/O subsystem with a number from which a power level, in db, is calculated. The display subsystem displays the calculated value of power on the numeric display.

(2) A step attenuator, controlled by the ATTENUATION DB 0-80 control, provides a means of attenuating the radar rf input to a level within the range where power measurement is possible. The step attenuator also provides coarse attenuation of the Test Set return rf. Fine attenuation of the Test Set return rf is provided by a pin attenuator, controlled by the FINE ATTENUATION signal from the ATTENUATION DB FINE control.

g. Measurements Subsystem. The measurements subsystem provides circuits for analog (dc voltage) measurements and digital (frequency or period) measurements required to complete the function of other subsystems. The analog measurements circuits measure the COARSE TUNE POSITION signal voltage and the TUNE FOR MAX signal voltage to complete the frequency measurement and frequency tune functions of the rf tune and frequency measurement subsystem. The analog measurements circuits also measure the DETECTED POWER signal voltage to complete the functions of the power measurements subsystem. The digital measurements circuits measure the VCO ÷ 256 signal frequency as part of the frequency measurement function of the rf tune and frequency measurement subsystem. A frequency measurement of the shaped trigger signal determines prf. The measurements subsystem operates in the following manner:

(1) Analog measurements are made by a comparator which compares the signal being measured with a reference voltage from a digital to analog (d/a) converter in the analog circuits. The CPU and I/O subsystem sends SIGNAL SELECT data to control selection of a signal for measurement. The selected signal is applied to the comparator. Then, the CPU and I/O subsystem sends REFERENCE DATA to the d/a converter to vary the reference voltage applied to the comparator. The COMPARATOR OUTPUT signal indicates to the CPU and I/O subsystem whether the reference voltage is greater or smaller than the voltage being measured. This allows the CPU and I/O subsystem to adjust the known reference until it is equal to the unknown voltage being measured. Then the reference value is the measurement result.

(2) Digital measurements are made by counters in the digital measurements circuits. The CPU and I/O subsystem sends SIGNAL SELECT data to select the signal for digital measurement, and sends the PERIOD signal to select between frequency count or period count operation for the counters. After the frequency or period count is made, the count result is sent (FREQ COUNTER OUT) to the CPU and I/O subsystem where it is used in frequency or prf calculations.

h. Power Distribution Subsystem. The power distribution subsystem supplies all ac and dc power required by the Test Set. Power distribution is as follows:

(1) Input power is applied at POWER connector J1 and is controlled by the PWR ON-OFF switch and the 115V circuit breaker to provide the input power to the power distribution subsystem. This ac power is directed to a multivoltage power supply, and through the POWER PNL ON-OFF switch to the Illuminated Panel.

(2) The multivoltage power supply provides +5V, +15V, and -15V voltages to all electronic assemblies in the Test Set.

4-3. CPU AND I/O SUBSYSTEM BLOCK DIAGRAM DESCRIPTION (Figure 4-1)

a. Function. The overall function of the CPU and I/O subsystem is to provide control, support, interface, and calibration of all the other subsystems. The CPU and I/O subsystem organizes the interactions of the other subsystems to make the entire Test Set function as an integrated system.

b. CPU. The CPU consists of a microprocessor, a crystal, a ROM (read only memory), a RAM (random access memory), an address decoder, and buffers. The microprocessor is the control element. The ROM contains the permanent control instructions and data necessary to perform the system functions. The RAM is used for temporary storage of current data and address locations used while specific functions are being performed. The address decoder activates specific components after decoding address signals. The buffers provide signals with more drive to be input to components which are not on the same printed circuit card as the CPU. The crystal provides the time base for the CPU clock.

c. I/O. The input/output (I/O) circuits consist of a programmable counter, a programmable timer, several transceivers (XCVR), and some direct I/O from other Test Set subsystems. The programmable counter is used by the measurements and target generation subsystems. It consists of three separately programmable 16-bit counters. The programmable timer is used in connection with the target generation subsystem and has 14 bits. The transceivers are used as programmable I/O ports and are used by all the subsystems for control and data information. Some direct I/O lines exist between the microprocessor and select subsystem functions. These lines are used to have priority access to the CPU over other I/O.

d. Integration. The CPU and I/O subsystem components are integrated by three major transmission line groups called buses. These buses are the address bus, the data bus, and the control bus. Part of the address bus is actually time multiplexed with the data bus and share the same physical lines. The address bus consists of 16 lines and determines the CPU and I/O components that are active in transmissions at any one time. The data bus consists of eight lines that carry the specific information which is to be transmitted between components. The control bus consists of six lines which have specific control functions. The READ and WRITE lines control the direction of transmissions on the data bus (i.e., inputs or outputs). The ALE line indicates which type of information is present on the multiplexed

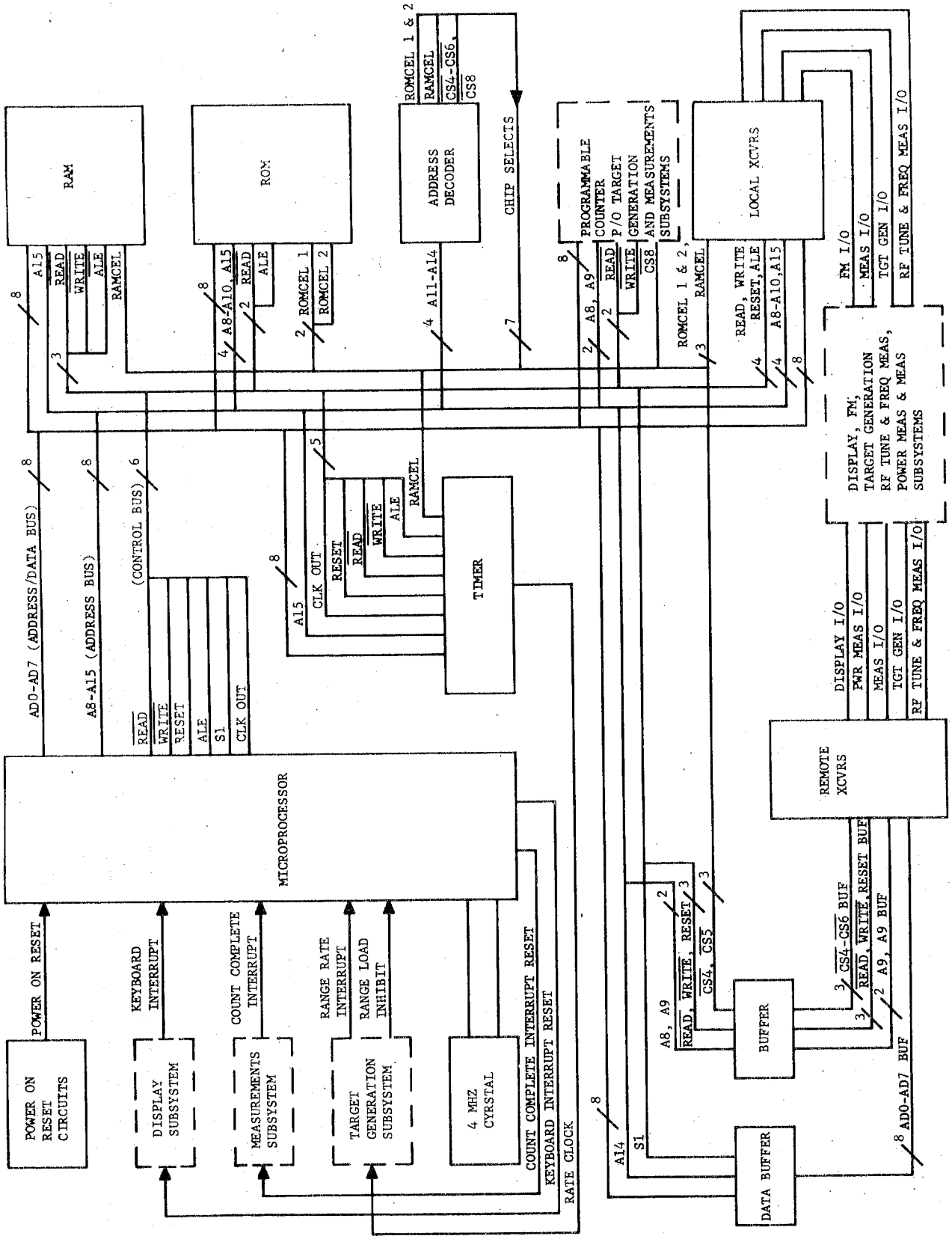

Figure 4-1. CPU and I/O Subsystem Block Diagram

address/data bus lines. This signal is high when address information is present and is low for data. The RESET line is used to initialize all programmable components to a known state. The S1 line is a bus status signal and is similar to the READ line with different timing. The CLK OUT line is an extension of the microprocessor time base and is used for other components which require time bases or synchronism with the microprocessor.

e. Operation. The microprocessor is the central controller of the subsystem and has control of the buses. The microprocessor outputs the address bus information and control bus information. The components of the CPU and I/O subsystem are identified by address location as are specific areas of the major components. The microprocessor outputs the address information on the address bus and the ALE control bus signal to start a transmission. The address decoder decodes the A11-A14 lines to determine the component that is being addressed. The A15 line indicates whether that component is memory or I/O, and the A0-A10 lines indicate the specific section or function of the address component. For the data transmission, the microprocessor outputs a READ or WRITE signal to indicate if the data is to be input from the address component or output to it. These types of transmissions are performed in an orderly manner as dictated by the instructions and data located in ROM. There are some direct I/O lines to the microprocessor which have priority over bus transmissions. These are called interrupts. When the power to the Test Set is turned on, a POWER ON RESET signal is supplied by a discrete circuit to initialize the microprocessor and the rest of the subsystem to a known status. This interrupt has priority over any other operation (i.e., it must be serviced when it occurs). The target generation subsystem supplies a RANGE RATE INTERRUPT. This has the next highest priority. The RANGE LOAD INHIBIT signal is not an interrupt. It is a serial data input and is monitored by the microprocessor only while it is servicing a range rate interrupt. The measurements subsystem supplies a COUNT COMPLETE INTERRUPT which has the next highest priority and the display subsystem supplies a KEYBOARD INTERRUPT which has lowest priority of these interrupts. The interrupts are reserved for data that cannot easily be handled by occasional sampling.

4-4. CPU AND I/O SUBSYSTEM FUNCTIONAL DIAGRAM DESCRIPTION (Figure 6-2). When Test Set power is applied, the power on reset circuitry (consisting of diode 1A1A2CR1, capacitor C31, and resistors R1 and R2) outputs a POWER ON RESET L signal to microprocessor 1A1A2U1. The microprocessor then initializes all internal registers and outputs the RESET signal from the reset out pin to initialize the entire subsystem. The function of the power on reset circuitry is to create a delay after power up to allow the microprocessor clock generator to start before receipt of the RESET signal. The 4 MHz crystal (1A1A2X1) supplies the time base control for the microprocessor clock generator which operates at half the crystal frequency or 2 MHz. The microprocessor then outputs address information on the A8-A15 and AD0-AD7 lines to address specific components and locations within components. When address information is present on the AD0-AD7 lines, the microprocessor pulses the ALE line high to indicate that this is address rather than data information. The A15 line is used to distinguish between memory and I/O on some components. The A14-A11 lines are used by address decoder 1A1A2U6 to provide component select lines that enable specific components for unique combinations of the A11-A14 signals.

In addition, the A14 signal is used to activate the data buffers (U7, U8), indicating I/O exchanges to components on printed circuit cards other than Digital Assembly 1A1A2. The AD0-AD7 and A8-A10 lines are used to designate the specific locations to be active within the active component. When the ALE signal is low, data is transferred between the microprocessor and I/O ports on eight parallel lines (AD0 through AD7). Data transfers to or from the I/O ports are indicated by low going pulses on the READL or WRITEL lines output from the RD and WR pins of the microprocessor. The S1 output line from the microprocessor functions in a manner similar to that of an inverted and advanced READL signal. It is used to configure the data buffers to be inputs. The microprocessor CLK OUT signal is used by the RAM timer as a time base for rate clock generation. The ROM's (1A1A2U2 and U3) contain the permanent instructions and data that impose an order to the data exchanges to make the entire system function. The RAM (1A1A2U5) is used for temporary storage of data and instructions for current functions. The microprocessor operates with interrupt inputs on a priority basis with RST 5.5 being the lowest priority interrupt and RST 7.5 being the highest. The range rate interrupt (RST 7.5) receives priority to achieve accuracy. The SID input is a serial data input which is monitored by the microprocessor after receipt of a range rate interrupt. The count complete interrupt (RST 6.5) indicates that a digital measurement is complete. The keyboard interrupt (RST 5.5) indicates that the keyboard is in use. The interrupt is reset by the serial data output (SOD) of the microprocessor. All input/output functions are described in the I/O signal dictionary (table 4-1). Address information is listed for the 16 address lines by a hexadecimal number (i.e., each group of four binary digits is represented by one hexadecimal digit). The Mode column indicates input or output data. The Description column indicates the component location. The data at each location is described by the Notes column and the eight columns from MSB to LSB (7 to 0) show the more specific form of the data.

4-5. DISPLAY SUBSYSTEM BLOCK DIAGRAM DESCRIPTION (Figure 4-2). The display subsystem provides the controls and indicators used to select the Test Set operating mode; display results of the selected test; and enter and display pulse width, range, and range rate values. The Test Set operating mode is determined by the mode control data input to the CPU and I/O subsystem. The mode control data is read in and decoded by the CPU and I/O subsystem that, in turn, sets up the Test Set circuits to operate in self-test mode, radar mode, or signal generator mode.

a. Self-Test Mode. When the self-test mode is selected, the CPU and I/O subsystem executes the automatic self-test program to check the operation of the display and keyboard portions of the display subsystem. The self-test program then checks parts of the remaining subsystems and displays the result of each test.

b. Radar or Signal Generator Mode. When the radar or signal generator mode is selected, the CPU and I/O subsystem reads in and decodes the display select data to determine the type of test, if any, to be made. For instance, when the MODE switch is set to RADAR CW, the CPU and I/O subsystem makes a test and displays the results if the DISPLAY SELECT switch is set to FREQ (MHZ), FREQ TUNE (MAX), RF IN PWR (DBM), or RF SIG PWR (DBM). A display is not generated (display blanked) if the DISPLAY SELECT switch is set to PRF (HZ), PW (MICROSEC), RANGE (YDS), or

Table 4-1. I/O Signal Dictionary

MODE	ADDRESS	DESCRIPTION	MSB 7 6 5 4 3 2 1 0 LSB	NOTES
WRITE	8000_{16}	PORT A PULSE	7 ← PW → 0	CONTAINS THE LSB'S OF THE PULSE WIDTH INFORMATION THAT IS USED BY THE PULSE WIDTH COUNTER.
	(ROM1A)	WIDTH OUT (LSB)		
WRITE	8001_{16}	PORT B PULSE	11 ← PW → 8	BITS 4-7, NOT AVAILABLE
	(ROM1B)	WIDTH OUT (MSB)		BITS 0-3, CONTAINS THE MSB'S OF THE PULSE WIDTH INFORMATION THAT IS USED BY THE PULSE WIDTH COUNTER.
READ	8001_{16}	PORT B STATUS	C AFC FMV FMM	BIT 7, COMPARATOR OUTPUT
	(ROM1B)			"0" - SELECTED SIGNAL IS MORE POSITIVE THAN D/A
				"1" - SELECTED SIGNAL IS MORE NEGATIVE THAN D/A
				BIT 6 - AFC VALID SIGNAL
				"1" - AFC VALID
				BIT 5 - FM VALID SIGNAL
				"1" - FM VALID
				BIT 4 - FM MOD SWITCH
				"0" - SWITCH IN HOLD HIGH OR LOW POSITION
				"1" - SWITCH IN FM MOD POSITION
				BITS 0-3, NOT AVAILABLE
WRITE	8002_{16}	PORT A CONTROL	1 1 1 1 1 1 1 1	CONTROLS THE DIRECTIONS OF EACH CORRESPONDING BIT OF PORT A.
	(RO1CA)			"0" = INPUT MODE
				"1" = OUTPUT MODE
WRITE	8003_{16}	PORT B CONTROL	0 0 0 0 1 1 1 1	CONTROLS THE DIRECTIONS OF EACH CORRESPONDING BIT OF PORT B.
	(RO1CB)			"0" = INPUT MODE
			7 6 5 4 3 2 1 0	"1" = OUTPUT MODE

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7 6 5 4 3 2 1 LSB 0	NOTES
READ	8800_{16}	TARGET COUNTER LSB.	7 ← LSB → 0	CONTAINS THE LSB'S OF THE TARGET COUNTER. THIS INFORMATION IS READ IN FOR SELF TEST ONLY.
	(ROM2A)	PORT A		
READ	8801_{16}	TARGET COUNTER MSB.	11 ← MSB → 8	BITS 4-7, NOT AVAILABLE
	(ROM2B)	PORT B		BITS 0-3, CONTAIN THE MSB'S OF THE TARGET COUNTER. THIS INFORMATION IS READ IN FOR SELF TEST ONLY.
WRITE	8801_{16}	COUNTER CONTROL.	P/F, INPUT	BIT 7 - SELECT PERIOD OR FREQUENCY
	(ROM2B)			"0" - FREQUENCY MEASUREMENT
				"1" - PERIOD MEASUREMENT
				BITS 4-6, COUNTER INPUT SELECT
				6 5 4
				0 0 0 GROUND
				0 0 1 SYSTEM TRIGGER
				0 1 0 PRESCALER OUTPUT
				0 1 1 RANGE CLOCK
				1 0 0 SPARE
				1 0 1 SPARE
				1 1 0 SPARE
				1 1 1 SPARE
WRITE	8802_{16}	PORT A CONTROL	0 0 0 0 0 0 0 0	CONTROLS THE DIRECTIONS OF EACH CORRESPONDING BIT OF PORT A
	(RO2CA)			"0" = INPUT MODE
				"1" = OUTPUT MODE
			7 6 5 4 3 2 1 0	

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7	6	5	4	3	2	1	LSB 0	NOTES
WRITE	8803_{16}	PORT B CONTROL	1	1	1	1	0	0	0	0	CONTROL THE DIRECTIONS OF EACH CORRESPONDING BIT OF PORT B.
	(RO2CB)										"0" = INPUT MODE
											"1" = OUTPUT MODE
			7	6	5	4	3	2	1	0	

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7	6	5	4	3	2	1	LSB 0	NOTES
R/W	9000_{16}	PORT A									SPARE, HARDWARE NOT INSTALLED
	(ROM3A)										
R/W	9001_{16}	PORT B									SPARE, HARDWARE NOT INSTALLED
	(ROM3B)										
WRITE	9002_{16}	PORT A CONTROL									SPARE, HARDWARE NOT INSTALLED
	(RO3CA)										
WRITE	9003_{16}	PORT B CONTROL									SPARE, HARDWARE NOT INSTALLED
	(RO3CB)										
			7	6	5	4	3	2	1	0	

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7	6	5	4	3	2	1	LSB 0	NOTES
READ	9800_{16}	COMMAND/STATUS	X	T	IE B	B BF	IR B	IE A	A BF	IR A	BIT 7 - NOT USED
	(RAMCT)	REGISTER									BIT 6 - TIMER INTERRUPT (BIT LATCHED HIGH WHEN TERMINAL COUNT IS REACHED, AND RESET LOW BY READING C/S REGISTER OR STARTING NEW COUNT.
											BIT 5 - PORT B INTERRUPT ENABLED
											BIT 4 - PORT B BUFFER FULL/EMPTY (INPUT/OUTPUT)
											BIT 3 - PORT B INTERRUPT REQUEST
											BIT 2 - PORT A INTERRUPT ENABLE
											BIT 1 - PORT A BUFFER FULL/EMPTY (INPUT/OUTPUT)
											BIT 0 - PORT A INTERRUPT REQUEST
READ	9801_{16}	PORT A	7 ← FREQ → 0								CONTAIN THE LSB'S OF THE FREQUENCY COUNTER.
	(RAMA)	FREQ COUNT IN									
WRITE	9802_{16}	PORT B	7 ← LSB → 0								CONTAIN THE LSB'S OF THE RANGE INFORMATION THAT WILL BE USED BY THE TARGET COUNTER.
	(RAMB)	TARGET COUNTER LSB'S									
WRITE	9800_{16}	COMMAND/STATUS	TM_2	TM_1	IE B	IE A	PC 2	PC 1	P B	P A	BITS 6,7 TIMER COMMAND
	(RAMCT)	REGISTER									TM2 = 0, TM1 = 0: NO-OPERATION
											TM2 = 0, TM1 = 1: STOP COUNTER
											TM2 = 1, TM1 = 0: STOP AFTER TERMINAL COUNT IS REACHED
											TM2 = 1, TM1 = 1: START COUNTER
											BIT 5, ENABLE PORT B INTERRUPT
											1 = ENABLE
			7	6	5	4	3	2	1	0	

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7 6 5 4 3 2 1 0 LSB	NOTES
				BIT 4 , ENABLE PORT A INTERRUPT
				1 = ENABLE
				BITS 2,3 DEFINES PORT C
				PC 2 / PC 1
				0 0 INPUT PORT
				1 1 OUTPUT PORT
				0 1 PC0 = PORT A INTERRUPT
				PC1 = PORT A BUFFER FULL
				PC2 = PORT A STROBE
				PC3-5 = OUTPUT PORT
				1 0 PC0 = PORT A INTERRUPT
				PC1 = PORT A BUFFER FULL
				PC2 = PORT A STROBE
				PC3 = PORT B INTERRUPT
				PC4 = PORT B BUFFER FULL
				PC5 = PORT B STROBE
				BIT 1, DEFINES PORT B
				"1" = OUTPUT
				"0" = INPUT
				BIT 0, DEFINES PORT A
				"1" = OUTPUT
				"0" = INPUT
			7 6 5 4 3 2 1 0	

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7 6 5 4 3 2 1 0 LSB	NOTES
WRITE	9803_{16}	PORT C	X SPARE ← MSB →	BITS 6,7 NOT AVAILABLE
	(RAMC)	TARGET COUNTER MSB'S		BITS 4,5 SPARE
				BITS 0-3 CONTAIN THE MSB'S OF RANGE TO BE USED BY THE TARGET COUNTER.
WRITE	9804_{16}	TIMER LENGTH LSB'S	7 ← LSB → 0	CONTAIN THE LSB'S OF THE COUNT LENGTH THAT WILL BE LOADED INTO THE TIMER.
	(RAMTIM)			
WRITE	9805_{16}	TIMER LENGTH & CONTROL	M2 M1 13 ← MSB → 8	BITS 6,7 TIMER MODE
	(RAMTIM+1)			M2 M1
				0 0 LOW DURING SECOND HALF OF COUNT
				0 1 SQUARE WAVE
				1 0 SINGLE PULSE AT TC
				1 1 REPETITIVE PULSE AT TC
				BITS 0-5 CONTAIN THE MSB'S OF THE COUNT LENGTH THAT WILL BE LOADED INTO THE TIMER.
			7 6 5 4 3 2 1 0	

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7 6 5 4 3 2 1 0 LSB	NOTES
READ	$A000_{16}$	READ COUNTER NO. 0	7 ← LSB → 0	EITHER THE LSB'S OR THE MSB'S OF COUNTER NO. 0 CAN BE READ BACK DEPENDING ON THE MODE OF THE
	(TIME0)		15 ← MSB → 8	TIMER THAT IS WRITTEN IN AT ADDRESS $A300_{16}$. THIS COUNTER WILL BE USED TO GENERATE THE RANGE RATE
				INTERRUPT.
READ	$A100_{16}$	READ COUNTER NO. 1	7 ← LSB → 0	EITHER THE LSB'S OR THE MSB'S OF COUNTER NO.1 CAN BE READ BACK DEPENDING ON THE MODE OF THE
	(TIME1)		15 ← MSB → 8	TIMER THAT IS WRITTEN IN AT ADDRESS $A300_{16}$. THIS COUNTER WILL BE USED IN GENERATING THE GATE
				THAT WILL BE USED FOR A FREQUENCY MEASUREMENT.
READ	$A200_{16}$	READ COUNTER NO. 2	7 ← LSB → 0	EITHER THE LSB'S OR THE MSB'S OF COUNTER NO. 2 CAN BE READ BACK DEPENDING ON THE MODE OF THE
	(TIME2)		15 ← MSB → 8	TIMER THAT IS WRITTEN IN AT ADDRESS $A300_{16}$. THIS COUNTER WILL BE USED TO STORE THE MSB'S OF
				COUNTER CONTROLLED BY THE GATE GENERATED BY COUNTER NO.1.
READ	$A300_{16}$	NO-OP	TRI-STATE OUTPUT	ILLEGAL READ OPERATION. PUTS TIMER INTO TRI-STATE OPERATION.
	(TIMER)			
WRITE	$A000_{16}$	LOAD COUNTER NO. 0	7 ← LSB → 0	EITHER THE LSB'S OR THE MSB'S OF COUNTER NO. 0 CAN BE LOADED DEPENDING ON THE MODE OF THE
	(TIME0)		15 ← MSB → 8	TIMER WRITTEN IN AT ADDRESS $A300_{16}$. THIS COUNTER WILL BE USED TO GENERATE THE RANGE RATE INTERRUPT.
WRITE	$A100_{16}$	LOAD COUNTER NO. 1	7 ← LSB → 0	EITHER THE LSB'S OR THE MSB'S OF COUNTER NO. 1 CAN BE LOADED DEPENDING ON THE MODE OF THE
	(TIME1)		15 ← MSB → 8	TIMER WRITTEN IN AT ADDRESS $A300_{16}$. THIS COUNTER WILL BE USED TO GENERATE THE GATE THAT WILL BE
				USED FOR A FREQUENCY MEASUREMENT.
			7 6 5 4 3 2 1 0	

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7 6 5 4 3 2 1 0 LSB	NOTES
WRITE	$A200_{16}$	LOAD COUNTER NO. 2	7 ← LSB → 0	EITHER THE LSB'S OR THE MSB'S OF COUNTER NO. 2 CAN BE LOADED DEPENDING ON THE MODE OF THE TIMER
	(TIME2)		15 ← MSB → 8	WRITTEN IN AT ADDRESS $A300_{16}$. THIS COUNTER WILL BE USED TO STORE THE MSB'S OF THE COUNTER
				CONTROLLED BY THE GATE GENERATED BY COUNTER NO. 1.
WRITE	$A300_{16}$	MODE WORD	SC1 SC0 RL1 RL0 M2 M1 M0 BCD	CONTROL WORD FOR TIMER.
	(TIMER)			BITS 6,7 SELECT COUNTER
				S_{C_1} | S_{C_0}
				0 | 0 SELECT COUNTER 0
				0 | 1 SELECT COUNTER 1
				1 | 0 SELECT COUNTER 2
				1 | 1 ILLEGAL
				BITS 4,5 READ, LOAD
				R_{L_1} | R_{L_0}
				0 | 0 COUNTER LATCHING OPERATION
				1 | 0 READ/LOAD MSB'S
				0 | 1 READ/LOAD LSB'S
				1 | 1 READ/LOAD LSB'S
				FOLLOWED BY MSB'S
			7 6 5 4 3 2 1 0	

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7 6 5 4 3 2 1 0 LSB	NOTES
				BITS 1,2,3 MODE
				M2 | M1 | M0
				0 | 0 | 0 — MODE 0, INTERRUPT ON TERMINAL COUNT
				0 | 0 | 1 — MODE 1, PROGRAMMABLE ONE SHOT
				X | 1 | 0 — MODE 2, RATE GENERATOR
				X | 1 | 1 — MODE 3, SQUARE WAVE RATE GENERATOR
				1 | 0 | 0 — MODE 4, SOFTWAVE TRIGGERED STROBE
				1 | 0 | 1 — MODE 5, HARDWARE TRIGGERED STROBE
				BIT 0 BINARY CODED DECIMAL
				BCD
				0 - BINARY COUNTER, 16 BITS
				1 - BCD COUNTER, 4 DECADES
			7 6 5 4 3 2 1 0	

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7 6 5 4 3 2 1 0 LSB	NOTES
WRITE	$C000_{16}$	PORT 1A	←5TH D→ ←LSD→	BITS 4-7 CONTAIN THE 5TH DIGIT OF THE DISPLAY IN BCD FORMAT.
	(DPLYA)	DISPLAY 1		BITS 0-3 CONTAIN THE LSD OF THE DISPLAY IN BCD FORMAT.
WRITE	$C100_{16}$	PORT 1B	←3RD→ ←4TH D→	BITS 4-7 CONTAIN THE 4TH DIGIT OF THE DISPLAY IN BCD FORMAT.
	(DPLYB)	DISPLAY 2		BITS 0-3 CONTAIN THE 3RD DIGIT OF THE DISPLAY IN BCD FORMAT.
WRITE	$C200_{16}$	PORT 1C	± MSD ←2ND D→	BITS 6,7 CONTROL THE SIGN OF THE DISPLAY.
	(DPLYC)	DISPLAY 3		7 6
				0 0 BLANK
				0 1 MINUS
				1 1 PLUS
				BITS 4,5 CONTROL THE MSD OF THE DISPLAY
				5 4
				0 0 BLANK
				1 1 "1"
				BITS 0-3 CONTAIN THE 2ND DIGIT OF THE DISPLAY IN BCD FORMAT.
WRITE	$C300_{16}$	PORT 1 CONTROL	1 0 0 0 0 0 0 0	CONFIGURES 8255 #1 SO THAT ALL BITS OF ALL PORTS ARE OUTPUTS.
	(DPLYD)			
			7 6 5 4 3 2 1 0	

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7	6	5	4	3	2	1	LSB 0	NOTES
READ	$C800_{16}$	PORT 2A	←			KEY				→	BITS 0-7 CONTAIN THE KEYBOARD INPUTS WITH THE FOLLOWING CODE:
	(KEYBD)	KEYBOARD.	1	0	1	1	1	1	1	0	KEY "0"
			0	1	1	1	1	0	1	1	KEY "1"
			0	0	1	1	1	1	1	1	KEY "2"
			0	1	0	1	1	1	1	1	KEY "3"
			1	1	1	0	1	0	1	1	KEY "4"
			1	0	1	0	1	1	1	1	KEY "5"
			1	1	0	0	1	1	1	1	KEY "6"
			1	1	1	1	1	0	0	1	KEY "7"
			1	0	1	1	1	1	0	1	KEY "8"
			1	1	0	1	1	1	0	1	KEY "9"
			1	1	1	1	1	0	1	0	KEY "."
			1	1	0	1	1	1	1	0	KEY "+/-"
			1	1	1	1	0	1	1	0	KEY "E"
			1	1	1	1	0	1	0	1	KEY "CK"
			0	1	1	1	0	1	1	1	KEY "CE"
			1	1	1	0	0	1	1	1	KEY "R"
READ	$C900_{16}$	PORT 2B	MODE				DISPLAY				BITS 4-7 CONTAIN THE OUTPUTS OF THE MODE SWITCH WITH THE FOLLOWING CODE:
	(MODE)	CONTROL SWITCHES	0	0	0	0	X	X	X	X	RADAR, CW
			0	0	0	1	X	X	X	X	RADAR, PULSE
			0	0	1	0	X	X	X	X	SIG GEN, CW
			0	0	1	1	X	X	X	X	SIG GEN, PULSE
			0	1	0	0	X	X	X	X	SIG GEN, SQW
			0	1	0	1	X	X	X	X	SIG GEN, FM
			7	6	5	4	3	2	1	0	

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7	6	5	4	3	2	1	LSB 0	NOTES
			0	1	1	0	X	X	X	X	SIG GEN, FM EXT
			0	1	1	1	X	X	X	X	SELF TEST
			1	0	0	0	X	X	X	X	SPARE
			1	0	0	1	X	X	X	X	SPARE
			1	0	1	0	X	X	X	X	SPARE
			1	0	1	1	X	X	X	X	SPARE
											BITS 0-3 CONTAIN THE OUTPUTS OF THE DISPLAY SELECT SWITCH WITH THE FOLLOWING CODE:
			X	X	X	X	0	0	0	0	FREQ (MHZ)
			X	X	X	X	0	0	0	1	FREQ TUNE (MAX)
			X	X	X	X	0	0	1	0	RF IN PWR (DBM)
			X	X	X	X	0	0	1	1	RF SIG PWR (DBM)
			X	X	X	X	0	1	0	0	PRF (HZ)
			X	X	X	X	0	1	0	1	PW (MICROSEC)
			X	X	X	X	0	1	1	0	RANGE (250 - 40000 YDS)
			X	X	X	X	0	1	1	1	RANGE RATE (0, 50, 250, 500, 1000, 2000)
			X	X	X	X	1	0	0	0	SPARE
			X	X	X	X	1	0	0	1	SPARE
			X	X	X	X	1	0	1	0	SPARE
			X	X	X	X	1	0	1	1	SPARE
			7	6	5	4	3	2	1	0	

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7	6	5	4	3	2	1	LSB 0	NOTES
WRITE	$CA00_{16}$	PORT 2C	←SPARE→				BD	S	5.	6.	BITS 4-7, SPARE
	(MISC)	DECIMAL POINTS &									BIT 3 - LEADING ZERO BLANKING
		KEYBOARD RESET									"0" = LEADING ZERO BLANKING
											"1" = NO BLANKING
											BIT 2 - SPARE
											BIT 1 - DECIMAL POINT FOR 5TH DISPLAY DIGIT.
											"1" - DECIMAL POINT ON
											BIT 0 - DECIMAL POINT FOR 6TH DISPLAY DIGIT.
											"1" - DECIMAL POINT ON
WRITE	$CB00_{16}$	PORT 2 CONTROL	1	0	0	1	0	0	1	0	CONFIGURES 8255 #2 SO THAT PORTS A AND B ARE INPUTS AND PORT C IS AN OUTPUT.
	(CNTRL)										
			7	6	5	4	3	2	1	0	

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7	6	5	4	3	2	1	LSB 0	NOTES
WRITE	$D000_{16}$	PORT 3A	7 ←	D/A						→ 0	CONTAINS THE D/A VOLTAGE IN STRAIGHT BINARY
	(VOLT)	D/A VOLTAGE									LSB = 0.04 VDC
											MSB = 5.12 VDC
WRITE	$D100_{16}$	PORT 3B	FM	A_{FC}		←	MUX			→	BIT 7, FM/FREQ CAL
	(MUX)	MUX/AFC CONTROL									"0" = FM OR FM EXT MODE
											"1" = ANY OTHER MODE
											BITS 5-7, AFC SWEEP AND CALIBRATION
			X	0	0						AFC LOW BAND
			X	0	1						AFC MIDDLE BAND
			X	1	0						AFC HIGH BAND
			0	1	1						HIGH FREQUENCY CALIBRATE
			1	1	1						LOW FREQUENCY CALIBRATE
											BITS 0-4 CONTROL THE DC MULTIPLEXER SELECTION
						0	0	0	0	0	SIG 0, +5 VDC
						0	0	0	0	1	SIG 1, 10 DB CORRECTION FACTOR
						0	0	0	1	0	SIG 2, 20 DB CORRECTION FACTOR
						0	0	0	1	1	SIG 3, 30 DB CORRECTION FACTOR
						0	0	1	0	0	SIG 4, 40 DB CORRECTION FACTOR
						0	0	1	0	1	SIG 5, 50 DB CORRECTION FACTOR
						0	0	1	1	0	SIG 6, 60 DB CORRECTION FACTOR
						0	0	1	1	1	SIG 7, 70 DB CORRECTION FACTOR
						0	1	0	0	0	SIG 8, 80 DB CORRECTION FACTOR
			7	6	5	4	3	2	1	0	

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7	6	5	4	3	2	1	LSB 0	NOTES
			X	X	X	0	1	0	0	1	SIG 9, POWER SUPPLY CHECK
			X	X	X	0	1	0	1	0	SIG 10, COARSE FREQUENCY
			X	X	X	0	1	0	1	1	SIG 11, FREQUENCY TUNE MAX
			X	X	X	0	1	1	0	0	SIG 12, DETECTED POWER
			X	X	X	0	1	1	0	1	SIG 13, RANGE CALIBRATION
			X	X	X	0	1	1	1	0	SIG 14, RF PWR OFFSET
			X	X	X	0	1	1	1	1	SIG 15, SIGNAL PWR OFFSET
			X	X	X	1	0	0	0	0	SIG 16, SPARE (NOT INSTALLED)
						↕					↕
			X	X	X	1	0	1	1	1	SIG 23, SPARE (NOT INSTALLED)
WRITE	$D200_{16}$	PORT 3C	←			RF CONTROL				→	BIT 7, RF SELF TEST
	(RFCTL)	RF CONTROL									"1" = RF SELF TEST
											BIT 6, CW/PULSE
											"0" = PULSE OR SQUARE WAVE MODES
											"1" = CW OR FM MODES
											BIT 5, SQUARE WAVE MODE
											"1" = SQUARE WAVE MODE
											BIT 4, TARGET ENABLE
											"0" = DISABLES RETURN TARGETS
											"1" = ENABLES TARGETS
											BIT 3, COAX SWITCH CONTROL
											"0" = OUTPUT POWER, REFERENCE POWER
											"1" = INPUT POWER, REFERENCE POWER
			7	6	5	4	3	2	1	0	

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7	6	5	4	3	2	1	LSB 0	NOTES
											BIT 2, ISOLATION PIN SWITCH CONTROL
											"0" = OFF, MOST ATTENUATION
											"1" = ON, LEAST ATTENUATION
											BITS 0,1 = RF REFERENCE CONTROL
											1 | 0
											0 | 0 REFERENCE OFF, INPUT/OUTPUT POWER
											0 | 1 LOW CALIBRATION = -27 DBM
											1 | 1 HIGH CALIBRATION = -14 DBM
											1 | 0 NOT USED
WRITE	$D300_{16}$	PORT 3 CONTROL	1	0	0	0	0	0	0	0	CONFIGURES 8255 #3 SO THAT PORTS A, B AND C ARE OUTPUTS.
	(ANALOG)										
			7	6	5	4	3	2	1	0	

Table 4-1. I/O Signal Dictionary - Continued

MODE	ADDRESS	DESCRIPTION	MSB 7	6	5	4	3	2	1	LSB 0	NOTES
WRITE		KEYBOARD INTERRUPT RESET							↓		WRITING A "1" OUT ON THE CPU SERIAL DATA LINE WILL RESET THE KEYBORAD INTERRUPT.
									↓		
READ		RANGE LOAD INHIBIT							↓		READ IN THROUGH THE CPU SERIAL INPUT DATA LINE. A "1" ON THIS LINE WILL INHIBIT THE
									↓		CHANGING OF THE RANGE DATA FROM 60 TO 240 USEC.
									↓		
INPUT		COUNT COMPLETE							↓		USED TO RESET THE COUNT COMPLETE INTERRUPT AND LSB'S OF THE FREQUENCY COUNTER.
		INTERRUPT RESET							↓		USES IO/$\overline{M}$ OUTPUT FROM CPU, USE IN FFH COMMAND.
									↓		
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			7	6	5	4	3	2	1	0	

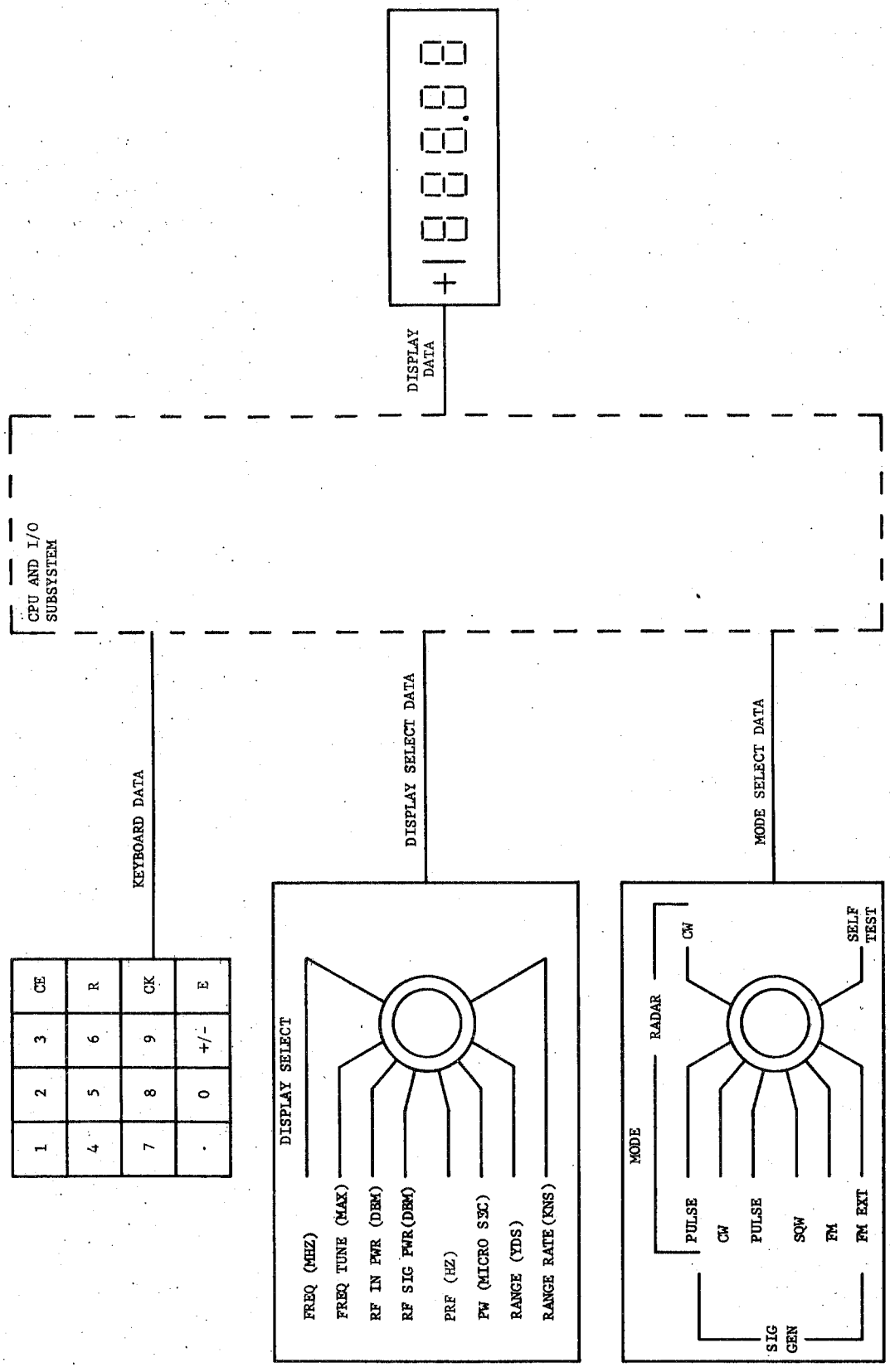


Figure 4-2. Display Subsystem Block Diagram

RANGE RATE (KNS) since these tests are not needed for operation in the radar cw mode. Likewise, when the MODE switch is set to SIG GEN PULSE, a test is performed and a display is generated only if the DISPLAY SELECT switch is set to FREQ (MHZ), RF SIG PWR (DBM), PRF (HZ), PW (MICROSEC), RANGE (YDS), or RANGE RATE (KNS). A display is not generated if the DISPLAY SELECT switch is set to FREQ TUNE (MAX) or RF IN PWR (DBM) since these tests are not needed for operation in the signal generator pulse mode. The type of display generated for each combination of the MODE and DISPLAY SELECT switch settings is provided in T.O. 33D7-44-225-1. Keyboard data is accepted by the CPU and I/O subsystem when the E key is pressed and the MODE switch is set to SIG GEN PULSE or RADAR PULSE and the DISPLAY SELECT switch is set to PW (MICROSEC), RANGE (YDS), or RANGE RATE (KNS). When these positions are selected, the data entered on the keyboard will change the pulse width, range, or range rate of the Test Set generated target. For example, if RANGE (YDS) is selected, the CPU and I/O subsystem outputs display data to indicate the current range value. The operator can change this value by entering a new range value on the keyboard and pressing the E (enter) key. If the entered range value is within limits, the CPU and I/O subsystem displays the new range value and changes the range of the generated target. Detailed keyboard operation is provided in the operation instructions of T.O. 33D7-44-225-1.

4-6. DISPLAY SUBSYSTEM FUNCTIONAL DIAGRAM DESCRIPTION (Figure 6-3)

a. MODE and DISPLAY SELECT Switch Operation. The keyboard, DISPLAY SELECT, and MODE switch data are applied to the CPU and I/O subsystem in the following manner. The display select data (DISPLAY SELECT 20-23) and mode data (MODE 20-23) are applied to Front Panel Interface 1A1A1, which supplies +5 vdc pullups for each signal line. The +5 vdc pullups provide for the generation of TTL logic level inputs to XCVR U2 I/O Bus 0 (addr C800H) and I/O Bus 1 (addr C900H) of the CPU and I/O subsystem. The sequence for reading the mode and display select data is as follows:

(1) When the Test Set is turned on, the DISPLAY SELECT and MODE switch data are read by the CPU and I/O subsystem for the first time. The CPU and I/O subsystem initializes the keyboard I/O bus and the mode and display select I/O bus for input. The CPU and I/O subsystem then reads the DISPLAY SELECT 20-23 and MODE 20-23 data at XCVR U2 I/O bus 1 (addr C900H) and stores the data. The stored MODE 20-23 data is then examined to determine the Test Set operating mode. If the MODE switch is set to SELF TEST, the DISPLAY SELECT 20-23 data is ignored and the CPU and I/O subsystem executes the self-test program.

(2) If the MODE switch is set to any one of the RADAR or SIG GEN positions, the stored DISPLAY SELECT data is examined to determine if a test needs to be performed. This is done by comparing the stored DISPLAY SELECT and MODE data with a table of legal switch combinations stored in the Test Set memory. If a test is required, the CPU and I/O subsystem executes the selected test program and displays the results. If a test is not required, the display is blanked. After the results of the test are displayed or the display is blanked because of an illegal switch combination, the CPU and I/O subsystem reads the DISPLAY SELECT 20-23 and MODE 20-23 data a second time. The switch data read at this time is compared with the

switch data that was stored when the Test Set was turned on. If the new switch data is the same as the stored switch data, the CPU and I/O subsystem continues to blank the display or repeats the selected test. If the new switch data is not the same as the stored switch data, the CPU and I/O subsystem determines if a new operating mode has been selected, replaces the stored switch data with the new switch data, and performs the operation selected by the new switch data. The process of comparing the current DISPLAY SELECT and MODE switch data with the stored switch settings and performing an operation or test is repeated as long as the Test Set is turned on.

b. Keyboard Operation. The keyboard data (ROW 1-4, COL 1-4) is applied to Front Panel Interface 1A1A1, which supplies +5 vdc pullup resistors for each signal line. The +5 vdc pullup resistors provide for the generation of TTL logic levels to XCVR U2 I/O Bus 0 (addr C800H) of the CPU and I/O subsystem. The keyboard data (ROW 1-4, COL 1-4) is read by the CPU and I/O subsystem each time a keyboard switch is pressed. When any key is pressed, the ROW 1, ROW 2, ROW 3, or ROW 4 signal line is at a low logic level. This low logic level forward biases one of the diodes of the diode matrix (CR1 - CR4, R9) on Front Panel Interface 1A1A1, forcing the KYBD INTRPTL signal to a low logic level. The low KYBD INTRPTL clocks flip-flop U29 which applies a high logic level to the RST 5.5 input of CPU U1 in Digital Assembly 1A1A2 in the CPU and I/O subsystem. This causes the CPU and I/O subsystem to read the keyboard data applied to XCVR U2 I/O Bus 0 (addr C800H). The CPU and I/O subsystem checks the loaded keyboard data to determine if the R (reset) key is pressed. If the reset key is pressed, the CPU and I/O subsystem performs a reset operation, which has the same effect as turning the Test Set on. This results in the CPU and I/O subsystem reading the DISPLAY SELECT and MODE switch data as described in previous paragraphs. Pressing the reset key also causes the Test Set signal generator pulse values for pulse width, range, and range rate to be reset (described in target generation subsystem description). If a data key (0-9, ., +/-) is pressed, the CPU and I/O subsystem checks the MODE and DISPLAY SELECT switch settings to determine if the MODE switch is set to SIG GEN PULSE or RADAR PULSE, and if the DISPLAY SELECT switch is set to PW (MICROSEC), RANGE (YDS), or RANGE RATE (KNS). If these switch positions are not selected, the CPU and I/O subsystem ignores the key data. If these switch positions are selected, the CPU and I/O subsystem stores the key data in temporary memory, displays the value of the key data, and goes to the keyboard entry mode. The keyboard entry mode allows each new key data entry to be stored in temporary memory with any previous entries. This continues until the E (enter), CE (clear entry), or CK (clear keyboard) key is pressed. When the enter key is pressed, the keyboard data stored in temporary memory is used to change the pulse width, range, or range rate of the Test Set generated target, and the CPU and I/O subsystem exits the keyboard entry mode. When the clear entry key is pressed, the CPU and I/O subsystem clears the display and the data stored in temporary memory. When the clear keyboard key is pressed, the CPU and I/O subsystem clears the display and the data stored in temporary memory, exits the keyboard entry mode, and displays the previous pulse width, range, or range rate display.

c. Display Operation. The six-digit Test Set display is provided by six 7-segment displays (DS1-DS6). Display DS1 provides the sign (+ or -) and the first

digit (1) display, while displays DS2 through DS6 provide the remaining five digits and two decimal points. Each segment of the six displays is connected to bias resistors, which keep each segment near the turn-on point to decrease the display turn-on time. Displays DS2 through DS4 are driven by BCD-to-seven-segment decoders, and the decimal points (DS5 and DS6) are driven directly by open collector inverters U8-2 and U8-4. Each segment of display DS1 is driven individually by an open collector gate. Operation is as follows:

(1) The display data is generated as a result of a test or operation, and is output to the display logic by the CPU and I/O subsystem as DIGIT 6 D.P. (decimal point), DIGIT 5 D.P., RIPPLE BLANK, DIGIT 6 BIT 0-3 through DIGIT 2 BIT 0-3, DIGIT 1 BIT 0, DIGIT 1 BIT 1, SIGN BIT 0, and SIGN BIT 1 to generate the required display. One of the two decimal points is selected by the CPU and I/O subsystem to provide the significance required by the test or operation.

(2) Leading zeros are blanked by setting the RIPPLE BLANK signal low. The low RIPPLE BLANK causes each display (starting with DS2) to be blanked, if a BCD zero is applied, until the first nonzero BCD code is encountered. For example, if a range rate of -250 is to be displayed, the CPU and I/O subsystem sets the DIGIT 5 D.P. and DIGIT 6 D.P. high (decimal points off). The low RIPPLE BLANK, high SIGN BIT 0 (minus display), low DIGIT 1 BIT 0, 1 (one display off), and the BCD code for 00250 are applied to the display drivers for digits two through six. Since the RIPPLE BLANK is set low, the BCD zero (0XXXX) applied to display driver U7 causes DS2 to go blank and RBO (ripple blank out) to go low; this low is applied to the RBI (ripple blank in) of display driver U6. Since the BCD input to U6 is also zero (X0XXX), DS3 is blanked and the RBO output goes low. Since the code applied to display driver U5 is two (XX2XX), the low applied to the RBI input of driver U5 has no effect; therefore, the last three digits (DS4-DS6) are 250. This makes the completed display -bb250 (b = blank).

d. Self-Test Operation. Self-test operation is started when the MODE switch is set to SELF TEST. The self-test code is detected by the CPU and I/O subsystem which starts execution of the self-test program. During self-test of the display subsystem, display logic operation and keyboard operation are checked in the following manner:

(1) The display logic check begins with the turn-on of all the segments of each indicator. This is done by setting DIGIT 6 D.P. high, DIGIT 5 D.P. high, and RIPPLE BLANK low to enable the two decimal points and the ripple blank; loading the code for a BCD eight (8H) for digits two through six; and setting DIGIT 1 BIT 0, DIGIT 1 BIT 1, SIGN BIT 0, and SIGN BIT 1 high to enable a plus one (+1). This display (+1888.8.8) is present for 2 seconds. Next, the two decimal points are turned off (DIGIT 6 D.P. and DIGIT 5 D.P. low) and the leading zero blanking is inhibited (RIPPLE BLANK low). The remaining display bits are set low to turn off the plus one (+1) and to display a zero for digits two through six (00000). The BCD code for digits one through nine (1H through 9H) are then output to digits two through six to cycle the display from 11111 to 99999. The display is then blanked by turning off the decimal points (DIGIT 6 D.P. and DIGIT 5 D.P. low), turning off the plus one (DIGIT 1 BIT 0, 1 and SIGN BIT 0, 1 low), and setting the remaining display bits high (DIGIT 2 through DIGIT 6 bits high). The self-test program continues to check keyboard operation.

(2) The keyboard self-test is performed by reading the keyboard data each time a key is pressed, converting the code to BCD format, and outputting the BCD code to digit six of the display logic. This cycle is repeated until the E (enter) key is pressed. When the enter code is detected, the self-test program continues through the rest of the self-test program.

4-7. RF TUNE AND FREQUENCY MEASUREMENT SUBSYSTEM BLOCK DIAGRAM DESCRIPTION (Figure 4-3). The function of the rf tune and frequency measurement subsystem is to indirectly measure radar rf frequency by tuning the Test Set rf frequency until it equals the radar rf frequency. This function then measures Test Set rf frequency to indicate the radar rf frequency. The rf tune and frequency measurement function can measure the Test Set rf frequency in all Test Set operating modes. Figure 4-3 shows how the rf tune and frequency measurement circuits work with the other Test Set subsystems to perform the rf tune operation and the Test Set rf frequency measurement operation. The CPU and I/O subsystem provides control data to all subsystems; however, figure 4-3 shows only control data directly used in the rf tune and Test Set rf frequency measurement operations.

a. RF Tune Operation

(1) The Test Set performs the rf tune operation by comparing the rf input frequency with the Test Set rf frequency provided by the Gunn Oscillator. A balanced mixer compares these frequencies, producing the RADAR IF output signal that has a frequency equal to the difference between the rf input frequency and the Test Set rf frequency. The tuning signal conditioning circuits convert the RADAR IF frequency to an RF TUNE voltage that has a maximum value when the RADAR IF frequency is near zero (Test Set rf frequency equals rf input frequency). The analog measurement portion of the measurements subsystem measures the RF TUNE signal voltage, providing the CPU and I/O subsystem with a binary number that is converted to binary coded decimal (BCD) and sent to the display subsystem for display on the analog digital display. The displayed number reaches a maximum value when the Test Set rf frequency is equal to the rf input frequency.

(2) The rf tune operation begins when the CPU and I/O subsystem reads switch data and finds the DISPLAY SELECT switch in the FREQ TUNE (MAX) position. The CPU and I/O subsystem then checks the switch data to determine if the MODE switch is in the RADAR PULSE or RADAR CW position. If the MODE switch is not in one of these positions, the CPU and I/O subsystem sends control data to the display subsystem, blanking the digital display, and then reads the switch data again. This process repeats until the MODE switch or the DISPLAY SELECT switch is moved to a new position. If the MODE switch is in the RADAR PULSE or RADAR CW position when the DISPLAY SELECT switch is in the FREQ TUNE (MAX) position, the CPU and I/O subsystem prepares the Test Set for a power measurement and turns on the rf tune circuits. To do this, the CPU and I/O subsystem sends rf control word data, with bit 2 and bit 3 set to 1, to address D200.

(3) Bit 3 of the rf control word data provides the COAX SWITCH CNTRL signal to close the Coaxial Switch. Then the rf input, applied at the RF IN/OUT connector, is attenuated by the Attenuator, sampled by the 23-db directional coupler, and connected through the Coaxial Switch to the power measurements subsystem. The power measurements subsystem produces an RF POWER signal voltage proportional to the power sampled by the 23-db directional coupler. The CPU and I/O subsystem then sends control data (not shown in figure 4-3) to the analog measurement subsystem

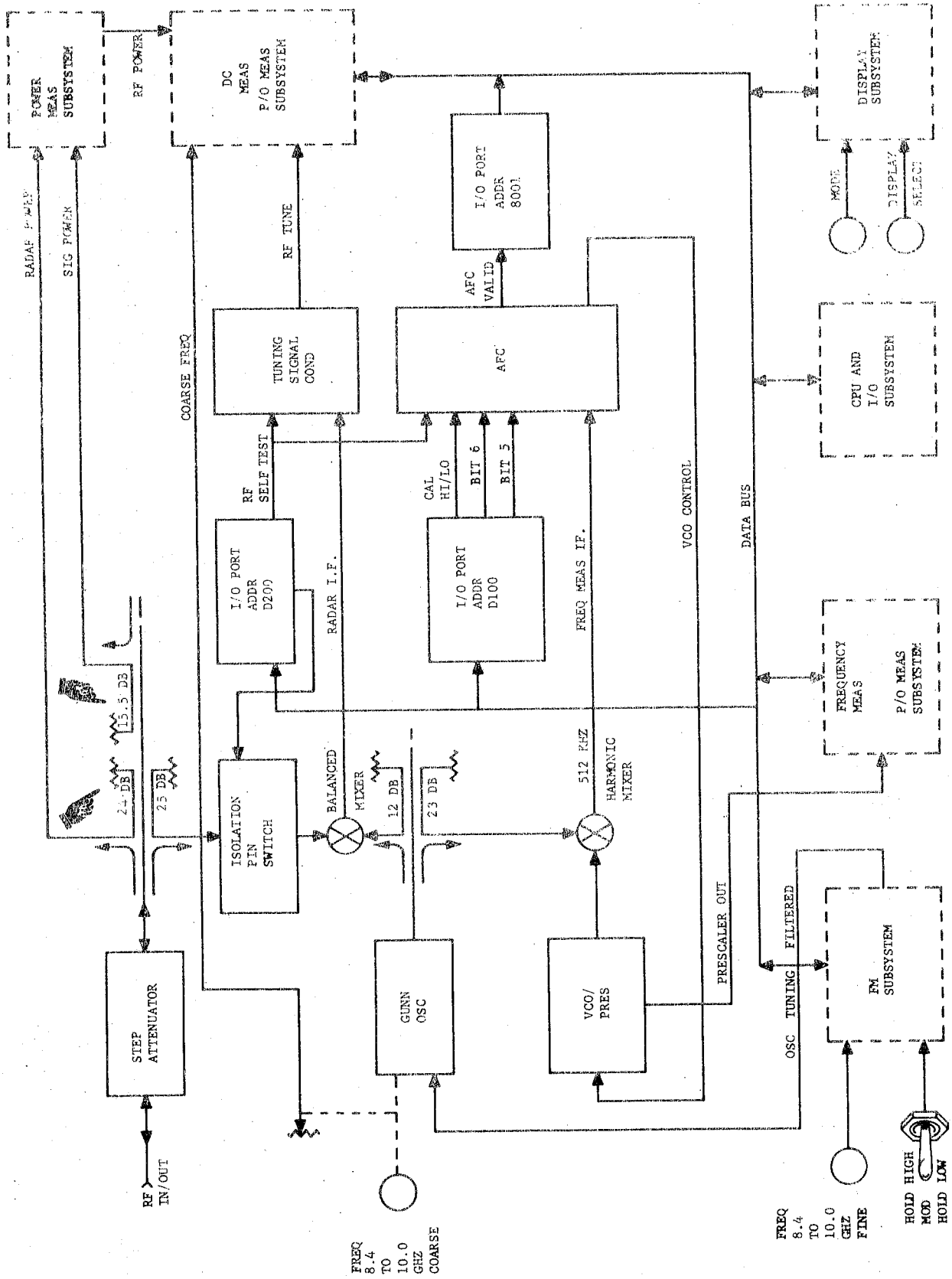


Figure 4-3. RF Tune and Frequency Measurement Subsystem Block Diagram

to cause measurement of the RF POWER signal voltage. If this measurement indicates that the power measurements subsystem is overdriven by too strong an rf signal, the CPU and I/O subsystem sends data to the display subsystem to display a + (plus sign) on the digital display. If the measurement indicates that the rf signal is too weak to be detected by the power measurements subsystem, the CPU and I/O subsystem sends data to display a - (minus sign) on the digital display. The power measurement is repeated until the measured rf power is neither too strong nor too weak.

(4) When the ATTENUATION DB 0-80 control is adjusted so that rf power is detected but does not overdrive the power measurements subsystem, the rf power level is in the range where the rf tune operation is possible. The CPU and I/O subsystem performs the rf tune operation by sending control data to the analog measurement subsystem to cause measurement of the RF TUNE signal voltage.

(5) Bit 2 of the rf control word data provides the ISOLATION PIN CONTROL signal to enable the isolation pin switch. The rf input from the RF IN/OUT connector is attenuated by the Step Attenuator, sampled by the 25-db directional coupler, and passes through the enabled isolation pin switch to one input of the balanced mixer. The Gunn Oscillator provides the Test Set rf frequency through the 12-db directional coupler to the second input of the balanced mixer. The balanced mixer output is a frequency equal to the difference between the rf input frequency and the Test Set rf frequency. Therefore, this RADAR IF signal output decreases in frequency as the Gunn Oscillator is tuned closer to the rf input frequency. As the Gunn Oscillator frequency (Test Set rf frequency) approaches the rf input frequency, the RADAR IF frequency approaches zero.

(6) The Gunn Oscillator is mechanically tuned by rotating the FREQ 8.4 TO 10.0 GHZ COARSE control. Eight complete turns of this control tunes the Gunn Oscillator frequency from 8.35 GHz to 10.05 GHz. Tuning is linear with a frequency change of approximately 0.57 MHz per degree of COARSE control rotation. Fine tuning is provided electronically by the OSCILLATOR TUNING FILTERED signal (tuning voltage) from the frequency modulation subsystem. In the RADAR PULSE or CW mode, the tuning voltage comes from a potentiometer connected to the FREQ 8.4 TO 10.0 GHZ FINE control. This FINE control provides a frequency tuning range of approximately 10 MHz or approximately 0.03 MHz per degree of FINE control rotation.

(7) The tuning signal conditioning circuits process the RADAR IF signal to produce the RF TUNE signal voltage. This voltage is near zero when the RADAR IF frequency is greater than 100 MHz and increases to a maximum value as the RADAR IF frequency approaches zero. Therefore, the rf tune signal voltage increases when the Test Set rf frequency (Gunn Oscillator) is tuned within 100 MHz of the rf input frequency and reaches a maximum voltage when the Test Set rf frequency equals the rf input frequency. The tuning signal conditioning circuits limit, filter (low-pass filter), and peak detect the RADAR IF signal to produce the RF TUNE signal voltage. Because the RADAR IF signal is limited, its amplitude has little effect on the RF TUNE voltage. Because the RADAR IF signal is peak detected, it may be continuous wave or pulsed and still produce a steady dc voltage as the RF TUNE voltage. However, the RF TUNE voltage produced is somewhat smaller for pulsed operation and depends on the pulse duty cycle.

(8) When the CPU and I/O subsystem sets up the analog measurement subsystem to measure the RF TUNE signal voltage, the measurement is made, resulting in a binary number value between 0 and 255. The CPU and I/O subsystem converts the binary number to BCD and sends the BCD number data to the display subsystem where the number value is displayed on the digital display. This number value is proportional to the RF TUNE signal voltage and is therefore a maximum value when the Test Set rf frequency is equal to the rf input frequency, since the RF TUNE signal voltage is maximum for this condition.

(9) After the rf tune value is displayed, the CPU and I/O subsystem repeats the entire cycle of operation again. The DISPLAY SELECT and MODE switch positions are read, the rf power is tested, the RF TUNE signal voltage is measured, and the result is displayed. The entire cycle takes approximately 250 milliseconds and repeats continuously. Therefore, the FREQ TIME (MAX) display is updated approximately four times per second, allowing the Test Set operator to monitor tuning as he adjusts the FREQ 8.4 TO 10.0 COARSE and FINE controls.

b. Test Set RF Frequency Measurement Operation. The Gunn Oscillator provides the Test Set rf frequency which ranges from 8.35 to 10.05 GHz. The Test Set measures this frequency indirectly by locking the frequency of a voltage-controlled oscillator (vco) to a fraction of the Gunn Oscillator frequency, then measuring the vco frequency. A harmonic mixer produces the FREQUENCY MEASUREMENT IF signal frequency which is equal to the difference between the Gunn Oscillator frequency and the 11th, 12th, or 13th harmonic of the vco frequency. The afc circuits receive the FREQUENCY MEASUREMENT IF signal and produce the VCO CONTROL signal to tune the vco such that the FREQUENCY MEASUREMENT IF signal frequency is 512 kHz. Therefore, the vco frequency multiplied by 11, 12, or 13 is 512 kHz less than the Gunn Oscillator frequency. A prescaler divides the vco frequency by 256 to provide the PRESCALER OUT signal frequency. The digital measurement subsystem measures this frequency (approximately 3 MHz) by a digital counting method and sends the count result to the CPU and I/O subsystem where the Test Set rf frequency is calculated as follows:

(1) The CPU and I/O subsystem calculates the Test Set rf frequency as though the 13th harmonic of the vco frequency is causing the harmonic mixer output. It multiplies the PRESCALER OUT frequency by 256 to account for the prescaling, multiplies by 13 to account for the 13th harmonic, then adds 512 kHz to account for the offset of the harmonic mixer. This calculation gives the correct Gunn Oscillator frequency if the 13th harmonic of the vco frequency is causing the harmonic mixer output. However, this calculated Gunn Oscillator frequency is too large by 13/12 or 13/11 if the 12th or 11th harmonic is causing the harmonic mixer output. The CPU and I/O subsystem corrects the calculated Gunn Oscillator frequency, if necessary, by multiplying by 12/13 or 11/13 to make the calculated frequency agree closely with the results of a coarse frequency measurement.

(2) The CPU and I/O subsystem does the coarse frequency measurement by causing the analog measurement subsystem to measure the COARSE FREQ signal voltage provided by a potentiometer connected to the FREQ 8.4 TO 10.0 COARSE control. This voltage indicates the position of the COARSE control and thus indicates coarse Gunn

Oscillator frequency. If the calculated frequency agrees with the measured coarse frequency, the CPU and I/O subsystem converts the calculated frequency data to binary coded decimal (BCD) and sends the BCD data to the display subsystem for display. If the calculated frequency does not agree with the coarse frequency, the CPU and I/O subsystem multiplies the calculated value by 12/13 or 11/13 to obtain a value that does agree. Then the CPU and I/O subsystem converts this value to BCD and sends it to the display subsystem. At the display subsystem, frequency is displayed as 8000.0 to 10000.0 MHz on the digital display. If the CPU and I/O subsystem is unable to calculate a frequency that agrees with the coarse frequency, it sends the afc error message to the display subsystem. The afc error message is displayed as ⊔104.

(3) The Test Set rf frequency measurement operation begins when the CPU and I/O subsystem reads switch data and finds the DISPLAY SELECT switch in the FREQ (MHZ) position. Then the CPU and I/O subsystem determines if the MODE switch is in the FM subsystem position. If it is, the CPU and I/O subsystem determines if the FM HOLD HIGH-MOD-HOLD LOW switch is in the MOD position. If it is, the frequency modulation subsystem is sweeping the Gunn Oscillator frequency and a frequency measurement is not possible. In this case, the CPU and I/O subsystem sends data to the display subsystem to blank the digital display. If the frequency modulation subsystem is not sweeping the Gunn Oscillator frequency, the CPU and I/O subsystem prepares to measure the PRESCALER OUT signal frequency.

(4) The CPU and I/O subsystem reads data from port 8001 to determine if the afc circuits are locked. Bit 6 of the data from port 8001 is 1 when the AFC VALID signal is high, indicating afc lock. Bit 6 is 0 when the AFC VALID signal is low, indicating afc sweep. If bit 6 is 1, the CPU and I/O subsystem sends data to the frequency measurement subsystem, causing a count of the PRESCALER OUT signal frequency. If bit 6 is 0, the CPU and I/O subsystem sends data to the afc circuits to attempt an afc lock.

(5) An afc lock exists when the FREQ MEAS IF signal out of the harmonic mixer has a frequency less than 1 MHz. This happens when a harmonic of the vco frequency is within 1 MHz of the Gunn Oscillator frequency. When the FREQ MEAS IF signal frequency is less than 1 MHz, the afc circuits produce the high AFC VALID signal, then adjust the VCO CONTROL signal voltage for a 512 kHz FREQ MEAS IF signal frequency. During this desired afc lock, the 11th, 12th, or 13th harmonic of the vco frequency is 512 kHz less than the Gunn Oscillator frequency. The afc circuits adjust the VCO CONTROL signal voltage, tuning the vco frequency to maintain this condition. For example, when the Gunn Oscillator frequency is 9,000.512 MHz, the afc circuits will tune the vco frequency to 750 MHz during afc lock. The 12th harmonic of the 750 MHz vco frequency is 9,000 MHz (12 X 750 MHz). This is 0.512 MHz or 512 kHz less than the Gunn Oscillator frequency.

(6) The desired output of the harmonic mixer is a frequency equal to the difference between frequencies at the two inputs (Gunn Oscillator frequency and a harmonic of the vco frequency). This is called a first order modulation product. For example, when the vco frequency is 750 MHz, the frequencies of its 11th, 12th, and 13th harmonics are 8,250 MHz, 9,000 MHz, and 9,750 MHz and are present at one

input to the harmonic mixer. Then a Gunn Oscillator frequency of 8,250.512 MHz, 9,000.512 MHz, or 9,750.512 MHz at the other input of the harmonic mixer causes a 512 kHz frequency as the desired first order modulation product. This is because each of these frequencies is 512 kHz (0.512 MHz) greater than a vco harmonic frequency. Frequencies of 8,249.488 MHz, 8,999.488 MHz, and 9,749.488 MHz could also cause a 512 kHz frequency as the first order modulation product since each is 512 kHz less than a vco harmonic frequency. Because the afc circuits are designed to lock with the Gunn Oscillator frequency 512 kHz greater than the vco harmonic frequency, only 8,250.512 MHz, 9,000.512 MHz, or 8,250.512 MHz will cause the desired lock as a result of a 512 kHz first order modulation product.

(7) The harmonic mixer also has second order modulation products present in its output. One second order modulation product is a frequency equal to the difference between the frequencies of two first order modulation products. It is possible that this second order modulation product could be 512 kHz and therefore could cause an undesired afc lock. For example, a 750 MHz vco frequency produces 11th and 12th harmonic frequencies of 8,250 MHz and 9,000 MHz at the harmonic mixer input. A Gunn Oscillator frequency of 8,625.256 MHz at the other harmonic mixer input causes first order modulation product frequencies at 375.256 MHz (8,625.256 MHz - 8,250 MHz) and 374.744 MHz (9,000 MHz - 8,625.256 MHz). The 512 kHz difference between these two frequencies causes a 512 kHz second order output from the harmonic mixer which can cause the undesired afc lock.

(8) When no afc lock exists, the afc circuit sweep the vco frequency over one of three bands by ramping the VCO CONTROL voltage from a lower limit voltage to an upper limit voltage. If no afc lock occurs before the upper limit voltage is reached, the afc circuits reset the VCO CONTROL voltage to the lower limit voltage and another ramp begins. This repeatedly sweeps the vco frequency over the selected band until afc lock occurs or another band is selected. Bits 5 and 6, stored at data port D100, select the high and low limit voltages for each band and therefore select the vco frequency range for each band.

(9) Typically, the vco frequency sweeps from 730 to 755 MHz for the low band, from 752 to 778 MHz for the mid band, and from 775 to 801 MHz for the high band. The 11th, 12th, and 13th harmonics of the vco frequency sweep the X-band frequency range as the vco frequency sweeps the three bands (figure 4-4). For example, as the vco frequency sweeps 730 to 755 MHz for low band, the 11th harmonic sweeps 8,030 to 8,305 MHz, the 12th harmonic sweeps 8,760 to 9,060 MHz, and the 13th harmonic sweeps 9,490 to 9,815 MHz. The remaining X-band frequencies are swept when the vco sweeps in the mid and high bands.

(10) Bits 5 and 6 from data port D100 select the low, mid, or high band and may also stop the sweep. Then bit 7 selects either a calibrate high voltage or a calibrate low voltage as the VCO CONTROL signal. These voltages tune the vco to a maximum or minimum frequency corresponding to the highest frequency in the high band (approximately 800 MHz) or the lowest frequency in the low band (approximately 725 MHz). During a calibration procedure, the calibrate high and calibrate low voltages are used to adjust the afc circuits so that the frequency bands covered by the vco harmonics overlap to cover the X-band, as shown in figure 4-4. The

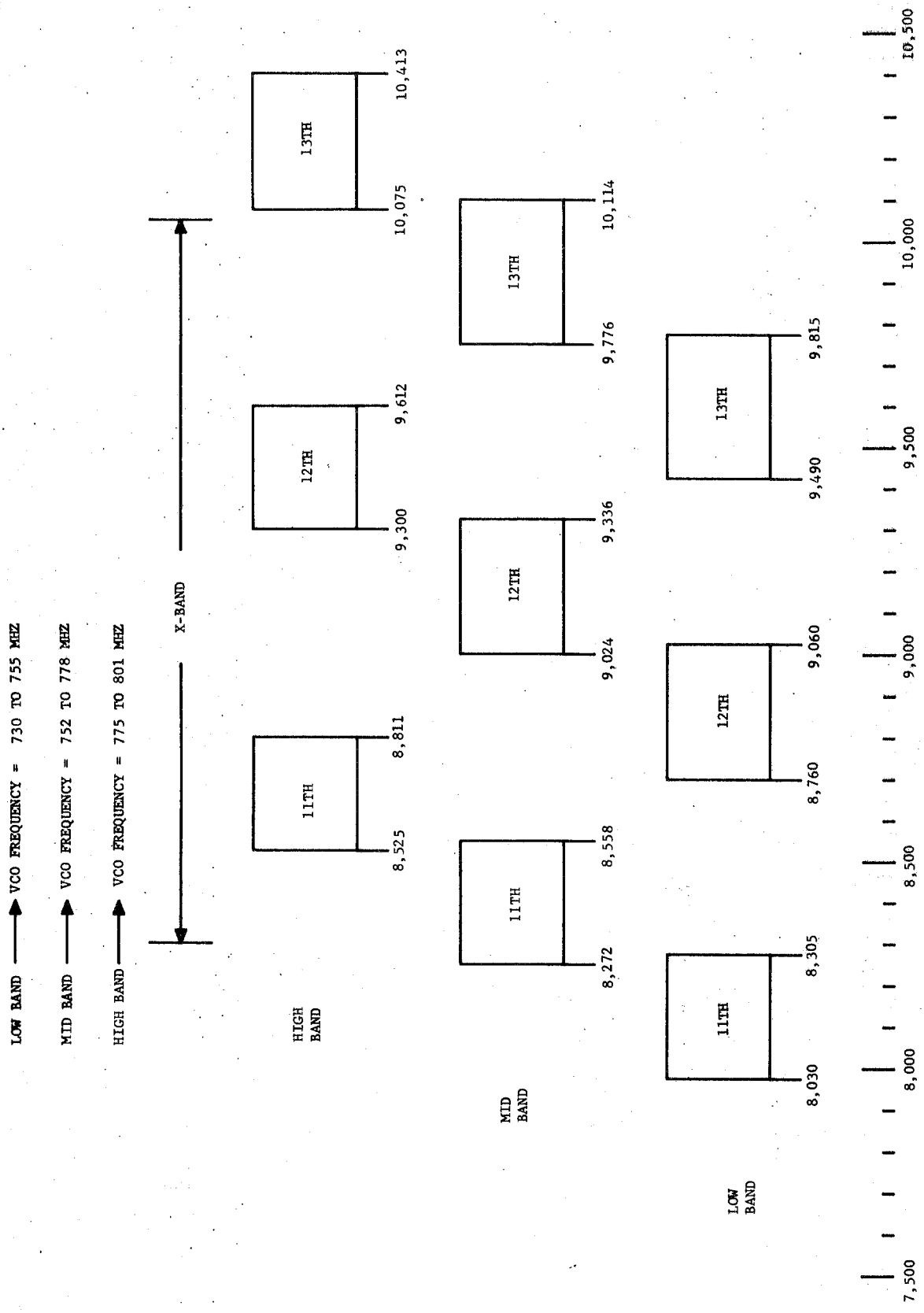


Figure 4-4. X-Band Frequency Coverage By VCO Harmonics

calibrate high and calibrate low voltages are also used to break the undesired lock when the afc circuits lock on a second order modulation product from the harmonic mixer.

(11) When an afc lock exists, the PRESCALER OUT signal frequency is counted to determine Test Set rf frequency. The CPU and I/O subsystem sends data to the digital measurement subsystem to select the PRESCALER OUT signal, to select frequency count operation, and to set the count gate time at 0.3328 second. The digital measurement subsystem counts the PRESCALER OUT signal pulses for 0.3328 second to obtain a count number. The CPU and I/O subsystem receives the count number, divides this number by 10, and adds an offset to calculate a frequency number to be displayed. This number is correct if the afc circuits are locked on the 13th harmonic, but must be corrected if the afc circuits are locked on the 12th or 11th harmonic. The CPU and I/O subsystem causes a voltage measurement of the COARSE FREQ signal to get a coarse measurement of Test Set rf frequency. If the coarse measurement is within 200 MHz of the calculated value, the calculated value is converted to binary coded decimal form and is sent to the display subsystem for display.

(12) If the calculated frequency is not within 200 MHz of the coarse measurement, a new frequency is calculated. This new frequency will be correct if the afc circuits are locked on the 12th harmonic. The original count number, divided by 10, is multiplied by 12/13 to correct for the 12th harmonic afc lock. An offset is added to calculate the new frequency. If the new calculated frequency is within 200 MHz of the coarse measurement, the new calculated frequency is displayed. If it is not within 200 MHz, a third frequency is calculated to correct for 11th harmonic afc lock. The original count, divided by 10, is multiplied by 11/13, and an offset is added to get the third calculated frequency. If this frequency is within 200 MHz of the coarse measurement, this new frequency is displayed. If the third calculated frequency is not within 200 MHz of the coarse measurement, the CPU and I/O subsystem finds the count invalid.

(13) For example, when the Test Set rf frequency from the Gunn Oscillator is 9,000.512 MHz, the afc circuits can lock with a 750 MHz vco frequency, since the 12th harmonic is 9,000 MHz, 512 kHz less than the Gunn Oscillator frequency. The PRESCALER OUT signal frequency is 2,929,687.5 Hz (750 MHz/256). The digital measurement subsystem counts this frequency for 0.3328 second, resulting in a count of 975,000 (2,929,687.5 X 0.3328). The CPU and I/O subsystem divides the count by 10 to get 97,500 and adds an offset of 5 to get a display value of 97,505. Since frequency is displayed in MHz with a decimal point between the two least significant digits, this number indicates a frequency of 9,750.5 MHz.

(14) The CPU and I/O subsystem causes the coarse frequency measurement and obtains a value close to 9,000 MHz. Since this is not within 200 MHz of the first calculated frequency, the CPU and I/O subsystem calculates a second frequency by multiplying 97,500 by 12/13 to get 90,000, then adding an offset of 5 to get 90,005. This number indicates a frequency of 9,000.5 MHz, and therefore is within 200 MHz of the 9,000 MHz coarse frequency. The CPU and I/O subsystem converts this number to a binary coded decimal and sends it to the display subsystem where it is displayed as 9,000.5 MHz.

(15) In the above example, the offset of 5 accounts for the 0.5 MHz (512 kHz) offset between the vco harmonic frequency and the Gunn Oscillator frequency. In an actual measurement, the gate time is not exactly 0.3328 seconds and, therefore, the count is slightly in error. In the actual calculation performed by the CPU and I/O subsystem, the offset added is not 5, but another number which compensates for this count error, and other errors, as well as the 0.5 MHz offset in frequencies.

(16) If, on the first attempt, the CPU and I/O subsystem finds no afc lock or finds an invalid count, it performs a sequence of steps to find a valid count. First, it sends data to data port D100 to cause the calibrate high voltage as the VCO CONTROL signal. After a 1-millisecond wait, it sends new data to cause the calibrate low voltage. This breaks an undesired afc lock which may have resulted in an invalid count. After another 1-millisecond wait, the CPU and I/O subsystem sends new data, causing the afc circuits to sweep the mid band. After a 250-millisecond wait, it checks for afc lock again and makes a count if the afc is locked. If there is no lock or if the count is invalid, the CPU and I/O subsystem performs the same steps again to attempt a count with afc lock in the high band. If there is no lock or if the high band count is invalid, the CPU and I/O subsystem attempts the same steps for low band. If there is no afc lock or if the count is invalid this time, the CPU and I/O subsystem sends an error message to the display subsystem. This error message is displayed as ␣104.

(17) Once the frequency or afc error message is sent for display, the CPU and I/O subsystem repeats the entire frequency measurement sequence: reading switch data, checking for FREQ (MHZ) position of the DISPLAY SELECT switch, checking that the FM HOLD HIGH-MOD-HOLD LOW switch is not in the MOD position if the MODE switch is in the FM position, checking for afc lock, making a count, calculating the frequency, making the coarse frequency measurement, comparing calculated frequency with coarse frequency, recalculating frequency when necessary, and displaying the correct frequency or the error message.

(18) After the first valid count is found, the afc circuits hold the desired lock, provided that the Gunn Oscillator frequency is not changing. Then the CPU and I/O subsystem finds afc lock and a valid count on the first attempt on each repetition of the frequency measurement. This sequence can then be repeated to update the displayed frequency faster than twice per second. If the Gunn Oscillator frequency is changing, the cycle takes longer because the afc circuits may have to sweep two or three bands, searching for a lock. If the Gunn Oscillator frequency is changing rapidly, it may not be possible to get afc lock and a valid count. Therefore, the afc error message may be displayed intermittently during rapid frequency tuning. The afc error message is also displayed as the FREQ 8.4 TO 10.0 GHZ COARSE control is turned in the range where the frequency returns from high to low end, because the COARSE FREQ voltage is invalid at that time.

c. Radar Frequency Measurement. In the RADAR PULSE or RADAR CW mode, radar frequency is determined by an rf tune operation followed by a Test Set rf frequency measurement. The rf tune operation occurs when the DISPLAY SELECT switch is in the FREQ TUNE (MAX) position. First, the Test Set measures the radar rf power to determine if it is in the range where the frequency tune operation is possible.

The Test Set displays a + (plus sign) on the digital display when the radar rf power is too large for the rf tune operation, and displays a - (minus sign) when the radar rf power is too small. The ATTENUATION DB 0-80 control is used to adjust the radar rf power until it is in the range where rf tune operation is possible. Then the digital display indicates a number between 0 and 255. The FREQ 8.4 TO 10.0 GHZ COARSE and FINE controls tune the Test Set rf frequency for a maximum number on the digital display. At this point, the Test Set rf frequency is equal to the radar rf frequency. In the RADAR CW mode, the maximum number displayed on the digital display during the rf tune operation is typically 170 or greater. In the RADAR PULSE mode, the maximum number displayed on the digital display during the rf tune operation depends on the radar duty cycle. For signals with duty cycles greater than 0.001, the maximum number is approximately 100 or greater.

d. Test Set RF Frequency Measurement

(1) The Test Set measures Test Set rf frequency when the DISPLAY SELECT switch is in the FREQ (MHZ) position. The Test Set rf frequency in megahertz is displayed as 8400.0 to 10000.0 on the digital display.

(2) During frequency measurement in RADAR modes (RADAR CW or RADAR PULSE), the DISPLAY SELECT switch may be placed to FREQ (MHZ) at any time to measure and display Test Set rf (target return) frequency. If the rf tune operation has been performed, the Test Set rf frequency displayed is equal to the radar rf frequency. The Test Set rf (target return) frequency may also be tuned to any desired X-band frequency, regardless of the radar frequency, by adjusting the FREQ 8.4 TO 10.0 GHZ COARSE and FINE controls until the desired frequency is displayed on the digital display.

(3) During Test Set rf frequency measurement in SIG GEN CW, SIG GEN PULSE, and SIG GEN SQW modes, the DISPLAY SELECT switch may be placed to FREQ (MHZ) at any time to measure and display Test Set rf frequency. The frequency may then be adjusted to any desired X-band frequency by adjusting the FREQ 8.4 TO 10.0 GHZ COARSE and FINE controls until the desired frequency is displayed on the digital display.

(4) During Test Set rf frequency measurement in SIG GEN FM mode, the undeviated Test Set rf frequency and the maximum deviation frequency are measured and displayed when the FM HOLD HIGH-MOD-HOLD LOW switch is in the HOLD LOW and HOLD HIGH positions, respectively, and the DISPLAY SELECT switch is in the FREQ (MHZ) position. No frequency is displayed when the FM HOLD HIGH-MOD-HOLD LOW switch is in the MOD position. The frequency is sweeping at this time and the digital display is blanked.

(5) During Test Set rf frequency measurement in SIG GEN FM EXT mode, the undeviated Test Set rf frequency is measured as described for the SIG GEN FM mode.

4-8. RF TUNE AND FREQUENCY MEASUREMENT DETAILED FUNCTIONAL DIAGRAM DESCRIPTION (Figure 6-4). Figure 6-4 shows the physical location of all circuits and signals in the rf tune and frequency measurement subsystem. The following paragraphs

describe, in detail, the purpose and characteristics of these circuits and signals, and the self-test operation.

a. RF Tune Circuits

(1) Sheet 1 of figure 6-4 shows the rf tune circuits which are used in tuning the Test Set rf frequency equal to the frequency of the radar under test. The rf tune circuits compare the Test Set rf frequency, provided by tunable Gunn Oscillator 1A1A5Y1, with the rf frequency of the radar input to the Test Set, and produce a FREQ TUNE output signal which has a maximum voltage when the two frequencies are equal. Other Test Set circuits measure this signal voltage to provide a digital display indication which reaches a maximum value when the Test Set rf frequency is tuned equal to the radar rf frequency.

(2) The radar signal is input at front panel RF IN/OUT connector 1A1J2 and passes through Detector 1A1A6 and cable 1A1W3 to Step Attenuator 1A1A8AT1. The Step Attenuator attenuates the RF IN/OUT signal from 0 to 80 db, in steps of 10 db, to provide the ATTENUATOR OUT/IN signal level of 0 to -14 db through cable 1A1W1 to connector J1 on Coupler Module 1A1A4A2. Inside Coupler Module 1A1A4A2, the signal is coupled, with a 20-db loss, through a directional coupler, and passes through an enabled isolation pin switch to the output at connector J5. This output is applied via cable 1A1A4W2 to connector J3 on Modulator/Mixer 1A1A4A1 where the output is applied as the radar frequency input to a balanced mixer.

(3) At the beginning of rf tune operation, the CPU and I/O subsystem turns on the isolation pin switch by sending rf control word data, with bit 2 set, to address D200. This data is latched in XCVR U1 on Microwave Interface 1A1A3, providing the high ISOLATION PIN CONTROL signal to turn off isolation pin switch driver Q6. This provides a negative voltage as the RF TUNE ON/OFF signal to connector J6 on Coupler Module 1A1A4A2. This voltage turns on the isolation pin switch in Coupler Module 1A1A4A2, allowing the radar frequency to pass as previously described. When the rf tune operation is not being done, the CPU and I/O subsystem sends the rf control word with bit 2 reset. This turns on Q6, providing a positive voltage as the RF TUNE ON/OFF signal. The positive voltage turns off the isolation pin switch, providing 60-db attenuation in the rf path. This keeps rf energy from feeding back from the balanced mixer, through the 25-db directional coupler to RF IN/OUT connector J2, and interfering with the Test Set return target signal.

(4) Tunable Gunn Oscillator 1A1A5Y1 in RF Oscillator 1A1A5 provides the Test Set rf frequency as the OSC OUTPUT signal. This signal is applied through cable 1A1W2 to connector J1 on Modulator/Mixer 1A1A4A1. Inside the Modulator/Mixer, the signal is applied through a 16-db directional coupler to the second input of the balanced mixer. The balanced mixer compares this frequency with the radar frequency at its other input and provides an output frequency equal to the difference between the two input frequencies. This difference frequency passes through a low-pass filter and is output as the RADAR IF signal at connector 1A1A4A1J8.

(5) The RADAR IF signal is applied through connector 1A1A3P1 and a cable to standoff E8 on Microwave Interface 1A1A3, then to the input of the tuning signal conditioning circuits. Differential amplifier U12 amplifies the RADAR IF signal by 100 to drive a limiter comprising diodes CR26 and CR27. The output of the limiter, monitored at test point TP1, is 0.7 volt peak to peak during rf tune operation. Because the limiter holds the signal amplitude constant at this point, radar signal amplitude variations will have no effect beyond this point. The limiter output is applied to differential amplifier U13. The amplifier bandwidth is 10 MHz and the amplifier outputs are applied to two peak detectors. Amplifier output 1 goes to a 500-kHz filter at the input to the 500-kHz peak detector. Therefore, the amplifier output 1, monitored at test point TP2, is at maximum amplitude when the RADAR IF frequency is less than 500 kHz, and decreases in amplitude as the RADAR IF frequency increases. Amplifier output 2 goes to the 10-MHz peak detector.

(6) The peak detectors detect the differential output of the amplifier to produce negative dc voltages at test points TP4 and TP3. These voltages are added, amplified, and inverted, by summing amplifier U14 to produce the FREQ TUNE signal at test point TP38. The FREQ TUNE signal is a dc voltage that increases from zero volts as the Test Set rf frequency from the Gunn Oscillator is tuned within 100 MHz of the radar frequency, causing a RADAR IF frequency less than 100 MHz. As the Test Set rf frequency is tuned within 500 kHz of the radar frequency, the RADAR IF frequency decreases below 500 kHz, and the FREQ TUNE voltage reaches a maximum value.

(7) When the radar input signal is continuous wave (CW), the RADAR IF signal is also CW and produces a maximum FREQ TUNE signal voltage of about 9.6 volts as the Test Set rf frequency is tuned within 500 kHz of the radar frequency.

(8) When the radar input signal is pulsed, the RADAR IF signal is also pulsed, but the peak detectors produce a dc voltage with a small amount of ripple at the radar prf rate. The peak detectors produce a dc voltage because their discharge time constant (680 milliseconds) is long when compared with the pulse repetition interval of the radar signal. The maximum FREQ TUNE signal voltage produced for a pulsed radar signal depends on the radar pulse width and prf but is typically about 5.2 volts or greater for radars with 0.001 or greater duty cycle.

(9) During the rf tune operation, the measurements subsystem circuits on Microwave Interface 1A1A3 measure the FREQ TUNE signal voltage to provide the CPU and I/O subsystem with a number between 0 and 255. This number is sent to the display subsystem for display to the Test Set operator. This number is maximum when the FREQ TUNE signal voltage is maximum, and is typically about 170 when tuning to CW radar signals, and about 100 when tuning to pulsed radar signals with a 0.001 duty cycle.

b. Self-Test of RF Tune Circuits

(1) Self-test checks the tuning signal conditioning circuits in Microwave Interface 1A1A3 by applying a 64-kHz square wave to simulate the RADAR IF signal.

The resulting FREQ TUNE signal voltage is equal to the maximum voltage possible during rf tune with a CW radar signal. The measurements subsystem measures this voltage, to check that it is between 5.87 and 10.16 volts dc. If it is not, error message ⌊170 is displayed on the digital display. Then self-test turns off the 64 kHz square wave and, after a 5-second wait to discharge the peak detectors, causes the measurements subsystem to measure the FREQ TUNE signal voltage again. This time, with no input to the tuning signal conditioning circuits, the FREQ TUNE signal voltage must be between 0.00 and 1.07 volts dc. If it is not, error message ⌊171 is displayed on the digital display.

(2) Self-test checks the tuning signal conditioning circuits, and verifies that the measurements subsystem can measure the FREQ TUNE signal (SIG 11 input to the analog multiplexer). Self-test does not check the rf tune components in Modulator/Mixer 1A1A4A1 or Coupler Module 1A1A4A2. The isolation pin switch driver on Microwave Interface 1A1A3 is also not tested.

(3) At the beginning of test number 170 of the self-test, the CPU and I/O subsystem sends rf control word data to address D200 with the rf self-test bit (bit 7) set. This data is stored in XCVR U1 on Microwave Interface 1A1A3 (sheet 3), causing the high RF SELF TEST signal which enables gate U15. Clock generator U24 on Digital Assembly 1A1A2 provides the 0.064-MHz signal through connector 1A1A3J2 to the input of enabled gate U15. The 64-kHz square wave out of gate U15 is reduced to about 8 millivolts peak to peak by a voltage divider comprising resistors R123 and R124 to provide the 64-kHz (RFST) signal.

(4) The 64-kHz rf self-test (RFST) signal goes to the input of the tuning signal conditioning circuits at input 2 of differential amplifier U12 (sheet 1). Limiter CR26, CR27 limits the diffferential amplifier outputs to 0.7 volt peak to peak to provide the two inputs to amplifier U13. Since the 64-kHz frequency is well within the bandpass of both outputs, maximum amplitude signals (about 14 volts peak to peak) are applied to the peak detectors, causing maximum negative voltages (about -6.5 volts) at test points TP4 and TP3. Summing amplifier U14 combines these inputs to produce the FREQ TUNE signal voltage of about 9.2 volts. This voltage is measured during test 170; if the voltage is between 5.87 and 10.16 volts, self-test goes on to test 171. If the FREQ TUNE signal voltage is not within these limits, self-test stops and ⌊170 is displayed on the digital display.

(5) At the beginning of test number 171, the CPU and I/O subsystem turns off the 64-kHz rf self-test (RFST) signal by sending all zero data as the rf control word to address D200. The CPU and I/O subsystem counts off a 5-second wait to allow the peak detectors to discharge, then causes a measurement of the FREQ TUNE signal voltage. If this voltage is now between 0.00 and 1.07 volts, self-test continues; if not, self-test stops with ⌊171 displayed on the digital display.

c. Frequency Measurement Circuits

(1) Sheets 2 and 3 of figure 6-4 show the frequency measurement circuits which measure the Test Set rf frequency provided by tunable Gunn Oscillator 1A1A5Y1 in RF Oscillator 1A1A5. Automatic frequency control (afc) circuits (sheet 3) tune

a voltage controlled oscillator (vco) to a fraction of the Gunn Oscillator frequency. The vco frequency is prescaled and counted to provide a number to the CPU and I/O subsystem. This number is used in calculating the Test Set rf frequency. The frequency measurement circuits also provide a COARSE FREQ signal voltage which is measured to provide an estimate of the Test Set frequency. If the calculated frequency agrees with the estimate, it is displayed on the digital display.

(2) Gunn Oscillator 1A1A5Y1 in RF Oscillator 1A1A5 produces the Test Set rf frequency as the OSC OUTPUT signal at connector J1. The FREQ 8.4 TO 10.0 GHZ COARSE control mechanically couples through an 8-to-1 gear reduction and cam, positioning a tuning slug to tune the Gunn Oscillator frequency. This coarse tunes the Test Set rf frequency over the 8.35 to 10.05 GHz range. The OSC TUNING FILTERED signal provides a tuning voltage to a varactor within the Gunn Oscillator to vary the Gunn Oscillator frequency over a 100-MHz range. This signal fine tunes the Test Set rf frequency, and also sweeps the frequency to provide frequency modulation during SIG GEN FM mode operation. The FREQ 8.4 TO 10.0 GHZ FINE control provides fine tuning of Test Set rf frequency over a 10-MHz range.

(3) The FREQ 8.4 TO 10.0 GHZ FINE control rotates potentiometer 1A1R5 to provide a voltage between +15 and -15 volts as the FINE FREQ signal. This signal is applied through connector J9-4 on Front Panel Interface 1A1A1 to one input of the linearizer circuit. The other input to the linearizer is grounded when the MODE switch is in any position except SIG GEN FM or FM EXT. With this input grounded, the linearizer produces a MOD/HOLD LOW signal voltage which varies from approximately 2.5 to approximately 3.5 volts as the FINE FREQ signal voltage varies from +15 volts (minimum frequency) to -15 volts (maximum frequency). This voltage passes through the FM HOLD HIGH-MOD-HOLD LOW switch when the switch is in the MOD or HOLD LOW position, through a connection on Front Panel Interface 1A1A1, through a filter circuit on Microwave Interface 1A1A3, and through connector J2 on RF Oscillator 1A1A5 to the tune in input of Gunn Oscillator 1A1A5Y1.

(4) The filter on Microwave Interface 1A1A3 removes noise from the OSC TUNING signal by shunting ac signal components through a capacitor to ground via the low output impedance of inverter U32. This happens when the MODE switch is in any position other than SIG GEN FM or FM EXT. Then the CPU and I/O subsystem sends a data word, with bit 7 reset, to address D100. This data, stored at XCVR U1, causes a high input to inverter U32 which switches its output to the low impedance state. When the MODE switch is in the SIG GEN FM or FM EXT position, the CPU and I/O subsystem sends the data word with bit 7 set, causing a high input to inverter U32. This switches off the open collector output of U32 (high impedance state), disabling the filter during FM operation.

(5) The Test Set rf frequency signal out of the Gunn Oscillator at connector 1A1A5J1 varies in amplitude with frequency and temperature. It is in the +16 to +21 dbm range for all frequency and temperature conditions. This OSC OUTPUT signal passes through cable 1A1W2 to connector J1 on Modulator/Mixer 1A1A4A1, and couples through a 23-db directional coupler to one input of the harmonic mixer.

(6) A voltage-controlled oscillator (vco) in VCO/Prescaler 1A1A4A3 provides a harmonic rich output signal, tunable from less than 725 MHz to greater than 800 MHz. This output is applied through a low-pass harmonic filter which eliminates unwanted higher harmonics, through a 7-db attenuator, and through connector 1A1A4A3J1. This +17 db signal passes through cable 1A1A4W1 and through connector J6 on Modulator/Mixer 1A1A4A1 to the second input of the harmonic mixer. The vco output also couples through a directional coupler to the input of the prescaler which divides the vco frequency by 256 to provide the VCO PRESCALER OUT signal at connector 1A1A4A3J2. This signal is applied thorugh a connection on Microwave Interface 1A1A3 to the measurements subsystem circuits on Digital Assembly 1A1A2 as the PRESCALER OUT signal. The measurements subsystem circuits count the PRESCALER OUT signal frequency to get the number used in calculating the Test Set rf frequency.

(7) The VCO CONTROL signal is a dc voltage, between +10 and -10 volts, which is applied through connector J3 to the vco in VCO/Prescaler 1A1A4A3. This voltage tunes the vco frequency in the 725 to 800 MHz range to produce a harmonic frequency close to the Test Set rf frequency. The 11th, 12th, or 13th harmonic of the vco frequency mixes with the Test Set rf frequency in the harmonic mixer to produce a difference frequency output as the FREQ MEAS IF signal. This ac signal has a 5-millivolt peak to peak amplitude, and has a 512-kHz frequency when one of the vco harmonic frequencies is 512 kHz less than the Test Set rf frequency.

(8) The automatic frequency control (afc) circuits, shown on sheet 3, receive the FREQ MEAS IF signal and produce the VCO CONTROL signal voltage to tune the vco such that the FREQ MEAS IF frequency is held at 512 kHz. This is afc lock operation. During afc lock, integrator U18 provides a nearly constant output voltage due to the charge on capacitor C47. Summing amplifier U18 inverts, amplifies, and offsets this voltage to provide the VCO CONTROL signal. A discriminator circuit compares the FREQ MEAS IF frequency with the 512-kHz frequency of a 0.512-MHz signal to provide a control current through resistor R82 to the integrator.

(9) Amplifier U21 amplifies the 5-millivolt FREQ MEAS IF signal to provide a 0.5-volt peak to peak level at test point TP16. When the signal level at TP16 is greater than the threshold voltage provided by THRESHOLD potentiometer VR13, comparator U22 converts the signal to a logic level square wave which is inverted by inverter U17-13 to provide the difference frequency input to the discriminator circuit. Each pulse of this signal produces a charge current, through diode CR32, to slightly charge capacitor C46 in the positive direction. The 0.512-MHz signal is a 512-kHz logic level square wave which is inverted by inverter U17-10 to provide the reference frequency input to the discriminator circuit. Each pulse of this signal produces a charge current through diode CR33, to slightly charge capacitor C46 in the negative direction. When the two frequencies are equal, the two charge currents cancel each other and the voltage across capacitor C46 does not change. For this condition to be stable, the voltage across capacitor C46, measured at test point TP9, must be zero volts.

(10) When the vco is tuned such that one of its harmonic frequencies is more than 512 kHz below the Test Set rf frequency, the harmonic mixer outputs a frequency greater than 512 kHz as the FREQ MEAS IF signal. This difference frequency causes

capacitor C46 to charge in the positive direction, producing a positive voltage at test point TP9. This positive voltage causes a control current through resistor R82 to make the integrator output voltage change in the negative direction. Because the summing amplifier inverts the signal, this results in a more positive VCO CONTROL voltage, increasing the vco frequency. The increase in vco frequency reduces the difference between the vco harmonic frequency and the Test Set rf frequency, thereby reducing the difference frequency out of the harmonic mixer.

(11) As the difference frequency (FREQ MEAS IF signal) decreases to 512 kHz, the discriminator output voltage at test point TP9 decreases to zero volts. Thus, the control current through resistor R82 decreases to zero, causing the rate of change of the integrator output voltage to slow to a stop. Therefore, the VCO CONTROL voltage stabilizes at the voltage required to tune the vco such that one of its harmonic frequencies is 512 kHz less than the Test Set rf frequency.

(12) The afc lock operation, described above, occurs when a vco harmonic frequency is within 10 MHz of the Test Set rf frequency, producing a FREQ MEAS IF signal frequency less than 10 MHz. This frequency then passes through the 1 MHz filter and is detected by the detector to bias off transistor switch Q18. The AFC VALID signal then goes to +5 volts (logic 1), turning on inverted mode switch transistor Q7 and grounding the junction of resistors R84 and R85, thereby preventing sweep current from flowing from the integrator. The AFC VALID signal is also applied through connector 1A1A3J2-8 to the CPU and I/O subsystem circuits on Digital Assembly 1A1A2. The CPU and I/O subsystem tests the AFC VALID signal to check for afc lock by reading bit 6 of the data from address 8001.

(13) When the FREQ MEAS IF signal frequency is greater than 10 MHz, afc sweep operation takes place. Th signal is attenuated by the 1-MHz filter such that too little signal is detected to bias off transistor switch Q18. Therefore, transistor Q18 turns on, pulling the AFC VALID signal to the low logic level. This turns off inverted mode switch transistor Q7, allowing 35 microamperes of sweep current to flow from the integrator input through resistors R85 and R84 to the +15 volt supply. The output voltage from integrator U8 must ramp in the negative direction to maintain a 35-microampere charge current through integrator capacitor C47 to the integrator input. Therefore, the integrator output voltage, monitored at test point TP10, ramps in the negative direction, causing the VCO CONTROL voltage to ramp in the positive direction, increasing vco frequency. If the increasing vco frequency brings a harmonic within 10 MHz of the Test Set rf frequency, the afc lock occurs. If no afc lock occurs, the voltage at test point TP10 ramps down to a low limit value.

(14) When the voltage at test point TP10 ramps down to equal the lower limit voltage at test point TP13, low limit comparator U19-9 outputs a high to set the latch circuit of gates U17. This causes a low from gate U17-4, turning on the sweep reset circuit to provide a reset current of 350 microamperes from the -15 volt supply to the integrator input. The reset current causes the integrator output voltage at test point TP10 to ramp rapidly in the positive direction. When this voltage ramps up to equal the high limit voltage at test point TP12, high limit comparator U19-1 outputs a high to reset the latch circuit. Then a high

from gate U17-4 turns off the sweep reset circuit, allowing the sweep reset cycle to begin again.

(15) The voltage at test point TP11 is high during the 0.1-second sweep, and low during the 0.01-second reset. The latch and comparators serve to control the integrator such that the voltage at test point TP10 sweeps between the limit voltages provided by the high limit reference circuit (test point TP12) and the low limit reference circuit (test point TP13). This limits the sweep of the VCO CONTROL signal voltage and therefore limits the vco frequency sweep.

(16) The AFC BIT 5 and AFC BIT 6 signals control the high limit reference and low limit reference circuit output voltages to sweep the vco frequency over a high band, mid band, and low band as shown in table 4-2. These signals are controlled by bits 5 and 6 of the data that the CPU and I/O subsystem sends to address D100. The data is stored in XCVR U1 on Microwave Interface 1A1A3. Bit 7 of the data stored in XCVR U1 provides the FM/FREQ CAL signal which controls the calibrate high and calibrate low operations.

(17) When both the AFC BIT 5 and AFC BIT 6 signals are high, gate U20-3 goes low, causing a high out of inverter U16-10. This high enables calibrate high or calibrate low operation by turning on inverted mode transistor switch Q14 which grounds the integrator output at the junction of resistors R107 and R108. This high also enables gate U20-8. The FM/FREQ CAL signal now selects between calibrate high and calibrate low operation as shown in table 4-2. When bit 7 of the data at address D100 is zero, the FM/FREQ CAL signal is low, selecting calibrate high operation. The low causes a high out of enabled gate U20-8, turning on inverted mode transistor switch Q15 to ground the junction of resistors R118 and R117. The summing amplifier output voltage at test point TP18 is +9.74 volts, determined by 15 volts across resistor R213. When bit 7 is one, the FM/FREQ signal is high, selecting calibrate low operation. The high causes a low out of enabled gate U20-8, turning off inverted mode transistor switch Q15. This allows +15 volts across resistors R118 and R117 to change the summing amplifier output to -10.00 volts at test point TP18.

(18) The calibrate high and calibrate low operations are used to break an undesired afc lock and to adjust AFC potentiometer VR12. A calibration procedure adjusts AFC potentiometer VR12 to calibrate the VCO CONTROL signal voltage such that the vco frequency changes 75 MHz from calibrate high to calibrate low. This adjusts the afc circuits to sweep the vco frequency in the ranges shown in table 4-2 during low band, mid band, and high band operation.

d. Self-Test of AFC Circuits

(1) Self-test checks the afc circuits on Microwave Interface 1A1A3 by applying a 64-kHz square wave to simulate the FREQ MEAS IF signal and by testing the AFC VALID signal for a high logic level. Self-test also measures the vco frequency for calibrate high and calibrate low operation to check the vco frequency range.

Table 4-2. AFC Control

AFC control data at address D100			High limit voltage at TP12	Low limit voltage at TP13	Integrator output voltage at TP10	Summing amplifier output voltage at TP18	VCO frequency	AFC operation
Bit 7	Bit 6	Bit 5						
X	0	0	5.07V	3.74V	5.07 to 3.74V	-9.5 to -4.4V	725 to 752 MHz	Low band
X	0	1	3.84V	1.91V	3.84 to 1.91V	-4.8 to +2.5V	750 to 777 MHz	Mid band
X	1	0	2.03V	0.00V	2.03 to 0.00V	+2.1 to +9.7V	775 to 800 MHz	High band
0	1	1	X	X	X	+9.74V	795.5 ±20.1 MHz	Cal high
1	1	1	X	X	X	-10.00V	727.1 ±20.1 MHz	Cal low

X = don't care condition

(2) Self-test checks the circuits which produce the AFC VALID signal, checks the summing amplifier, and checks the adjustment of AFC potentiometer VR12. Self-test does not check the discriminator or the ability of the integrator and its associated circuits to sweep over the high band, mid band, or low band voltage ranges. Self-test counts the PRESCALER OUT signal, checking the prescaler and verifying the vco frequency within VCO/Prescaler 1A1A4A3. Self-test does not check the vco output at connector 1A1A4A3J1, or the harmonic mixer in Modulator/Mixer 1A1A4A1.

(3) At the start of test number 160 of the afc self-test, the CPU and I/O subsystem sends data, with bit 7 set, to address D200. This data, stored in XCVR U1 on Microwave Interface 1A1A3, produces the high RF SELF TEST signal which enables gate U15-8 (sheet 3 of figure 6-4) to pass the 64-kHz square wave from the 0.064 MHz signal. This square wave, reduced to about 8 millivolts peak to peak by the voltage divider comprising resistors R123 and R124, is applied to amplifier U21 to simulate the FREQ MEAS IF signal. After a 10-millisecond wait, the CPU and I/O subsystem reads bit 6 of the data from address 8001 to test the AFC VALID signal. If the AFC VALID signal is high, bit 6 is set and self-test continues to test number 161. If bit 6 is reset, self-test stops and ⌊160 is displayed on the digital display.

(4) For test number 161, the CPU and I/O subsystem sends data to address D100 to cause calibrate low operation. Then the CPU and I/O subsystem causes a frequency measurement of the PRESCALER OUT signal to determine the vco frequency. If the vco frequency is between 707 and 747 MHz, self-test continues to test number 162. If not, self-test stops and ⌊161 is displayed on the digital display.

(5) In a manner similar to that of test number 161, test number 162 is a test for the calibrate high operation. If the vco frequency is between 775.5 and 815.5 MHz, self-test goes on to test number 163. If not, self-test stops and ⌊162 is displayed on the digital display.

(6) Test number 163 checks that the vco frequency range is great enough to sweep the entire X-band with the 11th, 12th, and 13th harmonics. This test uses the calibrate low frequency and calibrate high frequency measured in tests 161 and 162. If 12 times the calibrate low frequency is 25 to 75 MHz greater than 11 times the calibrate high frequency, the test passes and self-test continues. If not, self-test stops and ⌊163 is displayed on the digital display.

4-9. FREQUENCY MODULATION SUBSYSTEM BLOCK DIAGRAM DESCRIPTION (Figure 4-5). The function of the frequency modulation subsystem is to linearly sweep the Test Set rf frequency over a known range at a desired rate and desired repetition frequency. When the MODE switch is in the SIG GEN FM position, the Test Set rf output sweeps from a set low frequency to a set high frequency at a rate determined by the FM RATE potentiometer. The sweep repeats at an interval determined by the PRF potentiometer. When the PRF potentiometer is set such that the sweep cannot be completed at the rate selected by FM RATE potentiometer, before the time of the next sweep repetition, the Test Set displays ⌊103 on the digital display. When the FM invalid indication (⌊103) is displayed, the PRF or FM RATE potentiometer

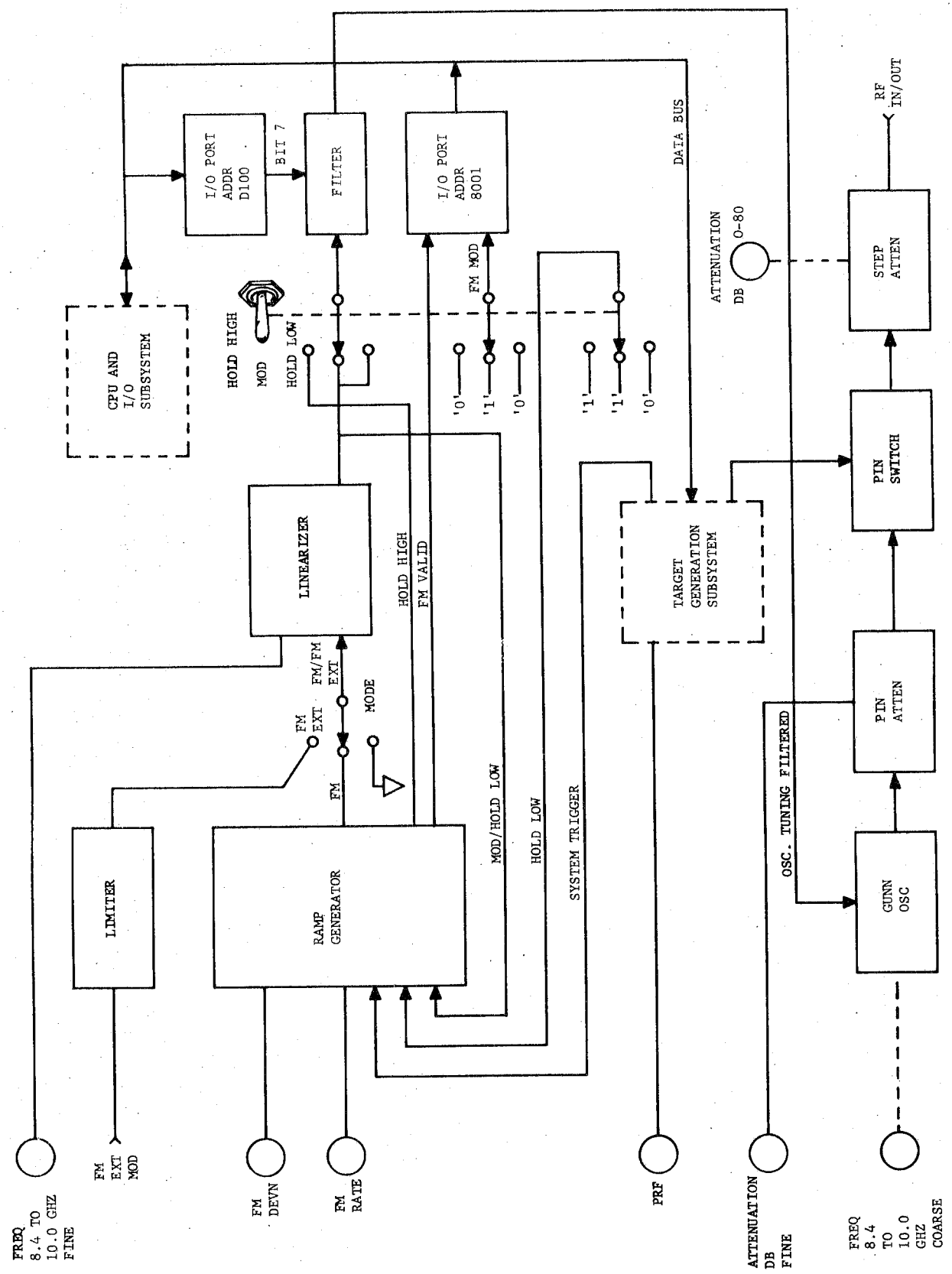


Figure 4-5. Frequency Modulation Subsystem Block Diagram

must be adjusted until the digital display goes blank. When the MODE switch is in the SIG GEN EXT position, the Test Set rf output frequency is modulated by an external signal applied at the FM EXT MOD connector. The external signal must be positive and between 0 and 10 volts. The Test Set rf frequency deviates upward approximately 10 MHz per volt of the external signal. Figure 4-5 depicts how the frequency modulation subsystem circuits work with the other Test Set subsystems to frequency modulate the Test Set rf output.

a. SIG GEN FM Operation

(1) The ramp generator provides a ramping sweep signal. The rate at which this signal sweeps is controlled by the FM RATE potentiometer, and the maximum voltage of this signal is controlled by the FM DEVN potentiometer. When the MODE switch is in the SIG GEN FM position, the sweep signal from the ramp generator combines, in the linearizer, with a dc voltage from the FREQ 8.4 TO 10.0 GHZ FINE potentiometer to produce a modulating voltage. When the HOLD HIGH-MOD-HOLD LOW switch is in the MOD position, this modulating voltage is applied through a disabled filter to provide the OSC TUNING FILTERED signal which frequency modulates the rf output of the Gunn Oscillator.

(2) When the MODE switch is in the SIG GEN FM position, the CPU and I/O subsystem sends data to address D100 and reads data from address 8001. Bit 7 of the address D100 data controls the filter. When the MODE switch is in SIG GEN FM or SIG GEN FM EXT position, bit 7 is 0, disabling the filter to prevent distortion of the OSC TUNING FILTERED signal waveform. With the MODE switch in any other position, bit 7 is 1 to enable the filter, thereby reducing any noise on the OSC TUNING FILTERED signal dc voltage. Bit 4 of the data from address 8001 indicates whether the HOLD HIGH-MOD-HOLD LOW switch is in the MOD position. Bit 5 of address 8001 data indicates whether the frequency modulation operation is valid or invalid. The CPU and I/O subsystem also sends data to the target generation subsystem to cause CW operation. This turns on the pin switch, allowing the frequency modulated rf to pass through the step attenuator to the RF IN-OUT connector.

(3) When the HOLD HIGH-MOD-HOLD LOW switch is in the HOLD LOW position, the HOLD LOW signal disables the ramp generator. At this time, the FREQ 8.4 TO 10.0 GHZ FINE potentiometer is used to set the undeviated rf frequency. When the switch is in the HOLD HIGH position, the HOLD HIGH signal voltage replaces the ramp generator output to tune the Gunn Oscillator. This voltage is equal to the maximum voltage of the sweep signal from the ramp generator. The FM DEVN potentiometer is used to adjust this voltage, thereby setting the maximum deviation of the rf frequency.

b. SIG GEN FM EXT Operation. When the MODE switch is in the SIG GEN FM EXT position, the linearizer is disconnected from the ramp generator sweep signal and is connected to the limited external modulation signal. This signal is applied at the FM EXT MOD connector and is clamped to 0 volt dc by the limiter to prevent negative voltage inputs to the linearizer.

4-10. FREQUENCY MODULATION SUBSYSTEM FUNCTIONAL DIAGRAM DESCRIPTION (Figure 6-5). Figure 6-5 shows the physical location of the circuits and signals in the frequency modulation subsystem. The following paragraphs describe, in detail, the purpose and characteristics of these circuits.

a. Ramp Generator. The ramp generator on Front Panel Interface 1A1A1 provides a sweep signal to frequency modulate the Gunn Oscillator output during SIG GEN FM operation. The sweep voltage is generated by charging capacitor C22 with a current from +15 volts, through FM RATE potentiometer 1A1R3 and resistor 1A1A1R58 (sheet 1 of figure 6-5). The voltage across capacitor C22 is applied through the MODE switch to the linearizer where it combines with a dc voltage provided by FREQ 8.4 TO 10.0 GHZ FINE potentiometer 1A1R1 (sheet 2). The linearizer output is applied to the + input of comparator U10. As capacitor C22 charges, the linearizer output voltage becomes more positive. When this voltage becomes equal to the voltage provided by FM DEVN potentiometer 1A1R4, comparator U10 outputs a high logic level as the SWEEP COMPLETE signal. This high logic level resets the latch comprising cross-coupled gates U16-1 and U16-7, turning on switch transistor Q1 (sheet 1). Switch transistor Q1 rapidly discharges capacitor C22, resetting the sweep voltage. Each negative going SYSTEM TRIGGER L signal pulse sets the latch (U16-1, U16-7), turning off switch transistor Q1 and allowing another sweep of the voltage across capacitor C22.

b. Invalid FM Operation. When the selected prf rate is too fast to allow each sweep to reach its maximum voltage at the selected rate, two or more consecutive SYSTEM TRIGGER L signal pulses occur without a high logic level SWEEP COMPLETE signal. When this happens, the latch comprising gates U16-1 and U16-7 is set when a SYSTEM TRIGGER L pulse arrives. The resulting positive going transition output from gate U16-13 clocks a high logic level output from gate U16-7 into flip-flop U17. This causes the low FM VALID signal to ROM/XCVR U2 on Digital Assembly 1A1A2. This causes a zero as bit 5 of the data for address 8001. When the CPU and I/O subsystem reads this data, invalid FM operation is determined and the FM invalid message (⊔103) is displayed on the digital display.

4-11. TARGET GENERATION SUBSYSTEM BLOCK DIAGRAM DESCRIPTION (Figure 4-6). The function of the target generation subsystem circuits is to provide an rf return target of selected range, pulse width, and range rate from a selected rf, internal, or external video trigger source. The target generation subsystem also must provide for the display of the selected target parameters, trigger output, and rf envelope output.

a. Trigger Selection. The SYSTEM TRIGGER used to initialize the target generation subsystem is provided by one of three sources selected by the TRIGGER switch. With the TRIGGER switch in the RF position, the trigger is supplied by the directional detector with a pulsed rf source connected to the RF IN/OUT connector on the front panel. The detected pulse or rf envelope is shaped and converted to a logic level pulse, then supplied to the trigger select circuits. The conditioned pulse is also output to the RF ENV/PULSE MON connector on the front panel. With the TRIGGER switch in the INT position, the output of the internal prf generator is selected as system trigger. The prf generator is controlled by the PRF

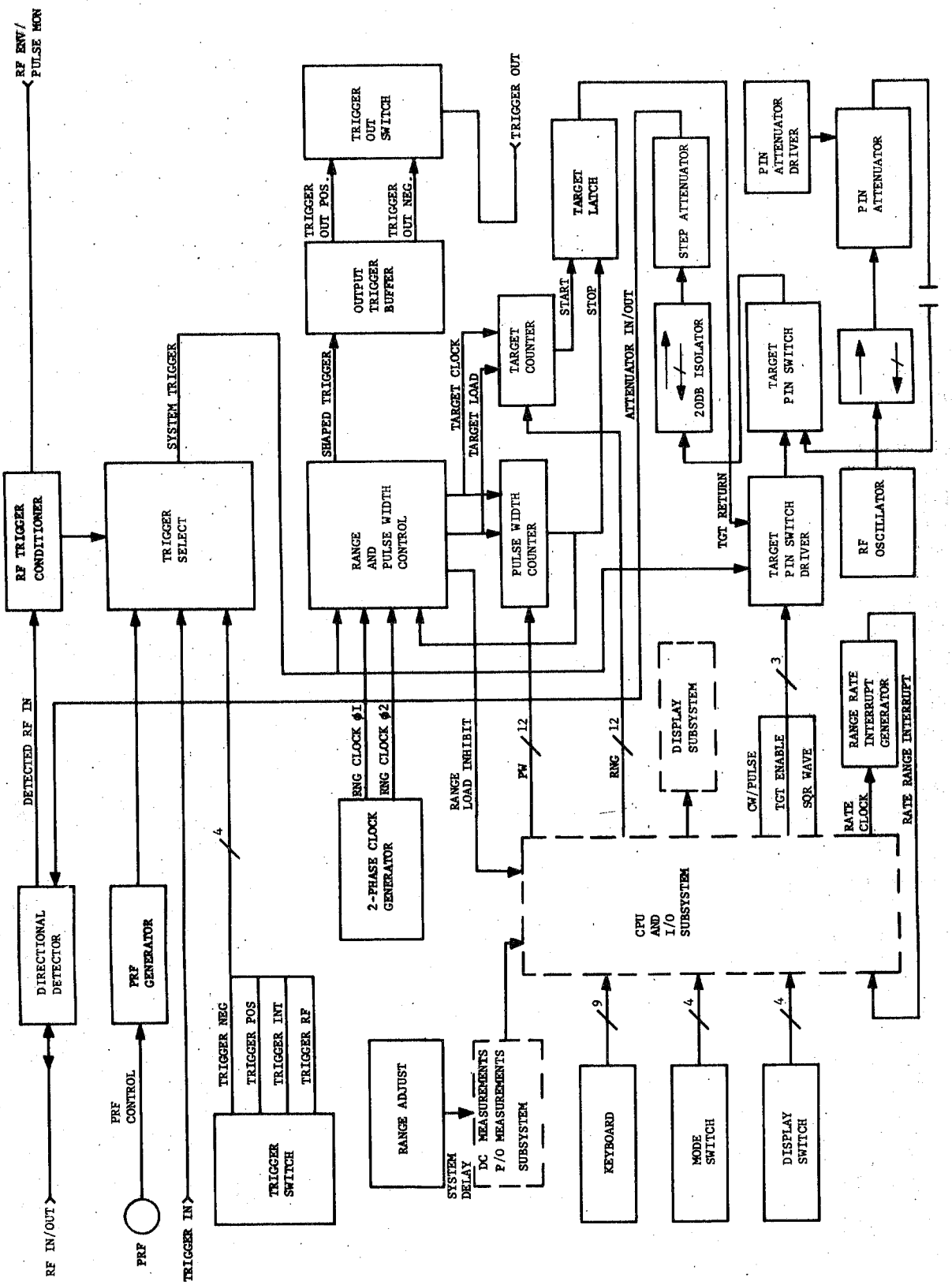


Figure 4-6. Target Generation Subsystem Block Diagram

potentiometer on the front panel. When the TRIGGER switch is in the POS or NEG position, the occurrence of a positive or negative level input at the TRIGGER IN connector is selected as system trigger.

b. Trigger Output. The selected SYSTEM TRIGGER is supplied to the range and pulse width control logic where it is shaped to a 0.5-microsecond pulse which is nonretriggerable for 10 microseconds. This shaped trigger pulse is then applied to a buffer to boost the signal level as well as to provide both positive and negative level pulses. The positive or negative level buffered trigger pulse is selected by the TRIG OUT switch for output at the TRIG OUT connector.

c. Target Return Video. The leading edge of SYSTEM TRIGGER gates the range clock phase 1 or phase 2 (whichever phase is most nearly in phase with the SYSTEM TRIGGER) through the range and pulse width control logic to start the target clock. This decreases startup error to one-half count rather than one full count. The target and pulse width counters start counting down from preset values present at the RNG and PW data inputs. The range clock is 16.392 MHz which gives a clock rate of 61 nanoseconds, or least significant bit value of 10 radar yards. When the target counter counts down to zero, it outputs a start pulse which sets the target latch. When the pulse width counter counts down to zero, it outputs a stop pulse which resets the target latch. The output of the target latch is the target video. When the target latch resets (end of target), the preset values of RNG and PW are loaded into the counters again in preparation for the next SYSTEM TRIGGER pulse, provided the end of target was at least 95 microseconds after SYSTEM TRIGGER. If it is not, the RNG and PW inputs will not be loaded until the 95-microsecond period has elapsed. This is also the case with short range targets. With the MODE switch in SIG GEN PULSE or RADAR PULSE and the DISPLAY SELECT switch in RANGE (YDS) or PW (MICROSEC), the values of RNG and PW data loaded into the counters will be changed by the CPU and I/O subsystem whenever these parameters are changed via the keyboard.

d. Range Rate. Range rate is entered via the keyboard when the MODE switch is set to SIG GEN PULSE or RADAR PULSE and the DISPLAY switch is in the RANGE RATE (KNS) position. The CPU and I/O subsystem programs the rate clock and range rate interrupt generator according to the value of range rate entered. The rate clock is a free running clock with one value for range rates under 50 knots and another for range rates from 50 to 2,000 knots. The range rate interrupt generator is initially set to its maximum count. It counts down as it is clocked from the rate clock until it reaches the terminal count preset by the CPU and I/O subsystem for the particular range rate. When the terminal count is reached, the range rate interrupt generator outputs an interrupt to the CPU and I/O subsystem. The CPU and I/O subsystem services the interrupt by incrementing (for positive or opening rates) or decrementing (for negative or closing rates) the count loaded into the range and pulse width counters by one count. Before changing the values, the CPU and I/O subsystem must sample the range load inhibit signal from the range and pulse width control logic. The inhibit signal allows the RNG and PW inputs to be changed only during a period of 65 microseconds immediately following SYSTEM TRIGGER for low prf. This insures that these values are not being changed at the time they are loaded into the counters.

e. RF Target Return. The video target return is applied to the target pin switch driver which also receives three control bits from the CPU and I/O subsystem. When the MODE switch is positioned to a PULSE mode, the target return video pulse controls the target pin switch driver provided a power measurement or an rf tune function is not being performed (indicated by the target enable control bit). The rf oscillator X-band output (OSC OUTPUT) is supplied through the pin attenuator to the target pin switch. The pin switch is driven by the pin switch driver which is gated on and off by the target video, thereby pulse modulating the rf and supplying an rf target return pulse. The rf return pulse then passes through a 20-db isolator, the step attenuator, and the directional coupler to the RF IN/OUT connector.

4-12. TARGET GENERATION SUBSYSTEM FUNCTIONAL DIAGRAM DESCRIPTION (Figure 6-6)

a. General. The operation of the target generation subsystem can be subdivided as follows:

(1) Selection of the SYSTEM TRIGGER. The SYSTEM TRIGGER initializes target generation.

(2) Generation of TRIGGER OUT output and RF ENVELOPE/PULSE MONITOR output. These signals are supplied to the front panel for observation purposes.

(3) Generation of the TARGET VIDEO pulse. The range, range rate, and pulse width parameters control the delay and width of the video pulse.

(4) Generation of the RF TARGET RETURN pulse. The target video pulse modulates the rf oscillator output to yield an RF target pulse.

b. Trigger Selection. The SYSTEM TRIGGER is selected from one of three sources by TRIGGER switch 1A1S3. The switch provides +5 volts on one of four output lines to the trigger select logic (1A1A1U18). With the TRIGGER switch in the IN NEG position, the negative level of an external trigger supplied at TRIGGER IN connector 1A1J3 is selected through the limiter (1A1A1D7, D8, and R73). The signal is then inverted by inverter U19-3, gated to gate U18-11, and inverted again by inverter U19-11 to become the SYSTEM TRIGGER. When the TRIGGER switch is in the IN POS position, the positive level of an external trigger supplied at the TRIGGER IN connector is selected through the limiter to gate 1A1A1U18-8 and inverted by inverter U19-11 to become the SYSTEM TRIGGER. Thus, the external trigger is one source for SYSTEM TRIGGER with two options dependent on the type of external signal supplied: negative level pulse or positive level pulse. With the TRIGGER switch in the INT position, the output of prf generator 1A1A1U15 is gated through gate U18-6 and inverted by inverter U19-11 to become SYSTEM TRIGGER. The PRF control (1A1R2) supplies the control voltage to the prf generator to vary the prf output. The internal prf generator is the second source for SYSTEM TRIGGER. When the TRIGGER switch is in the RF position, the output of directional detector 1A1A6 is selected through the rf trigger conditioner (formed by amplifiers 1A1A1U12 and U13). The signal is then gated through gate U18-3 and inverted by inverter U19-11 to become SYSTEM TRIGGER. The directional detector couples the RF IN/OUT signal

in the input direction from RF IN/OUT connector 1A1J2 and detects the modulating pulse. The rf trigger conditioner shapes the pulse and converts it to a logic level pulse. The RF IN/OUT input then is the third source for SYSTEM TRIGGER. The SYSTEM TRIGGER pulse will be a positive going logic level pulse with the duration of the trigger source pulse independent of which source is selected.

c. RF Envelope/Pulse and Trigger Out

(1) The RF ENV/PULSE MON output at RF ENV/PULSE MON connector 1A1J5 is present when an rf source is present at RF IN/OUT connector 1A1J2. The RF IN/OUT signal in the input direction is coupled and the rf envelope is detected and supplied via Cable 1A1W4 to the rf trigger conditioner circuits on Front Panel Interface 1A1A1. The detected rf envelope is inverted and scaled by amplifier 1A1A1U12 and buffered by buffer Q2, then supplied as an output at connector 1A1J5.

(2) The SYSTEM TRIGGER is output from Front Panel Interface connector 1A1A1J1-43 to Digital Assembly 1A1A2 at connector 1A1A2J3-43 and applied to the range and pulse width control circuits at one-shot 1A1A2U21-13. The output of one-shot U21-13 is a 10-microsecond positive going pulse which is supplied to one-shots U21-12, U20-12, and U20-4. The output at one-shot U21-12 is an inverted 0.5 microsecond pulse. Both pulse outputs from one-shot U21-13 and U21-12 have the leading edge coincident with the system trigger. The purpose of the transition through single-shots U21-13 and U21-12 is two-fold. The first 10-microsecond output insures that retriggering will not occur on any noise that may follow the system trigger pulse for up to 10 microseconds. The second 0.5 microsecond pulse is to return the trigger pulse width to a suitable width for an output trigger. The output of one-shot U21-12 is supplied as SHAPED TRIG L through connector 1A1A2P2-41 to Front Panel Interface 1A1A1 and applied to the output trigger buffer (1A1A1U19 and Q3 through Q6). The trigger buffer converts the SHAPED TRIG L signal to positive and negative level trigger outputs which are supplied to TRIG OUT switch 1A1S4. In the POS position of the TRIG OUT switch, the positive level trigger from the trigger buffer is output to TRIG OUT connector 1A1J4. In the NEG position of the TRIG OUT switch, the negative level trigger from the trigger buffer is output to the TRIG OUT connector.

d. Target Video Pulse

(1) The SHAPED TRIG L derivative of the SYSTEM TRIGGER signal from one-shot 1A1A2U21-12 is used to initialize the range delay for the target video pulse. The leading edge of the SHAPED TRIG L signal (coincident with SYSTEM TRIGGER) sets the output of gate U17-8 high. The resultant outputs of the latch comprising gates U17-8 and U17-11 are applied through J-K flip-flops U19 as enables to gates U18-8 and U18-3. This results in the output at gate U18-6 through U31-11 of phase 1 or 2 of 16.392 MHz range clock generator U30. Inverter U23-6 forms phase 2 of the range clock. Each phase is applied as a clock to the separate J-K flip-flops (U19). The J-K inputs to these flip-flops are the outputs of the latch formed by gates U17-8 and U17-11 which are set by the SHAPED TRIG L input. The clock phase having the first negative going edge after the SHAPED TRIG L occurs is selected by one of flip-flops U19 and the other phase is inhibited. Gates U18-3, -6, and -8 form a

multiplexer to gate the selected clock phase through to the range and pulse width counters (U11 through U16). The purpose of selecting between two clock phases is to decrease the error between the time when trigger occurs and the counters start counting. Since the counters are edge triggered, as much as one clock cycle error could be introduced by gating the clock with a spontaneous nonsynchronized trigger. Selecting between two clock phases cuts this error in half. The clock frequency is 16.392 MHz. Thus, each count or bit of the counter is 1 divided by 16.392 X 10^6 or nearly 61 nanoseconds, or roughly 10 radar yards in range (12.2 microseconds is nearly equal to 1 radar mile or 2,000 yards). The range error introduced to the counters at start is then about 5 yards.

(2) The CPU and I/O subsystem supplies the selected range and pulse width to the range and pulse width counters as the RNG0-11 and PW0-11 inputs. The RNG0-11 input is a 12-bit binary number equivalent to the selected target range minus the system delay. The system delay is calibrated by the range adjust and measured by the CPU and I/O subsystem through the measurements subsystem. The PW0-11 input is a 12-bit binary number equivalent to RNG0-11 plus the desired pulse width.

(3) The range and pulse width counters start counting when they receive the range clock output from gate 1A1A2U18-6. The counting is from their preset values of range and pulse width from the CPU and I/O subsystem. When the range counter counts down to zero, it outputs a low going pulse at the M-output coincident with the next rising edge of the clock. This output sets the latch formed by gate U17-3 and U17-6. The TARGET RETURN output at gate U17-3 is set high. When the pulse width counter counts down to zero, it outputs a low going pulse at the M-output coincident with the next rising edge of the clock. This output resets the latch formed by gates U17-3 and U17-6. The target return output at gate U17-3 returns to a low which completes video target pulse. The pulse from the M-output of the pulse width counter signals the end of the target pulse and is also supplied to gate U17-11, resetting the latch output at gate U17-11 which disables the range clock to the counters. This output is also applied to gate U18-11. A 95-microsecond low going pulse from one-shot U20-12, with a leading edge coincident with the SYSTEM TRIGGER, is also input to gate U18-11. The resulting output at gate U18-11 is dependent on how far the target range is. For targets ending less than 95 microseconds after SYSTEM TRIGGER, the output at gate U18-11 does not go low until the occurrence of the 95 microsecond pulse. For targets at ranges greater than 95 microseconds, the output at gate U18-11 goes low at the end of the target pulse. The output at gate U18-11 is supplied to the data load inputs of the range and pulse width counters to reset the counters to the values present on the RNG0-11 and PW0-11 inputs before the occurrence of the next SYSTEM TRIGGER pulse, which will repeat the whole cycle described thus far. The output at gate U18-11 will be reset high when next SYSTEM TRIGGER pulse sets the latch comprising gates U17-8 and U17-11.

(4) When a range rate is entered, the CPU and I/O subsystem programs counter 0 1A1A2U22 of the range rate interrupt generator as well as the rate clock output. The rate clock output is free running and is programmed for one speed for range rate values under 50 knots and at a faster speed for range rates from 50 to 2,000 knots. Counter 0 U22 starts counting from its maximum programmable count and

counts down as it is clocked by the RATE CLOCK until it reaches a terminal count programmed by the CPU and I/O subsystem for the specific range rate selected. When the terminal count is reached, a negative going pulse from the Y output of counter 0 U22 is inverted by inverter U23-4 and sent to the CPU and I/O subsystem as the RANGE RATE INTERRUPT signal. Upon receiving the RANGE RATE INTERRUPT, the CPU and I/O subsystem must increment or decrement the RNG0-11 and PW0-11 inputs to the range and pulse width counters by one count. For positive or opening range rates the count is incremented. For negative or closing range rates the count is decremented. Before changing the counter inputs, the CPU and I/O subsystem must monitor the RANGE LOAD INHIBIT input from one-shot U20-4. This is a low going 65-microsecond pulse with the leading edge coincident to the SYSTEM TRIGGER. When this signal is low, it is safe for the CPU and I/O subsystem to change the counter inputs since the counters cannot be loaded until at least 95 microseconds after SYSTEM TRIGGER as previously described. Thirty microseconds is allowed between the latest time the counter inputs can be changed and the earliest time they can be loaded into the counter to give the CPU and I/O subsystem enough time to complete updating the inputs if updating started right at 65 microseconds. The CPU and I/O subsystem is also free to change the counter inputs 249 microseconds after SYSTEM TRIGGER for a low prf that does not repeat before this time since this is the latest that the end of target can occur even though the RANGE LOAD INHIBIT signal will not go low again at this time.

e. RF Target Return Pulse. The video target pulse (TGT RETURN signal) is supplied to target pin switch driver logic 1A1A3U15 of Microwave Interface 1A1A3. When the Test Set is operating in a PULSE mode, and not making a power measurement or performing an rf tune function, the TGT ENABLE output from the CPU and I/O subsystem is high while the CW mode and SQR wave mode outputs are low. This allows the inverse TGT RETURN pulse to be gated through gate U15-3 to the driver circuit (Q1 and Q2) to produce the pin switch drive signal supplied to the target pin switch. This drive signal is of the same duration as the TGT RETURN pulse. The OSC OUTPUT signal from RF Oscillator 1A1A5 is applied to Modulator/Mixer 1A1A4A1 where it is attenuated to the desired output signal level by the pin attenuator and then applied to the target pin switch. The target pin switch gates or modulates the rf input with the pin switch drive pulse to produce the rf target return pulse. The rf target pulse then follows the normal rf output path through Coupler Module 1A1A4A2, Step Attenuator 1A1A8AT1, and Detector 1A1A6, to RF IN/OUT connector 1A1J2.

4-13. POWER MEASUREMENTS SUBSYSTEM BLOCK DIAGRAM DESCRIPTION (Figure 4-7). The function of the power measurements subsystem is to measure peak rf power of continuous wave or pulsed signals and to display the power level in dbm on the digital display. There are two power measurement operations, one to measure the power from a radar, the other to measure Test Set output power. Figure 4-7 shows the power measurements subsystem circuits and their relationship to the other Test Set subsystems in performing the radar power measurement and the Test Set power measurement operations. The CPU and I/O subsystem provides control data to all subsystems; however, figure 4-7 shows only the control data directly used in radar and Test Set power measurements.

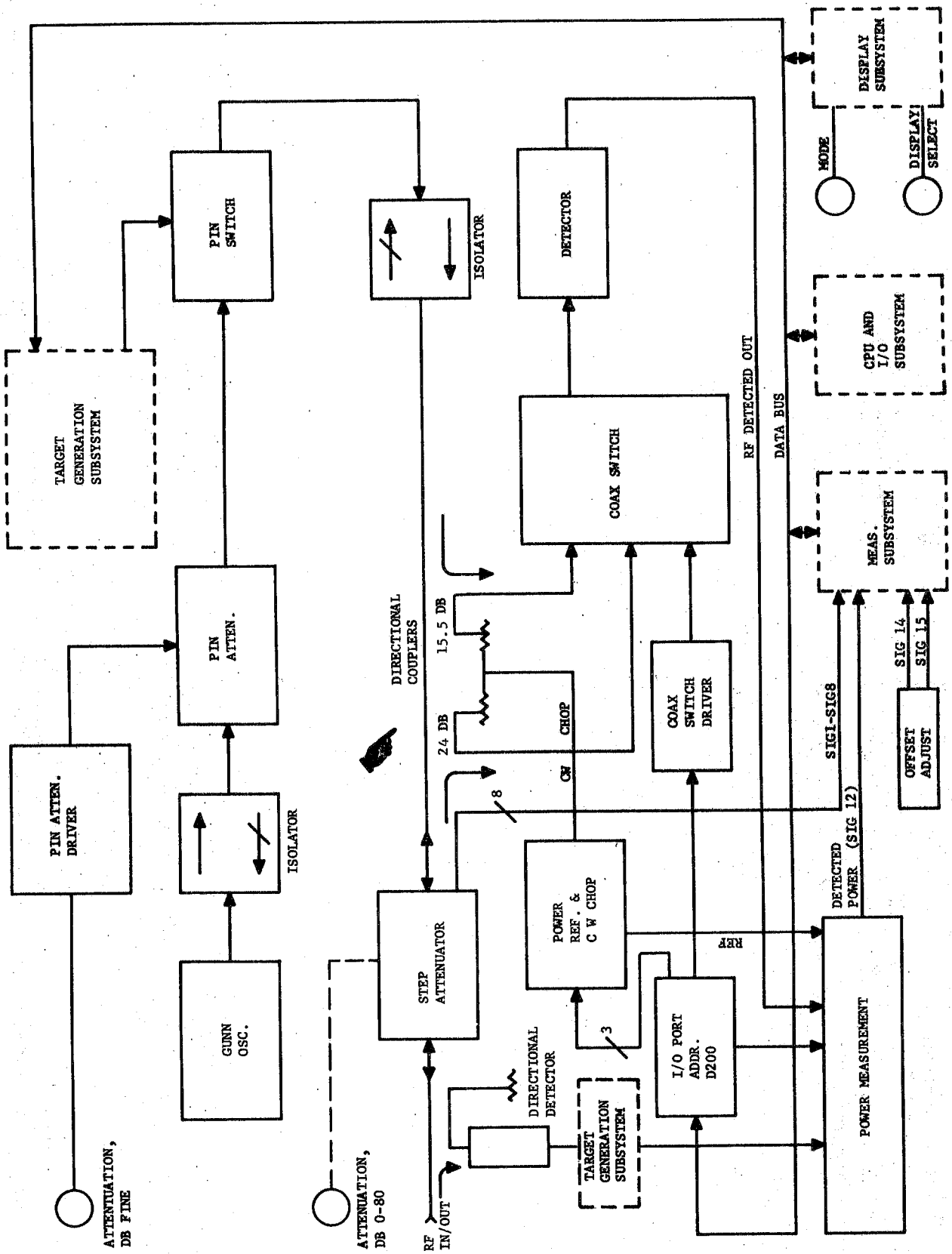


Figure 4-7. Power Measurements Subsystem Block Diagram

a. Power Measurement, Power Calibration, and Step Attenuator Attenuation

(1) The Test Set uses a crystal detector to envelope detect the rf signal to be measured. When CW power is to be measured, the power reference and CW chop circuits provide a 4-kHz signal to square wave modulate the rf signal. The detector output (RF DETECTED OUT signal) is a pulse signal for pulsed rf, and a 4-kHz square wave for CW rf. In either case, the peak to peak amplitude of the RF DETECTED OUT signal is proportional to the power of the rf signal to be measured. The power measurement circuits peak detect and amplify the RF DETECTED OUT signal to produce the DETECTED POWER signal (SIG 12) which is a dc voltage proportional to the rf power being measured. The measurements subsystem measures the DETECTED POWER signal voltage, providing the CPU and I/O subsystem with a binary number that represents the rf power level at the detector. The CPU and I/O subsystem converts this number to a number indicating power level in dbm, and adjusts the dbm number to account for the attenuation in the rf path between the detector and the RF IN/OUT connector. Then the CPU and I/O subsystem converts the adjusted dbm number to BCD format and sends it to the display subsystem for display as -85.0 to +50.0 dbm on the digital display.

(2) The Test Set calibrates the power measurements subsystem prior to a radar power measurement or a Test Set power measurement. Within the CPU and I/O subsystem, data in a memory location, called the power calibration flag, indicates whether the power measurements subsystem is calibrated. When a power measurement is to be made, the CPU and I/O subsystem checks the power calibration flag. If the flag is set, the power measurements subsystem is already calibrated and the CPU and I/O subsystem causes the measurement to be made. If the flag is not set, the CPU and I/O subsystem sets the power calibration flag, causes the calibration operation, and then causes the measurement to be made.

(3) Data stored at the address D200 I/O port controls the power reference and CW chop circuits during power calibration. Bit 0, when set, selects calibration operation and is reset for all other operations. When bit 0 is set, bit 1 selects between low calibration power reference (bit 1 reset) and high calibration power reference (bit 1 set). Bit 6, when set, turns on a 4-kHz chopping signal during RADAR, CW, SIG GEN CW, SIG GEN FM, and SIG GEN FM EXT operating modes. Bit 6 is reset, to inhibit chopping, during RADAR PULSE, SIG GEN PULSE, and SIG GEN SQW (square wave) operating modes. Bit 6 is set to provide chopping during power calibration operations.

(4) During power calibration, the power reference and CW chop circuits provide a calibrated signal which is applied to the power measurement circuits. This signal is a calibrated power level, chopped by a 4-kHz square wave. For the low calibration power reference, the 4-kHz square wave has a -27 dbm peak power level. For the high calibration power reference, the signal peak power is -13 dbm.

(5) The CPU and I/O subsystem starts the power calibration by sending data, with bits 0 and 6 set, to address D200. This causes the low calibration power reference (-27 dbm signal). Then the CPU and I/O subsystem causes the measurements subsystem to measure the resulting DETECTED POWER signal voltage. This measurement

produces a number that indicates the response of the power measurements subsystem to a -27 dbm power level at the detector. The CPU and I/O subsystem stores this number in RAM memory. Next, the CPU and I/O subsystem sends data, with bits 0, 1, and 6 set, to address D200. This causes the high calibration power reference (-13 dbm signal). The CPU and I/O subsystem causes the measurements subsystem to measure the DETECTED POWER signal voltage again. The number resulting from this measurement indicates the response of the power measurements subsystem to a -13 dbm power level at the detector. This number is also stored in RAM memory.

(6) To complete the power calibration, the CPU and I/O subsystem uses the -27 dbm voltage number and the -13 dbm voltage number to calculate a voltage number for each 1-db step between -27 dbm and -13 dbm. The resulting numbers are stored as a table in RAM memory. The CPU and I/O subsystem uses this table, during a radar or Test Set power measurement to convert DETECTED POWER signal voltages to dbm values that indicate the power level at the detector. By interpolating between the numbers in the table, the CPU and I/O subsystem calculates the power level to the nearest 0.1 db.

(7) Since the Step Attenuator is in the rf path between the RF IN/OUT connector and the detector, the CPU and I/O subsystem must use the Step Attenuator attenuation in calculating radar or Test Set power levels present at the RF IN/OUT connector. To find the Step Attenuator attenuation, the CPU and I/O subsystem causes the measurements subsystem to measure the voltages of SIG 1 through SIG 8 signals. These signals indicate the position of the ATTENUATION DB 0-80 control and a calibration value which indicates the attenuation, within 0.1 db, of the Step Attenuator.

(8) The SIG 1 through SIG 8 signals correspond to the 10 through 80 positions of the ATTENUATION DB 0-80 control. A voltage present on one of these signals indicates that the ATTENUATION DB 0-80 control is in the corresponding position. The value of the voltage indicates the calibration of the Step Attenuator. For example, if the ATTENUATION DB 0-80 control is in the 20 position and the Step Attenuator attenuation is 20.8 db, then the CPU and I/O subsystem finds a voltage on the SIG 2 signal. The presence of this voltage indicates 20-db attenuation. The value of this voltage indicates that 0.8 db must be added to 20 db to find the Step Attenuator attenuation.

(9) The SIG 1 through SIG 8 signals come from eight calibration potentiometers. A switch, connected to the Step Attenuator and to the ATTENUATION DB 0-80 control, switches 5 volts to the potentiometers. The calibration procedure of table 5-30 adjusts the potentiometers to provide SIG 1 through SIG 8 voltages that indicate the calibration of the Step Attenuator in the 10-db through 80-db steps.

(10) The CPU and I/O subsystem causes sequential measurement of the SIG 1 through SIG 8 signals until a voltage is detected. Then it calculates the Step Attenuator attenuation and stores the result in RAM memory for use in the power calculation. If the CPU and I/O subsystem does not find a voltage on any of the signals, it stores 0 db in RAM memory as the Step Attenuator attenuation.

b. Radar Power Measurement

(1) The Test Set measures radar peak rf power in the RADAR PULSE or RADAR CW mode when the DISPLAY SELECT switch is in RF IN PWR (DBM) position. The Test Set measures the rf power from the RF IN/OUT connector after attenuation by a Step Attenuator. The Test Set displays a + (plus sign) on the digital display when this power is too large to be measured, and displays a - (minus sign) when the rf power is too small. The ATTENUATION DB 0-80 control adjusts the rf power level until it is in the range where measurement is possible. Then the Test Set measures the power, adds the attenuation selected by the ATTENUATION DB 0-80 control, and displays the result on the digital display as +0.0 to +50.0 dbm. This displayed power is the peak input level at the front panel RF IN/OUT connector.

(2) For a radar power measurement, the Test Set energizes the coaxial (coax) switch to connect the detector to the 24-db directional coupler. Then, the radar signal, applied at the front panel RF IN/OUT connector, is applied through the Step Attenuator, 24-db directional coupler, and coax switch to the detector. The Test Set then measures the power level at the detector as described above. This power level must be between -27 and -13 dbm for a valid power measurement to take place. The Test Set displays a - (minus sign) on the digital display if this power is less than -27 dbm and displays a + (plus sign) if this power is greater than -13 dbm. For powers between -27 and -13 dbm, the Test Set adds the attenuation in the rf path from the RF IN/OUT connector to the detector to obtain the radar power level at the front panel RF IN/OUT connector. The Test Set displays this value as 0.0 to +50.0 dbm on the digital display.

(3) The radar power measurement operation begins when the CPU and I/O subsystem reads switch data and finds the DISPLAY SELECT switch in the RF IN PWR (DBM) position. The CPU and I/O subsystem then checks the switch data to determine if the MODE switch is in the RADAR PULSE or RADAR CW position. If the MODE switch is not in one of these positions, the CPU and I/O subsystem sends control data to the display subsystem, blanking the digital display, then reads the switch data again. This process repeats until the MODE switch or the DISPLAY SELECT switch is moved to a new position. If the MODE switch is in the RADAR PULSE or RADAR CW position when the DISPLAY SELECT switch is in the RF IN PWR (DBM) position, the CPU and I/O subsystem checks the power calibration flag to determine if the power measurements subsystem is calibrated, then either calibrates the power measurements subsystem or attempts a radar power measurement.

(4) If the power calibration flag is reset, the CPU and I/O subsystem sets the flag, causes the power calibration operation described above, then attempts a power measurement. If the power calibration flag is set, the CPU and I/O subsystem attempts the radar power measurement.

(5) To attempt a radar power measurement, the CPU and I/O subsystem first sends data, with bit 3 set, to address D200. This causes the coax switch to energize, connecting the detector to the 24-db directional coupler which picks off the input radar signal. The CPU and I/O subsystem sets bit 6 of this data if the MODE switch is in the RADAR CW position; this causes the power reference and CW

chop circuits to produce a 4-kHz square wave signal to chop the CW radar signal. If the MODE switch is in the RADAR PULSE position, the CPU and I/O subsystem sends the data with bit 6 reset, turning off the 4-kHz chopping signal. Next, the CPU and I/O subsystem causes a measurement of the DETECTED POWER signal, and compares the voltage with the two voltages measured during power calibration.

(6) If the DETECTED POWER signal voltage is not between the two voltages measured during power calibration, the power at the detector is not between -13 dbm and -27 dbm and the Test Set cannot convert the voltage to a dbm value. Therefore, no radar power measurement can be made until the Step Attenuator is adjusted to bring the power level at the detector within the -27 to -13 dbm range. If the voltage is greater than the high power calibration value (-13 dbm value), the CPU and I/O subsystem sends data to the display subsystem, causing a + (plus sign) display on the digital display. If the voltage is less than the -27 dbm value, the CPU and I/O subsystem causes a - (minus sign) display. After display of the plus or minus sign, the radar power sequence starts over with the CPU and I/O subsystem reading switch data again. The whole process repeats until the Step Attenuator (ATTENUATION DB 0-80 control) is adjusted to bring the power at the detector within -13 to -27 dbm, or until the MODE switch or DISPLAY SELECT switch is moved to a new position.

(7) If the DETECTED POWER signal voltage is between the two voltages measured during power calibration, the CPU and I/O subsystem reads the Step Attenuator attenuation, as described above, and saves the attenuation value for use in the radar power calculation. Then, the CPU and I/O subsystem causes another measurement of the DETECTED POWER signal voltage and uses the calibration table to convert this measured voltage value to a dbm value. The CPU and I/O subsystem then adds the Step Attenuator attenuation to this value and adjusts the result by a fixed offset to account for the fixed attenuation between the RF IN/OUT connector and the detector. This calculation results in a binary number that indicates the radar power level, in dbm, at the front panel RF IN/OUT connector. This number may contain a small error since the fixed offset may not exactly equal the actual fixed attenuation between the RF IN/OUT connector and the detector.

(8) The CPU and I/O subsystem corrects the calculated radar power by adding a calibrated correction value, which is equal to the difference between the fixed offset and the actual fixed attenuation, between the RF IN/OUT connector and the detector. The CPU and I/O subsystem determines this correction value by causing the measurements subsystem to measure the voltage of SIG 14 provided by the RF PWR potentiometer. The result of this measurement is a binary number which the CPU and I/O subsystem scales to a correction value between +3.2 and -3.2 db. Then, the CPU and I/O subsystem adds this correction value to the calculated radar power, converts the result to BCD, and sends it to the display subsystem for display on the digital display. The RF PWR potentiometer is adjusted, during the calibration procedure of table 5-29, such that the displayed radar power is within 0.1 db of a known power level input at the RF IN/OUT connector.

(9) After the radar power is displayed, the CPU and I/O subsystem waits 225 milliseconds and then repeats the entire radar power measurement sequence. This

process is repeated, updating the displayed radar power about three times per second, until the DISPLAY SELECT switch is moved out of the RF IN PWR (DBM) position.

c. Test Set Power Measurement

(1) The Test Set measures Test Set peak rf output power in the RADAR CW, RADAR PULSE, SIG GEN CW, SIG GEN PULSE, or SIG GEN SQW mode when the DISPLAY SELECT switch is in the RF SIG PWR (DBM) position. The Test Set also measures Test Set peak rf output power in the SIG GEN FM mode when the DISPLAY SELECT switch is in the SIG PWR (DBM) position, provided that the FM HOLD HIGH-MOD-HOLD LOW switch is held in the HOLD HIGH or HOLD LOW position. The Test Set displays a + (plus sign) when the output power, prior to the Step Attenuator, is too large to be measured, and displays a - (minus sign) when this power is too small to be measured. The ATTENUATION DB FINE control adjusts this power level within the range where measurement is possible. The Test Set measures the power, subtracts the attenuation selected by the ATTENUATION DB 0-80 control, and displays the result on the digital display as +0.0 to -85.0 dbm. This displayed power is the peak output level at the front panel RF IN/OUT connector.

(2) The Test Set rf, from the Gunn Oscillator, goes through the pin attenuator, pin switch, and Step Attenuator to the front panel RF IN/OUT connector. For a Test Set power measurement, the Test Set deenergizes the coax switch to connect the 15.5-db directional coupler to the detector. Then the Test Set rf, at a point prior to the Step Attenuator, couples through the 15.5-db directional coupler and coax switch to the detector. The Test Set measures this power by measuring the DETECTED POWER signal voltage as previously described. The Test Set displays a - (minus sign) on the digital display if this power is less than -27 dbm, and displays a + (plus sign) if this power is greater than -13 dbm. For powers between -27 and -13 dbm, the Test Set subtracts the attenuation in the rf path from the 16-db directional coupler to the RF IN/OUT connector and adds the attenuation in the rf path from the 16-db directional coupler to the detector. The result is the Test Set power level at the front panel RF IN/OUT connector. The Test Set displays this as 0.0 to -85.0 dbm on the digital display.

(3) The Test Set power measurement operation begins when the CPU and I/O subsystem reads switch data and finds the DISPLAY SELECT switch in the RF SIG PWR (DBM) position. The CPU and I/O subsystem then checks the switch data to determine if the MODE switch is in the RADAR PULSE, RADAR CW, SIG GEN PULSE, SIG GEN CW, SIG GEN SQW, or SIG GEN FM position. If the MODE switch is not in one of these positions, or if it is in the SIG GEN FM position and the FM HOLD HIGH-MOD-HOLD LOW switch is in the MOD position, the CPU and I/O subsystem sends control data to the display subsystem blanking the digital display. The CPU and I/O subsystem then reads the switch data again. This process repeats until the MODE switch, DISPLAY SELECT switch, or FM HOLD HIGH-MOD-HOLD LOW switch (SIG GEN FM mode only) is moved to a new position. If the MODE switch is in the RADAR CW, RADAR PULSE, SIG GEN CW, SIG GEN PULSE, or SIG GEN SQW position; or if the MODE switch is in the SIG GEN FM position and the FM HOLD HIGH-MOD-HOLD LOW switch is in the HOLD HIGH or HOLD LOW position, then the CPU and I/O subsystem checks the power calibration flag to determine if the power measurements subsystem is calibrated.

(4) If the power calibration flag is reset, the CPU and I/O subsystem sets the flag, causes the power calibration operation, then attempts a power measurement. If the power calibration flag is set, the CPU and I/O subsystem attempts the Test Set rf power measurement.

(5) To attempt a Test Set rf power measurement, the CPU and I/O subsystem sends data, with bit 3 reset, to address D200. This deenergizes the coax switch, connecting the detector to the 15.5-db directional coupler which picks off a sample of the Test Set rf signal. The CPU and I/O subsystem sets bit 6 of this data if the MODE switch is in the RADAR CW, SIG GEN CW, or SIG GEN FM position, causing the power reference and CW chop circuits to produce a 4-kHz square wave signal to chop the sampled Test Set rf. If the MODE switch is in the RADAR PULSE, SIG GEN PULSE, or SIG GEN SQW position, the CPU and I/O system sends the data with bit 6 reset, turning off the 4-kHz chopping signal. Next, the CPU and I/O subsystem causes a measurement of the DETECTED POWER signal and compares the voltage with the two voltages measured during power calibration.

(6) If the DETECTED POWER signal voltage is not between the two voltages measured during power calibration, the power at the detector is not between -13 dbm and -27 dbm and the Test Set cannot convert the voltage to a dbm value. Therefore, no Test Set rf power measurement can be made until the pin attenuator is adjusted to bring the power level at the detector within the -27 to -13 dbm range. If the voltage is greater than the high power calibration value (-13 dbm value), the CPU and I/O subsystem sends data to the display subsystem, causing a + (plus sign) display on the digital display. If the voltage is less than the -27 dbm value, the CPU and I/O subsystem causes a - (minus sign) display. After display of the plus or minus sign, the Test Set power sequence starts over with the CPU and I/O subsystem reading switch data again. The whole process repeats until the pin attenuator (controlled by the ATTENUATION DB FINE control) is adjusted to bring the power at the detector within -13 to -27 dbm, or until the MODE or DISPLAY SELECT switch is moved to a new position.

(7) If the DETECTED POWER signal voltage is between the two voltages measured during power calibration, the CPU and I/O subsystem reads the Step Attenuator attenuation, as previously described, and saves the attenuation value for use in the Test Set power calculation. Then the CPU and I/O subsystem causes another measurement of the DETECTED POWER signal voltage and uses the calibration table to convert this measured voltage value to a dbm value. The CPU and I/O subsystem then subtracts the Step Attenuator attenuation from this value and adjusts the result by a fixed offset to account for the fixed attenuation between the RF IN/OUT connector and the detector. This calculation results in a binary number that indicates the Test Set rf power level, in dbm, at the front panel RF IN/OUT connector. This number may contain a small error since the fixed offset may not exactly equal the actual attenuation between the RF IN/OUT connector and the detector.

(8) The CPU and I/O subsystem corrects the calculated Test Set rf power by adding a calibrated correction value (equal to the difference between the fixed offset and the actual attenuation) between the RF IN/OUT connector and the detector.

The CPU and I/O subsystem determines this correction value by causing the measurements subsystem to measure the voltage of SIG 15 provided by the SIG PWR potentiometer. The result of this measurement is a binary number which the CPU and I/O subsystem scales to a correction value between +3.2 and -3.2 db. Then, the CPU and I/O subsystem adds this correction value to the calculated Test Set rf power, converts the result to BCD, and sends it to the display subsystem for display on the digital display. The SIG PWR potentiometer is adjusted, during the calibration procedure of table 5-29, such that the displayed Test Set rf power is within 0.1 db of a measured power level at the RF IN/OUT connector.

(9) After the Test Set rf power is displayed, the CPU and I/O subsystem waits 250 milliseconds and then repeats the entire Test Set rf power measurement sequence. This process is repeated, updating the displayed Test Set rf power about three times per second, until the DISPLAY SELECT switch is moved out of the RF SIG PWR (DBM) position.

d. Power Measurement Considerations

(1) RF Cable (W2) is calibrated and marked with an attenuation value. When radar power measurements are made, this attenuation must be added to the displayed power to determine the peak power level out of the radar signal source. When Test Set output power measurements are made, this attenuation must be subtracted from the displayed power to determine the peak power level delivered to the radar under test.

(2) The Test Set or Test Set/RF Cable W2 combination provides a 50-ohm load impedance to the radar unit under test. Similarly, the Test Set output or Test Set/RF Cable W2 combination output provides a 50-ohm source impedance.

(3) The pulse width (PW) and pulse repetition interval (PRI) must be considered to determine the average radar or Test Set power for pulsed modes. The Test Set always measures peak power. This peak power is converted to average power by using the following equations:

$$AVG = PEAK + 10 \log (PW/PRI)$$
$$AVG = PEAK + 10 \log (PW \times PRF)$$

where:

AVG = average power in dbm
PEAK = peak power in dbm
log = base 10 (common) logarithm
PW = pulse width in seconds
PRI = pulse repetition interval in seconds
PRF = pulse repetition frequency in hertz

For CW signals, average power equals peak power.

4-14. POWER MEASUREMENTS SUBSYSTEM FUNCTIONAL DIAGRAM DESCRIPTION (Figure 6-7). Figure 6-7 shows the physical location of all circuits and signals in the power measurements subsystem. The following paragraphs describe, in detail, the purpose and characteristics of these circuits and signals, and the self-test operation.

a. Radar Power Measurement

(1) A radar signal is input to the Test Set at RF IN/OUT connector 1A1J2. This signal may be continuous wave (CW), or pulsed rf having a prf from 50 Hz to 50 kHz. The Test Set measures the peak power of this radar rf signal and displays the power, from 0.0 to +50.0 dbm on the digital display.

(2) The radar signal passes through Detector 1A1A6 and cable 1A1W3 to connector J2 on Step Attenuator 1A1A8AT1 (sheet 1 of figure 6-7). Detector 1A1A6 mounts directly on the rear of RF IN/OUT connector J2. The Step Attenuator is part of Attenuator Assembly 1A1A8 and is operated by the ATTENUATION DB 0-80 control to provide 0 to 80 db attenuation in steps of 10 db. During radar power measurements, the ATTENUATION DB 0-80 control is set to a position where the peak power of the ATTENUATOR IN/OUT signal out of the attenuator is between -4 and +10 dbm.

(3) The ATTENUATOR IN/OUT signal is applied through cable 1A1W1 to connector J1 on Coupler Module 1A1A4A2 in Microwave Assembly 1A1A4 (sheet 2). Within the Coupler Module, the radar power is coupled through the 24-db directional coupler and connector 1A1A4A2J3 to the normally open terminal (2) on Coaxial Switch 1A1A4S1. During radar power measurements, the Coaxial Switch energizes to connect the radar power from connector 1A1A4A2J3 to connector J1 on RF Detector 1A1A4A4.

(4) The energizing coil in the Coaxial Switch connects between -15V (-) and the COAX SWITCH DRIVE signal (+). During radar power measurements, the CPU and I/O subsystem sends data, with bit 3 set, to address D200. This data is stored in XCVR U1 on Microwave Interface 1A1A3 (sheet 1), causing a high logic level output as the COAX SWITCH CNTRL signal to the driver (U32, Q5). At the driver, inverter U32 inverts the high to a low logic level, turning on transistor Q5. This causes a COAX SWITCH DRIVE signal voltage of approximately +12 volts dc, energizing the Coaxial Switch.

(5) During radar power measurements in the RADAR CW mode, the chopper signal generator (U28, U16) provides a 4-kHz logic level square wave as a chopping signal to chop the radar rf signal. The CPU and I/O subsystem sends data, with bit 6 set, to address D200. This data is stored in XCVR 1A1A3U1, causing a high logic level output as the CW/PULSE MODE signal. This high logic level removes the reset from counter U28, allowing the counter to divide the 64-kHz clock (received at connector 1A1A3J2-5) to produce 8-kHz and 4-kHz outputs. Inverters U16-2 and U16-4 buffer the 4-kHz output to provide the CW CHOP signal at standoff E9 on Microwave Interface 1A1A3. The CW CHOP signal is applied to connector J7 on Coupler Module 1A1A4A2 in the Microwave Assembly (sheet 2). This 4-kHz square wave follows a dc path from connector 1A1A4A2J7, through the load and 24-db directional coupler, connector 1A1A4A2J3, and Coaxial Switch 1A1A4S1 to connector J1 on RF Detector 1A1A4A4.

(6) During RADAR CW mode, the RF INPUT signal at connector J1 on RF Detector 1A1A4A4 has two components: the sampled radar rf signal and the 4-kHz logic level square wave chopping signal. The 4-kHz component of this signal causes the limiter diode at the detector input to chop the radar rf.

(7) During RADAR PULSE mode, the CPU and I/O subsystem sends data, with bit 6 reset, to address D200. This causes the low CW/PULSE MODE signal, holding counter U28 of Microwave Interface 1A1A3 in the reset condition (chopper signal generator, sheet 1). This causes a low logic level output from inverter U16-4 as the CW CHOP signal, disabling the chopping operation of the limiter diode in the detector at RF Detector 1A1A4A4 (sheet 2).

(8) At the detector, the radar rf is coupled through the dc block and is detected by the detector diode and rf bypass to produce a 4-kHz square wave (RADAR CW mode) or negative going pulse (RADAR PULSE mode) signal. This signal is applied through connector J2 of the RF Detector as the RF DETECTED OUT signal to standoff 1A1A3E10 on the Microwave Interface. The amplitude of this signal is proportional to the power of the radar rf signal at the detector input and is between 10 and 100 millivolts peak to peak during power measurements.

(9) At the power measurements circuits (sheet 3) of Microwave Interface 1A1A3, the RF DETECTED OUT signal, from standoff 1A1A3E10, is ac coupled through capacitor C68 to differential video amplifier U25. GAIN potentiometer VR17 adjusts the gain of differential video amplifier U25 to calibrate the power measurements circuits. The GAIN potentiometer is adjusted (during calibration procedure of table 5-29) such that a +11-dbm radar signal at RF IN/OUT connector J2 produces an 8.0-volt DETECTED POWER signal.

(10) The noninverting output of differential video amplifier U25 (OUT 1 signal, monitored at test point TP21) is applied to a negative peak detector (U29, U30). The inverting output (OUT 2 signal, monitored at test point TP19) is applied to a positive peak detector (U26, U27). The two peak detectors are similar, each consisting of a comparator (U29 or U26), a storage capacitor (C76 or C86), and an operational amplifier (U30 or U27) with a voltage divider feedback to the reference input of the comparator. The operational amplifier has a gain of 10, producing a dc voltage at the output (test point TP20, TP22) that is 10 times greater than the positive peak voltage of the input waveform.

(11) The peak detector outputs are combined and amplified in summing amplifier U31 to produce the DETECTED POWER output signal, monitored at test point TP23 or TP39. For pulsed rf signals, the negative peak detector output provides most of the input to summing amplifier U31 because the negative going detector output (RF DETECTED OUT signal) is inverted to produce positive going pulses at the input to the negative peak detector (test point TP21). The positive peak detector output is very small for pulsed rf signals because its input waveform (test point TP19) is a very small positive voltage with negative going pulses. Typically, for pulsed rf signals, the positive peak detector output at test point TP20 is less than 5 millivolts dc, and the negative peak detector output voltage at test point TP22 is one-half the DETECTED POWER signal voltage at test point TP23. The DETECTED POWER signal voltage is in the 1-volt to 8-volt range during power measurements.

(12) For continuous wave (CW) rf signals, the RF DETECTED OUT signal is a 4-kHz square wave. Differential video amplifier U25 amplifies this to provide two equal out of phase, 4-kHz square wave inputs to the peak detectors. Because both square wave signals swing equally in the positive and negative directions, the two peak detectors respond equally. During CW operation, the chopper signal generator (sheet 1) provides 8-kHz square wave signals to the peak detectors, disabling them during the first half of each 4-kHz input signal pulse. This makes the peak detectors insensitive to transient voltages produced in the detectors at the leading edge of the 4-kHz chopping signal. For CW rf signals, the peak detector output voltages at test points TP20 and TP22 are equal to each other and are three-fourths of the DETECTED POWER signal voltage.

(13) The DETECTED POWER signal is applied as signal 12 (SIG 12) to analog multiplexer U6 in the measurements subsystem. During a power measurement, the CPU and I/O subsystem causes a dc voltage measurement of this signal to obtain a number from which power is calculated.

b. Test Set Power Measurement

(1) Gunn Oscillator 1A1A5Y1 in RF Oscillator 1A1A5 provides rf power which is attenuated and modulated to provide a Test Set rf output at RF IN/OUT connector J2. This rf output may be continuous wave, square wave modulated, or pulse modulated rf having a prf from 50 to 1500 Hz. The Test Set measures the peak power of this output rf and displays the power, from 0.0 to -85.0 dbm, on the digital display.

(2) The OSC OUTPUT signal from RF Oscillator 1A1A5 is applied through cable 1A1W2 to connector J1 on Modulator/Mixer 1A1A4A1 in Microwave Assembly 1A1A4 (sheet 2). The power of this continuous wave 8.4 to 10.0 GHz signal depends on frequency and temperature, but is in the +16 to +21 dbm range. Inside the Modulator/Mixer, this signal passes through an isolator, a pin attenuator, and a pin switch to provide the attenuated and modulated RF SIGNAL RETURN signal output at connector 1A1A4A1J2.

(3) The pin attenuator in the Modulator/Mixer provides fine attenuation and has a maximum attenuation from 16 to greater than 20 db. Attenuation of the pin attenuator is controlled by the PIN ATTENUATOR OUT signal current which enters the Modulator/Mixer at connector 1A1A4A1J4. This current comes from the pin attenuator driver circuit on Microwave Interface 1A1A3 (sheet 3). Potentiometer 1A1R1, coupled to the ATTENUATION DB FINE control on the front panel, provides 0 to -15 volts as the FINE RF POWER signal to the pin attenuator driver.

(4) The FINE RF POWER signal from connector 1A1A3J25-2 is inverted by unity gain operational amplifier U24 to provide attenuation of 0 volts (maximum) to +15 volts (minimum) at test point 1A1A3TP24. This voltage is converted to a current through the resistance of series resistor R208 and MAX ATTEN potentiometer VR14. This current leaves Microwave Interface 1A1A3 at standoff E4 as the PIN ATTENUATOR OUT signal. This current varies from 0 milliamperes (maximum attenuation) to a range of 2 to 5 milliamperes (minimum attenuation).

(5) In Modulator/Mixer 1A1A4A1 (sheet 2), the pin attenuator output is applied to a pin switch which switches the rf power on and off to provide square wave or pulse modulation. The PIN SWITCH DRIVE signal current, from the target pin switch driver on Microwave Interface 1A1A3, enters the Modulator/Mixer at connector 1A1A4A1J5 to control the pin switch. This current turns on the pin switch to provide CW rf during RADAR CW, SIG GEN CW, SIG GEN FM, and SIG GEN FM EXT modes. This current provides pulse modulation in the RADAR PULSE and SIG GEN PULSE modes and provides square wave modulation in the SIG GEN SQW mode.

(6) The RF SIGNAL RETURN output of the pin switch is applied to connector J2 on Coupler Module 1A1A4A2 in the Microwave Assembly. This attenuated and modulated rf is then routed through an isolator and connector 1A1A4A2J1, Step Attenuator 1A1A8AT1, and Detector 1A1A6 to RF IN/OUT connector 1A1J2 at the front panel (sheet 1). The isolator output (sheet 2) is also coupled through a 16-db directional coupler to provide a sample of the Test Set rf for power measurement. This sample is applied through connector 1A1A4A2J4 and deenergized Coaxial Switch 1A1A4S1 to the input of the detector of RF Detector 1A1A4A4. The CW CHOP signal enters connector J7 on Coupler Module 1A1A4A2 and is applied through the load and 16-db directional coupler, connector 1A1A4A2J4, and deenergized Coaxial Switch 1A1A4S1 to the input of the detector.

(7) During Test Set power measurements, the CPU and I/O subsystem sends data, with bit 3 reset, to address D200. This causes a low logic level output as the COAX SWITCH CNTRL signal from XCVR U1 on Microwave Interface 1A1A3 (sheet 1). This turns off transistor Q5 in the driver, producing -15 volts as the COAX SWITCH DRIVE signal and deenergizing Coaxial Switch 1A1A4S1.

(8) With one exception, the chopper signal generator, detector, and power measurements circuits function, during Test Set power measurements, in the manner previously described for radar power measurements. The one exception is the operation of blanker 1A1A3Q4, Q24 and switch Q3 in the power measurements circuits (sheet 3). During Test Set power measurements in the RADAR PULSE mode, radar pulses in Coupler Module 1A1A4A2 (sheet 2) reflect from the isolator and couple through the 16-db directional coupler along with the Test Set rf power to be measured. These reflected radar pulses may be larger than the Test Set rf signal; therefore, they could cause a false response in the negative peak detector in the power measurements circuits. The switch and blanker circuit turn off the negative peak detector during the reflected radar pulse time, insuring that the reflected radar pulses do not interfere with Test Set power measurements.

(9) Radar pulses from RF IN/OUT connector 1A1J2 (sheet 1) are coupled through a directional coupler and are detected in Detector 1A1A6 to provide pulses as the DETECTED RF IN signal to the target generation subsystem. The target generation subsystem amplifies these pulses to provide the RF ENV/PULSE MOD signal to Microwave Interface 1A1A3 at connector 1A1A3J25-9 (sheet 3). The RF ENV/PULSE MOD pulses drive a blanker (Q4, Q24) which is a saturating differential amplifier circuit. The blanker switches on during each radar pulse, providing a blanking pulse to disable the negative peak detector. The COAX SWITCH DRIVE signal controls switch Q3 which provides the DISABLE signal to the blanker. During Test Set power

measurements, the -15 volt COAX SWITCH DRIVE signal turns off switch Q3, biasing the blanker circuit to switch on during each radar pulse. During radar power measurements, the +12 volt COAX SWITCH DRIVE signal turns on switch Q3, providing the DISABLE signal which biases the blanker circuit to remain in the off condition.

c. Power Calibration

(1) The power reference generator circuits on Microwave Interface 1A1A3 provide a 4-kHz square wave as the REF signal during the power calibration operation (sheet 1). This square wave has a calibrated amplitude equivalent to -13 dbm during calibrate high operation and -27 dbm during calibrate low operation. Operational amplifier U24 provides one of two precision voltages to a resistive voltage divider. A 4-kHz logic level square wave (4-kHz signal) from the chopper signal generator passes through gates U20-6 and U20-11 and inverter U16-12 to the voltage divider. At the voltage divider, the 4-kHz square wave chops the divided precision voltage, producing the REF signal.

(2) The REF signal is applied to input 1 of differential video amplifier 1A1A3U25 in the power measurements circuits (sheet 3). During power calibration, this signal replaces the RF DETECTED OUT signal from the detector. The Test Set rf signal is turned off, then selected for power measurement. This disables the RF DETECTED OUT signal, insuring that the DETECTED POWER signal voltage during calibration operations is the response of power measurements circuits to the REF signal and not to the RF DETECTED OUT signal.

(3) Operational amplifier 1A1A3U24 has HI CAL potentiometer 1A1A3VR15 in its feedback circuit and LO CAL potentiometer 1A1A3VR16 in its input circuit (sheet 1). These potentiometers are adjusted, during the procedure of table 5-29, to produce precision high and low voltages out of operational amplifier U24 such that the resulting high and low levels of the REF signal produce DETECTED POWER signal voltages identical to the DETECTED POWER signal voltages produced by -13 dbm and -27 dbm power levels at the detector.

(4) Data stored in XCVR U1 on Microwave Interface 1A1A3 controls the calibrate operations (sheet 1). When bit 0 is set, the high PWR 20 signal enables gate U20-11 to pass the 4-kHz square wave to chop the REF signal. This selects the calibrate operation. Bit 6 must also be set to provide the high CW/PULSE MODE signal which enables the chopper signal generator to produce the 4-kHz signal. Bit 1 selects between high and low calibrate operations. When bit 1 is high, switch U32, Q19 is off, switching LO CAL potentiometer VR16 out of the input circuit of operational amplifier U24. This causes the calibrate high operation. When bit 1 is low, switch U32, Q19 turns on to provide a ground to the LO CAL potentiometer. This reduces the voltage out of operational amplifier U24, causing the calibrate low operation.

d. Self-Test of Power Measurements Subsystem Circuits

(1) Tests 180 through 185 of the self-test check the function of all components in the power measurements subsystem except for the attenuation calibration

potentiometers in Microwave Interface 1A1A3 and Step Attenuator Switch 1A1A8S1 in Attenuator Assembly 1A1A8. Self-test does not verify the calibration of the power measurements circuits. Each of tests 180 through 185 sends data to address D200 to set up a desired condition in the power measurements subsystem, then measures the DETECTED POWER signal voltage to determine the response of the power measurements subsystem to the desired condition. If the measured voltage of the DETECTED POWER does not fall within limits, self-test stops and [ ] and the applicable test number are displayed.

(2) Test 180 sets up a Test Set CW rf power measurement. Because self-test is run with the ATTENUATION DB FINE potentiometer turned to its maximum clockwise position, the Test Set rf power should be large enough to cause a maximum DETECTED POWER signal voltage out of the power measurements circuits. For test 180 to pass, this voltage must cause the maximum response of 10.2 volts (255 counts) from the measurement circuits. Test 180 fails if the ATTENUATION DB FINE potentiometer is not set fully clockwise.

(3) Test 181 sets up the calibrate low operation. For test 181 to pass, the DETECTED POWER voltage must measure between 0.00 and 1.50 volts.

(4) Test 182 sets up the calibrate high operation. For test 182 to pass, the DETECTED POWER voltage must measure between 5.48 and 10.20 volts.

(5) Test 183 sets up square wave rf power. For test 183 to pass, the DETECTED POWER voltage must measure between 5.48 and 10.20 volts.

(6) Test 184 disables the Test Set rf power. For test 184 to pass, the DETECTED POWER voltage must measure between 0.00 and 1.50 volts.

(7) Test 185 sets up Test Set CW rf power, but energizes Coaxial Switch 1A1A4S1 to cause measurement of input radar power. For test 185 to pass, the DETECTED POWER voltage must measure between 0.00 and 9.50 volts. If Coaxial Switch 1A1A4S1 does not energize, Test Set CW rf power is measured, causing test 185 to fail. Test 185 may also fail if a radar signal is input to the Test Set RF IN/OUT connector during self-test. When test 185 passes, [ ] is displayed on the digital display, indicating the end of self-test.

4-15. MEASUREMENTS SUBSYSTEM BLOCK DIAGRAM DESCRIPTION (Figures 4-8 and 4-9). Figures 4-8 and 4-9 depict the analog and digital measurements functions of the measurements subsystem.

a. Analog Measurements

(1) The analog measurements block diagram (figure 4-8) shows the selection of the signal to be measured, comparison of the selected signal with a predetermined reference voltage, and the resultant comparator output indication of the comparison to the CPU and I/O subsystem.

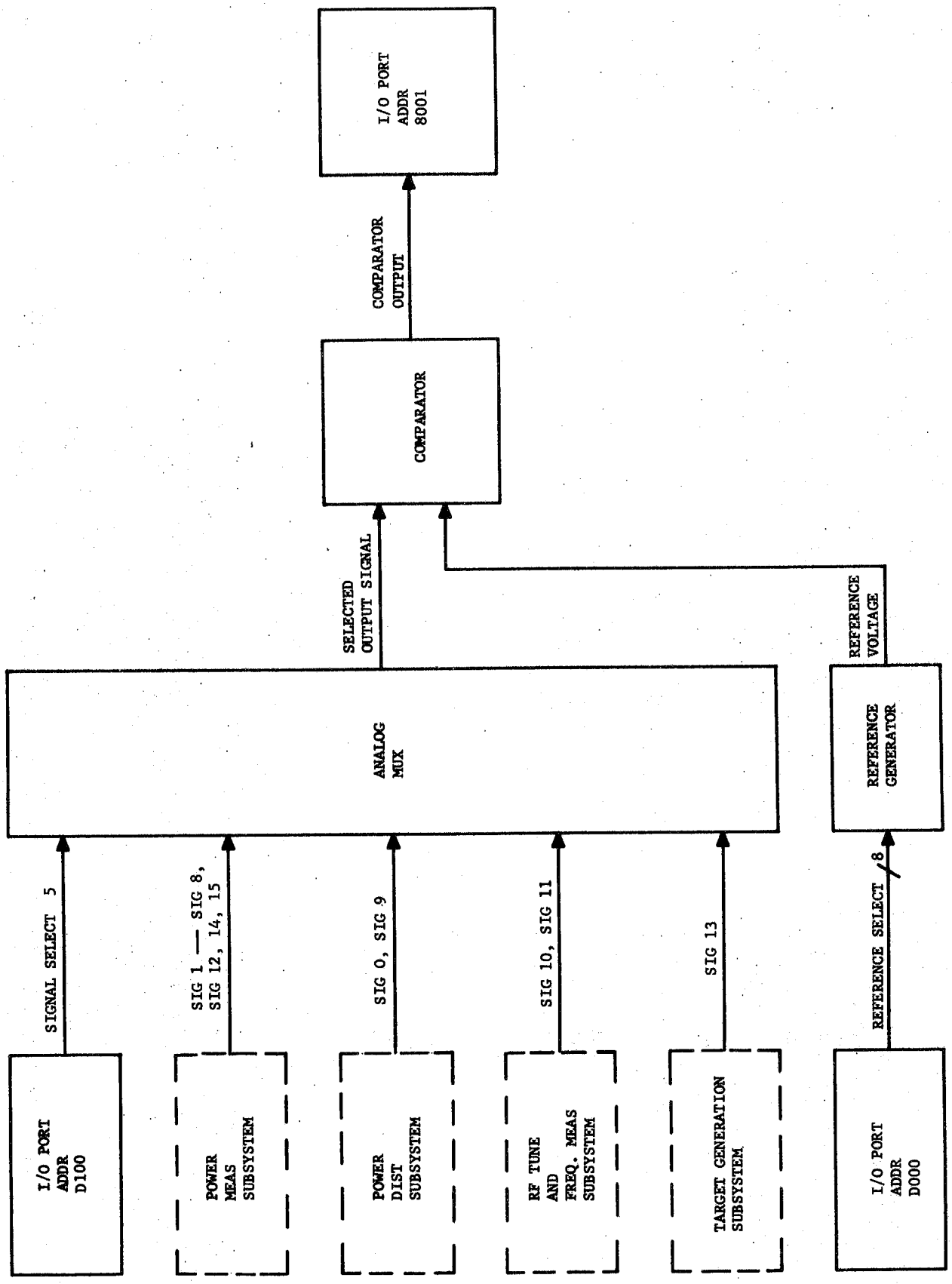


Figure 4-8. Analog Measurements Block Diagram

(2) The data stored at address D100 of the I/O port controls the signal selection of the analog multiplexer (1A1A3U5 and 1A1A3U6). These 5 bits control which of the 16 available signals to the analog multiplexer from the power measurements, power distribution, RF tune and frequency measurement, or target generation subsystems will be selected and applied as the output signal to the comparator. The data stored at address D000 of the I/O port controls the reference voltage supplied by the reference generator. The combination of these eight bits permits the reference generator to supply a reference voltage to the comparator; this voltage is from 00.0 to 10.2 volts in incremental steps of 0.04 volt. The comparator compares the selected signal with the reference voltage and provides a binary digit comparator output signal (one indicates the signal is greater than the reference voltage or zero indicates the signal is less than the reference voltage). The binary digit is stored at address 8001 at the I/O port.

b. Digital Measurements

(1) The digital measurements block diagram (figure 4-9) shows the selection of the frequency to be measured, type of measurement to be performed, counting of frequency, resetting of the frequency counters and control logic, and the counter outputs to the CPU and I/O subsystem.

(2) The RF tune and frequency measurement subsystem provides the VCO PRESCALED signal and the target generation subsystem provides the SYSTEM TRIGGER signal and the RANGE CLOCK PHASE 2 signal to the counter selector circuits. One of these three frequencies is routed through the counter selector by the FREQ SELECT bits from addr 8801 of the I/O port. The SELECTED FREQUENCY, RANGE CLOCK PHASE 2, and CLOCK FREQUENCY are applied to the frequency counter and control logic circuits and when the PERIOD/FREQUENCY MEASUREMENT signal is low (frequency measurement), the CLOCK FREQUENCY enables a gate to permit the selected frequency signal to be counted. When the gate is disabled, the frequency counter and control logic provides the COUNT COMPLETE signal and the contents of the frequency counter to the CPU and I/O subsystem. The CPU and I/O subsystem responds by providing a RESET signal to reset and clear the frequency counter and control logic circuits to prepare for the next count. When the PERIOD/FREQUENCY MEASUREMENT signal is high (period measurement), the SELECTED FREQUENCY signal enables a gate to permit the RANGE CLOCK PHASE 2 signal to be counted. When the gate is disabled, the frequency counter and control logic provides a COUNT COMPLETE signal and the contents of the frequency counter to the CPU and I/O subsystem. The CPU and I/O subsystem then provides the RESET signal to reset and clear the frequency counter and control logic.

4-16. MEASUREMENTS SUBSYSTEM FUNCTIONAL DIAGRAM DESCRIPTION (Figure 6-8)

a. Analog Measurements

(1) The address stored at address D100 in memory is supplied through XCVR U1 (I/O bus 1) of the CPU and I/O subsystem as binary bits MUX/AFC CNTRL 2^0 through 2^4 to gates U2 and U3 and analog switches U5 and U6 of the analog multiplexer. Also, analog switches U5 and U6 receive the respective SIG 0 through SIG 15 signals from the power distribution subsystem, power measurements subsystem, RF tune and

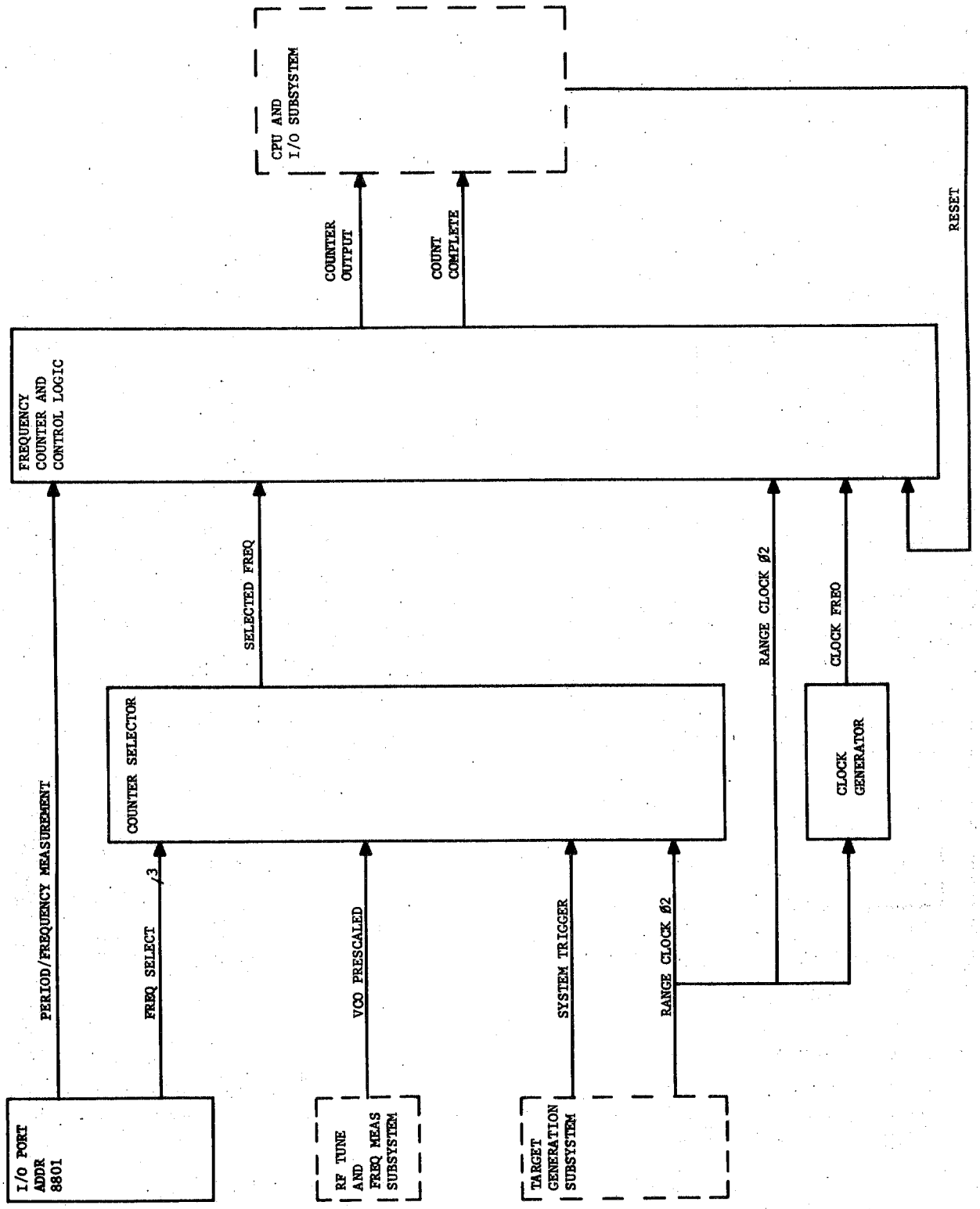


Figure 4-9. Digital Measurements Block Diagram

frequency measurement subsystem, and target generation subsystem. Gates U2 and U3 utilize MUX/AFC CNTRL 2^3 and 2^4 to determine whether analog switch U5 or U6 is gated on. The gated analog switch uses MUX/AFC CNTRL 2^0 through 2^2 to permit one of eight input signals to be switched to the output of the analog switch. The output signal is buffered by buffer U9 and is applied to the plus input of comparator U8.

(2) Address D000 in memory is supplied through XCVR U1 (I/O bus 0) of the CPU and I/O subsystem as binary bits D/A 2^0 through 2^7 to D/A converter U4 of the reference generator. D/A converter U4 provides an output voltage equivalent to the binary input (lsb = 0.04 volt, msb = 5.12 volts) to regulator U10 and buffer U11; this voltage is supplied as a reference voltage to the negative input of comparator U8. Comparator U8 compares the reference voltage with the selected signal voltage and provides a binary output indication of the comparison (binary one indicates the selected signal is negative with respect to the reference voltage, binary zero indicates the selected signal is positive with respect to the reference voltage). This binary digit is applied to address 8001 (I/O bus 1) on ROM/XCVR 1A1A2U2.

(3) The stored program uses a binary search routine to determine the value (within 0.04 volt) of an incoming signal. This method requires the Test Set to perform eight measurements (changing the reference bits while monitoring the comparator output) to complete this routine. Upon completion of this routine, voltage bits D/A 2^0 through 2^7 represent the value of the incoming signal. An example of the binary search routine is as follows: Step 1. Select 8.80-volt signal, set voltage bit D/A 2^7 high (voltage = 5.12 volts), check comparator output (zero = signal is more positive than reference voltage). Step 2. Set voltage bits D/A 2^7 and 2^6 high (voltage = 7.68 volts), and check comparator output (zero = signal is more positive than reference voltage). Step 3. Set voltage bits D/A 2^7, 2^6, and 2^5 (voltage = 8.96 volts), and check comparator output (one = signal is more negative than reference voltage). Step 4. Set voltage bits D/A 2^7, 2^6, and 2^4 (voltage = 8.32 volts), and check comparator output (zero = signal more positive than reference voltage). Step 5. Set voltage bits D/A 2^7, 2^6, 2^4, and 2^3 (voltage = 8.64 volts), and check comparator output (zero = signal more positive than reference voltage). Step 6. Set voltage bits D/A 2^7, 2^6, 2^4, 2^3, and 2^2 (voltage = 8.80 volts), and check comparator output (one = signal more negative than reference voltage). Step 7. Set voltage bits D/A 2^7, 2^6, 2^4, 2^3, and 2^1 (voltage = 8.72 volts), and check comparator output (zero = signal more positive than reference voltage). Step 8. Set voltage bits D/A 2^7, 2^6, 2^4, 2^3, 2^1, and 2^0 (voltage = 8.76 volts), and check comparator output (zero = signal more positive than reference voltage). Save D/A voltage bits. The D/A voltage bits can now be used for displaying the signal value.

(4) When calibration mode sets binary bits D/A 2^0 through 2^7 all high (10.2 volts), address D000 to D/A converter U4 through buffer U10 of reference generator is applied across scaling potentiometer 1A1A3VR2. The resultant signal is applied to D/A converter as a feedback signal. The D/A REFERENCE potentiometer is adjusted during the procedure of table 5-33 to produce precision output voltages from the D/A converter.

b. Digital Measurements

(1) Address 8801 in memory is supplied through ROM/XCVR U3 (I/O bus 0) of the CPU and I/O subsystem as binary bits counter input select bits 2^4 through 2^6 to signal selector U25. Also, signal selector U25 receives SHAPED TRIG L (system trigger), RNG CLK PH 2 (range clock), and VCO PRESCALED (vco divided by 256) frequencies from the target generation and RF tune and frequency measurement subsystems. Counter input select bits 2^4 through 2^6 determine which of the three frequencies is selected.

BITS 6	5	4	U25 OUTPUT
0	0	0	Ground
0	0	1	System trigger
0	1	0	VCO prescaled
0	1	1	Range clock

Also, address 8801 provides bit 2^7 (period) which determines the type of measurement to be performed.

(2) Before any frequency counting can be performed, 16-bit programmable counter U22 (CNTR 1) must be loaded with a value from address A100 and 16-bit programmable counter U22 (CNTR 2) is loaded with all ones from address A200. Then the READ L and I/O M signals from the microprocessor are applied to the reset input of flip-flop U29-11 to supply reset signals to the frequency counter and control logic. When the READ L signal is low and the I/O M signal is high, the 1 output of flip-flop U29 goes high and resets 8-bit up counter U28, and inhibits 16-bit down counter 1 U22. The 0 output from flip-flop U29 inhibits gates U31-3 and U31-6, preventing 16-bit down counter 2 U22 from counting, and sets flip-flop U27-11, removing the count complete signal to the microprocessor. After one instruction time, the READ L and I/O M signals change states, causing flip-flop U29-11 to reset. This removes the reset from 8-bit counter U28, provides the count enable to 16-bit programmable counter 1 U22, to gates U31-3 and U31-6, and to 16-bit programmable counter 2 U22.

(3) For a frequency measurement, the bit 7 from address 8801 goes low, causing flip-flop U27-15 to reset. The 0 output from U27 goes high and enables gate U26-8, the 1 output goes low and inhibits gate U26-11. Gate U23-8 inverts a low freq gate signal and applies a high to enable gate U26-3. Gate U26-3 passes the output frequency from signal selector U25 and gate U26-6 applies the frequency as an input to frequency counter U28 and U22. Clock generator U24 receives the range clock phase 2 signal and provides a 64-kHz clock pulse input to 16-bit programmable counter 1 U22. When counter 1 U22 reaches its terminal count, the Y output goes

high, causing the output of gate U26-8 to go low. On the positive to negative transition of the output of gate U26-8, flip-flop U27 changes states and the COUNT COMPLETE signal goes high. The CPU and I/O subsystem then receives the contents of counter U28 and counter 2 U22 to perform required computations and display the results. The microprocessor momentarily provides a low READ L and a high I/O M signal to flip-flop U29, resetting counter U28 and setting flip-flop U27 (count complete) so that the sequence can be repeated.

(4) When a period measurement is to be performed, 16-bit programmable counter 1 U22 is set to an off state, causing the Y output to go high and inhibit gate U26-3; counter 2 U22 is now loaded with all ones. The PERIOD signal from address 8801 is high for a period measurement, allowing flip-flop U27-15 to change states. When the Y output from signal selector U25 makes a positive to negative excursion, the 1 output of flip-flop U27-15 goes high, enabling gate U26-11 and permitting the RANGE CLOCK PHASE 2 frequency to be applied through gate U26-6 as an input to frequency counter U28. Frequency counter U28 continues to count until the Y output of signal selector U25 makes the next positive to negative transition. When this transition occurs, the 1 output of flip-flop U27-15 goes low and inhibits the RANGE CLOCK PHASE 2 frequency being applied to counter U28; the 0 output of flip-flop U27-15 goes high and causes gate U26-8 to go low, resulting in a high COUNT COMPLETE signal to the microprocessor. The resultant counts in counter U28 and counter 2 U22 are read and the cycle is repeated.

4-17. POWER DISTRIBUTION BLOCK DIAGRAM DESCRIPTION (Figure 4-10). Figure 4-10 shows the major components in the Test Set ac and dc power distribution. Power Cable W1 connects a 115 volt, 60 or 400 Hz, single phase power source to the Test Set at POWER connector J1. This ac power goes through the circuit breaker, the electromagnetic interference (EMI) filter, and the PWR ON-OFF switch to become the 115 VAC FILTERED power. The 115 VAC FILTERED power goes to the Power Supply and through the PNL ON-OFF switch to the front panel where it powers the electroluminescent illumination. The Power Supply provides +5, +15, and -15 vdc power which is distributed to circuits of all subsystems in the Test Set. When the power is on, +5 VDC power illuminates the POWER ON lamp, indicating that both ac and dc power is present in the Test Set.

4-18. POWER DISTRIBUTION SUBSYSTEM FUNCTIONAL DIAGRAM DESCRIPTION (Figure 6-9). Figure 6-9 is a complete schematic of Test Set ac and dc power distribution. Because Power Supply 1A1PS1 is not repairable, no schematic of its internal circuits is provided. The following paragraphs describe, in detail, the characteristics of the Power Supply, and the characteristics and connections of all ac and dc power in the Test Set.

a. AC Power Distribution

(1) Sheet 2 of figure 6-9 contains the complete schematic of Test Set ac power distribution. Power Cable W1 connects the Test Set to the ac power source. This source must be 115 vac ±10% at 60 ±10 Hz or 400 ±20 Hz, and must be capable of supplying 5 amperes. Connector W1P2 connects to the power source with 115 VAC on pin A, 115 VAC NEUTRAL on pin B, and the safety ground (CHASSIS GND) on pin C.

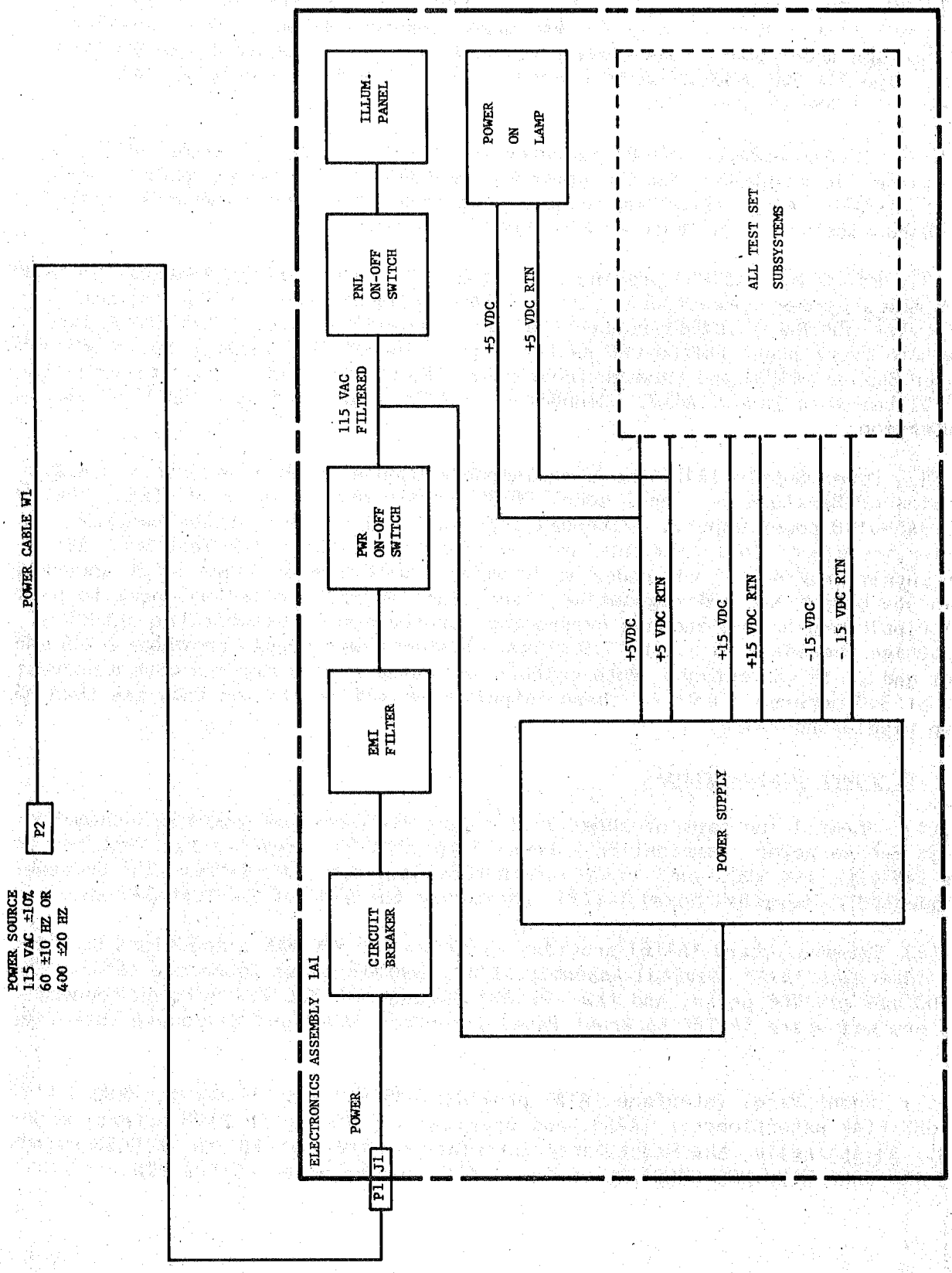


Figure 4-10. Power Distribution Block Diagram

Connector W1P1 connects to the Test Set at front panel POWER connector 1A1J1. The CHASSIS GND, from connector 1A1J1, pin C, connects to the Test Set chassis at the case of EMI filter 1A1FL1. The 115 VAC power connects from pin A of connector 1A1J1 through front panel 115V circuit breaker 1A1CB1, to terminal 1 of EMI filter 1A1FL1. The 115 VAC NEUTRAL return connects from pin B of connector 1A1J1 to terminal 2 of EMI filter 1A1FL1.

(2) Circuit breaker 1A1CB1 is rated at 5 amperes. It is turned on or reset by pressing the pushbutton switch which extends through the front panel. When circuit breaker 1A1CB1 is off or tripped, the pushbutton switch extends, making a white band visible at the base of the pushbutton switch.

(3) EMI filter 1A1FL1 prevents rf signals from entering or leaving the Test Set on the ac power connections. The 115 VAC FILTERED power (1A1FL1, terminal 3) and 115 VAC NEUTRAL FILTERED return (1A1FL1, terminal 4) out of the EMI filter connect to front panel PWR ON-OFF switch 1A1S1. The ON-OFF switch outputs connect to Power Supply 1A1PS1 and through front panel PNL ON-OFF switch 1A1S2 to connector P1 on Illuminated Panel 1A1A7. Connector 1A1A7P1 provides power for the panel illumination.

(4) Power Supply 1A1PS1 is a replaceable module which is either a C.E.A. (Division of Berkleonics, Inc.) model PB3359 power supply, or an ETATECH, INC. model 3AS5-15B power supply. Although physically dissimilar, these two power supplies are electrically similar, and are interchangeable in the Test Set. Either power supply provides +5 vdc power at 10 amperes with current limit at 20 amperes. The +5 vdc output has $\pm$3% regulation, less than 150 millivolts (mV) peak to peak (p-p) ripple and noise, and has overvoltage protection to disable the output if the voltage increases to 6.5 to 7.0 volts. Either power supply provides a +15 vdc output and a -15 vdc output. Both outputs are rated at 1.5 amperes with a current limit at 3.0 amperes. Both of these outputs have $\pm$2% regulation and less than 50 mV p-p ripple and noise.

b. DC Power Distribution

(1) Sheet 1 and part of sheet 2 of figure 6-9 show the complete schematic of Test Set dc power distribution. Power Supply 1A1PS1 provides all Test Set dc power (+5 VDC, +15 VDC, and -15 VDC) from terminal board 1A1PS1TB2. The dc power is connected to terminal board 1A1TB1, located on the side of the Test Set chassis.

(2) Terminal board 1A1TB1 provides +5 VDC and +5 VDC RTN connections to Front Panel Interface 1A1A1, Digital Assembly 1A1A2, and Microwave Interface 1A1A3. The -15 VDC and +15 VDC power, and the -15 VDC RTN and +15 VDC RTN returns connect from terminal board 1A1TB1 to Front Panel Interface 1A1A1 and Microwave Interface 1A1A3.

(3) Front Panel Interface 1A1A1 provides +15 VDC and -15 VDC to FREQ 8.4 TO 10.0 GHZ FINE potentiometer 1A1R5, and provides +15 VDC to FM RATE potentiometer 1A1R3. Additionally, the Front Panel Interface provides +5 VDC to TRIGGER switch 1A1S3 and HOLD HIGH-MOD-HOLD LOW switch 1A1S7, and provides +5 VDC RTN to PRF

potentiometer 1A1R2, DISPLAY SELECT switch 1A1S6, and MODE switch 1A1S5. Both +5 VDC and +5 VDC RTN for POWER ON indicator lamp 1A1DS1 comes from the Front Panel Interface. Front Panel Interface 1A1A1 also provides a ground connection for keyboard 1A1S8.

(4) Microwave Interface 1A1A3 provides +5 VDC to Step Attenuator Switch 1A1A8S1 and provides +5 VDC and +5 VDC RTN to Microwave Assembly 1A1A4. The Microwave Interface also provides +15 VDC and +15 VDC RTN to RF Oscillator 1A1A5 and -15 VDC and -15 VDC RTN to Microwave Assembly 1A1A4 and to ATTENUATION FINE potentiometer 1A1R1. On the Microwave Interface, +15 VDC and -15 VDC provide power for the +6V regulator and -6V regulator, respectively. These regulators supply power for operational amplifiers in the power measurements subsystem. Also, +15 VDC powers a +3.3V regulator which provides a clamp voltage for the input circuits to the analog multiplexer in the measurements subsystem.

c. Self-Test of Power Distribution Subsystem. During self-test, the measurements subsystem circuits on the Microwave Interface measure two power signals. For test number 110, signal 0 (+5 VDC) is measured. If the +5 VDC signal voltage is between +4.63 and +5.37 vdc, the test passes and self-test continues to test 111. If not, self-test stops and ␣110 is displayed on the digital display. A summing network comprising resistors R68 and R70 connects between the +15 VDC and -15 VDC to provide +5 vdc as the POWER SUPPLY signal (signal 9). For test number 111, signal 9 is measured. If the POWER SUPPLY signal is between +2.95 and +6.15 vdc, the test passes and self-test continues to test number 120. If either the +15 VDC signal or -15 VDC signal is absent or out of tolerance, the POWER SUPPLY signal will not be between +2.95 and +6.15 vdc; therefore, the test fails, self-test stops, and ␣111 is displayed on the digital display.

4-19. CALIBRATION MODE OF OPERATION

a. The Test Set calibration routines are programmed as part of self-test to set references for self-test comparison and at the end of self-test for manual intervention for Test Set calibration. The calibration routines are required to set conditions that are not controllable by front panel controls. The calibration steps are looped, in that, by repeatedly pressing E (enter) key on keyboard, the Test Set will proceed to cal step 1, as indicated by display of b1bbbb, through 4 then return to cal step 1. The cal steps are used as follows:

Attenuation DB 0-8 switch is calibrated in cal step 1.

Digital to analog reference in cal step 2.

Power measurement calibration high reference in cal step 3 with low reference in cal step 4.

Frequency of VCO Control Voltage in cal step 3 with high limit reference while cal step 4 checks the voltage with low limit reference.

b. Calibration step 1 is used to calibrate the ATTENUATOR DB 0-80 switch by scaling the output of the switch in each of the eight positions using 1A1A3VR3 through 1A1A3VR10. Detailed operation is explained in Power Measurement Subsystem Description.

c. Calibration step 2 sets the program for alinement of the Reference Generator D/A converter 10V reference using 1A1A3VR2. Detailed operation is explained in Measurements Subsystem Description.

d. Calibration steps 3 and 4 set the program for alignment using 1A1A3VR12 for correct VCO control signal during the Frequency Calibration procedure. The detailed description is explained in RF Tune and Frequency Measurement Subsystem Description.

e. Calibration steps 3 and 4 are also used to set Lo Cal and Hi Cal potentiometers as the reference for RF power using 1A1A3VR15 and 1A1A3VR16. Detailed description is explained in Power Measurements Subsystem Description.

4-20. TEST SET OPERATION. The Test Set operating instructions are provided in T.O. 33D7-44-225-1.

SECTION V

MAINTENANCE INSTRUCTIONS

5-1. GENERAL. This section contains the procedures for system checkout, inspection and preventive maintenance, troubleshooting, repair, test, and calibration of the Test Set. These procedures are provided to aid the technician in the maintenance of the Test Set. The procedures are supplemented by the theory of operation provided in Section IV, and the diagrams provided in Section VI.

5-2. MAINTENANCE CONCEPT. Maintenance of the Test Set is accomplished by isolating the malfunction to a replaceable subassembly, and replacing the faulty subassembly. The malfunctioning assembly is then repaired to component level, using the theory of operation provided in Section IV, and the troubleshooting procedures provided in Section V.

5-3. OPERATIONAL CHECKOUT. The Test Set operational checkout is accomplished by performing the system checkout procedures of table 5-1. The system checkout procedures are a step-by-step check of the eight major subsystems contained in the Test Set. The technician performs each task and observes the required indications on the Test Set or test equipment. Any indication other than the listed correct indication is to be considered a fault. When a fault occurs, refer to the fault isolation column for a description of the observed fault and the action to be taken to correct the fault.

5-4. INSPECTION AND PREVENTIVE MAINTENANCE. The inspection and preventive maintenance requirements are provided in table 5-2. The procedures are presented in tabular format and are listed according to the interval in which they must be performed.

5-5. TROUBLESHOOTING. The system fault isolation procedures (table 5-3) are provided to aid the maintenance technician in isolating a fault to a subassembly or functional group of components. The repair procedures of paragraph 5-6 provide information on gaining access to the subassemblies. Unless otherwise noted, all voltages are referenced to the Test Set chassis; a "high" is a logic level between +2.0 and +5.0 volts, a "low" is a logic level between 0.0 and +0.8 volts, and waveforms vary between logic levels ("high" and "low"). Test equipment required for troubleshooting is listed in table 2-1. Unless otherwise noted, where waveforms are viewed with an oscilloscope, the 10X probe and internal trigger should be used.

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
1	Apply power to the Test Set as follows:	Power source circuit breaker trips - table 5-3, step 1a.
	Set PWR ON-OFF switch to OFF.	
	Press circuit breaker 115V (5).	Test Set circuit breaker trips, indicated by white band visible; press circuit breaker 115V (5).
	Set PNL ON-OFF switch to OFF.	If circuit breaker trips again, refer to table 5-3, step 2a.
	Connect P1 of Power Cable W1 to Test Set Power connector J1.	POWER ON indicator does not light - table 5-3, step 3a.
	Connect P2 of Power Cable W1 to suitable 115 vac, 60 Hz or 400 Hz power source.	
	Set PWR ON-OFF switch to ON and verify that POWER ON indicator lights.	
	NOTE Allow Test Set to warm-up and stabilize for 5 minutes before proceeding.	
2	Verify that digital display does not display ␣100, ␣101, or ␣102.	␣100 displayed - faulty Digital Assembly 1A1A2 (probable CPU U1 or ROM/XCVR-U2). ␣101 displayed - faulty Digital Assembly 1A1A2 (probable ROM/XCVR U2 or U3 or decoder U6). ␣102 displayed - faulty Digital Assembly 1A1A2 (probable RAM/XCVR/ CNTR U5 or decoder U6.)

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
3	Initialize the Test Set as follows: Set TRIGGER switch to INT. Turn PRF potentiometer fully ccw. Set ATTENUATION DB 0-80 switch to 10. Turn ATTENUATION DB FINE potentiometer fully cw. Set DISPLAY SELECT switch to FREQ (MHZ). NOTE If MODE switch is in SELF TEST position, set to any position other than SELF TEST.	
	Set MODE switch to SELF TEST and observe the following:	Frequency display or L103 is displayed - faulty MODE switch 1A1S5.
	Display indicates ±1888.8.8 for 2 seconds.	+1bbb.b.b is displayed - table 5-3, step 4.
	Display indicates 00000, then increments at a 0.7 second rate until display indicates 99999.	Display is blank - table 5-3, step 5a.
	Display goes blank.	Any display other than those listed above - table 5-3, step 6a.
4	Press R key on keyboard and observe display.	Does not repeat indications of step 3 - table 5-3, step 7a.
	Display indicates 0 momentarily, then repeats indications of step 3.	
	Proceed to step 5.	

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
5	Press each of the following keys on the keyboard and verify the display (do not press R key): Key / Display / Key / Display 1 / 1 / 4 / 4 2 / 2 / 5 / 5 3 / 3 / 6 / 6 CE / ⊏ / 7 / 7 8 / 8 / . / ⊏ 9 / 9 / 0 / 0 CK / ⊆ / +/- / ⊐	Display is incorrect for one or more entries - table 5-3, step 8a.
6	Press E key on keyboard. The Test Set performs automatic self-test. The Test Set will stop momentarily at test numbers between 110 and 185; this is a normal indication. When [ ] is displayed, the automatic self-test is complete; proceed to step 7. NOTE If the Test Set display indicates ⌊⌋ XXX (example: ⌊⌋ 110), a fault has occurred. Refer to the Fault isolation column for the displayed fault.	Test Set remains in keyboard entry mode of step 5 - faulty keyboard 1A1S8. ⌊⌋ 110 displayed - table 5-3, step 9a. ⌊⌋ 111 displayed - table 5-3, step 10a. ⌊⌋ 120 displayed - table 5-3, step 11a. ⌊⌋ 121 displayed - table 5-3, step 12. ⌊⌋ 122 displayed - table 5-3, step 13a. ⌊⌋ 123 displayed - faulty Digital Assembly 1A1A2. Refer to table 5-3, step 14 for further troubleshooting. ⌊⌋ 130 displayed - faulty Digital Assembly 1A1A2. Refer to table 5-3, step 15a for further troubleshooting.

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
6 Cont		␣131 displayed - faulty Digital Assembly 1A1A2. Refer to table 5-3, step 16 for further troubleshooting. ␣132 or ␣133 displayed - faulty Digital Assembly 1A1A2. Refer to table 5-3, step 17a for further troubleshooting. ␣140 displayed - faulty Digital Assembly 1A1A2. Refer to table 5-3, step 18a for further troubleshooting. ␣141 or ␣142 displayed - faulty Digital Assembly 1A1A2. Refer to table 5-3, step 19a for further troubleshooting. ␣143 displayed - faulty Digital Assembly 1A1A2. Refer to table 5-3, step 20a for further troubleshooting. ␣150 displayed - faulty Digital Assembly 1A1A2. Refer to table 5-3, step 21a for further troubleshooting. ␣151 displayed - faulty Digital Assembly 1A1A2. Refer to table 5-3, step 22a for further troubleshooting.

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
6 Cont		☐152 displayed - faulty Digital Assembly 1A1A2. Refer to table 5-3, step 23a for further testing. ☐153 displayed - faulty Digital Assembly 1A1A2. Refer to table 5-3, step 24 for further testing. ☐154 displayed - faulty Digital Assembly 1A1A2. Refer to table 5-3, step 25 for further troubleshooting. ☐155 displayed - faulty Digital Assembly 1A1A2. Refer to table 5-3, step 26 for further troubleshooting. ☐160 displayed - table 5-3, step 27a. ☐161 displayed - table 5-3, step 28a. ☐162 displayed - table 5-3, step 29a for further troubleshooting. ☐163 displayed. If tests 161 and 162 pass, perform AFC calibration procedures of table 5-26. ☐170 displayed - faulty Microwave Interface 1A1A3. Refer to table 5-3, step 30a for further troubleshooting.

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
6 Cont		☐ 171 displayed - faulty Microwave Interface 1A1A3. Refer to table 5-3, step 31a for further troubleshooting. ☐ 180 displayed - table 5-3, step 32a. ☐ 181 displayed - table 5-3, step 33a. ☐ 182 displayed - faulty Microwave Interface 1A1A3. Refer to table 5-3, step 34 for further troubleshooting. ☐ 183 displayed - faulty Microwave Interface 1A1A3. Refer to table 5-3, step 35 for further troubleshooting.
	When automatic self-test is completed, the display will indicate [ ].	☐ 185 displayed-faulty Coaxial Switch 1A1A4S1. Refer to table 5-3, step 73 for further troubleshooting.
7	Set PNL ON-OFF switch to ON and observe that panel illuminates. NOTE Panel lighting may be turned off after this step.	Panel does not illuminate - table 5-3, step 37.
8	Set MODE switch to SIG GEN PULSE. Press R key on keyboard. Set DISPLAY SELECT switch to RANGE RATE (KNS).	Zero displayed in right digit and zero displayed in one or more other digits, and no nonzero digits displayed - table 5-3, step 38.

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
6 Cont	Verify that display indicates bbbbb0 (b = blank digit).	All digits are blank - table 5-3, step 39a. Display contains nonzero digits or decimal point is on - table 5-3, step 39b.
9	Verify that MODE switch is set to SIG GEN PULSE. Set DISPLAY SELECT switch to RANGE (YDS). Display indicates b20000 (b = blank).	Display is incorrect - table 5-3, step 40.
10	Verify that MODE switch is set to SIG GEN PULSE. Set DISPLAY SELECT switch to PW (MICROSEC). Display indicates bbb1.00 (b = blank).	Display is incorrect - table 5-3, step 41.
11	Verify that MODE switch is set to SIG GEN PULSE. Set DISPLAY SELECT switch to PRF (HZ). Display indicates between 20 and 50.	Display is incorrect - faulty DISPLAY SELECT switch 1A1S6.
12	Verify the following: MODE switch is set to SIG GEN PULSE. DISPLAY SELECT switch is set to PRF (HZ). TRIGGER switch is set to INT. Slowly rotate PRF potentiometer from the fully ccw to fully cw position. Display increases smoothly from less than 50 to greater than 5500.	Display is incorrect - faulty PRF potentiometer 1A1R2 or possible faulty prf generator 1A1A1U15.

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
13	Verify the following: MODE switch is set to SIG GEN PULSE. TRIGGER switch is set to INT. Set DISPLAY SELECT switch to RF SIG PWR (DBM). Press R key on keyboard. Display indicates +bbbbb (b = blank).	Display in incorrect - table 5-3, step 42.
14	Verify the following: MODE switch is set to SIG GEN PULSE. TRIGGER switch is set to INT. DISPLAY SELECT switch is set to PRF (HZ). ATTENUATION DB 0-80 switch is set to 10. Set PRF potentiometer to obtain 405 pps. Set DISPLAY SELECT switch to RF SIG PWR (DBM). Slowly turn ATTENUATION DB FINE potentiometer from fully cw to fully ccw position. Display indicates "+" in fully cw position, varies smoothly to greater than 10 db, then displays "-" in the fully ccw position.	Display is incorrect - table 5-3, step 43a.
15	Verify the following: MODE switch is set to SIG GEN PULSE. DISPLAY SELECT is set to RF SIG PWR (DBM). TRIGGER switch is set to INT.	Display is incorrect for any switch position - table 5-3, step 44a.

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
15 Cont	Set ATTENUATION DB 0-80 switch to 0 and adjust ATTENUATION DB FINE potentiometer for display of -5.0 ±0.2. Set ATTENUATION DB 0-80 switch to each of the following positions and verify the display: Switch Position / Display 10 / -15 ±4 20 / -25 ±4 30 / -35 ±4 40 / -45 ±4 50 / -55 ±4 60 / -65 ±4 70 / -75 ±4 80 / -85 ±4	
16	Verify that MODE switch is set to SIG GEN PULSE. Set DISPLAY SELECT switch to RF IN PWR (DBM). Display is blank.	Display is not blank - table 5-3, step 45a.
17	Verify that MODE switch is set to SIG GEN PULSE. Set DISPLAY SELECT switch to FREQ TUNE (MAX). Display is blank.	Display is not blank - table 5-3, step 46.
18	Verify the following: MODE switch is set to SIG GEN PULSE. FREQ 8.4 TO 10.0 GHZ FINE potentiometer is set fully ccw.	☐ 104 is displayed for all positions of FREQ 8.4 TO 10.0 GHZ COARSE control - table 5-3, step 47a.

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
18 Cont	NOTE ␣104 is momentarily displayed if FREQ 8.4 TO 10.0 GHZ COARSE control is rapidly turned (afc error).	Display is blank - faulty DISPLAY SELECT switch 1A1S6.
	Set DISPLAY SELECT switch to FREQ (MHZ).	Display does not change when FREQ 8.4 TO 10.0 GHZ COARSE control is turned - table 5-3, step 48.
	Turn FREQ 8.4 TO 10.0 GHZ COARSE control until display indicates less than 8400.0.	Display changes as FREQ 8.4 TO 10.0 GHZ COARSE control is turned, but display cannot be adjusted to less than 8400.0 - table 5-3, step 49.
19	Verify the following: MODE switch is set to SIG GEN PULSE. DISPLAY SELECT switch is set to FREQ (MHZ). FREQ 8.4 TO 10.0 GHZ FINE potentiometer is set fully ccw.	Display frequency does not increase by more than 10 MHz - table 5-3, step 50a.
	Note displayed frequency.	
	Slowly turn FREQ 8.4 TO 10.0 GHZ FINE potentiometer to fully cw position.	
	Displayed frequency increases smoothly until frequency is more than 10.0 MHz greater than noted frequency.	

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
20	Verify the following: MODE switch is set to SIG GEN PULSE. DISPLAY SELECT switch is set to FREQ (MHZ). FREQ 8.4 TO 10.0 GHZ FINE potentiometer is fully cw. NOTE ␣104 may appear momentarily; this is a normal indication. Slowly turn FREQ 8.4 TO 10.0 GHZ COARSE control cw until displayed frequency is greater than 10000.0.	Displayed frequency cannot be adjusted to greater than 10000.0 - table 5-3, step 51a.
21	Set MODE switch to RADAR PULSE. Set DISPLAY SELECT switch to PRF (HZ). Set TRIGGER switch to RF. Display indicates bbbbb0 (b = blank).	Display is incorrect - table 5-3, step 52a.
22	Verify the following: DISPLAY SELECT switch is set to PRF (HZ). TRIGGER switch is set RF. Set MODE switch to RADAR CW. Display is blank.	Display is not blank - table 5-3, step 53.
23	Verify the following: MODE switch is set to RADAR CW. TRIGGER switch is set to RF. Set DISPLAY SELECT switch to FREQ TUNE (MAX). Display is -bbbbb (b = blank).	Display is blank - table 5-3, step 54a.

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
24	Verify that TRIGGER switch is set to RF. Set MODE switch to SIG GEN CW. Set DISPLAY SELECT switch to the following positions and observe listed display. Position — Display FREQ (MHZ) — any frequency FREQ TUNE (MAX) — blank PRF (HZ) — blank	Any display incorrect - faulty MODE switch 1A1S5.
25	Set MODE switch to SIG GEN SQW. Set TRIGGER switch to INT. Set DISPLAY SELECT switch to following positions and verify the listed display. Position — Display PRF (HZ) — any prf PW (MICROSEC) — blank	Any display incorrect - faulty MODE switch 1A1S5.
26	Verify that TRIGGER switch is set to INT. Set MODE switch to SIG GEN FM. Set DISPLAY SELECT switch to FREQ (MHZ). Display is blank or indicates ⊔103.	Incorrect display - table 5-3, step 55.
27	Verify that switch settings of step 26 are correct. Turn FM RATE potentiometer fully cw. Turn FM DEVN potentiometer fully cw.	Display is not blank - table 5-3, step 56a.

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
27 Cont	Turn PRF potentiometer fully ccw. Display is blank.	
28	Verify that switch settings of step 26 and 27 are correct. Turn FM RATE potentiometer fully ccw. Turn PRF potentiometer fully cw. Display indicates ␣103.	Display remains blank - table 5-3, step 57a.
29	Verify the following: TRIGGER switch is set to INT. MODE switch is set to SIG GEN FM. DISPLAY SELECT switch is set to FREQ (MHZ). FM RATE potentiometer is fully ccw. FM DEVN potentiometer is fully cw. PRF potentiometer is fully cw. Slowly turn PRF potentiometer ccw to the point where the display goes blank. Set MODE switch to SIG GEN SQW. Set DISPLAY SELECT switch to PRF (HZ). The display indicates between 450 and 600 Hz.	Displayed prf is out of range - table 5-3, step 58.
30	Verify the following: FM RATE potentiometer is fully ccw. FM DEVN potentiometer is fully cw.	Frequency is not displayed in HOLD LOW position - faulty FM HOLD HIGH-MOD-HOLD LOW switch 1A1S7.

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
30 Cont	TRIGGER switch is set to INT. Turn PRF potentiometer fully ccw. Set MODE switch to SIG GEN FM. Set DISPLAY SELECT switch to FREQ (MHZ). Hold FM HOLD HIGH-MOD-HOLD LOW switch in HOLD LOW position. NOTE ␣104 may appear momentarily; this is a normal indication. Adjust FREQ 8.4 TO 10.0 GHZ COARSE control and FINE potentiometer for a display of 9200.0 ±0.5 MHz.	
31	Verify that switch settings of step 30 are correct. Hold FM HOLD HIGH-MOD-HOLD LOW switch in HOLD HIGH position. The displayed frequency is greater than 9300.0 MHz.	Displayed frequency is incorrect - table 5-3, step 59a.
32	Verify that switch settings of step 30 are correct. Turn the FREQ 8.4 TO 10.0 GHZ FINE potentiometer fully cw. Hold FM HOLD HIGH-MOD-HOLD LOW switch in HOLD LOW position and note the displayed frequency. Turn FM DEVN potentiometer fully ccw. Hold FM HOLD HIGH-MOD-HOLD LOW switch in HOLD HIGH position. The displayed frequency is less than the noted frequency.	Displayed frequency is incorrect - table 5-3, step 60a.

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
33	Verify that DISPLAY SELECT switch is set to FREQ (MHZ).	Displayed frequency is the same as the noted frequency - faulty MODE switch 1A1S5.
	Set MODE switch to SIG GEN FM EXT.	
	Note displayed frequency.	Displayed frequency is less than 50 MHz greater than noted frequency - table 5-3, step 61.
	Connect a 6-volt battery to FM EXT MOD connector J6 (+ side to center conductor). Displayed frequency is more than 50 MHz greater than the noted frequency.	
	Disconnect the battery.	
34	Set MODE switch to SIG GEN CW.	Power meter indication is incorrect - table 5-3, step 62a.
	Set DISPLAY SELECT switch to RF SIG PWR (DBM).	
	Set ATTENUATION DB 0-80 switch to 0.	
	Adjust ATTENUATION DB FINE potentiometer for display of 0 dbm.	
	Connect thermistor mount and power meter to Test Set RF IN/OUT connector J2.	
	Power meter indicates 0 ±1.0 dbm.	
35	Verify that settings and adjustments of step 34 are correct.	Power meter indication is incorrect - table 5-3, step 63a.
	Set ATTENUATION DB 0-80 switch to 10.	
	Power meter indicates within ±1.0 dbm of the displayed Test Set power.	
36	Verify that settings and adjustments of step 34 are correct.	Power meter indication is incorrect - table 5-3, step 64a.

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
36 Cont	Set ATTENUATION DB 0-80 switch to 20. Power meter indicates within ±1.0 dbm of the displayed Test Set power.	
37	Verify that settings and adjustments of step 34 are correct. Set ATTENUATION DB 0-80 switch to 30. Power meter indicates within ±1.0 dbm of displayed Test Set power.	Power meter indication is incorrect - table 5-3, step 65a.
38	Disconnect thermistor mount and power meter from Test Set RF IN/OUT connector J2. Verify that MODE switch is set to SIG GEN CW. Set ATTENUATION DB 0-80 switch to 0. Adjust ATTENUATION DB FINE potentiometer for display of 0 dbm. Set DISPLAY SELECT switch to FREQ (MHZ). Connect frequency counter with X-band plug-in to Test Set RF IN/OUT connector J2. Measured frequency is within ±1.0 MHz of the displayed Test Set frequency. NOTE ␣104 may appear momentarily; this is a normal indication. Adjust FREQ 8.4 TO 10.0 GHZ COARSE control and FINE potentiometer for a display of 8,400.0 ±50 MHz.	Displayed Test Set frequency does not agree with measured frequency - table 5-3, step 66.

Table 5-1. System Checkout Procedures - Continued

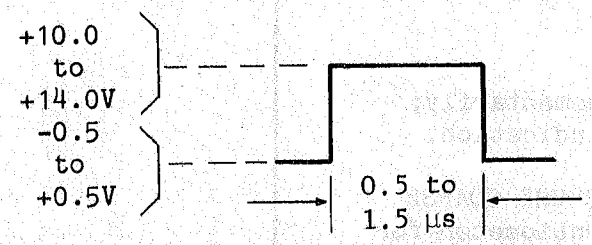
Step	Test or correct indication	Fault isolation
38 Cont	Measured frequency is within ±1.0 MHz of the displayed Test Set frequency. Adjust FREQ 8.4 TO 10.0 GHZ COARSE control and FINE potentiometer for a display of 10,000 ±50 MHz. Measured frequency is within ±1.0 MHz of the displayed Test Set frequency. Disconnect frequency counter after this step.	
39	Set TRIG OUT POS-NEG switch to POS. Set MODE switch to SIG GEN PULSE. Turn PRF potentiometer fully cw. Set TRIGGER switch to INT. Set DISPLAY SELECT switch to RANGE (YDS) and enter a 250-yard range. Connect the Test Set, crystal detector, and oscilloscope as shown in figure 5-1. Display channel 1 and trigger from channel 1. Verify the following:  	Trigger not present, polarity not correct, or amplitude is less than 9.5V - table 5-3, step 67. Trigger pulse width is not correct - faulty Digital Assembly 1A1A2 (single-shot U21).
40	Verify that settings and connections of step 39 are correct. Set TRIG OUT POS-NEG switch to NEG.	Trigger not present or polarity is incorrect - table 5-3, step 68.

Table 5-1. System Checkout Procedures - Continued

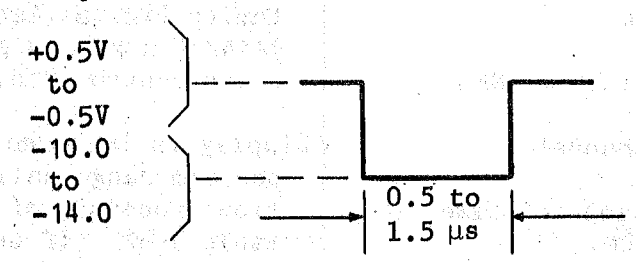
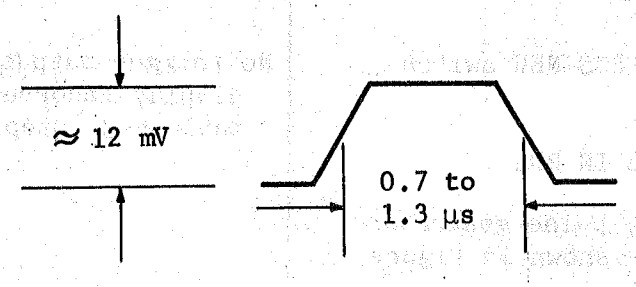
Step	Test or correct indication	Fault isolation
40 Cont	Verify the following: 	
41	Verify that settings and connections of step 39 are correct. Verify that ATTENUATION DB 0-80 switch is set to 0. Turn ATTENUATION DB FINE potentiometer fully cw. Display channel 2 and trigger from channel 2. Verify the following: 	No pulse present or pulse width is incorrect - table 5-3, step 69.

Table 5-1. System Checkout Procedures - Continued

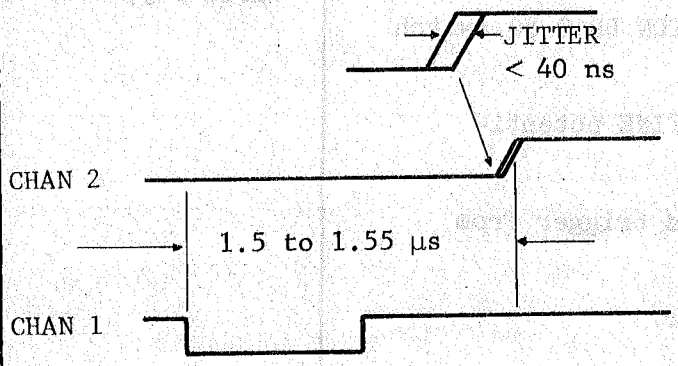
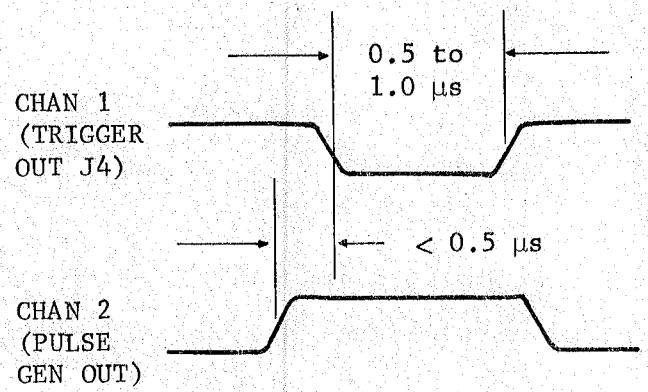
Step	Test or correct indication	Fault isolation
42	Verify that settings and connections of step 39 are correct. Set TRIG OUT POS-NEG switch to NEG. Display channel 1 and channel 2. Trigger from channel 1 and set time base to 0.2 MICROSEC/CM. Verify the following: 	Jitter is 60 nanoseconds - faulty Digital Assembly 1A1A2 (range and pulse width control U18, U19). Display is incorrect - perform range calibration procedure of table 5-32. If unable to perform procedure - faulty Microwave Interface 1A1A3 (RANGE potentiometer VR11 or analog multiplexer U6).
43	Verify that TRIG OUT POS-NEG switch is set to NEG. Set TRIGGER switch to IN POS. Connect the Test Set, pulse generator, and oscilloscope as shown in figure 5-2. Verify the following: 	No trigger output or display incorrect - table 5-3, step 70.

Table 5-1. System Checkout Procedures - Continued

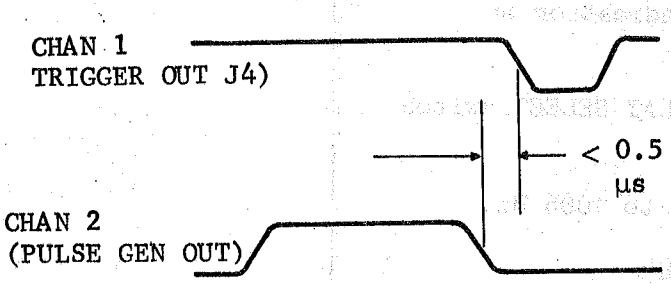
Step	Test or correct indication	Fault isolation
44	Verify that settings and connections of step 43 are correct. Set pulse generator pulse polariy to - (negative). Set TRIGGER switch to IN NEG. Verify the following:  	No trigger output or display is incorrect - table 5-3, step 71.
45	Connect test equipment as shown in figure 5-3. Connect test setup to Test Set RF IN/OUT connector J2. On Test Set: Set ATTENUATION DB 0-80 switch to 10. Set TRIGGER switch to RF. Set MODE switch to RADAR PULSE. Set DISPLAY SELECT switch to RF IN PWR (DBM).	Display does not indicate between 994 and 1006 Hz - table 5-3, step 72a.

Table 5-1. System Checkout Procedures - Continued

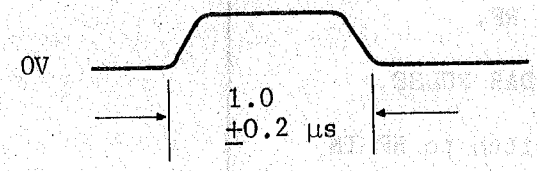
Step	Test or correct indication	Fault isolation
45 Cont	Make the following adjustments: Set pulse generator pulse width to 1.00 ±0.05 microseconds and prf to 1.0 ±0.05 KHz. Adjust sweep generator frequency to 9,200 ±10 MHz. Adjust sweep generator output for a +20 dbm nominal indication on Test Set display. On Test Set; set DISPLAY SELECT switch to PRF (Hz). Display indicates 994 to 1006 Hz. NOTE Do not change the test setup unless directed to do so.	
46	Verify test setup of step 45. Connect oscilloscope channel 1 input to to Test Set RF ENV/PULSE MON connector J5 through 50 ohm load. Observe the following waveform:  	Pulse not present or amplitude is low - faulty Front Panel Interface 1A1A1 (buffer Q2 or rf trigger U12).
47	Verify test setup of step 45. Verify that MODE switch is set to RADAR PULSE.	Display indicates only minus (-bbbbb) - table 5-3, step 73. No plus (+) or decimal point (.) in display - faulty DISPLAY SELECT switch 1A1S6.

Table 5-1. System Checkout Procedures - Continued

Step	Test or correct indication	Fault isolation
47 Cont	Set DISPLAY SELECT switch to RF IN PWR (DBM). Display indicates +bb20.0 ±1.0 dbm (b = blank).	Displayed power is out of tolerance - faulty Microwave Interface 1A1A3. Refer to table 5-3, step 74a for further troubleshooting.
48	Verify that MODE switch is set to RADAR PULSE. Set DISPLAY SELECT switch to FREQ TUNE (MAX). Adjust FREQ 8.4 TO 10.0 GHZ COARSE control and FINE potentiometer for maximum display. Display indicates bb100.0 ±50.	Display indicates +bb20.0 +1.0 (b = blank) - faulty DISPLAY SELECT switch 1A1S6. Display does not indicate 100 ±50 - table 5-3, step 75a.
49	Verify that MODE switch is set to RADAR PULSE. Set DISPLAY SELECT switch to FREQ (MHZ). Display frequency is the same as test setup counter frequency ±1.0 MHz.	Frequency display is incorrect - faulty Microwave Interface 1A1A3 (tuning signal conditioner 500 kHz peak detector CR30, CR31, C37, C39).
50	Verify that MODE switch is set to RADAR PULSE. Set DISPLAY SELECT switch to RF SIG PWR (DBM). Adjust ATTENUATION DB FINE potentiometer for display of -23.0 ±0.1 dbm. Disconnect test setup from Test Set RF IN/OUT connector J2.	Display value changes - faulty Microwave Interface 1A1A3 (power measurements blanker Q3, Q4, Q24).
51	Disconnect all test equipment.	

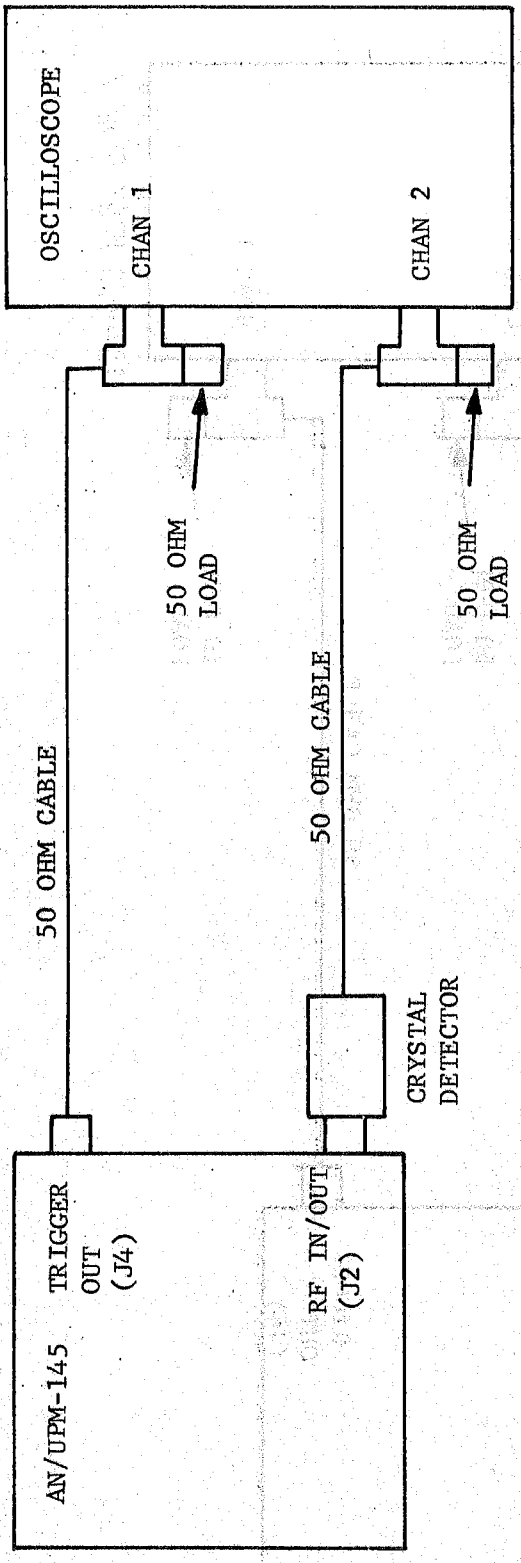


Figure 5-1. System Test Setup A

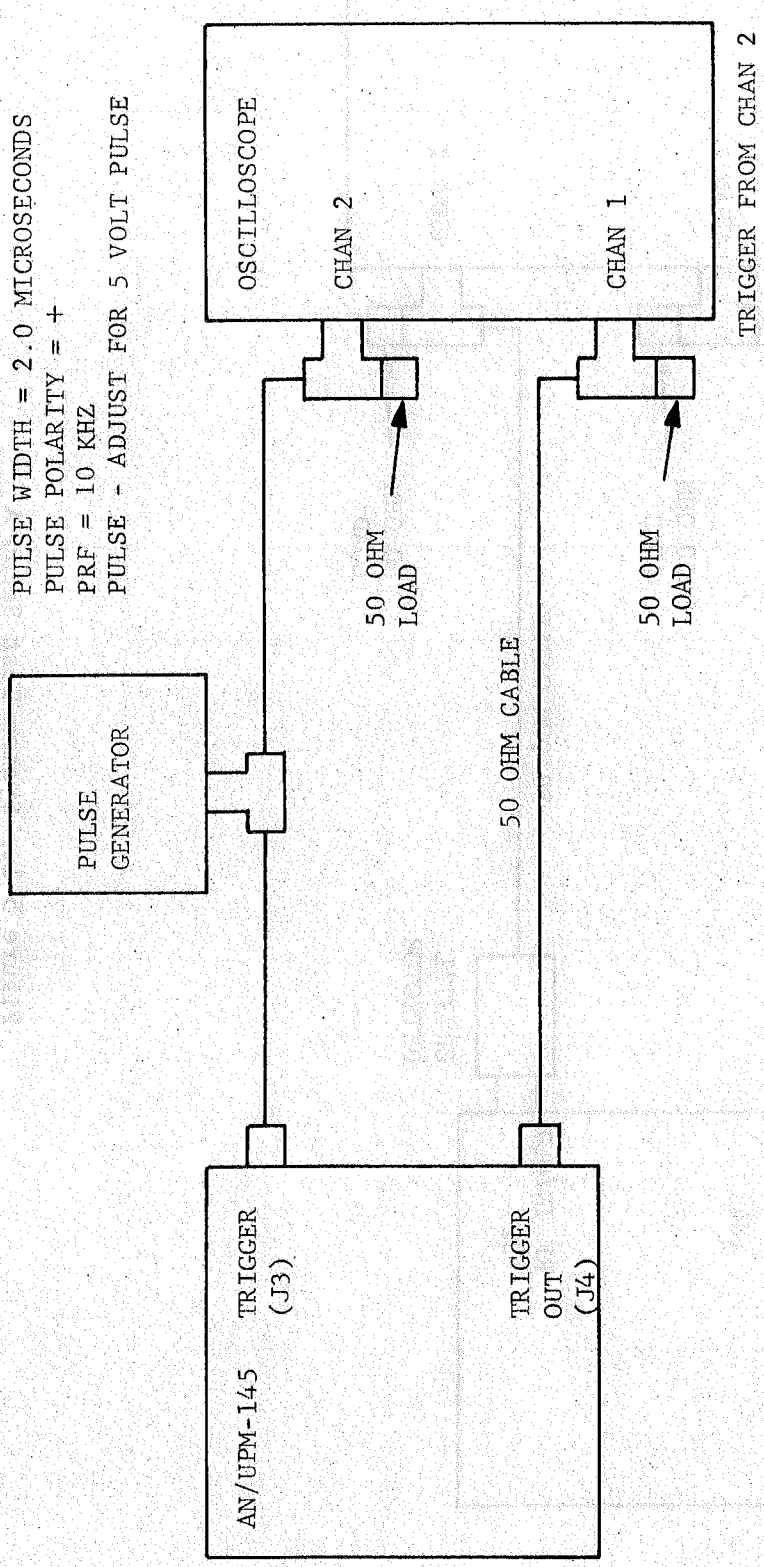


Figure 5-2. System Test Setup B

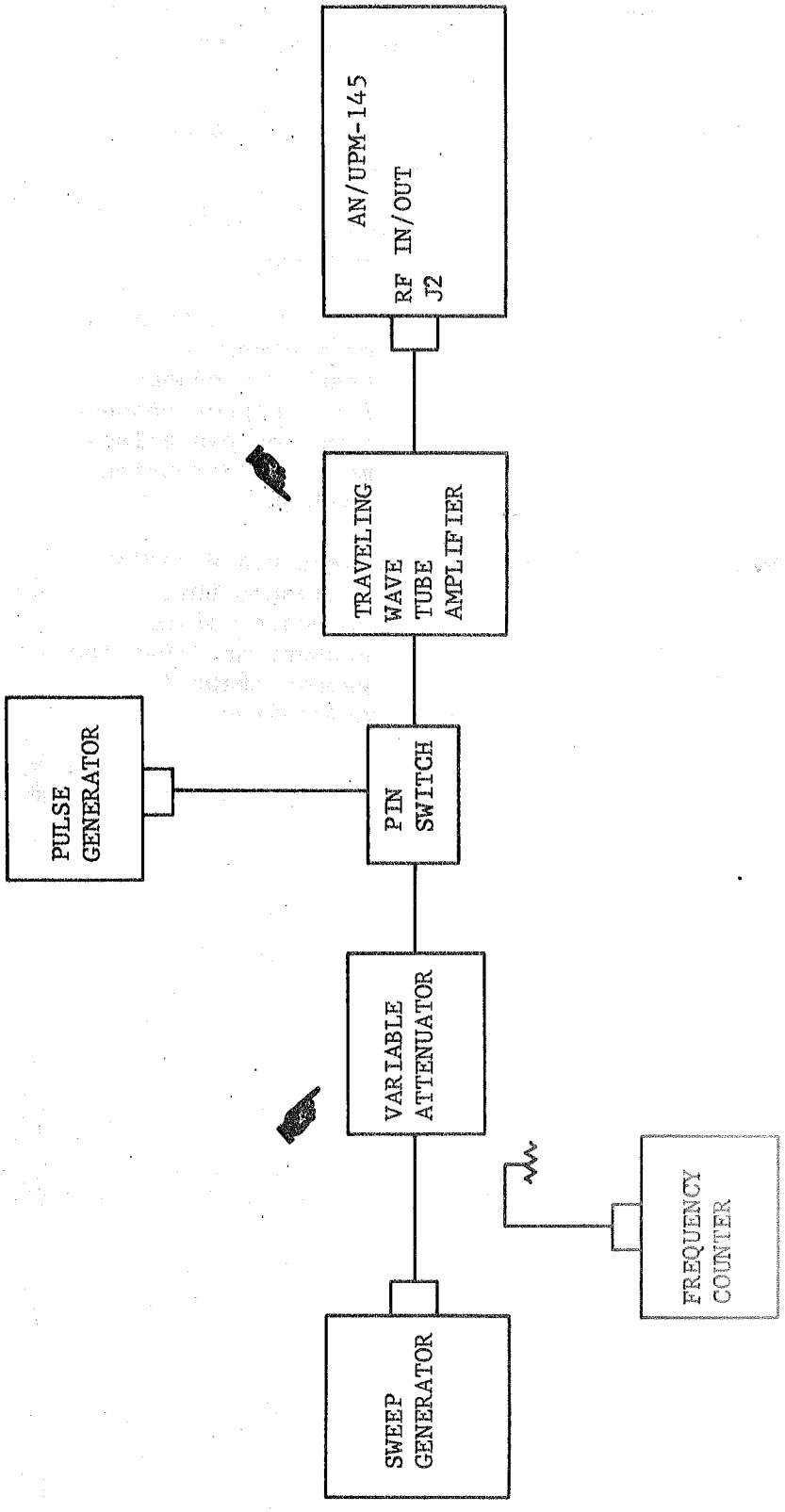


Figure 5-3. System Test Setup C

Table 5-2. Inspection and Preventive Maintenance

Inspected item	Task	Interval	Maintenance procedure
Test Set	Checkout system.	180 days	Perform procedures of table 5-1.
Front Panel controls	Inspect for damage.	180 days	Clean and replace as necessary.
Interconnecting cables	Check physical condition	180 days	Inspect insulation and connectors for breaks or cracks. Also inspect connectors for pin alinement and corrosion buildup.
Internal rigid cables	Check physical condition and shape	180 days	Inspect rigid cables to insure that corrosion is not present and that the proper shape is maintained.

Table 5-3. System Fault Isolation

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
1a	W1P1-A W1P1-B	Multimeter	**WARNING** 115 vac is present on Power Cable W1 when connected to power source. Disconnect W1 from Test Set and power source. Measure resistance between W1P1-A and W1P1-B.	Greater than 100 megohms.	Proceed to step 1b.	Repair W1.
1b	W1P1-A W1P1-C	Multimeter	Measure resistance between W1P1-A and W1P1-C.	Greater than 100 megohms.	Proceed to step 1c.	Repair W1.
1c	W1P1-B W1P1-C	Multimeter	Measure resistance between W1P1-B and W1P1-C.	Greater than 100 megohms.	Repair wiring from 1A1J1 to 1A1CB1 and 1A1FL1 (figure 6-9).	Repair W1.
2a	-	-	Inspect wire insulation and wiring connections on wires to PWR ON-OFF switch 1A1S1, 115V circuit breaker 1A1CB1, filter 1A1FL1, PNL ON-OFF switch 1A1S2, and Power Supply 1A1PS1.	Insulation intact, all connections are secure, no foreign material.	Proceed to step 2b.	Repair wiring as necessary, using figure 6-9.
2b	1A1J1-A 1A1J1-B 1A1J1-C	Multimeter	Set PWR ON-OFF switch to OFF. WARNING 115 vac is present in the Test Set when Power Cable W1 is connected to the power source. Disconnect cable connector W1P2 from power source. Set PWR ON-OFF switch to ON. Reset circuit breaker 1A1CB1.	Resistance increases capacitively to greater than 10 megohms for both measurements.	Proceed to step 2c.	Proceed to step 2e.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
2b Cont			Measure resistance between 1A1J1-A and -C, then between 1A1J1-B and -C.			
2c	1A1J1-A 1A1J1-B	Multimeter	Measure resistance between 1A1J1-A and -B.	Resistance is greater than 10 ohms.	Replace circuit breaker 1A1CB1.	Proceed to step 2d.
2d	1A1J1-A 1A1J1-B	Multimeter	Remove 115 VAC and case connections to 1A1PS1. Measure resistance between 1A1J1-A and -B.	Resistance is greater than 10 megohms.	Replace Power Supply 1A1PS1.	Replace filter 1A1FL1.
2e	1A1J1-A 1A1J1-B 1A1J1-C	Multimeter	Remove 115 VAC and case connections to 1A1PS1. Measure resistance between 1A1J1-A and -C, then between 1A1J1-B and -C.	Resistance increases capacitively to greater than 10 megohms for both measurements.	Replace Power Supply 1A1PS1.	Replace filter 1A1FL1.
3a	-	-	Set MODE switch to RADAR PULSE and DISPLAY SELECT switch to FREQ (MHZ).	Digital display indicates a frequency or ␣ 104.	Replace POWER ON lamp 1A1DS1.	Proceed to step 3b.
3b	-	-	Set PNL ON-OFF switch to ON.	Panel lights.	Proceed to step 3c.	Proceed to step 3i.
3c	1A1PS1 +5 VDC and +5 RET	Multimeter	Set PWR ON-OFF switch to OFF. Remove +5 VDC and +5 RET connections to 1A1PS1. Set PWR ON-OFF switch to ON. Measure dc voltage between +5 VDC and +5 RET terminals of 1A1PS1.	4.2 to 5.8 vdc.	Proceed to step 3d.	Replace Power Supply 1A1PS1.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
3d	1A1TB1-11 1A1TB1-23	Multimeter	Set PWR ON-OFF switch to OFF. Reconnect wires removed in step 3c. Disconnect the following: 1A1P1 from 1A1A3J1 1A1P3 from 1A1A2J1 1A1P4 from 1A1A1J2 Set PWR ON-OFF switch to ON. Measure dc voltage between 1A1TB1-23 (+) and 1A1TB1-11 (-).	+4.2 to +5.8 vdc.	Proceed to step 3e.	Repair short in +5 vdc power distribution (figure 6-9).
3e	Same as step 3d	Multimeter	Reconnect the following: 1A1P1 to 1A1A3J1 1A1P4 to 1A1A1J2 Measure dc voltage between 1A1TB1-23 (+) and 1A1TB1-11 (-).	+4.2 to +5.8 vdc.	Faulty Digital Assembly 1A1A2 (+5V distribution).	Proceed to step 3f.
3f	Same as step 3d	Multimeter	Set PWR ON-OFF switch to OFF. Reconnect 1A1P3 to 1A1A2J1. Disconnect 1A1P1 from 1A1A3J1. Set PWR ON-OFF switch to ON. Measure dc voltage between 1A1TB1-23 (+) and 1A1TB1-11 (-).	+4.2 to +5.8 vdc.	Proceed to step 3h.	Proceed to step 3g.
3g	Same as step 3d	Multimeter	Set PWR ON-OFF switch to OFF. Reconnect 1A1P1 to 1A1A3J1. Disconnect 1A1P4 from 1A1A1J2. Set PWR ON-OFF switch to ON. Measure voltage between 1A1TB1-23 (+) and 1A1TB1-11 (-).	+4.2 to +5.8 vdc.	Faulty Front Panel Interface 1A1A1 (+5V distribution) or faulty switch 1A1S7 or 1A1S3.	Replace Power Supply 1A1PS1.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
3h	Same as step 3d	Multimeter	Set PWR ON-OFF switch to OFF. Reconnect 1A1P1 to 1A1A3J1. Disconnect 1A1A4P1 from 1A1A3J23. Set PWR ON-OFF switch to ON. Measure dc voltage between 1A1TB1-23 (+) and 1A1TB1-11 (-).	+4.2 to +5.8 vdc.	Replace VCO/ Prescaler 1A1A4A3.	Faulty Microwave Assembly 1A1A3 (+5V distribution).
3i	1A1S1-2 1A1S1-5	Multimeter	WARNING 115 vac is present on PWR ON-OFF switch 1A1S1. Measure ac voltage between 1A1S1-2 and -5.	Greater than 100 vrms.	Replace PWR ON-OFF switch 1A1S1.	Proceed to step 3j.
3j	1A1FL1-1 1A1FL1-2	Multimeter	WARNING 115 vac is present on filter 1A1FL1. Measure ac voltage between 1A1FL1-1 and 1A1FL1-2.	Greater than 100 vrms.	Replace filter 1A1FL1.	Proceed to step 3k.
3k	1A1CB1-1 1A1FL1-2	Multimeter	WARNING 115 vac is present on PWR ON-OFF switch 1A1S1. Measure ac voltage between 1A1CB1-1 and 1A1FL1-2.	Greater than 100 vrms.	Replace 115V circuit breaker 1A1CB1.	Repair open in cable W1, or check power source.
4	1A1A1J2-1 1A1A1J2-4	DVM	Measure dc voltage between 1A1A1J2-1 (+) and 1A1A1J2-4 (rtn).	+4.75 to +5.25 vdc.	Proceed to step 5a.	Replace Power Supply 1PS1.
5a	1A1A1U2-22, 23, 24, 25	Oscilloscope or logic probe	Measure logic levels at pins 22, 23, 24, and 25 of transceiver U2 on Front Panel Interface 1A1A1.	High logic level on 1A1A1U2-22, 23, and 24.	Proceed to step 5b.	Proceed to step 5f.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
5a Cont				Low logic level on 1A1A1U2-25.		
5b	-	-	Replace Front Panel Interface 1A1A1.	Fault corrected.	Faulty Front Panel Interface 1A1A1 (XCVR U2).	Faulty Digital Assembly 1A1A2. Proceed to step 5c.
5c	1A1A2U9-7	Logic probe	Reinstall Front Panel Interface 1A1A1 removed in step 5b. Measure logic level pulses at pin 7 of buffer U9 on Digital Assembly 1A1A2.	Logic level pulses present.	Proceed to step 5d.	Faulty buffer 1A1A2U9 (figure 6-12, sheet 2).
5d	1A1A2U9-16	Logic probe	Measure logic level pulses at pin 16 of buffer U9.	Logic level pulses present.	Faulty data buffer 1A1A2U7, U8, U23, or CPU U1.	Proceed to step 5e.
5e	1A1A2U9-4	Logic probe	Measure logic level pulses at pin 4 of buffer U9.	Logic level pulses present.	Faulty buffer 1A1A2U9 (figure 6-12, sheet 2).	Faulty decoder 1A1A2U6 or CPU U1 (figure 6-12, sheet 2).
5f	1A1A1U2-22, 23, 24, 25	Oscillo-scope or logic probe	Disconnect 1A1P5 from 1A1A1J5. Measure logic levels.	High logic level on 1A1A1U2-22, 23, 24, 25.	Faulty MODE switch 1A1S5.	Faulty Front Panel Interface 1A1A1 (XCVR U2 or pullup resistors R11-R15).
6a	1A1TB1-12, 1A1TB1-24	DVM and oscillo-scope	Measure dc voltage between 1A1TB1-24 (+) and 1A1TB1-12 (rtn) at terminal board 1A1TB1.	+4.75 to +5.25 vdc, ripple less than	Proceed to step 6b.	Faulty Power Supply 1A1PS1.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
6a Cont				150 mV p-p.		
6b	1A1A2U1-36	-	Momentarily ground pin 36 of CPU U1 on Digital Assembly 1A1A2.	Self-test starts. Momentary display of +1888.8.8 for 2 seconds, then display increments from 00000 to 99999 at a 0.7-second rate, then display goes blank.	Faulty Digital Assembly 1A1A2 (power on reset) (figure 6-12, sheet 2).	Proceed to step 6c.
6c	-	-	Replace Front Panel Interface 1A1A1.	Fault corrected.	Faulty Front Panel Interface 1A1A1. Proceed to step 6d.	Faulty Digital Assembly 1A1A2 (CPU U1, decoder U6, RAM/ XCVR/CNTR U5, or ROM/ XCVR U2, U3) (figure 6-2, sheets 1, 2, and 3).
6d	-	-	Reinstall faulty Front Panel Interface 1A1A1 removed in step 6c. Set MODE switch to SIG GEN PULSE. Set DISPLAY SELECT switch to RANGE (YDS). Enter 88888 on keyboard (do not press E key).	Flashing "1" in far left digit of display and non-flashing 88888 present in remaining	Faulty decimal point or sign operation, faulty XCVR 1A1A2U1 or U2, inverter U8, or dis-	Faulty XCVR 1A1A2U1 or display driver U3, U4, U5, U6, or U7, or inverter U8, or displays DS1,

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
6d Cont				display digits.	plays DS1, DS5, or DS6. After replacing displays, check pull-up resistors. Refer to figure 6-11, sheet 3.	2, 3, 4, 5, or 6. After replacing displays, check pull-up resistors. Refer to figure 6-11, sheet 3.
7a	-	-	Replace 1A1. Press R key.	Restarts self-test.	Faulty Front Panel Interface 1A1A1 (pullup resistors, diode matrix, or XCVR) (figure 6-3, sheet 1).	Proceed to step 7b.
7b	1A1A1U2-1, 2, 3, 4, 37, 38, 39, 40.	Oscilloscope or logic probe	Press and hold R key. Measure logic levels at indicated test points.	High logic levels at 1A1A1U2-2, 3, 4, 37, 38, 39. Low logic level at 1A1A1U2-1 and 40.	Faulty Digital Assembly 1A1A2 (CPU or keyboard interrupt logic) (figure 6-3, sheet 1).	Faulty keyboard 1A1S8.
8a	1A1A1U2-1, 2, 3, 4, 37, 38, 39, 40.	Oscilloscope or logic probe	Press and hold faulty key. Measure logic levels at indicated test points.	Refer to S8 truth table (figure 6-3, sheet 1).	Faulty Front Panel Interface 1A1A1. Proceed to step 8b.	Faulty keyboard 1A1S8.
8b	1A1A1J1-5	Oscilloscope or	Press and hold faulty key.	Low logic level.	FAULTY XCVR 1A1A1U2.	Faulty diode

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
8b Cont		logic probe	Measure logic level.			matrix 1A1A1CR1-CR4.
9a	1A1A3TP51	DVM	Measure dc voltage.	+4.7 to +5.3 vdc.	Proceed to step 9b.	Proceed to step 9d.
9b	1A1A3J1-5	DVM	Measure dc voltage.	+14.0 to +16.0 vdc.	Proceed to step 9c.	Faulty Power Supply 1A1PS1.
9c	1A1A3J1-9	DVM	Measure dc voltage.	-14.0 to -16.0 vdc.	Faulty Microwave Interface 1A1A3 (XCVR U1, comparator U8, reference generator U4, U10, U11) (figure 6-8, sheet 1).	Faulty Power Supply 1A1PS1.
9d	1A1TB1-23	DVM	Measure dc voltage.	+4.75 to +5.3 vdc.	Proceed to step 9e.	Replace Power Supply 1A1PS1.
9e	1A1A3U1-18, 19, 20, 21, 22	Oscilloscope or logic probe	Measure logic levels.	Low logic level at all test points.	Faulty Microwave Interface 1A1A3 (analog multiplexer) (figure 6-8, sheet 1).	Proceed to step 9f.
9f	-	-	Replace Microwave Interface 1A1A3.	Self-test step □ 110 passes.	Faulty Microwave Interface 1A1A3 (XCVR U1).	Faulty Digital Assembly 1A1A2 (decoder U6

Table 5-3. System Fault Isolation - Continued

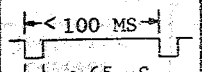
Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
9f Cont						or buffer U9) (figure 6-12, sheet 2).
10a	1A1TB1-15 1A1TB1-3	DVM	Measure dc voltage between 1A1TB1-15 (+) and 1A1TB1-3 (rtn).	+14.0 to +16.0 vdc	Proceed to step 10b.	Faulty Power Supply 1A1PS1.
10b	1A1TB1-19 1A1TB1-7	DVM	Measure dc voltage between 1A1TB1-19 (-) and 1A1TB1-7 (rtn).	-14.0 to -16.0 vdc	Faulty Microwave Interface 1A1A3. Proceed to step 10c.	Faulty Power Supply 1A1PS1.
10c	1A1A3U1-18, 21	Oscilloscope or logic probe	Measure logic level at test points.	High logic level.	Faulty analog multiplexer 1A1A3U6, R14 or summing network R68, R70).	Faulty XCVR 1A1A3U1.
11a	1A1A1TP2	Oscilloscope	Measure logic level pulses.	Pulse signal present with prf greater than 10 Hz.	Proceed to step 11b.	Proceed to step 11d.
11b	1A1AU19-11	Oscilloscope	Measure logic level pulses.	Same as above.	Faulty Digital Assembly 1A1A2. Proceed to step 11c.	Faulty Front Panel Interface 1A1A1 (trigger select logic U19).
11c	1A1A2U20-4	Oscilloscope	Measure logic level pulses.		Faulty CPU 1A1A2U1.	Faulty range and pulse width control 1A1A2U20, U21.

Table 5-3. System Fault Isolation - Continued

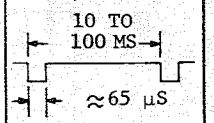
Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
11d	1A1A1TP6	Oscillo-scope	Measure logic level pulses.	Pulse signal present with prf greater than 10 Hz.	Proceed to step 11f.	Proceed to step 11e.
11e	1A1R2-2, -3	Multimeter	Disconnect 1A1P7 from 1A1A1J7. Measure resistance between 1A1R2-2 and -3 while rotating PRF potentiometer (pot) 1A1R2 from fully cw to fully ccw.	Resistance increases smoothly from 0 to 250 kilohms ±10%.	Faulty Front Panel Interface 1A1A1 (PRF Generator).	Faulty PRF pot 1A1R2.
11f	1A1A1U18-4, 1, 10, 12	DVM	Measure logic levels.	High logic level at U18-4. Low logic level at U18-1, 10, 12	Faulty Front Panel Interface 1A1A1 (trigger select U18).	Faulty TRIGGER switch 1A1S3.
12	1A1A2U20-4	Oscillo-scope	Measure logic level pulses.		Faulty Digital Assembly 1A1A2 (CPU U1).	Faulty Digital Assembly 1A1A2 (range and pulse width control (U20).
13a	1A1A2U21-2	Frequency counter	Measure frequency.	Frequency less than 600 Hz.	Faulty Digital Assembly 1A1A2. Proceed to step 13b.	Perform step 11e.
13b	1A1A2U5-1, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39	Oscillo-scope	Measure logic level.	High logic level at all test points.	Proceed to step 13c.	Faulty RAM/XCVR 1A1A2U5.

Table 5-3. System Fault Isolation - Continued

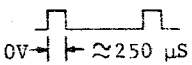
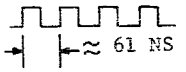
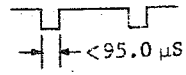
Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
13c	1A1A2U18-11	Oscilloscope	Measure logic level pulses.		Faulty range counter U11, U12, U13, or ROM/XCVR U3.	No pulses; proceed to step 13d.
13d	1A1A2U23-6	Oscilloscope	Measure logic level pulses.		Faulty range and pulse width control 1A1A2U18, U19 or pulse width counter U14, U15, U16 (fig. 6-6, sheet 2).	Faulty 2-Phase clock generator 1A1A2U30 (figure 6-6, sheet 2).
14	1A1A2U5-1, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39	Oscilloscope	Measure logic level.	Low logic level at all test points.	Faulty range counter 1A1A2U11, U12, U13, or ROM/XCVR U3.	Faulty RAM/XCVR/ CNTR 1A1A2U5.
15a	1A1A2U2-24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35	Oscilloscope or logic probe	Measure logic level.	Low logic level on 1A1A2U2-24, 25, 26, 27, 28, 29, 30, 31, 33, and 35. High logic level on 1A1A2U2-32, 34.	Proceed to step 15b.	Faulty ROM/XCVR 1A1A2U2.
15b	1A1A2U20-12	Oscilloscope	Measure logic level pulses.		Proceed to step 15c.	Faulty range and pulse width control 1A1A2U20.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
15c	1A1A2U23-6	Frequency Counter	Measure frequency.	13.500 to 16.343 MHz.	Faulty pulse width counter 1A1A2U14, U15, U16.	Faulty 2-phase clock generator 1A1A2U30, U23.
16	1A1A2U2-24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35	Oscilloscope or logic probe	Measure logic level.	High logic level on 1A1A2U2-24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34. Low logic level on 1A1A2U2-35.	Faulty pulse width counter 1A1A2U14, U15, or U16.	Faulty ROM/XCVR 1A1A2U2.
17a	1A1A2U23-6	Frequency Counter	Measure frequency.	15.6 to 18.5 MHz.	Proceed to step 17b.	Faulty 2-phase clock generator 1A1A2U30.
17b	1A1A2U2-24 through 35	Oscilloscope or logic probe	Measure logic level.	High logic level at all test points.	Faulty pulse width counter 1A1A2U14, U15, U16.	Faulty ROM/XCVR 1A1A2U2.
18a	1A1A2U22-9	Oscilloscope or logic probe	Measure logic level.	High logic level (no pulses).	Proceed to step 18b.	Faulty RAM/XCVR/CNTR 1A1A2U5.
18b	1A1A2U23-4	Oscilloscope or logic probe	Measure logic level.	Low logic level (no pulses).	Faulty CPU 1A1A2U1.	Faulty range interrupt generator 1A1A2U22, U23.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
19a	1A1A2U1-37	Frequency counter	Measure frequency.	1.99 to 2.01 MHz.	Proceed to step 19b.	Faulty CPU 1A1A2U1 or 4 MHz crystal X01.
19b	1A1A2U22-9	Frequency counter	Measure frequency.	0.995 to 1.005 MHz.	Proceed to step 19c.	Faulty RAM/XCVR/ CNTR 1A1A2U5.
19c	1A1A2U23-4	Frequency counter	Measure frequency.	30.15 to 30.45 Hz.	Faulty CPU 1A1A2U1.	Faulty range interrupt generator 1A1A2U22, U23.
20a	1A1A2U1-37	Frequency counter	Measure frequency.	1.99 to 2.01 MHz.	Proceed to step 20b.	Faulty CPU 1A1A2U2 or 4 MHz crystal X01.
20b	1A1A2U22-9	Frequency counter	Measure frequency.	3.10 to 3.14 KHz.	Proceed to step 20c.	Faulty RAM/XCVR/ CNTR 1A1A2U5.
20c	1A1A2U23-4	Frequency counter	Measure frequency.	103.6 to 104.7 Hz.	Faulty CPU 1A1A2U1.	Faulty range interrupt generator 1A1A2U22.
21a	1A1A2U25-6	Oscillo-scope or logic probe	Measure logic level.	Low level logic (no pulses).	Proceed to step 21b.	Proceed to step 21e.
21b	1A1A2U27-10	Oscillo-scope or logic probe	Measure logic level.	Low logic level (no pulses).	Faulty CPU 1A1A2U1.	Proceed to step 21c.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
21c	1A1A2U22-13	Oscillo-scope or logic probe	Measure logic level.	High logic level (no pulses).	Proceed to step 21d.	Faulty CNTR 1A1A2U22.
21d	-	-	Press E key on keyboard.	Test 151 passes.	Faulty frequency counter control logic 1A1A2U27.	Faulty CPU 1A1A2U1 or frequency counter control logic U29.
21e	1A1A2U3-36, 37, 38	Oscillo-scope or logic probe	Measure logic level.	Low logic level at all test points.	Faulty signal selector 1A1A2U25.	Faulty ROM/XCVR 1A1A2U3.
22a	1A1A2U28-3, 4, 5, 6, 8, 9, 10, 11	Oscillo-scope or logic probe	Measure logic level.	Low logic level at all test points (no pulses).	Faulty RAM/XCVR/ CNTR 1A1A2U5.	Proceed to step 22b.
22b	1A1A2U28-1	Oscillo-scope or logic probe	Measure logic level.	Low logic level (no pulses).	Faulty frequency counter 1A1A2U28.	Proceed to step 22c.
22c	-	-	Press E key on keyboard.	Test 152 passes.	Faulty frequency counter control logic 1A1A2U27, U26.	Proceed to step 22d.
22d	1A1A2U3-39	Oscillo-scope or logic probe	Measure logic level.	Low logic level.	Faulty frequency counter control logic 1A1A2U26, U27.	Faulty ROM/XCVR 1A1A2U3.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
23a	1A1A2U27-14	Oscilloscope or logic probe.	Measure logic level.	High logic level.	Proceed to step 23b.	Proceed to step 23e.
23b	1A1A2U26-8	Oscilloscope or logic probe	Measure logic level.	Low logic level (no pulses).	Proceed to step 23c.	Proceed to step 23d.
23c	1A1A2U27-10	Oscilloscope or logic probe .	Measure logic level.	High logic level.	Faulty CPU 1A1A2U1.	Faulty frequency counter control logic 1A1A2U27.
23d	1A1A2U22-15	Oscilloscope	Measure logic level pulses.	64 kHz logic level square wave.	Faulty frequency counter control logic 1A1A2U22.	Faulty clock generator 1A1A2U24.
23e	1A1A2U3-39	Oscilloscope or logic probe	Measure logic level.	Low logic level.	Faulty frequency counter control logic 1A1A2U27.	Faulty ROM/XCVR 1A1A2U3.
24	1A1A2U24-1	Frequency counter	Measure frequency.	16.22 to 16.53 MHz.	Faulty clock generator 1A1A2U24.	Faulty 2-phase clock generator 1A1A2U30.
25a	1A1A2U25-6	Oscilloscope or logic probe	Measure logic level pulses.	16.22 to 16.53 MHz	Proceed to step 25b.	Proceed to step 25c.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
25b	1A1A2U3-39	Oscilloscope or logic probe	Measure logic level.	Low logic level.	Faulty frequency counter control logic 1A1A2U27, frequency counter U28, or RAM/XCVR/CNTR U5 (figure 6-8, sheet 2).	Faulty ROM/XCVR 1A1A2U3.
25c	1A1A2U3-36, 37, 38	Oscilloscope or logic probe	Measure logic level.	High logic level on 1A1A2U3-36, 37. Low logic level on 1A1A2U3-38.	Faulty signal selector 1A1A2U25.	Faulty ROM/XCVR 1A1A2U3.
26a	1A1A2U25-6	Oscilloscope	Measure logic level pulses.	Logic level pulses with period of 20 to 50 ms.	Proceed to step 26b.	Proceed to step 26c.
26b	1A1A2U3-39	Oscilloscope	Measure logic level.	High logic level.	Faulty frequency counter control logic 1A1A2U26, U27.	Faulty ROM/XCVR 1A1A2U3.
26c	1A1A2U3, 36, 37, 38	Oscilloscope or logic probe	Measure logic level.	High logic level on 1A1A2U3-36. Low logic level on 1A1A2U3-37, 38.	Faulty signal selector 1A1A2U25.	Faulty ROM/XCVR 1A1A2U3.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
27a	1A1A3TP8	Oscilloscope or logic probe	Measure logic level.	High logic level.	Faulty Digital Assembly 1A1A2 (ROM/XCVR U2).	Faulty Microwave Interface 1A1A3. Proceed to step 27b.
27b	1A1A3TP17	Oscilloscope	Measure logic level pulses.	64 kHz logic level square wave.	Faulty 1 MHz filter 1A1A3L3, detector CR36, CR37, or switch Q18 (figure 6-4, sheet 3).	Proceed to step 27c.
27c	1A1A3U15-10	Oscilloscope or logic probe	Measure logic level.	High logic level.	Proceed to step 27d.	Faulty XCVR 1A1A3U1.
27d	1A1A3U15-8	Oscilloscope	Measure logic level pulses.	64 kHz logic level square wave.	Proceed to step 27e.	Faulty gate 1A1A3U15.
27e	1A1A3TP16	Oscilloscope	Measure signal.	64 kHz square wave greater than 0.5 vp-p.	Faulty comparator 1A1A3U22.	Faulty amplifier 1A1A3U21 or voltage divider R123, R124.
28a	1A1A2U25-6	Oscilloscope	Measure logic level pulses.	Logic level 2 to 3.5 MHz square wave.	Proceed to step 28b.	Proceed to step 28c.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
28b	1A1A3TP18	DVM	Measure dc voltage.	-10.5 to -12.5 vdc.	Perform AFC calibration procedures of table 5-26. If calibration cannot be performed, faulty Microwave Interface 1A1A3 (VR12) or faulty VCO/Prescaler 1A1A4A3.	Faulty Microwave Interface 1A1A3. Proceed to step 28e.
28c	1A1A2U23-13	Oscilloscope	Measure logic level pulses.	Logic level 2.5 to 3.5 MHz square wave.	Faulty Digital Assembly 1A1A2. Proceed to step 28d.	Faulty VCO/Prescaler 1A1A4A3 or faulty signal path between 1A1A4A3J2 and 1A1A2J2-2. Refer to figure 6-4, sheet 2.
28d	1A1A2U3-36, 37, 38	Oscilloscope or logic probe	Measure logic level.	High logic level on 1A1A2U3-37. Low logic level on 1A1A2U3-36, 38.	Faulty signal gelector 1A1A2U23, U25.	Faulty ROM/XCVR 1A1A2U3.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
28e	1A1A3U1-23, 24, 25	Oscilloscope or logic probe	Measure logic level.	High logic level at all test points.	Proceed to step 28f.	Faulty XCVR 1A1A3U1.
28f	1A1A3U16-10 and U20-8	Oscilloscope or logic probe	Measure logic level.	High logic level at 1A1A3U16-10. Low logic level at 1A1A3U20-8.	Faulty switch 1A1A3Q14, Q15 or summing amplifier U18 circuits. Refer to figure 6-4, sheet 3.	Faulty gate 1A1A3U16 or U20.
29a	1A1A3TP18	DVM	Measure dc voltage.	+10.5 to +12.5 vdc.	Perform AFC calibration procedures of table 5-26. If calibration cannot be performed, faulty Microwave Interface 1A1A3 (VR12) or VCO/ Prescaler 1A1A4A3.	Faulty Microwave Interface 1A1A3. Proceed to step 29b.
29b	1A1A3U1-25	Oscilloscope or logic probe	Measure logic level.	Low logic level.	Faulty gate 1A1A3U20 or switch Q15.	Faulty XCVR 1A1A3U1.
30a	1A1A3TP38 (FT MAX)	DVM	Measure dc voltage.	+5.87 to +10.16 vdc.	Proceed to step 30b.	Proceed to step 30c.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
30b	1A1A3U1-18, 19, 20	Oscilloscope or logic probe	Measure logic level.	High logic level on 1A1A3U1-18, 19. Low logic level on 1A1A3U1-20.	Faulty analog multiplexer (SIG 11) 1A1A3U6.	Faulty XCVR 1A1A3U1.
30c	1A1A3TP2	Oscilloscope	Measure ac signal.	64 kHz square wave greater than 5.0 vp-p.	Proceed to step 30d.	Proceed to step 30e.
30d	1A1A3TP3, TP4	Oscilloscope	Measure dc signal.	Greater than -4.0 vdc.	Faulty summing amplifier 1A1A3U14.	Faulty 500 kHz peak detector 1A1A3CR30, CR31, or 10 MHz peak detector CR28, CR29 (figure 6-13, sheet 4).
30e	1A1A3TP1	Oscilloscope	Measure ac signal.	64 kHz square wave greater than 50 mV p-p.	Faulty diff. amplifier 1A1A3U13.	Faulty diff. amplifier 1A1A3U12 or voltage divider R123, R124.
31a	1A1A3U1-10	Oscilloscope or logic probe	Measure logic level.	Low logic level.	Proceed to step 31b.	Faulty XCVR 1A1A3U1.
31b	1A1A3U15-8	Oscilloscope or logic probe	Measure logic level.	High logic level.	Proceed to step 31c.	Faulty gate 1A1A3U15.

Table 5-3. System Fault Isolation - Continued

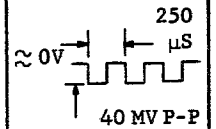
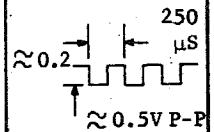
Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
31c	1A1A3TP3, TP4	Oscilloscope	Measure dc voltage.	Less than 0.5 vdc.	Faulty summing amplifier 1A1A3U14.	Faulty oscillating amplifier 1A1A3U12, U13 or leaky capacitors C34, C36.
32a	1A1A3TP39 (DET PWR)	DVM	Measure dc voltage.	Greater than 10.24 vdc.	Faulty Microwave Interface 1A1A3. Proceed to step 32b.	Proceed to step 32c.
32b	1A1A3U1-18, 19, 20	Oscilloscope or logic probe	Measure logic level.	High logic level on 1A1A3U1-20. Low logic level on 1A1A3U1-18, 19.	Faulty analog multiplexer (SIG 12) 1A1A3U6.	Faulty XCVR 1A1A3U1.
32c	1A1A3E10	Oscilloscope	Observe waveform.		Faulty Microwave Interface 1A1A3. Proceed to step 32p.	Proceed to step 32d.
32d	1A1A3E9	Oscilloscope	Observe waveform.		Proceed to step 32e.	Faulty Microwave Interface 1A1A3. Proceed to step 32o.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
32e	1A1A3E4	Oscillo-scope	Measure dc voltage.	Less than +0.3 vdc.	Proceed to step 32f.	Faulty Microwave Interface 1A1A3 (pin attenuator driver U24) or ATTENUATION DB FINE pot 1A1R1 (figure 6-7, sheet 3).
32f	1A1A3E5	Oscillo-scope	Measure dc voltage.	Greater than -1.0 vdc.	Proceed to step 32g.	Faulty Microwave Interface 1A1A3. Proceed to step 32n.
32g	1A1A3J13-1	Oscillo-scope	Disconnect 1A1A4P2 from 1A1A3J13. Measure dc voltage.	-14.75 to -15.25 vdc.	Proceed to step 32h.	Faulty Microwave Interface 1A1A3. Proceed to step 32m.
32h	1A1J2 (RF IN/OUT)	Power meter	Reconnect 1A1A4P2 to 1A1A3J2. Connect power meter to 1A1J2 (RF IN/OUT).	0 to -10 dbm.	Faulty Microwave Assembly 1A1A4 (coax switch S1 or rf detector A4).	Proceed to step 32i.
32i	1A1J2 (RF IN/OUT)	Power meter	Set ATTENUATION DB 0-80 switch to 0. Measure power at 1A1J2 (RF IN/OUT).	0 to +10 dbm.	Faulty Attenuator Assembly 1A1A8.	Proceed to step 32j.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
32j	1A1W2P1	Power meter	Disconnect 1A1W2P1 from 1A1A4A1J1. Connect power meter to 1A1W2P1.	Greater than +12 dbm.	Insure that all connectors are tight. If fault persists, replace modulator/mixer 1A1A4A1 or coupler module 1A1A4A2 in that order.	Faulty RF Oscillator 1A1A5 or cable 1A1W2. Proceed to step 32k.
32k	1A1A5Y1-A	DVM	Measure dc voltage.	Greater than 6.0 vdc.	Faulty Gunn Oscillator 1A1A5Y1.	Proceed to step 321.
321	1A1A5A1-E4, E5	DVM	Measure dc voltage.	Greater than 6.0 vdc.	Faulty filter (1A1A5FL1).	Faulty Gunn Oscillator Regulator 1A1A5A1 or voltage regulator 1A1A5U1.
32m	1A1A3U1-17	Oscilloscope or logic probe	Measure logic level.	Low logic level.	Faulty coaxial switch driver 1A1A3U32, Q5.	Faulty XCVR 1A1A3U1.
32n	1A1A3U1-11, 13	Oscilloscope or logic probe	Measure logic level.	High logic level at all test points.	Faulty target pin switch driver 1A1A3U15, Q1, Q2.	Faulty XCVR 1A1A3U1.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
32o	1A1A3U28-7	Oscilloscope	Observe waveform.	Logic level 4 kHz square wave.	Faulty chopper signal generator 1A1A3U16.	Proceed to step 32t.
32p	1A1A3TP19	Oscilloscope	Observe waveform.	4 kHz square wave greater than 0.9 vp-p.	Proceed to step 32q.	Faulty amplifier 1A1A3U25.
32q	1A1A3TP20	Oscilloscope	Measure dc voltage.	4.5 to 5.5 vdc.	Proceed to step 32r.	Faulty positive peak detector 1A1A3U26 or U27.
32r	1A1A3TP21	Oscilloscope	Observe waveform.	4 kHz square wave greater than 0.9 vp-p.	Proceed to step 32s.	Faulty amplifier 1A1A3U25.
32s	1A1A3TP22	Oscilloscope	Measure dc voltage.	4.5 to 5.5 vdc.	Faulty summing amplifier 1A1A3U31.	Faulty negative peak detector 1A1A3U29 or U30 or blanker 1A1A3Q3, Q4, Q24.
32t	1A1A3U28-11	Oscilloscope or logic probe	Measure logic level.	High logic level.	Faulty chopper signal generator 1A1A3U28.	Faulty XCVR 1A1A3U1.

Table 5-3. System Fault Isolation - Continued

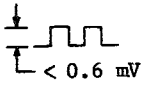
Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
33a	1A1A3TP39 DET PWR	DVM	Measure dc voltage.	0.0 to +1.5 vdc.	Faulty Microwave Interface 1A1A3 (analog multiplexer U6).	Proceed to step 33b.
33b	1A1A3E5	DVM	Measure dc voltage.	More positive than -0.3 vdc	Proceed to step 33f.	Proceed to step 33c.
33c	1A1A3U25-14	Oscillo-scope	Observe waveform.	 < 0.6 mV P-P	Faulty Microwave Interface 1A1A3 (power measurements circuits oscillating) (figure 6-13, sheet 5).	Proceed to step 33d.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
33d	1A1A3U4-2	DVM	Measure dc voltage.	+1.2 to +2.6 vdc	Proceed to step 33e.	Faulty reference generator 1A1A3U4.
33e	1A1A3U32-3	Oscilloscope or logic probe	Measure logic level.	Low logic level.	Faulty power reference generator 1A1A3U16, U20, U24, Q19.	Faulty XCVR 1A1A3U1.
33f	1A1A3U1-13	Oscilloscope or logic probe	Measure logic level.	Low logic level.	Proceed to step 32g.	Faulty Microwave Interface 1A1A3 (XCVR U1).
33g	1A1A3E5	DVM	Measure dc voltage.	More positive than -1.2 vdc.	Faulty Microwave Interface 1A1A3 (target pin switch driver Q1, Q2) (figure 6-13, sheet 2).	Faulty Modulator/ Mixer 1A1A4A1.
34	1A1A3U1-15	Oscilloscope or logic probe	Measure logic level.	High logic level.	Faulty power reference generator 1A1A3U32, U24, Q19.	Faulty XCVR 1A1A3U1.
35	1A1A3U1-12	Oscilloscope or logic probe	Measure logic level.	High logic level.	Faulty target pin switch driver 1A1A3U15.	Faulty XCVR 1A1A3U1.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
36a	1A1A3U1-17	Oscilloscope or logic probe	Measure logic level.	High logic level.	Proceed to step 36b.	Faulty Microwave Interface 1A1A3 (XCVR U1).
36b	1A1A3J13-1	DVM	Measure dc voltage.	+10.0 to +13.0 vdc	Faulty Coaxial Switch 1A1A4S1.	If voltage is greater than +13.0 vdc, faulty coaxial switch 1A1A4S1. If voltage is less than +10.0 vdc, faulty Microwave Interface 1A1A3 (coax switch driver U32, Q5).
37	1A1S2-2 1A1S2-5	DVM	**WARNING** 115 vac present on switch 1A1S2. Measure ac voltage between 1A1S2-2 and -5.	Greater than 100 vrms.	Faulty Illuminated Panel 1A1A7.	Faulty PNL ON-OFF switch 1A1S2.
38	1A1A1U2-17	Oscilloscope or logic probe	Measure logic level.	Low logic level.	Faulty Front Panel Interface 1A1A1 (display logic) (figure 6-11, sheet 3).	Faulty Front Panel Interface 1A1A1 (XCVR U2).

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
39a	1A1A1U2-22, 23, 24, 25	Oscilloscope or logic probe	Measure logic level.	High logic level at 1A1A1U2-22, 23. Low logic level at 1A1A1U2-24, 25.	Proceed to step 39b.	Faulty MODE switch 1A1S5.
39b	1A1A1U2-18, 19, 20, 21	Oscilloscope or logic probe	Measure logic level.	High logic level on 1A1A1U2-18, 19, 20. Low logic level on 1A1A1U2-21.	Faulty Front Panel Interface 1A1A1 (XCVR U2).	Faulty DISPLAY SELECT switch 1A1S6.
40	1A1A1U2-18, 19, 20, 21	Oscilloscope or logic probe	Measure logic level.	High logic level on 1A1A1U2-19, 20. Low logic level on 1A1A1U2-18, 21.	Faulty Front Panel Interface 1A1A1 (XCVR U2).	Faulty DISPLAY SELECT switch 1A1S6.
41	1A1A1U2-18, 19, 20, 21.	Oscilloscope or logic level	Measure logic level.	High logic level on 1A1A1U2-18, 20. Low logic level on 1A1A1U2-19, 21.	Faulty Front Panel Interface 1A1A1 (XCVR U2).	Faulty DISPLAY SELECT switch 1A1S6.
42	1A1A1U2-18, 19, 20, 21	Oscilloscope or logic probe	Measure logic level.	High logic level on 1A1A1U2-18, 19.	Faulty Front Panel Interface 1A1A1 (XCVR U2).	Faulty DISPLAY SELECT switch 1A1S6.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
42 Cont				Low logic level on 1A1A1-20, 21.		
43a	1A1A3E4	DVM	Disconnect 1A1A3P5 from 1A1A4A1J4. Observe voltage change at 1A1A3E4 as ATTENUATION DB FINE pot is turned from fully cw to fully ccw position.	Voltage goes from less than 0.5 to greater than 14.0 vdc.	Proceed to step 43b.	Proceed to step 43f.
43b	1A1A3E6	DVM	Reconnect 1A1A3P5 to 1A1A4A1J4. Disconnect 1A1A3P4 from 1A1A4A2J6. Measure dc voltage.	+3.6 to +4.0 vdc.	Proceed to step 43c.	Faulty Microwave Interface 1A1A3. Proceed to step 43e.
43c	-	-	Reconnect 1A1A3P4 to 1A1A4A2J6. Turn ATTENUATION DB FINE pot fully ccw. Turn MAX ATTEN pot 1A1A3VR14 fully cw. Observe digital display.	Minus sign present on left side of display.	Perform power measurement calibration procedure of table 5-29.	Proceed to step 43d.
43d	-	-	Disconnect 1A1A4W2 from 1A1A4A1J3. Observe digital display.	Minus sign present on left side of display.	Faulty Coupler Module 1A1A4A2. Perform calibration procedure of table 5-29.	Faulty Modulator/ Mixer 1A1A4A1. Perform calibration procedure of table 5-29.
43e	1A1A3U1-16	Oscillo-scope or logic probe	Measure logic level.	Low logic level.	Faulty isolation pin switch driver 1A1A3Q6.	Faulty XCVR 1A1A3U1.

Table 5-3. System Fault Isolation - Continued

<table>
<tr><th>Step</th><th>Test point</th><th>Test equipment</th><th>Settings and instructions</th><th>Correct indication</th><th>If correct</th><th>If incorrect</th></tr>
<tr><td>43f</td><td>1A1R1-2, -3</td><td>Multimeter</td><td>Disconnect 1A1P2 from 1A1A3J25.

Measure resistance between 1A1R1-2 and -3 while rotating ATTENUATION DB FINE pot 1A1R1 from fully cw to fully ccw.</td><td>Resistance increases smoothly from 0 to 10 kilohms +10%.</td><td>Faulty Microwave Interface 1A1A3 (attenuator driver U24).</td><td>Faulty ATTENUATION DB FINE pot 1A1R1.</td></tr>
<tr><td>44a</td><td>1A1A3TP28 thru TP35</td><td>DVM</td><td>Set ATTENUATION DB 0-80 switch to faulty position.

Find the row corresponding to faulty position in the following table:
<table><tr><th>ATTEN. position</th><th>1A1A3 test point</th></tr><tr><td>10</td><td>TP28 10 DB</td></tr><tr><td>20</td><td>TP29 20 DB</td></tr><tr><td>30</td><td>TP30 30 DB</td></tr><tr><td>40</td><td>TP31 40 DB</td></tr><tr><td>50</td><td>TP32 50 DB</td></tr><tr><td>60</td><td>TP33 60 DB</td></tr><tr><td>70</td><td>TP34 70 DB</td></tr><tr><td>80</td><td>TP35 80 DB</td></tr></table>Observe dc voltage at designated test point.</td><td>+0.4 to +5.0 vdc</td><td>Faulty Microwave Interface 1A1A3. Proceed to step 44b.</td><td>Proceed to step 44c.</td></tr>
<tr><td>44b</td><td>1A1A3U1-18, 19, 20</td><td>Oscillo-scope or logic probe</td><td>Find the row corresponding to the faulty position in the following table:
<table><tr><th rowspan="2">ATTEN. position</th><th colspan="3">Select bits 1A1A3U1 pins</th></tr><tr><th>20</th><th>19</th><th>18</th></tr><tr><td>10</td><td>L</td><td>L</td><td>H</td></tr><tr><td>20</td><td>L</td><td>H</td><td>L</td></tr><tr><td>30</td><td>L</td><td>H</td><td>H</td></tr><tr><td>40</td><td>H</td><td>L</td><td>L</td></tr><tr><td>50</td><td>H</td><td>L</td><td>H</td></tr><tr><td>60</td><td>H</td><td>H</td><td>L</td></tr><tr><td>70</td><td>H</td><td>H</td><td>H</td></tr><tr><td>80</td><td>L</td><td>L</td><td>L</td></tr></table>Measure logic level at 1A1A3U1-18, 19, 20.</td><td>Correct logic levels.</td><td>Faulty analog multi-plexer (figure 6-13, sheets 6, 7).</td><td>Faulty XCVR 1A1A3U1.</td></tr>
</table>

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
44c	1A1A3J3-1 thru 8	DVM	Find the row corresponding to the faulty position in the following table: ATTEN. position / 1A1A3J3 pin / 1A1A3 pot 10 / 1 / VR3 10 DB 20 / 2 / VR4 20 DB 30 / 3 / VR5 30 DB 40 / 4 / VR6 40 DB 50 / 5 / VR7 50 DB 60 / 6 / VR8 60 DB 70 / 7 / VR9 70 DB 80 / 8 / VR10 80 DB Observe dc voltage at designated pin.	+4.5 to +5.5 vdc	Faulty potentiometer listed in third column of table.	Faulty Attenuator Assembly 1A1A8.
45a	1A1A1U2-18, 19, 20, 21	Oscilloscope or logic probe	Measure logic levels.	Low logic level at 1A1A1U2-18, 20, 21. High logic level at 1A1A1U2-19.	Proceed to step 45b.	Faulty DISPLAY SELECT switch 1A1S6.
45b	1A1A1U2-22, 23, 24, 25	Oscilloscope or logic probe	Measure logic levels.	High logic level at 1A1A1U2-22, 23. Low logic level at 1A1A1U2-24, 25.	Faulty Front Panel Interface 1A1A1 (XCVR U2).	Faulty MODE switch 1A1S5.
46	1A1A1U2-18, 19, 20, 21	Oscilloscope or logic probe	Measure logic levels.	High logic level at 1A1A1U2-18. Low logic level at	Proceed to step 45b.	Faulty DISPLAY SELECT switch 1A1S6.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
46 Cont				1A1A1U2-19, 20, 21.		
47a	1A1A3TP51	DVM	Slowly rotate FREQ 8.4 TO 10.0 GHZ COARSE control 10 full turns clockwise while observing dc voltage at 1A1A3TP51.	Stays at null.	Proceed to step 47b.	Proceed to step 47c.
47b	1A1A3TP37 C FREQ	DVM	Slowly rotate FREQ 8.4 TO 10.0 GHZ COARSE control 10 full turns clockwise while observing dc voltage at 1A1A3TP37.	Voltage varies smoothly over a range from less than +1.2 vdc to greater than +9.0 vdc as COARSE control is rotated.	Faulty Microwave Interface 1A1A3 (analog switch U6).	Perform coarse frequency calibration. If calibration cannot be performed, faulty Microwave Interface 1A1A3 (CFREQ pot VR1), or faulty RF Oscillator 1A1A5 (pot R1).
47c	1A1A3E7, E17 (rtn)	Oscilloscope	Disconnect 1A1A3P7 from 1A1A4A3J3. Slowly turn FREQ 8.4 TO 10.0 GHZ COARSE control until a maximum signal level (greater than 10 mV p-p) signal is observed at 1A1A3E7.	Maximum signal is greater than 40 mV p-p.	Faulty Microwave Interface 1A1A3. Proceed to step 47d.	Proceed to step 47f.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
47d	1A1A3TP8	Oscilloscope or logic probe	Measure logic level.	High logic level.	Proceed to step 47e.	Faulty AFC circuits 1A1A3U21, C51.
47e	1A1A3TP9	DVM	Turn FREQ 8.4 TO 10.0 GHZ COARSE control while observing voltage at 1A1A3TP9.	Stays at null.	Faulty AFC Circuits Integrator 1A1A3U8, High Limit Ref, Low Limit Ref, or Sweep Reset Switch (figure 6-sheet 3).	Faulty Discriminator (1A1A3U17, CR32, CR33).
47f	1A1A4A3J1	Power meter and thermistor mount	Disconnect 1A1A4W1 from 1A1A4A3J1. Connect power meter and thermistor mount to 1A1A4A3J1.	Greater than +6 dbm.	Faulty Modulator/ Mixer 1A1A4A1 or Gunn Oscillator frequency does not change; check mechanical linkage in RF Oscillator 1A1A5.	Faulty VCO/ Prescaler 1A1A4A3.
48	-	-	Observe frequency display.	Greater than 8400.0 and less than 10100.0.	Faulty RF Oscillator 1A1A5. Check mechanical linkage.	Faulty DISPLAY SELECT switch 1A1S6.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
49	1A1J2 (RF IN/OUT)	Frequency counter with x-band plug-in	Using RF Cable W2, connect frequency counter to 1A1J2 (RF IN/OUT). Adjust FREQ 8.4 TO 10.0 GHZ COARSE control for frequency less than 8400 MHz.	Adjusts to less than 8400 MHz.	Perform coarse frequency calibration. If calibration of table 5-27. If calibration cannot be performed, faulty Microwave Interface 1A1A3 (CFREQ pot R1) or faulty RF Oscillator 1A1A5 (COARSE pot R1).	Faulty RF Oscillator 1A1A5.
50a	1A1A3E1 1A1A3E2 (rtn)	DVM	While observing dc voltage at 1A1A3E1, slowly turn FREQ 8.4 TO 10.0 GHZ FINE pot from fully ccw to fully cw position.	Voltage varies by more than 0.9 vdc.	Proceed to step 50d.	Proceed to step 50b.
50b	1A1A1U11-6	DVM	While observing dc voltage at 1A1A1U11-6, slowly turn FREQ 8.4 TO 10.0 GHZ FINE pot from fully ccw to fully cw position.	Voltage varies by more than 0.9 vdc.	Faulty FM HOLD HIGH-MOD-HOLD LOW switch 1A1S7.	Proceed to step 50c.
50c	1A1R5-2	DVM	While observing dc voltage at 1A1R5-2, turn the FREQ 8.4 TO 10.0 GHZ FINE pot from fully ccw to fully cw position.	Voltage varies from more negative than -14.0 vdc to greater than +14.0 vdc.	Faulty Front Panel Interface 1A1A1 (linearizer U11).	Faulty FREQ 8.4 TO 10.0 GHZ FINE pot 1A1R5.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
50d	1A1A3E13 1A1A3E23 (rtn)	DVM	While observing dc voltage at 1A1A3E13, turn the FREQ 8.4 TO 10.0 GHZ FINE pot from fully ccw to fully cw position.	Voltage varies by more than 0.9 vdc.	Faulty RF Oscillator 1A1A5 (Gunn Oscillator 1A1A5Y1).	Faulty Microwave Interface 1A1A3 (filter R109, C102).
51a	-	Frequency counter and x-band plug-in	Set MODE switch to SIG GEN CW. Turn FREQ 8.4 TO 10.0 GHZ FINE pot fully cw. Turn ATTENUATION DB FINE pot fully cw. Using RF Cable W2, connect frequency counter to RF IN/OUT connector J2. Adjust FREQ 8.4 TO 10.0 GHZ COARSE control for maximum frequency display on frequency counter.	Frequency display is greater than 10,100 MHz.	Faulty Microwave Interface 1A1A3 (XCVR U1, high limit referencet Q10, Q11, or low limit reference Q12, Q13).	Proceed to step 51b.
51b	1A1A3E13 1A1A3E23 (rtn)	DVM	Measure dc voltage.	Greater than 0 vdc.	Faulty RF Oscillator 1A1A5. Proceed to step 51c.	Faulty Front Panel Interface 1A1A1 (linearizer U11).
51c	-	-	Inspect RF Oscillator gear and cam assembly as FREQ 8.4 TO 10.0 GHZ COARSE control is turned.	No slippage or binding of gear and cam assembly.	Proceed to step 51d.	Replace RF Oscillator 1A1A5.
51d	1A1A5A1E5 1A1A5A1E4 (rtn)	DVM	Measure dc voltage between 1A1A5A1E5 (+) and 1A1A5A1E4 (rtn).	Voltage is equal to the bias voltage marked on Gunn Oscillator 1A1A5Y1.	Perform Gunn tuning range calibration of table 5-23. If calibration cannot be performed, replace Gunn	Adjust or repair Gunn Oscillator Regulator 1A1A5A1 or voltage regulator 1A1A5U1.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
51d Cont					Oscillator 1A1A5Y1.	
52a	-	-	Set TRIGGER switch to RF. While observing display, turn the PRF pot.	Display changes as PRF is turned.	Proceed to step 52b.	Proceed to step 52c.
52b	1A1A1U18-4	Oscilloscope or logic probe	Measure logic level.	Low logic level.	Faulty Front Panel Interface 1A1A1 (trigger select circuit U18).	Faulty TRIGGER switch 1A1S3.
52c	1A1A1U2-22, 23, 24, 25	Oscilloscope or logic probe	Measure logic level at all test points.	High logic level on 1A1A1U2-22. Low logic level on 1A1A1U2-23, 24, 25.	Faulty Front Panel Interface 1A1A1 (XCVR U2).	Faulty MODE switch 1A1S5.
53	1A1A1U2-22, 23, 24, 25	Oscillo-scope or logic probe	Measure logic level at all test points.	Low logic level at all test points.	Faulty Front Panel Interface 1A1A1 (XCVR U2).	Faulty MODE switch 1A1S5.
54a	1A1A1U2-22, 23, 24, 25	Oscillo-scope or logic probe	Measure logic level at all test points.	Low logic level at all test points.	Proceed to step 54b.	Faulty MODE switch 1A1S5.
54b	1A1A1U2-18, 19, 20, 21	Oscillo-scope or logic probe	Measure logic level at all test points.	High logic level at 1A1A1U2-18. Low logic level at 1A1A1U2-19, 20, 21.	Faulty Front Panel Interface 1A1A1 (XCVR U1).	Faulty DISPLAY SELECT switch 1A1S6.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
55	1A1A2U2-36	DVM	Measure dc voltage.	+4.7 to +5.3 vdc	Faulty MODE switch 1A1S5.	Faulty FM HOLD HIGH-MOD-HOLD LOW switch 1A1S7.
56a	1A1A2U2-37	Oscilloscope or logic probe	Measure logic level.	High logic level (no pulses).	Faulty Digital Assembly 1A1A2 (ROM/XCVR U2).	Proceed to step 56b.
56b	1A1A1TP5	Oscilloscope or logic probe	Ground 1A1A1TP3. Measure logic level at 1A1A1TP5.	High logic level.	Proceed to step 56c.	Proceed to step 56d.
56c	-	-	Remove ground from 1A1A1TP3. Short 1A1R3-1 to 1A1R3-3. Observe digital display.	Display is blank.	Faulty FM RATE pot 1A1R3.	Faulty Front Panel Interface 1A1A1 (ramp generator R1 open).
56d	1A1A1U14-3	Oscilloscope or logic probe	Ground 1A1A1TP3. Measure dc voltage at 1A1A1U14-3.	Less than +13.5 vdc	Proceed to step 56e.	Faulty Front Panel Interface 1A1A1 (resistor R1 open).
56e	1A1A1U11-3	DVM	Ground 1A1A1TP3. Measure dc voltage at 1A1A1U11-3.	Greater than +13.5 vdc.	Faulty Front Panel Interface 1A1A1. Proceed to step 56f.	Proceed to step 56g.
56f	1A1A1U10-2	DVM	Ground 1A1A1TP3. Measure dc voltage at 1A1A1U10-2.	Greater than +13.5 vdc	Faulty ramp generator 1A1A1U10, U14.	Faulty linearizer 1A1A1U11.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
56g	1A1S5-6	DVM	Ground 1A1A1TP3. Measure dc voltage at 1A1S5-6.	Greater than +13.5 vdc	Faulty MODE switch 1A1S5.	Proceed to step 56h.
56h	1A1S5-6	DVM	Ground 1A1A1TP3. Short 1A1R3-1 to 1A1R3-3. Measure dc voltage at 1A1S5-6.	Greater than +13.5 vdc	Faulty FM RATE pot 1A1R3.	Faulty Front Panel Interface 1A1A1 (ramp generator Q1, C22, R58).
57a	1A1A2U2-37	Oscilloscope or logic probe	Measure logic level.	Low logic level (no pulses).	Faulty Digital Assembly 1A1A2 (ROM/XCVR U2).	Proceed to step 57b.
57b	-	-	Ground 1A1A1TP5. Observe digital display indication.	Digital display indicates ␣103.	Proceed to step 57c.	Faulty Front Panel Interface 1A1A1 (ramp generator U16, U17).
57c	1A1A1U14-3	DVM	Measure dc voltage.	Greater than +12.0 vdc.	Proceed to step 57d.	Proceed to step 57e.
57d	1A1R3-1 1A1R3-3	Multimeter	Remove ground from 1A1A1TP5. Set PWR ON-OFF switch to OFF. Disconnect 1A1P10 from 1A1A1J10. Measure resistance between 1A1R3-1 and -3.	220 to 280 kilohms.	Faulty Front Panel Interface 1A1A1 (ramp generator Q1, C22, U10, U14).	Faulty FM RATE pot 1A1R3.
57e	1A1R4-3	DVM	Measure dc voltage.	Greater than +12 vdc.	Faulty FM DEVN pot 1A1R4.	Faulty Front Panel Interface 1A1A1 (resistor R46).

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
58	1A1R3-1 1A1R3-3	Multimeter	Set PWR ON-OFF switch to OFF. Disconnect 1A1P10 from 1A1A1J10. Measure resistance between 1A1R3-1 and -3.	220 to 280 kilohms.	Faulty Front Panel Interface 1A1A1 (ramp generator R58, C22).	Faulty FM RATE pot 1A1R3.
59a	1A1A1U14-6	DVM	Measure dc voltage.	Greater than +12.9 vdc.	Proceed to step 59b.	Proceed to step 59c.
59b	1A1S7-8	DVM	Measure dc voltage.	Greater than +12.9 vdc.	Faulty RF Oscillator 1A1A5.	Faulty FM HOLD HIGH-MOD-HOLD LOW switch 1A1S7.
59c	1A1A1U14-3	DVM	Measure dc voltage.	Greater than +12.9 vdc.	Faulty Front Panel Interface 1A1A1 (ramp generator U14).	Proceed to step 59d.
59d	1A1R4-3	DVM	Measure dc voltage.	Greater than +12.9 vdc.	Faulty FM DEVN pot 1A1R4.	Proceed to step 59e.
59e	1A1R4-1 1A1R4-3	Multimeter	Set PWR ON-OFF switch to OFF. Disconnect 1A1P10 from 1A1A1J10. Measure resistance between 1A1R4-1 and -3.	8.5 to 11.5 kilohms.	Faulty Front Panel Interface 1A1A1 (resistor R46 or R59).	Faulty FM DEVN pot 1A1R4.
60a	1A1A1U14-3	DVM	Measure dc voltage. Record voltage.	Less than +3.0 vdc.	Faulty Front Panel Interface 1A1A1. Proceed to step 60b.	Proceed to step 60c.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
60b	1A1A1U11-6	DVM	Measure dc voltage.	Voltage greater than voltage recorded in step 60a.	Faulty voltage follower 1A1A1U14.	Faulty linearizer 1A1A1U11.
60c	1A1R4-1	DVM	Measure dc voltage.	Less than +3.0 vdc.	Faulty FM DEVN pot 1A1R4.	Proceed to step 60d.
60d	1A1R4-1 1A1R4-3	Multimeter	Set PWR ON-OFF switch to OFF. Disconnect 1A1P10 from 1A1A1J10. Measure resistance between 1A1R4-1 and -3.	8.5 to 11.5 kilohms.	Faulty Front Panel Interface 1A1A1 (resistors R46, R59).	Faulty FM DEVN pot 1A1R4.
61	-	-	Set MODE switch to SIG GEN FM EXT. Set DISPLAY SELECT switch to RF SIG PWR (DBM). Observe display.	Display is blank.	Faulty Front Panel Interface 1A1A1 (limiter D12).	Faulty MODE switch 1A1S5.
62a	-	-	Perform RF in power calibration procedure of table 5-29.	Calibration performed correctly.	Proceed to step 62b.	Check path from 1A1J2 (RF IN/OUT) to J1 of Coupler Module 1A1A4A2. Refer to fig. 6-7, sheet 1.
62b	-	-	Perform signal power offset calibration procedure of table 5-29.	Calibration performed correctly.	Perform RF power offset calibration procedure of table 5-29.	Faulty Microwave Interface 1A1A3. Proceed to step 62c.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
62c	1A1A3TP42 (SIG PWR)	DVM	Observe dc voltage at 1A1A3TP42 (SIG PWR) and turn pot 1A1A3VR19 (SIG PWR) from fully ccw to fully cw position.	Voltage varies smoothly from less than 0 to greater than +4.75 vdc.	Faulty analog switch 1A1A1U6.	Faulty SIG PWR pot 1A1A3VR19.
63a	1A1J2 (RF IN/OUT)	Power meter and thermistor mount	Same settings as step 35 of table 5-1. Observe power meter indication.	-7.5 to -12.5 dbm.	Proceed to step 63b.	Faulty Attenuator Assembly 1A1A8 (step attenuator AT1).
63b	1A1J2 (RF IN/OUT)	Same as above.	Same settings as step 35 of table 5-1. Adjust pot 1A1A3VR3 (10 DB) until digital display indication is the same as the power meter indication.	Adjustment can be accom-plished.	Perform attenuator calibration procedure for 10 DB switch position (table 5-30).	Faulty Microwave Interface 1A1A3 (10 DB pot VR3).
64a	1A1J2 (RF IN/OUT)	Power meter and thermistor mount	Same settings as step 36 of table 5-1. Observe power meter indication	-17.5 to -22.5 dbm.	Proceed to step 64b.	Faulty Attenuator Assembly 1A1A8 (step attenuator AT1).
64b	1A1J2 (RF IN/OUT)	Same as above.	Same settings as step 36 of table 5-1. Adjust pot 1A1A3VR4 (20 DB) until digital display indication is the same as the power meter indication.	Adjustment can be accom-plished.	Perform attenuator calibration procedure for 20 DB switch position (table 5-30).	Faulty Microwave Interface 1A1A3 (20 DB pot VR4).

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
65a	1A1J2 (RF IN/OUT)	Power meter and thermistor mount	Same settings as step 37 of table 5-1. Observe power meter reading.	-27.5 to -32.5 dbm.	Proceed to step 65b.	Faulty Attenuator Assembly 1A1A8 (step attenuator 1A1A8AT1).
65b	1A1J2 (RF IN/OUT)	Same as above.	Same settings as step 37 of table 5-1. Adjust pot 1A1A3VR5 (30 DB) until digital display indication is the same as the power meter indication.	Adjustment can be accomplished.	Perform attenuator calibration procedure for 30 DB switch position (table 5-30).	Faulty Microwave Interface 1A1A3 (30 DB pot VR5).
66	1A1A2U23-6	Frequency counter	Measure frequency.	16.341 to 16.343 MHz.	Faulty Microwave Interface 1A1A3 (discriminator circuits C44, C45, CR32, CR33, R180, R181).	Faulty Digital Assembly 1A1A2 (2-phase clock generator U30).
67	1A1S4-3	Oscilloscope	Observe waveform.	+10.0V TO +14.0V -0.5V TO +0.5V	Faulty TRIG OUT switch 1A1S4.	Faulty Front Panel Interface 1A1A1 (output trigger buffer U19, Q3, Q5).
68	1A1S4-1	Oscilloscope	Observe waveform.	+0.5V TO -0.5V -10.0V TO -14.0V	Faulty TRIG OUT switch 1A1S4.	Faulty Front Panel Interface 1A1A1 (output

Table 5-3. System Fault Isolation - Continued

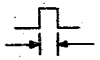
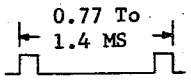
Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
68 Cont						trigger buffer Q4, Q6).
69	1A1A3U15-1	Oscilloscope	Observe logic level pulse.	 0.9 To 1.1 µS	Faulty Microwave Interface 1A1A3 (target pin switch driver U15).	Faulty Digital Assembly 1A1A2 (latch U17 or range counter U11).
70	1A1A1U18-9	Oscilloscope or logic probe	Measure logic level.	High logic level.	Faulty Front Panel Interface 1A1A1 (trigger select U18).	Faulty TRIGGER switch 1A1S3.
71	1A1A1U18-12	Oscilloscope or logic probe	Measure logic level.	High logic level.	Faulty Front Panel Interface 1A1A1 (trigger select U18, U19).	Faulty TRIGGER switch 1A1S3.
72a	1A1A1U18-1	Oscilloscope or logic probe	Measure logic level.	High logic level.	Proceed to step 72b.	Faulty TRIGGER switch 1A1S3.
72b	1A1A1TP7	Oscilloscope	Observe logic level waveform.	 0.77 To 1.4 MS	Faulty Front Panel Interface 1A1A1 (trigger select U18).	Proceed to step 72c.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
72c	1A1A1U19-6	Oscilloscope or logic probe	Measure logic level.	High logic level.	Faulty Detector 1A1A6 or faulty Front Panel Interface 1A1A1 (rf trigger U12, U13).	Faulty Front Panel Interface 1A1A1 (rf trigger U19).
73	1A1A3J13-1	DVM	Measure dc voltage.	Voltage more positive than +12 vdc.	Faulty Coaxial Switch 1A1A4S1 or faulty Coupler Module 1A1A4A2.	Faulty Microwave Interface 1A1A3 (coax switch driver U32, Q5).
74a	-	-	Same settings as step 48 of table 5-1. Adjust RF PWR pot 1A1A3VR18 for digital display indication of +bb20.0 dbm (b = blank).	1A1A3VR18 can be adjusted for digital display indication of +bb20.0 dbm.	Perform rf in power calibration procedure of table 5-29.	Proceed to step 74b.
74b	1A1A3 (RF PWR)	DVM or oscilloscope	Observe voltage at test point 1A1A3 RF PWR as RF PWR pot 1A1A3VR18 is adjusted from fully ccw to fully cw.	Voltage at 1A1A3TP41 varies smoothly from 0 to greater than +4.75 vdc as 1A1A3VR18 is adjusted.	Faulty analog multiplexer 1A1A3U6.	Faulty RF PWR pot 1A1A3VR18.

Table 5-3. System Fault Isolation - Continued

Step	Test point	Test equipment	Settings and instructions	Correct indication	If correct	If incorrect
75a	1A1A3E6	DVM	Disconnect 1A1A3P4 from 1A1A4A2J6. Measure dc voltage.	-1.0 vdc.	Faulty Coupler Module 1A1A4A2 or Modulator/ Mixer 1A1A4A1.	Faulty Microwave Interface 1A1A3. Proceed to step 75b.
75b	1A1A3U1-16	Oscillo-scope or logic probe	Measure logic level.	High logic level.	Faulty isolation pin switch driver 1A1A3Q6.	Faulty XCVR 1A1A3U1.

5-6. REPAIR. Repair procedures for the Test Set consist of disassembly, cleaning, inspection, repair, and assembly of the Test Set. Figures 5-4 through 5-9 are provided for aid in disassembly and assembly.

WARNING

Prior to disassembly, cleaning, inspection, repair, or assembly, insure that power to the Test Set is disconnected.

CAUTION

Exercise extreme care when connecting or disconnecting coaxial cables to avoid damaging connectors.

a. Disassembly. Disassembly consists of removal of Electronics Assembly 1A1, printed circuit cards (1A1A1, 1A1A2, and 1A1A3), Microwave Assembly 1A1A4 and components, RF Oscillator 1A1A5 and components, Detector 1A1A6, Illuminated Panel 1A1A7, Attenuator Assembly 1A1A8 and components, and Power Supply 1A1PS1.

(1) Removal of Test Set Electronics Assembly 1A1 (Figure 5-4). The procedure for removing Electronics Assembly 1A1 is provided in table 5-4.

(2) Removal of Printed Circuit Cards (1A1A1, 1A1A2, and 1A1A3) (Figure 5-5). The procedures for removal of printed circuit cards are provided in table 5-5 for Front Panel Interface 1A1A1, in table 5-6 for Digital Assembly 1A1A2, and in table 5-7 for Microwave Interface 1A1A3.

(3) Removal of Microwave Assembly 1A1A4. The procedure for removing Microwave Assembly 1A1A4 is provided in table 5-8.

(4) Removal of Microwave Assembly 1A1A4 Components. The procedures for removing the components of Microwave Assembly 1A1A4 are provided in tables 5-9 through 5-13.

(5) Removal of RF Oscillator 1A1A5 (Figure 5-6). The procedure for removing RF Oscillator 1A1A5 is provided in table 5-14.

(6) Removal of RF Oscillator 1A1A5 Components. The procedures for removing the components of RF Oscillator 1A1A5 are provided in table 5-15.

(7) Removal of Detector 1A1A6. The procedure for removing Detector 1A1A6 is provided in table 5-16.

(8) Removal of Illuminated Panel 1A1A7. The procedure for removing Illuminated Panel 1A1A7 is provided in table 5-17.

(9) Removal of Attenuator Assembly 1A1A8. The procedure for removing Attenuator Assembly 1A1A8 is provided in table 5-18.

(10) Removal of Attenuator Assembly 1A1A8 Components. The procedures for removing the components of Attenuator Assembly 1A1A8 are provided in table 5-19.

(11) Removal of Power Supply 1A1PS1. The procedure for removing Power Supply 1A1PS1 is provided in table 5-20.

b. Cleaning. Cleaning procedures consist of the cleaning of coaxial connectors. Coaxial connectors must be clean and free of metallic chips and other foreign particles. To clean the coaxial connectors, use MS-180 Freon TF Degreaser and a stiff, short bristle brush.

c. Inspection. Inspection consists of inspection of the printed circuit card assemblies and coaxial cables and connectors.

(1) Printed Circuit Card Assemblies. Inspect printed circuit cards for cuts in tracks and loose or damaged components.

(2) Coaxial Cables and Connectors. Inspect coaxial cables for insulation cracks or breaks. Inspect coaxial cable connectors for breaks or cracks and pin alinement. The female connector center pin should be concentric and positioned in the longitudinal plane. The male center pin should be concentric and have a well-formed point.

CAUTION

Coaxial connector mating should be performed with extreme care. Connectors must be axially alined when joined together. Excessive force applied when mating connectors will cause damage to the female connector. Connectors should be tightened to a 8 $\pm$0.5 inch-pound torque, using a torque wrench.

d. Repair or Replacement. Repair or replacement procedures contain repair procedures to be followed after a fault is isolated to a subassembly. Repair procedures are provided for printed circuit cards, microwave signal cables, and ribbon cables. Figures 5-7 through 5-9 are provided for aid in identifying subassemblies and component locations.

WARNING

Prior to performing any repair or replacement procedure, insure that power to the Test Set is disconnected.

(1) Printed Circuit Card Components. Refer to disassembly procedures of paragraph 5-6a to gain access to the printed circuit card. When components are being replaced, good soldering techniques should be used. Refer to the instruction manual for the benchtop repair center (listed in table 2-1) for proper repair procedures.

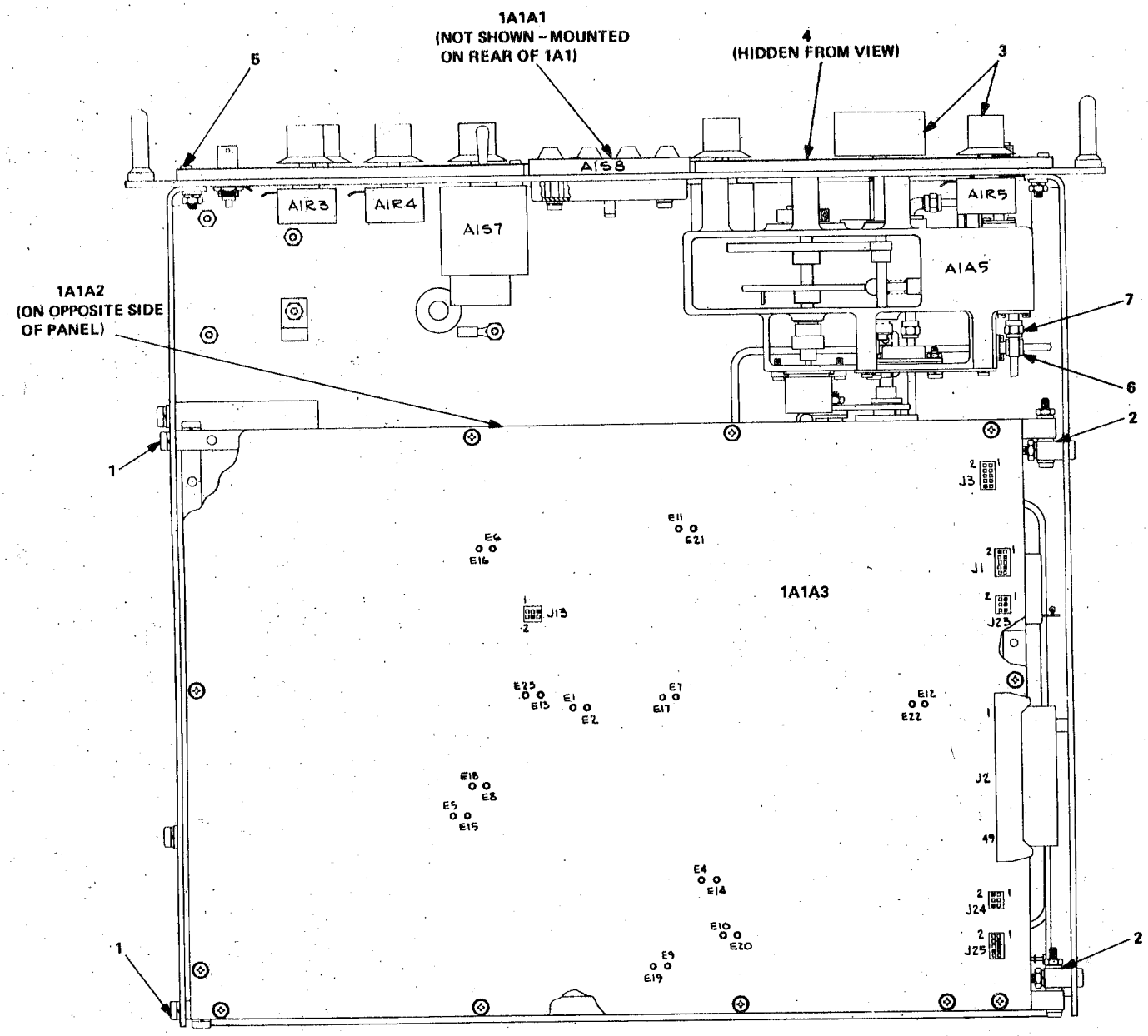


Figure 5-4. Electronics Assembly 1A1 Showing Hinged Panel and Components

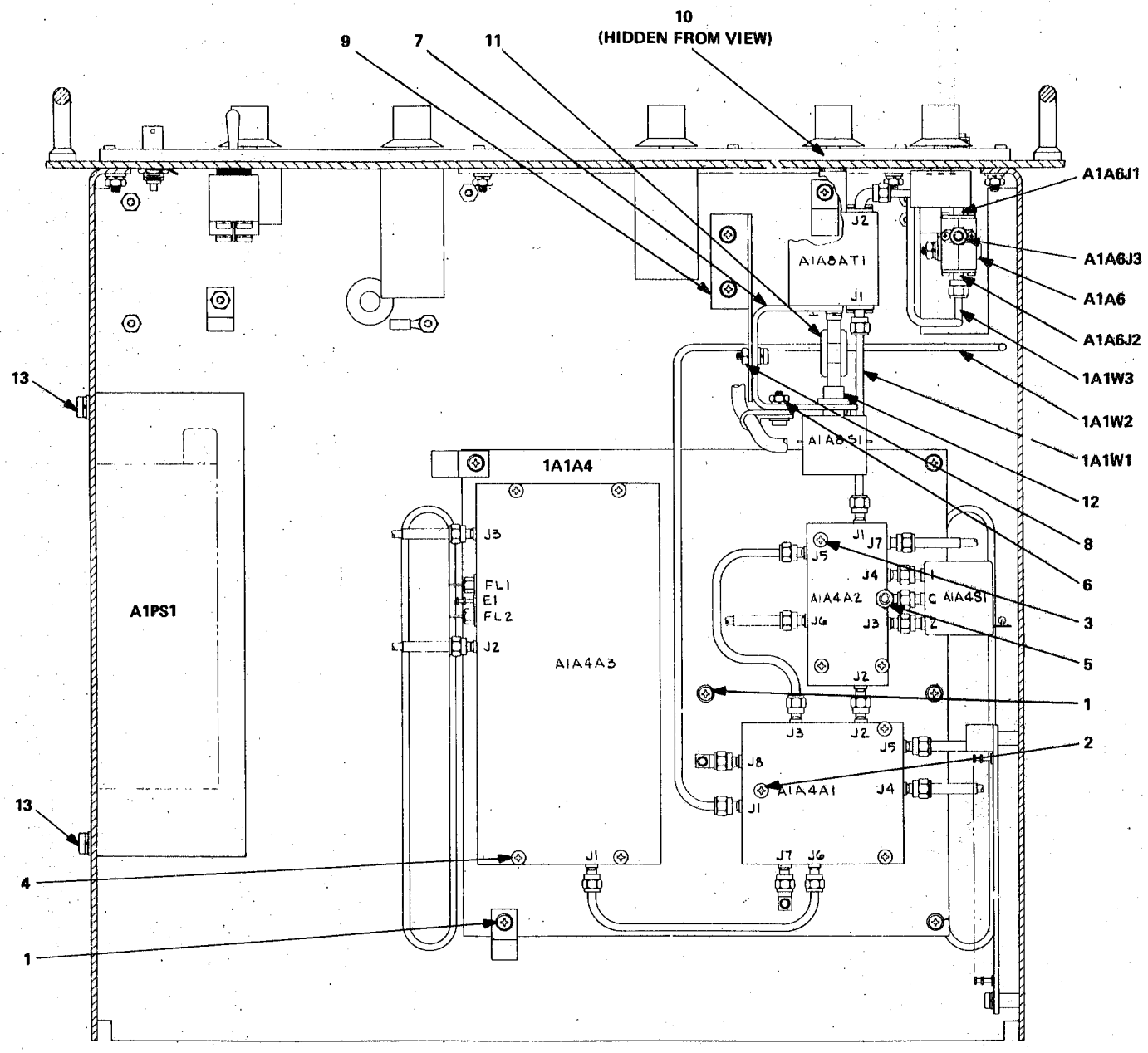
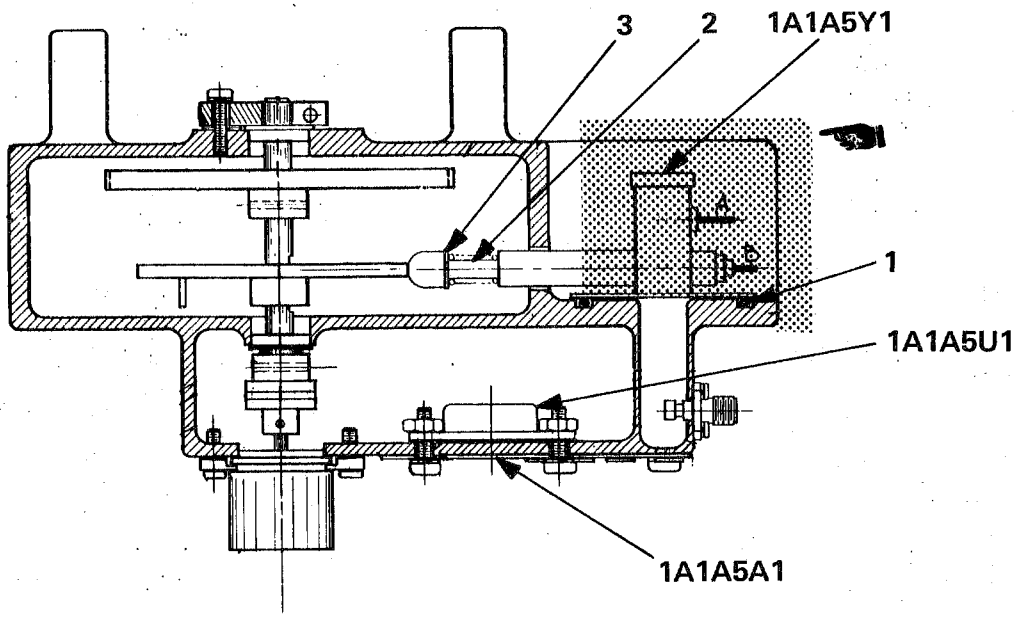


Figure 5-5. Electronics Assembly 1A1 With Digital Assembly 1A1A2 and Microwave Interface 1A1A3 Removed



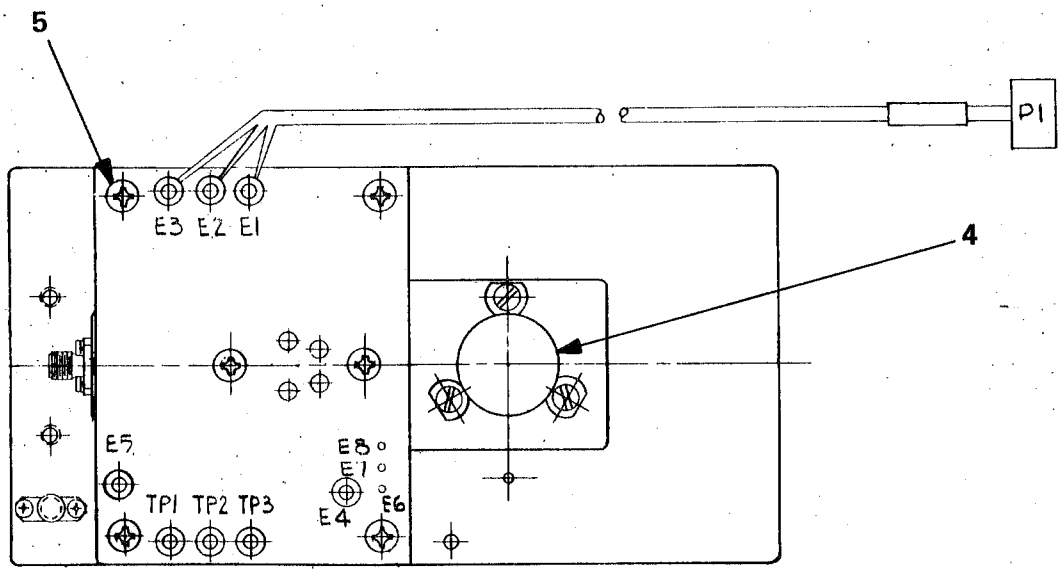


Figure 5-6. RF Oscillator 1A1A5

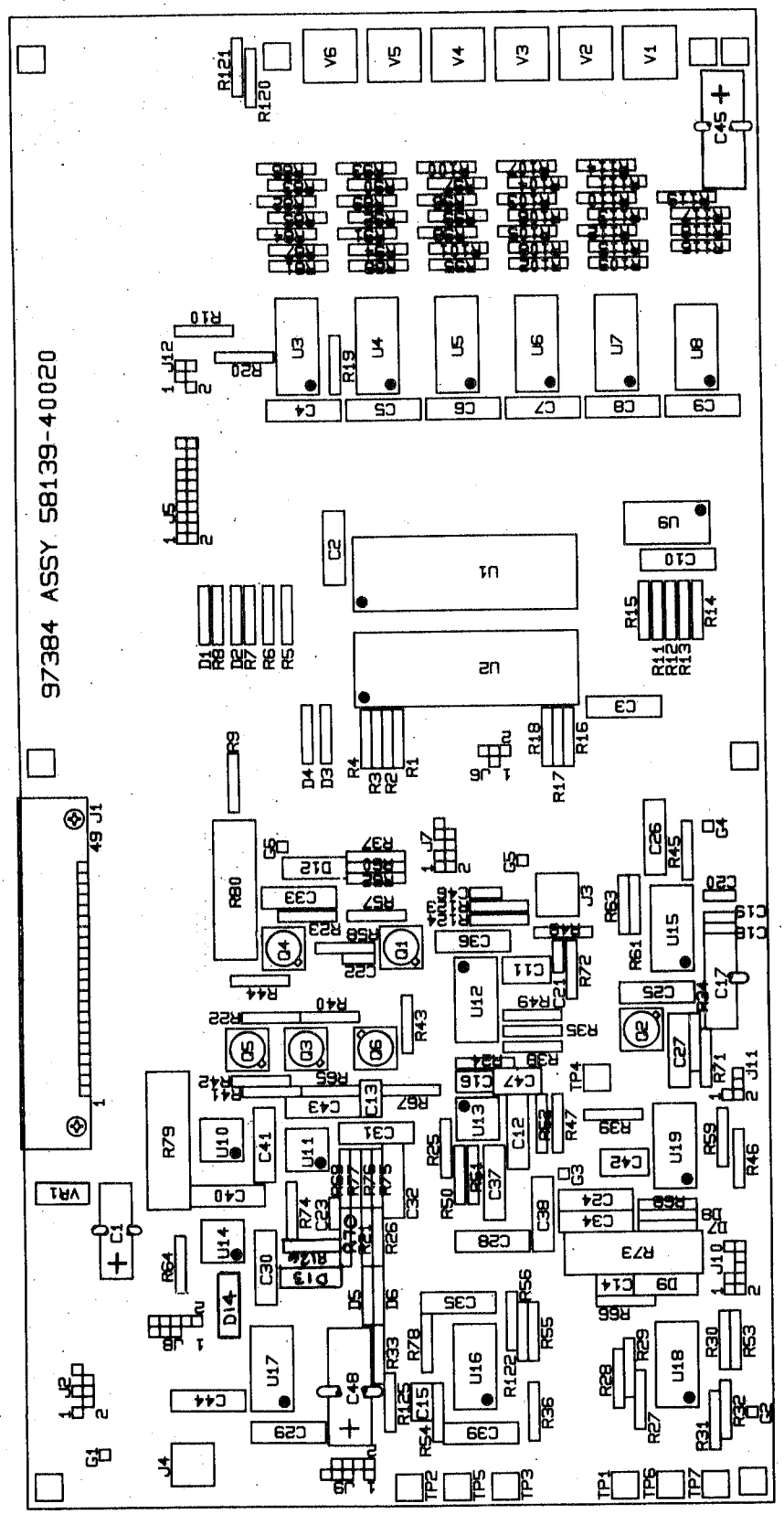


Figure 5-7. Front Panel Interface 1A1A1 - Component Location Diagram

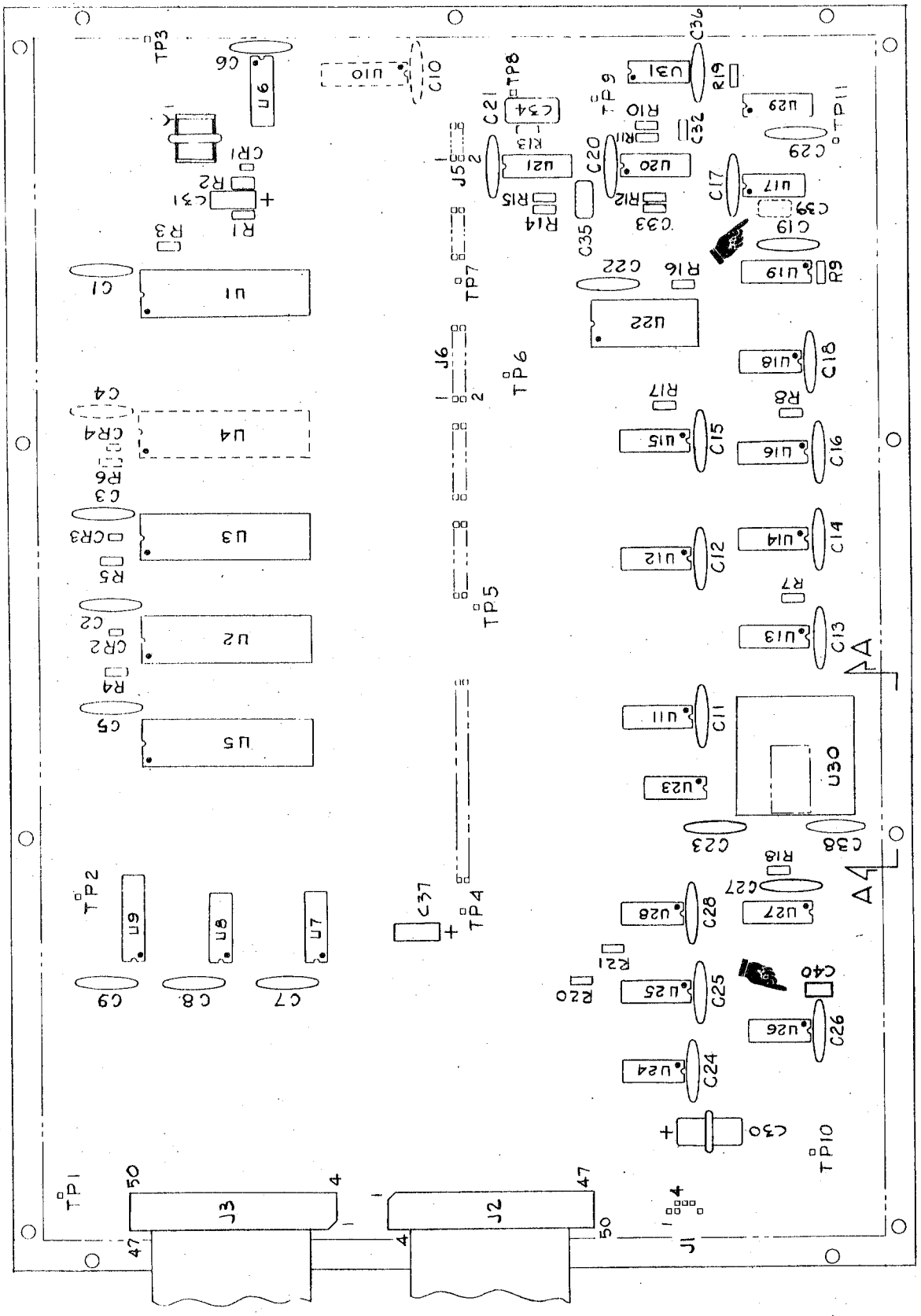


Figure 5-8. Digital Assembly 1A1A2 - Component Location Diagram

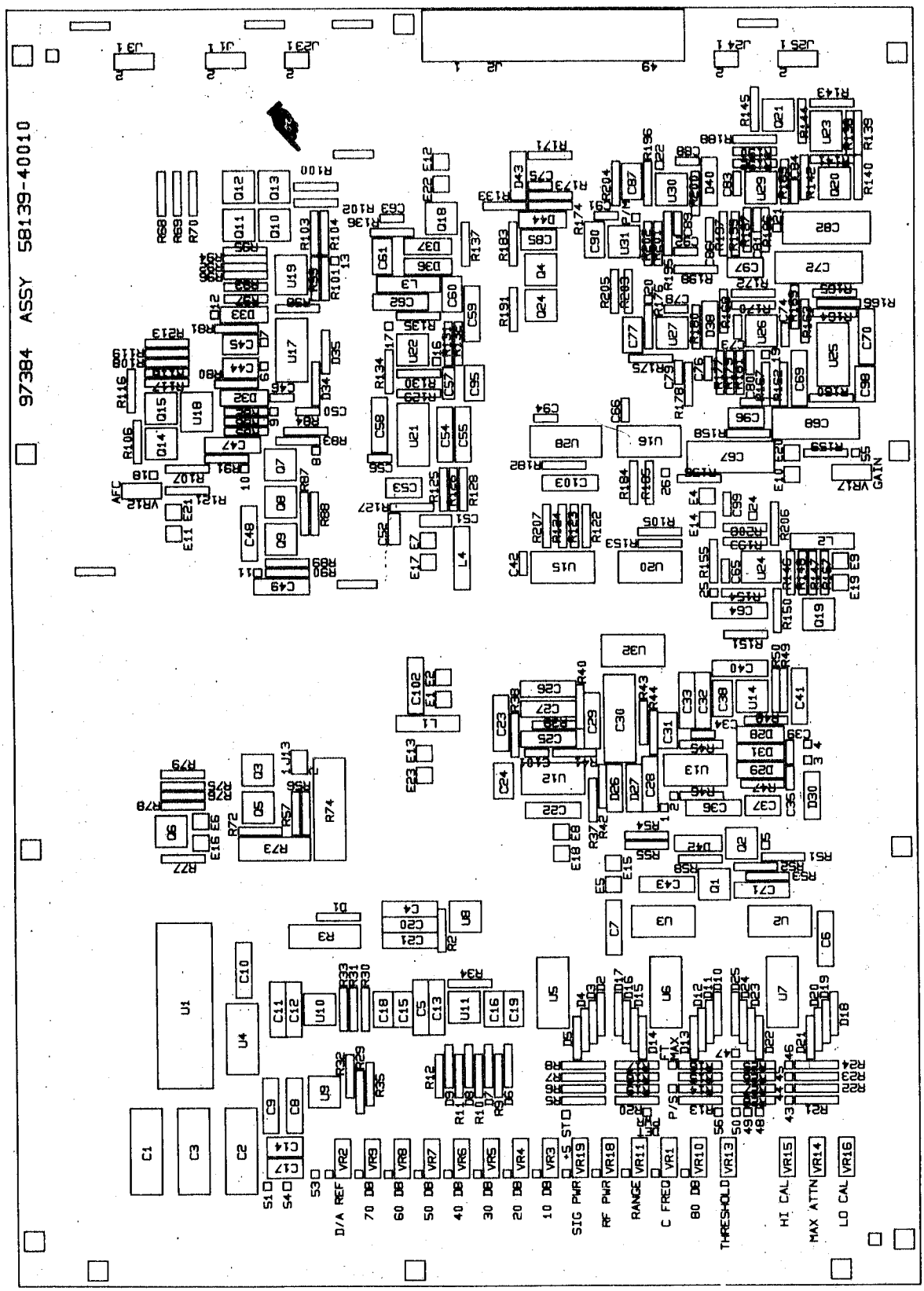


Figure 5-9. Microwave Interface 1A1A3 - Component Location Diagram

Table 5-4. Removal of Electronics Assembly 1A1

Step	Procedure
1	Place Test Set in an upright position on a firm, smooth surface such as a large workbench.
2	Open Test Set case by unsnapping the four snap lock fasteners that secure the top section of the case to the bottom portion.
3	Remove top section of case and store in a safe place. WARNING If top of Test Set combination case has been removed, insure that all power is removed from Test Set before attempting disassembly.
4	Release Electronics Assembly 1A1 from bottom portion of case by removing the 18 screws from perimeter of Test Set front panel.
5	Carefully lift Electronics Assembly up and out of the bottom portion of combination case.
6	Place Electronics Assembly on workbench with front panel up. NOTE If removal is to facilitate alignment or calibration, continue with steps 7 through 11.
7	Apply power to the Test Set as follows: Set PWR ON-OFF switch to OFF. Press circuit breaker 115V (5). Set PNL ON-OFF switch to OFF. Connect P1 of Power Cable W1 to Test Set Power connector J1. Connect P2 of Power Cable W1 to suitable 115 vac, 60 Hz or 400 Hz power source. NOTE If Test Set displays any display other than specified display, refer to table 5-1 for Fault Isolation.

Table 5-4. Removal of Electronics Assembly 1A1 - Continued

Step	Procedure
7 Cont	Set PWR ON-OFF switch to ON and verify that POWER ON indicator lights.
	NOTE Allow Test Set to warm-up and stabilize for 5 minutes before proceeding.
8	Verify that digital display does not display ␣100, ␣101, or ␣102.
9	Initialize the Test Set as follows: Set TRIGGER switch to INT. Turn PRF potentiometer fully ccw. Set ATTENUATION DB 0-80 switch to 10. Turn ATTENUATION DB FINE potentiometer fully cw. Set DISPLAY SELECT switch to FREQ (MHZ).
	NOTE If MODE switch is in SELF TEST position, set to any position other than SELF TEST.
	Set MODE switch to SELF TEST and observe the following: Display indicates ±1888.8.8 for 2 seconds. Display indicates 00000, then increments at a 0.7 second rate until display indicates 99999. Display goes blank.
10	Press E key on keyboard. The Test Set performs automatic self-test. The Test Set will stop momentarily at test numbers between 110 and 185; this is a normal indication. When [ ] is displayed, the automatic self-test is complete.

Table 5-4. Removal of Electronics Assemably 1A1 - Continued

Step	Procedure
10 Cont	NOTE When [ ] is displayed, by repeatedly pressing E key, calibration mode of operation is entered.
11	Press E key on keyboard to advance to desired calibration step as indicated by bXbbbb on display.

Table 5-5. Removal of Front Panel Interface 1A1A1

Step	Procedure
1	Perform the procedures of table 5-4, steps 1 through 6.
2	Disconnect, and tag if necessary, the following connectors that mate with connectors on Front Panel Interface 1A1A1: Disconnect connector — From connector 1A1A2P2 (ribbon) — 1A1A1J1 1A1P4 (twisted pair) — 1A1A1J2 1A1P5 — 1A1A1J5 1A1P7 and 1A1P14 — 1A1J1J7 1A1P8 and 1A1P15 — 1A1A1J8 1A1P9 — 1A1A1J9 1A1P10 and 1A1P16 — 1A1A1J10 1A1P11 and 1A1P17 — 1A1A1J11 1A1P12 — 1A1A1J12 CAUTION Exercise caution when removing rigid microwave cable to insure that the shape of the cable is not distorted. Use the proper torque wrench when removing or tightening coaxial cable connectors.
3	Disconnect, and tag if necessary. The following coaxial connectors that mate with connectors on Front Panel Interface 1A1A1: Disconnect connector — From connector 1A1W4P2 — 1A1A1J3 1A1A3P11 — 1A1A1J4

Table 5-5. Removal of Front Panel Interface 1A1A1 - Continued

Step	Procedure
3 Cont.	NOTE Hold Front Panel Interface 1A1A1 firmly in place when removing mounting hardware.
4	Carefully remove the six mounting screws that attach Front Panel Interface 1A1A1 to Electronics Assembly 1A1.

Table 5-6. Removal of Digital Assembly 1A1A2

Step	Procedure
1	Perform the procedures of Table 5-4, steps 1 through 6.
2	Remove the two screws and lockwashers (1, figure 5-4) that attach the panel containing Digital Assembly 1A1A2 and Microwave Interface 1A1A3.
3	Swing the panel outward on the hinges (2) mounted on the right side of Electronics Assembly 1A1 until the panel is at right angles to the Electronics Assembly.
4	Disconnect, and tag if necessary, the following connectors that mate with connectors on Digital Assembly 1A1A2: Disconnect connector — From connector 1A1P3 (twisted pair) — 1A1A2J1 1A1A2P2 (ribbon) — 1A1A1J1 1A1A2P1 (ribbon) — 1A1A3J2 NOTE Hold Digital Assembly 1A1A2 firmly in place when removing mounting hardware.
5	Carefully remove the 12 mounting screws that secure Digital Assembly 1A1A2.

Table 5-7. Removal of Microwave Interface 1A1A3

Step	Procedure
1	Perform the procedures of table 5-4, steps 1 through 6.
2	Remove the two screws and lockwashers (1, figure 5-4) that attach the panel containing Digital Assembly 1A1A2 and Microwave Interface 1A1A3.
3	Swing the panel outward on the hinges (2) mounted on the right side of Electronics Assembly 1A1 until the panel is at right angles to the Electronics Assembly.
4	Disconnect, and tag if necessary, the following connectors that mate with connectors on Microwave Interface 1A1A3. Disconnect connector — From connector 1A1P1 (twisted pair) — 1A1A3J1 1A1A2P1 (ribbon) — 1A1A3J2 1A1A8P1 (cable harness) — 1A1A3J3 1A1A4P2 (twisted pair) — 1A1A3J13) 1A1A4P1 (twisted pair) — 1A1A3J23) 1A1A5P1 (from Gunn Oscillator Regulator 1A1A5A1) — 1A1A3J24 1A1P2 — 1A1A3J25 CAUTION Use care when removing the coaxial cable connections from Microwave Assembly 1A1A4 to avoid damage to the ends of the cables that are hardwired to Microwave Interface 1A1A3 (refer to figure 5-5). NOTE Use the proper torque wrench when removing or tightening coaxial cable connections.
5	Disconnect, and tag if necessary, the following coaxial connectors of Microwave Interface 1A1A3 from their respective connectors: Coaxial connector — From connector 1A1A3P1 — J8 of Modulator/Mixer 1A1A4A1 1A1A3P2 — J5 of Modulator/Mixer 1A1A4A1 1A1A3P3 — J2 of VCO/Prescaler 1A1A4A3 1A1A3P4 — J6 of Coupler Module 1A1A4A2

Table 5-7. Removal of Microwave Interface 1A1A3 - Continued

Step	Procedure
5 Cont	Coaxial connector / From connector 1A1A3P5 — J4 of Modulator/Mixer 1A1A4A1 1A1A3P6 — J7 of Modulator/Mixer 1A1A4A1 1A1A3P7 — J3 of VCO/Prescaler 1A1A4A3 1A1A3P8 — J7 of Coupler Module 1A1A4A2 1A1A3P9 — J2 of RF Detector 1A1A4A4 1A1A3P10 — J2 of RF Oscillator 1A1A5 1A1A3P11 — J4 of Front Panel Interface 1A1A1 NOTE Hold Microwave Interface 1A1A3 firmly in place when removing mounting hardware.
6	Carefully remove the 12 mounting screws that secure Microwave Interface 1A1A3 to Electronics Assembly 1A1.
7	Remove Microwave Interface to a safe place.

Table 5-8. Removal of Microwave Assembly 1A1A4

Step	Procedure
1	Perform the procedures of table 5-4, steps 1 through 6.
2	Remove the two screws and lockwashers (1, figure 5-4) that attach the panel containing Digital Assembly 1A1A2 and Microwave Interface 1A1A3.
3	Swing the panel outward on the hinges (2) mounted on the right side of Electronics Assembly 1A1 until the panel is at right angles to the Electronics Assembly. CAUTION Exercise caution when removing rigid microwave cable (1A1W1 and 1A1W2) to insure that the shape of the cable is not distorted

Table 5-8. Removal of Microwave Assembly 1A1A4 - Continued

Step	Procedure
3 Cont	NOTE Use the proper torque wrench when disconnecting or connecting coaxial connectors.
4	Disconnect, and tag if necessary, the following coaxial connectors from connectors on components of Microwave Assembly 1A1A4: Coaxial connector — From connector 1A1A3P1 — J8 of Modulator/Mixer 1A1A4A1 1A1A3P2 — J5 of Modulator/Mixer 1A1A4A1 1A1A3P3 — J2 of VCO/Prescaler Output 1A1A4A3 1A1A3P4 — J6 of Coupler Module 1A1A4A2 1A1A3P5 — J4 of Modulator/Mixer 1A1A4A1 1A1A3P6 — J7 of Modulator/Mixer 1A1A4A1 1A1A3P7 — J3 of VCO/Prescaler 1A1A4A3 1A1A3P8 — J7 of Coupler Module 1A1A4A7 1A1A3P9 — J2 of RF Detector 1A1A4A4 1A1W1P2 — J1 of Coupler Module 1A1A4A2 1A1W2P1 — J1 of Modulator/Mixer 1A1A4A1
5	Disconnect connector 1A1A4P1 from connector J23 of Microwave Interface 1A1A3.
6	Disconnect connector 1A1A4P2 from connector J13 of Microwave Interface 1A1A3.
	NOTE Mounting screws have larger screw heads than the case screws of Microwave Assembly 1A1A4.
7	Remove the six mounting screws (1, figure 5-5) that secure Microwave Assembly 1A1A4 to Electronics Assembly 1A1. Three of the mounting screws also secure cable clamps; leave the cable clamp loosely attached to cable.
8	Remove Microwave Assembly to a safe place.

Table 5-9. Removal of Modulator/Mixer 1A1A4A1 From Microwave Assembly 1A1A4

Step	Procedure
1	Perform the procedures of table 5-4, steps 1 through 6.
2	Remove the two screws and lockwashers (1, figure 5-4) that attach the panel containing Digital Assembly 1A1A2 and Microwave Interface 1A1A3.
3	Swing the panel outward on the hinges (2) mounted on the right side of Electronics Assembly 1A1 until the panel is at right angles to the Electronics Assembly. CAUTION Exercise extreme care to avoid damaging cables or wiring connections to surface of printed circuit cards when removing components from Microwave Assembly 1A1A4. NOTE Use proper torque wrench when removing coaxial cables.
4	Disconnect, and tag if necessary, the following coaxial connectors from connectors on Modulator/Mixer 1A1A4A1 (refer to figure 5-5). Coaxial connector — From connector 1A1A3P1 — 1A1A4A1J8 1A1A3P2 — 1A1A4A1J5 1A1A3P5 — 1A1A4A1J4 1A1A3P6 — 1A1A4A1J7 1A1W2P1 — 1A1A4A1J1 CAUTION Exercise caution when removing rigid microwave cable (1A1A4W1 and 1A1A4W2) to insure that the shape of the cable is not distorted. NOTE Use proper torque wrench when removing coaxial cables.

Table 5-9. Removal of Modulator/Mixer 1A1A4A1 From Microwave Assembly 1A1A4 - Continued

Step	Procedure
5	Using the proper torque wrench, disconnect end of rigid cable 1A1A4W1 that mates with connector 1A1A4A1J6.
6	Using the proper torque wrench, disconnect end of rigid cable 1A1A4W2 that mates with connector 1A1A4A1J3.
7	Remove the three mounting screws (2, figure 5-5) that secure Modulator/Mixer 1A1A4A1 to Microwave Assembly 1A1A4.
8	Using the proper torque wrench, disconnect rigid microwave coupling between connector 1A1A4A1J2 and connector J2 of Coupler Module 1A1A4A2.

Table 5-10. Removal of Coupler Module 1A1A4A2 From Microwave Assembly 1A1A4

Step	Procedure
1	Perform the procedures of table 5-4, steps 1 through 6.
2	Remove the two screws and lockwashers (1, figure 5-4) that attach the panel containing Digital Assembly 1A1A2 and Microwave Interface 1A1A3.
3	Swing the panel outward on the hinges (2) mounted on the right side of Electronic Assembly 1A1 until the panel is at right angles to the Electronics Assembly. CAUTION Exercise extreme care to avoid damaging cables or wiring connections to surface of printed circuit cards when removing components from the Microwave Assembly 1A1A4.

Table 5-10. Removal of Coupler Module 1A1A4A2 From Microwave Assembly 1A1A4 - Continued

Step	Procedure
	NOTE Use proper torque wrench when removing coaxial cables.
4	Disconnect, and tag if necessary, the following coaxial connectors from connectors on Coupler Module 1A1A4A2 (refer to figure 5-5): Coaxial connector — From connector 1A1A3P4 — 1A1A4A2J6 1A1A3P8 — 1A1A4A2J7 1A1W1P2 — 1A1A4A2J1
	CAUTION Exercise caution when removing rigid microwave cable (1A1A4W2) to insure that the shape of the cable is not distorted.
	NOTE Use proper torque wrench when removing coaxial cables.
5	Using the proper torque wrench, disconnect end of rigid cable 1A1A4W2 that mates with connector 1A1A4A2J5.
6	Using the proper torque wrench, disconnect rigid microwave coupling between connector 1A1A4A2J4 and Coaxial Switch 1A1A4S1-1, and between connector 1A1A4A2J3 and Coaxial Switch 1A1A4S1-2.
7	Remove the three mounting screws (2, figure 5-5) that secure Modulator/Mixer 1A1A4A1 to Microwave Assembly 1A1A4.
8	Using the proper torque wrench, disconnect rigid microwave coupling between connector 1A1A4A1J2 and connector J2 of Coupler Module 1A1A4A2.
9	Remove the three mounting screws (3, figure 5-5) that secure Coupler Module 1A1A4A2 to Microwave Assembly 1A1A4.

Table 5-11. Removal of VCO/Prescaler 1A1A4A3 From Microwave Assembly 1A1A4

Step	Procedure
1	Perform the procedures of table 5-4, steps 1 through 6.
2	Remove the two screws and lockwashers (1, figure 5-4) that attach the panel containing Digital Assembly 1A1A2 and Microwave Interface 1A1A3.
3	Swing the panel outward on the hinges (2) mounted on the right side of Electronics Assembly 1A1, until the panel is at right angles to the Electronics Assembly. CAUTION Exercise extreme care to avoid damaging cables or wiring connections to surface of printed circuit cards when removing components from Microwave Assembly 1A1A4. NOTE Use proper torque wrench when removing coaxial cables.
4	Disconnect, and tag if necessary, the following coaxial connectors from connectors on VCO/Prescaler 1A1A4A3 (refer to figure 5-5): Coaxial connector — From connector 1A1A3P3 — 1A1A4A3J2 1A1A3P7 — 1A1A4A3J3 CAUTION Exercise caution when removing rigid microwave cable (1A1A4W1) to insure that the shape of the cable is not distorted. NOTE Use proper torque wrench when removing coaxial cables.
5	Using the proper torque wrench, disconnect end of rigid cable 1A1A4W1 that mates with connector 1A1A4A3J1.

Table 5-11. Removal of VCO/Prescaler 1A1A4A3 From Microwave Assembly 1A1A4 - Continued

Step	Procedure
6	Disconnect connector P1 of Microwave Assembly 1A1A4 from connector J23 of Microwave Interface 1A1A3. This cable terminates on standoff terminals (FL1, FL2, and E1) on VCO/Prescaler 1A1A4A3. NOTE Hold VCO/Prescaler 1A1A4A3 firmly in place when removing mounting hardware.
7	Remove the four mounting screws (4, figure 5-5) that secure VCO/Prescaler 1A1A4A3 to Microwave Assembly 1A1A4.

Table 5-12. Removal of RF Detector 1A1A4A4 From Microwave Assembly 1A1A4

Step	Procedure
1	Perform the procedures of table 5-4, steps 1 through 6.
2	Remove the two screws and lockwashers (1, figure 5-4) that attach the panel containing Digital Assembly 1A1A2 and Microwave Interface 1A1A3.
3	Swing the panel outward on the hinges (2) mounted on the right side of Electronics Assembly 1A1 until the panel is at right angles to the Electronics Assembly.
4	Using the proper torque wrench, disconnect and remove RF Detector 1A1A4A4 that mates with 90° rf connector attached to center terminal of Coaxial Switch 1A1A4S1 (5, figure 5-5).

Table 5-13. Removal of Coaxial Switch 1A1A4S1 From Microwave Assembly 1A1A4

Step	Procedure
1	Perform the procedures of table 5-4, steps 1 through 6.
2	Remove the two screws and lockwashers (1, figure 5-4) that attach the panel containing Digital Assembly 1A1A2 and Microwave Interface 1A1A3.
3	Swing the panel outward on the hinges (2) mounted on the right side of Electronics Assembly 1A1 until the panel is at right angles to the Electronics Assembly. CAUTION Exercise caution when removing rigid microwave cable to insure that the shape of the cable is not distorted.
4	Using the proper torque wrench, disconnect rigid microwave coupling between Coaxial Switch 1A1A4S1-1 and connector J4 of Coupler Module 1A1A4A2 and between 1A1A4S1-2 and connector J3 of Coupler Module 1A1A4A2 (refer to figure 5-5).
5	Remove Coaxial Switch 1A1A4S1 and attached RF Detector 1A1A4A4 (5, figure 5-5) from Microwave Assembly 1A1A4. CAUTION Exercise caution when removing rigid microwave cable to insure that the shape of the cable is not distorted.
6	Using the proper torque wrench, disconnect and remove RF Detector 1A1A4A4 that mates with 90° rf connector attached to center terminal of Coaxial Switch 1A1A4S1. Remove twisted pair cable 1A1A4P2 from connector 1A1A3J3 on Microwave Interface 1A1A3.

Table 5-14. Removal of RF Oscillator 1A1A5

Step	Procedure
1	Perform the procedures of table 5-4, steps 1 through 6.
2	Remove two screws and lockwashers (1, figure 5-4) that attach panel containing Digital Assembly 1A1A2 and Microwave Interface 1A1A3.
3	Swing the panel outward on the hinges (2) mounted on the right side of Electronics Assembly 1A1 until the panel is at right angles to the Electronics Assembly.
4	Disconnect connector 1A1A5P1 from connector J24 of Microwave Interface 1A1A3. NOTE Use proper torque wrench when removing coaxial cables. CAUTION Exercise caution when removing rigid microwave cable to insure that the shape of the cable is not distorted.
5	Disconnect coaxial cable connector 1A1W2P2 from connector J1 (6) of Modulator/Mixer 1A1A4A1 that connects to connector J1 of Gunn Oscillator 1A1A5Y1.
6	Disconnect coaxial cable connector 1A1W5P1 from connector J4 of Front Panel Interface 1A1A1 that connects to connector J2 (7) of Gunn Oscillator 1A1A5Y1.
7	Disconnect connector 1A1P9 from connector J9 of Front Panel Interface 1A1A1.

Table 5-14. Removal of RF Oscillator 1A1A5 - Continued

Step	Procedure
8	Using hexagonal spline wrench, loosen and remove the control knobs (3) that attach to RF Oscillator 1A1A5 as shown in figure 5-4. NOTE Hold RF Oscillator 1A1A5 firmly in place from underneath the front panel of Electronics Assembly 1A1 when removing mounting hardware.
9	Remove the three mounting screws (4) that attach RF Oscillator 1A1A5 to the Test Set front panel. Access to the three mounting screws is through the recessed holes in the front panel as shown in figure 5-4. NOTE Use care when lowering RF Oscillator 1A1A5 through opening in front panel to avoid bendoring or twisting cable assemblies and connectors attached to RF Oscillator 1A1A5.
10	Carefully lower RF Oscillator 1A1A5 through opening in front panel and slide out through the bottom of Electronics Assembly 1A1.

Table 5-15. Removal of Components From RF Oscillator 1A1A5

Step	Procedure
1	Remove RF Oscillator 1A1A5 from Electronics Assembly 1A1 by performing the procedures of table 5-14, steps 1 through 10.
	GUNN OSCILLATOR 1A1A5Y1
	NOTE Refer to figure 5-6 (view A) when performing the procedures to remove Gunn Oscillator 1A1A5Y1.
2	Remove RF Absorber from Gunn Oscillator 1A1A5Y1.
3	Tag and unsolder the wires that connect to terminals A (B+ terminal) and B (varactor terminal) on Gunn Oscillator 1A1A5Y1.
4	Remove the four screws, lockwashers, and flat washers that secure Gunn Oscillator 1A1A5Y1 to the housing of RF Oscillator 1A1A5.
5	Carefully slide Gunn Oscillator 1A1A5Y1 out of RF Oscillator 1A1A5, being careful not to damage the tuning rod (2) or tuning rod guide (3) portions of the Gunn Oscillator.
	GUNN OSCILLATOR REGULATOR 1A1A5A1
	NOTE Refer to figure 5-6 (view B) when performing the procedures to remove Gunn Oscillator Regulator 1A1A5A1.
6	Tag and unsolder the wires that connect to terminals E4 (dc return to Gunn Oscillator) and E5 (+10V $\pm$2.5V to Gunn Oscillator).
7	Tag and unsolder the wires that attach to terminals E6, E7, and E8 of coarse frequency potentiometer 1A1A5R1 (4) on rear of RF Oscillator 1A1A5.
	NOTE Hold Gunn Oscillator Regulator 1A1A5A1 firmly in place when removing mounting hardware.
8	Remove Voltage Regulator 1A1A5V1 from RF Oscillator 1A1A5 by removing two screws, lockwashers, and nuts (refer to figure 5-6, view A).
9	Remove the four screws, lockwashers, and flat washers that secure Gunn Oscillator Regulator 1A1A5A1 to RF Oscillator housing.
10	Remove Gunn Oscillator Regulator 1A1A5A1 from RF Oscillator housing.

Table 5-16. Removal of Detector 1A1A6

Step	Procedure
1	Perform the procedures of table 5-4, steps 1 through 6. CAUTION Exercise caution when removing rigid cables (1A1W3 and 1A1W4) to insure that the cable shape is not modified. NOTE Hold Detector 1A1A6 firmly in place when removing coaxial connectors if mounting hardware has been removed.
2	Using the proper torque wrench, disconnect end of rigid cable 1A1W3P2 that mates with connector 1A1A6J2, as shown in figure 5-5.
3	Using the proper torque wrench, disconnect end of rigid cable 1A1W4P1 that mates with connector 1A1A6J3 (figure 5-5).
4	Using the proper torque wrench, disconnect end of rigid coupling between connector 1A1J2 and connector 1A1A6J1 (figure 5-5).
5	Remove two screws, lockwashers, flat washers, and nuts that attach Detector 1A1A6 to support.
6	Remove Detector 1A1A6 from Electronics Assembly 1A1.

Table 5-17. Removal of Illuminated Panel

Step	Procedure
1	Place Test Set in an upright position on a firm, smooth surface such as a large workbench.
2	Open Test Set case by unsnapping the four snap lock fasteners that secure the top section of the case to the bottom portion.
3	Remove top section of case and store in a safe place.
4	Using hexagonal spline wrench, tag, loosen, and remove all knobs that attach to controls mounted on the front panel of Electronics Assembly 1A1.
5	Remove the 12 screws (5, figure 5-4) that secure Illuminated Panel 1A1A7 to Electronics Assembly 1A1 and lift the Illuminated Panel from the Electronics Assembly.

Table 5-18. Removal of Attenuator Assembly 1A1A8

Step	Procedure
1	Perform the procedures of table 5-4, steps 1 through 6.
2	Remove the two screws and lockwashers (1, figure 5-4) that attach the panel containing Digital Assembly 1A1A2 and Microwave Interface 1A1A3.
3	Swing the panel outward on the hinges mounted on the right side of Electronics Assembly 1A1 until the panel is at right angles to the Electronics Assembly.
4	Remove RF Oscillator 1A1A5 from Electronics Assembly 1A1 by performing the procedures of table 5-14, steps 1 through 10.
5	Using hexagonal spline wrench, tag, loosen, and remove the knobs necessary to remove Illuminated Panel 1A1A7. CAUTION Exercise caution when removing rigid cables (1A1W1 and 1A1W3) to insure that the cable shape is not modified. NOTE Hold Attenuator Assembly 1A1A8 (refer to figure 5-5) firmly in place when removing from Electronics Assembly 1A1.
6	Remove cable harness 1A1A8P1 from connector J3 of Microwave Interface 1A1A3.
7	Using the proper torque wrench, disconnect end of rigid cable 1A1W1P1 that mates with connector J1 of Step Attenuator AT1 on Attenuator Assembly 1A1A8. Refer to figure 5-5.
8	Using the proper torque wrench, disconnect end of rigid cable 1A1W3P1 that mates with connector J2 of Step Attenuator AT1 on Attenuator Assembly 1A1A8.
9	Remove the 12 screws (5, figure 5-4) that secure Illuminated Panel 1A1A7 to Electronics Assembly 1A1 and lift the Illuminated Panel from the Electronics Assembly.
10	Remove the screw, washer, and nut (6, figure 5-5) that attach the cable clamp to the bracket (7).
11	Detach the cable clamp from the bracket (7) and leave the cable clamp loosely attached to the cable.

Table 5-18. Removal of Attenuator Assembly 1A1A8 - Continued

Step	Procedure
12	Remove the two screws, flat washers, lockwashers, and nuts (8) that secure the bracket to the housing (9).
13	Unscrew the mounting nut and washer (10) that attach Attenuator Assembly 1A1A8 to Electronics Assembly 1A1 and lower Attenuator Assembly 1A1A8 through Electronics Assembly 1A1.
14	Remove Attenuator Assembly 1A1A8 from Electronics Assembly 1A1.

Table 5-19. Removal of Components From Attenuator Assembly 1A1A8

Step	Procedure
1	Remove Attenuator Assembly 1A1A8 from Electronics Assembly 1A1 by performing the procedures of table 5-18, steps 1 through 14.
	NOTE Refer to figure 5-5 when performing the following procedures.
	STEP ATTENUATOR 1A1A8AT1
2	Using hexagonal spline wrench, loosen the coupling (11) that attaches Step Attenuator 1A1A8AT1 to Step Attenuator Switch 1A1A8S1.
3	Loosen and remove the two screws that secure Step Attenuator 1A1A8AT1 to the bracket (7).
4	Remove Step Attenuator 1A1A8AT1 from the bracket and remove coupling.
	STEP ATTENUATOR SWITCH 1A1A8S1
5	Using hexagonal spline wrench, loosen the coupling (11) that attaches Step Attenuator Switch 1A1A8S1 to Step Attenuator 1A1A8AT1.
6	Loosen and remove the nut and washer (12) that secure Step Attenuator Switch 1A1A8S1 to the bracket (7).
7	Remove Step Attenuator Switch 1A1A8S1 from the bracket (7) and remove coupling.

Table 5-20. Removal of Power Supply 1A1PS1

Step	Procedure
1	Perform the procedures of table 5-4, steps 1 through 6.
2	Remove the two screws and lockwashers (1, figure 5-4) that attach the panel containing Digital Assembly 1A1A2 and Microwave Interface 1A1A3.
3	Swing the panel outward on the hinges (2) mounted on the right side of the assembly until the panel is at right angles to Electronics Assembly 1A1. NOTE Two different configurations of Power Supply 1A1PS1 may be used in the Test Set. One configuration has two physical terminal strips, one for input power (TB1) connections and the other for output voltage (TB2) connections. The other power supply has a single terminal strip but is labeled for both input (TB1) and output (TB2) connections. Hold Power Supply 1A1PS1 firmly in place when removing mounting hardware.
4	Remove the four screws, lockwashers, and flat washers (13, figure 5-5) that secure Power Supply 1A1PS1 to Electronics Assembly 1A1. CAUTION Do not allow Power Supply to hang by wire attached to terminal boards 1A1PS1TB1 and TB2.
5	Tag and remove the spade lug connections to Power Supply terminal board(s) TB1 and TB2. Refer to figure 5-5.
6	Remove Power Supply 1A1PS1 from Electronics Assembly 1A1.

CAUTION

Some printed circuit card components are sensitive to electrostatic discharge. Insure that a wrist strap, grounded to the printed circuit card, is used when handling these components.

(2) RF Cable W2 Repair. For procedure to repair RF Cable W2, refer to T.O. 1-1A-14.

(3) BNC Cable W3 Repair. For procedure to repair BNC Cable W3, refer to T.O. 1-1A-14.

(4) Ribbon Cable Repair. For procedure to repair ribbon cable, refer to T.O. 1-1A-14.

e. Assembly. The assembly procedures for all subassemblies except RF Oscillator 1A1A5 and Attenuator Assembly 1A1A8 are accomplished by reversing the disassembly procedures of paragraph 5-6a. All attaching hardware removed during disassembly shall be replaced during reassembly. After assembly is complete, perform the test procedures of paragraph 5-7 to verify operation. The assembly procedure for RF Oscillator 1A1A5 is provided in table 5-21. The assembly procedure for Attenuator Assembly 1A1A8 is provided in table 5-22.

CAUTION

Exercise extreme caution when connecting coaxial cables to avoid damaging connectors or distorting shape of rigid cables. When connecting coaxial connectors, connectors must be axially aligned when joined together. Excessive force applied when mating connector will cause damage to the connector. Connectors must be tightened to 8 $\pm$0.5 inch-pounds.

f. Alinement. The alinement procedure for RF Oscillator 1A1A5 is provided in table 5-23.

Table 5-21. Assembly of RF Oscillator 1A1A5

Step	Procedure
	NOTE Hold Gunn Oscillator Regulator 1A1A5A1 firmly in place when securing the RF Oscillator 1A1A5 (refer to figure 5-6, view A).
1	Mount the Gunn Oscillator Regulator on the RF Oscillator housing, using four screws, lockwashers, and flat washers (5, figure 5-6).
2	Mount voltage regulator 1A1A5U1 to RF Oscillator assembly with two screws, lockwashers, and nuts (refer to figure 5-6, view A).
3	Attach and solder the wires to terminals E6, E7, and E8 (figure 5-6) from coarse frequency potentiometer 1A1A5R1 (4) on rear of RF Oscillator 1A1A5.
4	Attach and solder the wires that connect to terminals E4 (dc return to Gunn Oscillator) and E5 (+10V $\pm$2.5V to Gunn Oscillator) as shown on figure 5-6, view B.
5	Carefully slide Gunn Oscillator 1A1A5Y1 into the RF Oscillator, being careful not to damage the tuning rod (2) or tuning rod guide (3) portions of the Gunn Oscillator as shown in figure 5-6, view A. CAUTION Insure that proper control is made between the oscillator tuning rod and the cam when assembly is attempted.
6	Attach Gunn Oscillator 1A1A5Y1 to the housing of the RF Oscillator, using the four screws, lockwashers, and flat washers (1) previously removed, as shown in figure 5-6, view A.
7	Attach and solder the wires that connect to terminals A (B+ terminal) and B (varactor terminal) on Gunn Oscillator 1A1A5Y1, as shown on figure 5-6.

Table 5-21. Assembly of RF Oscillator 1A1A5 - Continued

Step	Procedure
	NOTE If Electronics Assembly 1A1 is installed in Test Set combination case, perform step 8 through 10; otherwise, proceed to step 11.
8	Place RF Absorber over and around Gunn Oscillator 1A1A5Y1 using caution not to disturb wires and terminals.
9	Perform the procedures of table 5-4, steps 1 through 6.
10	Remove the two screws and lockwashers (1, figure 5-4) that attach the panel containing Digital Assembly 1A1A2 and Microwave Interface 1A1A3.
11	Swing the panel outward (as shown in figure 5-4) on the hinges (2) mounted on the right side of Electronics Assembly 1A1 until the panel is at right angles to the Electronics Assembly.
	CAUTION Use care when raising the RF Oscillator through the opening in the front panel of Electronics Assembly 1A1 to avoid bending or twisting cable assemblies and connectors attached to the RF Oscillator.
12	Carefully slide the RF Oscillator in through the bottom of Electronics Assembly 1A1 and raise the RF Oscillator up through the opening in the front panel.
	NOTE Hold the RF Oscillator firmly in place from underneath the front panel when attaching mounting hardware.
13	Secure the RF Oscillator to the front panel with three mounting screws (4, figure 5-4). Attach the screws to the RF Oscillator through the recessed holes in the front panel as shown in figure 5-4.

Table 5-21. Assembly of RF Oscillator 1A1A5 - Continued

Step	Procedure
14	Mount the control knobs (3) that attach to the RF Oscillator.
15	Using hexagonal spline wrench, tighten the control knobs (3) on the shafts.
16	Attach connector 1A1P9 to connector J9 of Front Panel Interface 1A1A1.
	CAUTION Exercise extreme caution when connecting coaxial cables to avoid damaging connectors or distorting shape of rigid cables. When connecting coaxial connectors, connectors must be axially aligned when joined together. Excessive force applied when mating connector will cause damage to the connector. Connectors must be tightened to 8 ±0.5 inch-pounds.
17	Using torque wrench, attach coaxial cable connector 1A1W5P1 from connector J4 of Front Panel Interface 1A1A1 to connector J2 of Gunn Oscillator 1A1A5Y1. Torque connector to 8 ±0.5 inch-pounds.
18	Using torque wrench, attach coaxial cable connector 1A1W2P2 from connector J1 of modulator/mixer 1A1A4A1 to connector J1 of Gunn Oscillator 1A1A5Y1. Torque connector to 8 ±0.5 inch-pounds.
19	Using torque wrench, attach connector 1A1A5P1 to connector J24 of Microwave Interface 1A1A3.
20	Swing the panel containing Digital Assembly 1A1A2 and Microwave Interface 1A1A3 to the left and secure to Electronics Assembly frame with two screws and lockwashers (1, figure 5-4).
21	Place the bottom portion of the Test Set combination case in the upright position.
22	Carefully lift Electronics Assembly 1A1 up and lower into the bottom portion of the combination case.

Table 5-21. Assembly of RF Oscillator 1A1A5 - Continued

Step	Procedure
23	Secure the Electronics Assembly to the bottom portion of the combination case by attaching the 18 screws to the perimeter of the Test Set front panel.
24	Place top section of combination case securely on bottom portion.
25	Close Test Set combination case by closing the four snap lock fasteners that secure the top section of the case to the bottom portion.

Table 5-22. Assembly of Attenuator Assembly 1A1A8

Step	Procedure
1	Secure Step Attenuator Switch 1A1A8S1 to the bracket (7, figure 5-5) by attaching the nut and washer (12) as shown in figure 5-5.
2	Secure Step Attenuator 1A1A8AT1 to the bracket (7) by attaching the nut. CAUTION Insure that Step Attenuator 1A1A8AT1 and Step Attenuator Switch 1A1A8S1 are positioned correctly before connecting them together with the coupling (11).
3	Attach Step Attenuator 1A1A8AT1 and Step Attenuator Switch 1A1A8S1 to the coupling (11) as shown in figure 5-5.
4	Using hexagonal spline wrench, tighten the setscrews on the coupling (11).
5	Route the Attenuator Assembly through the bottom of Electronics Assembly 1A1.

Table 5-22. Assembly of Attenuator Assembly 1A1A8 - Continued

Step	Procedure
6	Raise the Attenuator Assembly up through the Electronics Assembly until the shift of the attenuator is through the hole in the front panel.
7	Secure the Attenuator Assembly to the Electronics Assembly with the mounting nut and washer (10).
8	Attach the bracket (7) to the housing (9) with the screw, flat washer, lockwasher, and nut (8).
9	Position the cable clamp over the hole in the bracket (7).
10	Attach the cable clamp to the bracket, using the screw, washer, and nut (6) as shown in figure 5-5.
11	Position Illuminated Panel 1A1A7 on Electronics Assembly and secure with the 12 screws (5, figure 5-4) previously removed. CAUTION Exercise caution when connecting coaxial cables (1A1W1 and 1A1W3) to avoid damaging connectors or distorting shape of rigid cables. When connecting coaxial connectors, connectors must be axially aligned when joined together. Excessive force applied when mating connector will cause damage to the connector. Connectors must be tightened to 8 ±0.5 inch-pounds. CAUTION Exercise caution when connecting rigid cables (1A1W1 and 1A1W3 to insure that the cable shape is not modified).
12	Using torque wrench, connect end of rigid cables 1A1W3P1 that mates with connector J2 of Step Attenuator AT1 on Attenuator Assembly 1A1A8. Torque connector to 8 ± inch-pounds.

Table 5-22. Assembly of Attenuator Assembly 1A1A8 - Continued

Step	Procedure
13	Using torque wrench, connect end of rigid cables 1A1W3P1 that mates with connector J2 of Step Attenuator AT1 on Attenuator Assembly 1A1A8. Torque connector to 8 ±0.5 inch-pounds.
14	Connect cable harness 1A1A8P1 from Step Attenuator 1A1A8AT1 to connector J3 of Microwave Interface 1A1A3.
15	Place RF Oscillator 1A1A5 in Electronics Assembly 1A1 by performing the assembly procedures of table 5-21, steps 1 through 18.
16	Replace all of the knobs removed to facilitate removal of Illuminated Panel 1A1A7 on their respective shafts and tighten with hexagonal spline wrench.
17	Swing the panel containing Digital Assembly 1A1A2 and Microwave Interface 1A1A3 to the left and secure to Electronics Assembly frame with two screws and lockwashers (1, figure 5-4).
18	Place the bottom portion of the Test Set combination case in the upright position, firmly on the workbench.
19	Carefully lift Electronics Assembly 1A1 up and lower into the bottom portion of the combination case.
20	Secure Electronics Assembly to the bottom portion of the combination case by attaching the 18 screws to the perimeter of the Test Set front panel.
21	Place top section of combination case securely on bottom portion.
22	Close Test Set combination case by closing the four snap lock fasteners that secure the top section of the case to the bottom portions.

Table 5-23. RF Oscillator 1A1A5 Alinement - Tuning Range Adjustment

Step	Procedure
1	Connect frequency counter (table 5-25, item 4) and X-band plug-in (table 5-25, item 5) to RF IN-OUT connector J2.
2	Set ATTENUATION DB 0-80 switch to 0.
3	Set ATTENUATION DB FINE potentiometer to the middle of its range.
4	Set MODE switch to SIG GEN CW.
5	Set DISPLAY SELECT switch to FREQ (MHZ).
6	Set FREQ 8.4 TO 10.0 GHZ FINE potentiometer to the middle of its range.
7	While observing cam in RF Oscillator 1A1A5, rotate FREQ 8.4 TO 10.0 GHZ COARSE control until the hole in the cam lines up with the hole in the housing.
8	Observe and note frequency indication on frequency counter. If this frequency is between 9,180 and 9,220 MHz, go to step 18; otherwise, perform steps 9 through 17.
9	Loosen setscrew in cam.
10	While restraining spring-loaded plunger, slide cam inward (toward gear) until it is clear of plunger.
11	Remove plunger from RF Oscillator housing.
12	Subtract frequency noted in step 8 from 9,200 MHz to obtain a frequency difference.
13	Rotate plastic tip of plunger 1 degree for each MHz of frequency difference calculated in step 12. Rotate plunger cw if frequency difference is positive; rotate plunger ccw if frequency difference is negative.
14	Reinstall plunger in the RF Oscillator housing and slide cam outward (away from gear) until the plastic tip of the plunger is centered on the edge of the cam.
15	Rotate cam until the hole in the cam lines up with the hole in the housing.

Table 5-23. RF Oscillator 1A1A5 Alinemcnt - Tuning Range Adjustment - Continued

Step	Procedure
16	Tighten setscrew in cam.
17	Repeat steps 8 through 16 until frequency counter indication in step 8 is between 9,180 and 9,220 MHz.
18	Disconnect test equipment.
19	Perform calibration procedures of tables 5-26 and 5-27.

5-7. TEST. Table 5-24 lists the test requirements to insure proper operation of the Test Set after repair or replacement of a subassembly. Table 5-25 lists the test equipment required to perform the required calibration/test.

5-8. CALIBRATION

a. Frequency Measurement Calibration. Perform procedures of tables 5-26 through 5-28 for frequency measurement calibration.

b. RF Power Calibration. Perform procedures of tables 5-29 and 5-30 for rf power calibration.

c. Attenuator Assembly 1A1A8 Calibration. Perform procedure of table 5-31 for adjustment of attenuator potentiometer assembly.

d. Range Calibration. Perform procedure of table 5-31 for range calibration.

e. Reference D/A Calibration. Perform procedure of table 5-32 for reference D/A calibration.

f. RF Oscillator 1A1A5 Calibration. Perform procedures of table 5-33 and 5-23 for calibration of RF Oscillator 1A1A5.

Table 5-24. Calibration and/or Tests Required After Major Subassembly Repair/Replacement

Subassembly repaired/replaced	Reference designator	Required calibration and/or test
Front Panel Interface	1A1A1	System checkout (table 5-1).
Digital Assembly	1A1A2	System checkout (table 5-1).
Microwave Interface	1A1A3	AFC calibration (table 5-26).
		Coarse frequency potentiometer calibration (table 5-27).
		AFC threshold calibration (table 5-28).
		Power measurement calibration (table 5-29).
		Attenuator potentiometer adjustment (table 5-30).
		Range calibration (table 5-31).
		Reference D/A calibration (table 5-32).
		System checkout (table 5-1).
Microwave Assembly	1A1A4	
Modulator/Mixer	1A1A4A1	Range calibration (table 5-31).
		System checkout (table 5-1).
Coupler Module	1A1A4A2	Power measurement calibration
VCO/Prescaler	1A1A4A3	System checkout (table 5-1).
RF Detector	1A1A4A4	Power measurement calibration (table 5-29).
		System checkout (table 5-1).

Table 5-24. Calibration and/or Tests Required After Major Subassembly Repair/Replacement - Continued

Subassembly repaired/replaced	Reference designator	Required calibration and/or test
Microwave Assembly - Continued		
Coaxial Switch	1A1A4S1	Power measurement calibration (table 5-29). System checkout (table 5-1).
RF Oscillator	1A1A5	Gunn oscillator regulator adjustment (table 5-33). Gunn oscillator tuning range adjustment (table 5-23). Coarse frequency potentiometer calibration (table 5-27). System checkout (table 5-1).
Detector	1A1A6	Power measurement calibration (table 5-29). System checkout (table 5-1).
Illuminated Panel	1A1A7	System checkout (table 5-1).
Attenuator Assembly	1A1A8	Power measurement calibration (table 5-29) Attenuator calibration (table 5-30). System checkout (table 5-1).
Power Supply	1A1PS1	System checkout (table 5-1).
Potentiometers	1A1R1 through 1A1R5	System checkout (table 5-1).
Switches	1A1S1 through 1A1S8	System checkout (table 5-1).

Table 5-25. List of Required Test Equipment

Item no.	Nomenclature	Part or model number	Application	Range	Accuracy
1	Oscilloscope	66-25-00-397-4179	Provides visual display of electrical signals.		
2	Digital multimeter (DVM)	6625-00-439-5154	Provides precision voltage measurement capability.	DC - 0.001 mV to 1000.00 volts dc, ratio 1.0000:1 to 100.00:1. AC - 0.001 to 500.00 volts ac, 50 to 10,000 Hz. Ohms - 0.0001 to 1000 kilohms	Refer to PD-SANE-6625-70-163A
3	Pulse generator	6625-01-022-2247	Provides trigger for simulated target return pulses.		
4	Frequency counter	MIL-C-9988A	Measures frequency.	0-50 MHz	±1 count + time base accuracy.

Table 5-25. List of Required Test Equipment - Continued

Item no.	Nomenclature	Part or model number	Application	Range	Accuracy
5	Frequency counter X-band plug-in	6625-00-058 3042	Extends range of frequency counter.	3 to 12.4 GHz	Maintains counter accuracy.
6	Sweep generator	6625-00-442-3470	Provides X-band frequency source.	0.25 to 40 GHz	
7	Sweep generator X-band plug-in	6625-00-460-3304	Extends frequency range of sweep generator to X-band.	8 to 12.4 GHz	
8	Power meter	6625-436-4883	Provides rf power measurement.	7 ranges from -20 to +10 dbm.	±1% of full scale indication.
9	Thermistor mount	6625-811-2435	Extends power meter capabilities to X-band.	10 to 18 GHz, 200 ohm.	
10	Crystal detector	6625-436-4883	Detects rf pulses.		
11	Pin modulator	6625-113-6300YA	Pulse modulates X-band source.	7.0 to 12.4 GHz, 80 db dynamic range.	

Table 5-25. List of Required Test Equipment - Continued

Item no.	Nomenclature	Part or model number	Application	Range	Accuracy
12	Attenuator and signal calibrator	6625-909-3185	Provides accurate attenuation measurements.		
13	Heterodyne mixer-oscillator	6625-909-3084	Used with attenuator and signal calibrator.		
14	Attenuation standards	6625-869-2394	Provides precision attenuation standards when using attenuator and signal calibrator.		

Table 5-26. Frequency Measurement Calibration

Step	Procedure
1	Remove Electronics Assembly 1A1, using the procedures of table 5-4.
2	Connect frequency counter (table 5-25, item 4) to standoff 1A1A3E12 on the Microwave Interface. Connect frequency counter return to standoff 1A1A3E22.
3	Using the procedures of table 5-1, perform steps 1, 2, 3, and 6. NOTE When [ ] is displayed, the automatic self-test is completed. By pressing E key, calibration mode of operation is entered.
3a	Press E key on the keyboard to advance to calibration step 3 as indicated by b3bbbb on display.
4	Adjust AFC potentiometer 1A1A3VR12, if necessary, to obtain a frequency counter indication between 3.074 and 3.230 MHz. Record the frequency counter indication as frequency A.
5	Press E key on the keyboard to advance to calibration step 4.
6	Observe frequency counter indication and record this frequency as B.
7	Subtract frequency B from frequency A. If the difference is between 0.275 and 0.283 MHz, go to step 10; otherwise, proceed to step 8.
8	Adjust AFC potentiometer 1A1A3VR12 as follows: If frequency difference is greater than 0.283 MHz, turn the AFC potentiometer slightly ccw. If frequency difference is less than 0.275 MHz, turn the AFC potentiometer slightly cw.
9	Repeatedly press E key to advance to calibration step 3. Repeat procedural steps 4 through 7.
10	Disconnect frequency counter.

Table 5-27. Coarse Frequency Potentiometer Calibration

Step	Procedure
1	Remove Electronics Assembly 1A1, using the procedure of table 5-4.
2	On the Test Set: Set MODE switch to SIG GEN CW. Set FREQ 8.4 TO 10.0 GHZ FINE potentiometer to the middle of its range. Set ATTENUATION DB 0-80 switch to 10. Set ATTENUATION DB FINE potentiometer to the middle of its range.
3	Connect DVM (table 5-25, item 2) to CFREQ test point 1A1A3TP37 on Microwave Interface 1A1A3. Connect DVM return lead to ground.
4	Using a clip lead, ground test point 1A1A3TP56.
	CAUTION During steps 5 and 6, insure that the rf power level at the frequency counter input does not exceed the limits of the counter input circuits.
5	Using RF Cable W2, connect frequency counter (table 5-25, item 4) with X-band plug-in (table 5-25, item 5) to Test Set RF IN/OUT connector J2.
6	Set Test Set ATTENUATION DB 0-80 switch and ATTENUATION DB FINE potentiometer until a frequency is indicated on the frequency counter.
7	Adjust FREQ 8.4 TO 10.0 GHZ COARSE control for a 8,400 (plus or minus 5) MHz indication on the frequency counter.
8	Observe DVM. If DVM indicates between +1.1 and +1.3 vdc, go to step 10; otherwise, perform step 9.
9	Loosen the three clamp screws that hold potentiometer 1A1A5R1 in position. Being careful not to move the FREQ 8.4 TO 10.0 GHZ COARSE control, rotate potentiometer 1A1A5R1 until DVM indicates +1.2 (plus or minus 0.1) vdc. Tighten the three clamp screws and insure that the DVM still indicates +1.2 (plus or minus 0.1) vdc.
10	Adjust FREQ 8.4 TO 10.0 GHZ COARSE control for a 10,000 (plus or minus 5) MHz indication on the frequency counter.

Table 5-27. Coarse Frequency Potentiometer Calibration - Continued

Step	Procedure
11	Verify that DVM indicates between +9.4 and +9.6 vdc. If not, adjust CFREQ potentiometer 1A1A3VR1 until DVM indicates +9.5 (plus or minus 0.1) vdc. Then repeat steps 7 through 11.
12	Disconnect test equipment and remove ground clip lead from test point 1A1A3TP56.

Table 5-28. AFC Threshold Calibration

Step	Procedure
1	Remove Electronics Assembly 1A1, using the procedure of table 5-4.
2	Connect oscilloscope (table 5-25, item 1) to test point 1A1A3TP16 on Microwave Interface 1A1A3. Connect oscilloscope return lead to ground.
3	On the Test Set: Set MODE switch to SIG GEN CW. Set DISPLAY SELECT switch to FREQ (MHZ).
4	While observing oscilloscope, slowly turn the FREQ 8.4 TO 10.0 GHZ COARSE control to vary the Test Set frequency over the entire 8,400 to 10,000 MHz range and record the lowest peak-to-peak 600 kHz waveform voltage observed on oscilloscope. Minimum acceptable peak-to-peak voltage is 350 mV.
5	Multiply the voltage recorded in step 4 by -25 to obtain the threshold voltage. Example: 400 mV p-p observed as smallest voltage in step 4 yields -10.0 vdc as the threshold voltage (0.400 X -25 = -10.0). NOTE Maximum adjustment is -15 vdc, which is used for amplitudes of 600 mV and above.

Table 5-28. AFC Threshold Calibration - Continued

Step	Procedure
6	Connect DVM (table 5-25, item 2) to THRESHOLD test point. Connect DVM return lead to standoff ground. Set DVM for dc volts.
7	Adjust THRESHOLD potentiometer 1A1A3VR13 for DVM indication equal to the threshold voltage calculated in step 5 (0 to -15 vdc).
8	Repeat step 4 to verify that AFC lock is maintained. If AFC lock is not maintained, position frequency to the point at which AFC breaks lock and adjust 1A1A3VR13 until AFC lock is reestablished and maintained across band. Insure that voltage reading is between -7 vdc and -15 vdc.
9	Disconnect test equipment.

Table 5-29. Power Measurement Calibration

Step	Procedure
1	Connect test equipment as shown in figure 5-10. Set Variable Attenuator to 50 db. Set Sweep Oscillator for maximum cw power output at 9,200 MHz. While observing power meter and thermistor mount, adjust Variable Attenuator and Sweep Generator for an input power indication of +10.0 (plus or minus 0.1) dbm at Test Set J2.
2	On the Test Set: Set MODE switch to RADAR CW. Set DISPLAY SELECT switch to RF IN PWR (DBM). Set ATTENUATION DB 0-80 switch to 0.
3	Connect positive lead of DVM (table 5-25, item 2) to DET PWR test point 1A1A3TP39 and the negative lead to circuit ground. Adjust GAIN potentiometer 1A1A3VR17 for a +8.00 (plus or minus 0.03) vdc indication on DVM.
4	While observing power meter and thermistor mount, adjust Variable Attenuator and Sweep Generator for an input power indication of -4.0 (plus or minus 0.1) dbm at Test Set J2.

Table 5-29. Power Measurement Calibration - Continued

Step	Procedure
5	Connect positive lead of DVM to DET PWR test point 1A1A3TP39; note voltage and record.
6	Turn Sweep Oscillator RF POWER to OFF.
7	Using the procedures of table 5-1, perform steps 1, 2, 3, and 6.
	NOTE When [ ] is displayed, the automatic self-test is completed. By pressing E key, calibration mode of operation is entered.
8	Press E key on the keyboard to advance to calibration step 3 as indicated by b3bbbb on display.
9	Connect positive lead of DVM to DET PWR test point 1A1A3TP39. Adjust HI CAL potentiometer 1A1A3VR15 for an indication of +8.00 (plus or minus 0.03) vdc.
10	Press E key on keyboard to advance to calibration step 4. While observing DVM, adjust LO CAL potentiometer 1A1A3VR16 for voltage within 0.03 vdc of voltage recorded in step 5.
11	While observing power meter and thermistor mount, turn Sweep Oscillator RF Power to ON and adjust Variable Attenuator for an input power indication of +8.0 (plus or minus 0.05) dbm at Test Set J2.
12	On the Test Set: Set MODE switch to RADAR CW. Set DISPLAY SELECT switch to RF IN PWR (DBM).
13	Set ATTENUATOR DB 0-80 switch to 80.
14	Press R key on keyboard.
15	Set ATTENUATOR DB 0-80 switch to 0.
16	Adjust Sweep Oscillator frequency from 8.4 to 10.0 GHz while adjusting Variable Attenuator to maintain +8.0 (plus or minus 0.05) dbm input to Test Set. Monitor Test Set digital display and note most positive and most negative Test Set display over entire frequency range.

Table 5-29. Power Measurement Calibration - Continued

Step	Procedure
17	Calculate the correction factor as shown below and adjust 1A1A3VR18 for the most positive display plus correction factor. [(nominal value in dbm) + (worse case error)] - (most positive Test Set display) = correction factor where: nominal value in dbm = power at J2 worse case error = $\frac{\text{(most positive error)} - \text{(most negative error)}}{2}$ most positive error = (most positive Test Set display) - (nominal value) most negative error = (least positive Test Set display) - (nominal value)
18	Repeat step 16 while maintaining -2.0 (plus or minus 0.05) dbm. NOTE The Test Set display does not change readout directly with a change of 1A1A3VR16.
19	Calculate the correction factor and adjust LO CAL potentiometer 1A1A3VR16 ccw to increase display readout or cw to decrease display readout for a reading of the most positive display plus correction factor.
20	Repeat steps 13, 14, and 15. Continue to adjust 1A1A3VR16 and repeat steps 13, 14, and 15 until display readout is correct within 0.2 dbm of value determined in step 19.
21	While observing power meter, adjust Variable Attenuator for an input power indication of +13.0 dbm at Test Set J2. Set ATTENUATOR DB 0-80 switch to 10. Adjust Sweep Oscillator frequency from 8.4 to 10.0 GHz while adjusting Variable Attenuator to maintain +13.0 (±0.05) dbm input to Test Set. Monitor Test Set display and note minimum and maximum display.
22	Calculate the correction factor and adjust 1A1A3VR3 for a display of the most positive display plus correction factor.
23	Disconnect test equipment setup from Test Set connector J2, and connect power meter (table 5-25, step 8) and thermistor mount (table 5-25, item 9) to Test Set RF IN/OUT connector J2.

Table 5-29. Power Measurement Calibration - Continued

Step	Procedure
24	On the Test Set: Set MODE switch to SIG GEN CW. Set DISPLAY SELECT switch to FREQ (MHZ). Adjust FREQ 8.4 to 10.0 GHZ COARSE and FINE controls for frequency indication of 8,400 (plus or minus 20) MHz. Verify that ATTENUATION DB 0-80 switch is set to 0.
25	While observing power meter, adjust ATTENUATION DB FINE potentiometer for an indication of 0.00 (plus or minus 0.05) dbm.
26	Set DISPLAY SELECT switch to RF SIG PWR (DBM).
27	Adjust FREQ 8.4 TO 10.0 GHZ COARSE control over the entire 8.4 to 10.0 GHz range while maintaining a 0.00 (plus or minus 0.05) dbm reading on power meter using ATTENUATION DB FINE control. Monitor the Test Set digital display and note both the maximum and minimum reading.
28	Calculate the correction factor and adjust SIG PWR potentiometer 1A1A3VR19 for a display indication of the most positive display plus correction factor.
29	Repeat step 27. Insure that Test Set digital display does not exceed plus or minus 1.0 dbm.
30	Turn ATTENUATION DB FINE potentiometer to midrange.
31	Adjust FREQ 8.4 TO 10.0 GHZ COARSE control over the entire 8.4 to 10.0 GHz range while monitoring the power meter reading. Note the maximum reading.
32	Adjust FREQ 8.4 TO 10.0 GHZ COARSE control to the frequency where maximum power meter reading was obtained.
33	Turn ATTENUATION DB FINE potentiometer ccw until Test Set display value blanks and only -bbbbb is displayed.
34	If Test Set display indicates -bbbbb, proceed to step 35. If Test Set display indicates a value with ATTENUATION DB FINE potentiometer fully ccw, adjust 1A1A3VR14 until display indicates -bbbbb.
35	Disconnect power meter and thermistor mount from Test Set RF IN/OUT connector J2.

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Table 5-30. Attenuator Calibration

Step	Procedure
	NOTE The Power Measurement Calibration procedure of table 5-29 must be performed prior to this procedure.
1	Remove Electronics Assembly 1A1, using the procedure of table 5-4.
2	Set MODE switch to SIG GEN CW.
3	Set DISPLAY SELECT switch to FREQ (MHZ).
4	Set FREQ 8.4 TO 10.0 COARSE control for a digital display indication of 9,200.0 (plus or minus 20.0) MHz.
5	Using thermistor mount (table 5-25, item 9), connect power meter (table 5-25, item 8) to Test Set RF IN/OUT connector J2.
6	Set DISPLAY SELECT switch to RF SIG PWR (DBM).
7	Set ATTENUATION DB 0-80 switch to 0.
8	Set ATTENUATION DB FINE potentiometer for a power meter indication of 0.0 (plus or minus 0.0) dbm.
9	Adjust SIG PWR potentiometer 1A1A3VR19 for a digital display indication of 0.0 (plus or minus 0.0) dbm.
10	Set ATTENUATION DB 0-80 switch to 10.
11	Set ATTENUATION DB FINE potentiometer for a power meter indication of -10.0 (plus or minus 0.0) dbm.
12	Adjust 10 DB potentiometer 1A1A3VR3 for a digital display indication of -10.0 (plus or minus 0.0) dbm.
13	Set ATTENUATION DB 0-80 switch to 20.
14	Set ATTENUATION DB FINE potentiometer for a power meter indication of -20.0 (plus or minus 0.0) dbm.
15	Adjust 20 DB potentiometer 1A1A3VR4 for a digital display indication of -20.0 (plus or minus 0.0) dbm.

Table 5-30. Attenuator Calibration - Continued

Step	Procedure
	NOTE Do not disturb the setting of the ATTENUATION DB FINE potentiometer during steps 16 through 18.
16	Disconnect power meter.
17	Connect attenuator and signal calibrator (table 5-25, item 12), heterodyne mixer-oscillator (table 5-25, item 13), and attenuation standards (table 5-25, item 14) to calibrate the signal from RF IN/OUT connector J2.
18	Adjust heterodyne mixer-oscillator and attenuation standards to obtain a reference indication on the attenuator and signal calibrator. Record this reference indication.
19	Set standard attenuator to increase attenuation by 10.0 db.
20	Set ATTENUATION DB 0-80 switch to 30.
21	Set ATTENUATION DB FINE potentiometer for an attenuator and signal calibrator indication equal to the reference indication recorded in step 18.
22	Adjust 30 DB potentiometer 1A1A3VR5 for a digital display indication of -30.0 (plus or minus 0.0) dbm.
23	Repeat steps 19 through 22 for the 40 through 60 positions of the ATTENUATION DB 0-80 switch, adjusting the 40 DB through 60 DB potentiometers as follows:

ATTENUATION DB 0-80 switch position	Adjust potentiometer 1A1A3	Test Set digital display indication
40	VR6 (40 DB)	-40.0 (plus or minus 0.0) dbm
50	VR7 (50 DB)	-50.0 (plus or minus 0.0) dbm
60	VR8 (60 DB)	-60.0 (plus or minus 0.0) dbm

Table 5-30. Attenuator Calibration - Continued

Step	Procedure
24	Without disturbing the test setup or Test Set control settings, place Electronics Assembly 1A1 in the combination case. It is not necessary to install the screws.
25	Set standard attenuator to increase attenuation by 10.0 db.
26	Set ATTENUATION DB 0-80 switch to 70.
27	Set ATTENUATION DB FINE potentiometer for an attenuator and signal calibrator indication equal to the reference indication recorded in step 18.
28	Observe indication on Test Set digital display, add 70.0 dbm to the displayed value to obtain the 70 db correction, and record this 70 db correction value. For example, if digital display indicates -70.4 dbm, record -0.4 as the 70 db correction value (-70.4 + 70.0 = -0.4).
29	Set standard attenuator to increase attenuation by 10.0 db.
30	Set ATTENUATION DB 0-80 switch to 80.
31	Set ATTENUATION DB FINE potentiometer for an attenuator and signal calibrator indication equal to the reference indication recorded in step 18.
32	Observe indication on digital display, add 80.0 dbm to the displayed value, and record the result as the 80 db correction value.
33	Disconnect test equipment.
34	Remove the Electronics Assembly from the combination case.
35	Using the procedures of table 5-1, perform steps 1, 2, 3, and 6.
	NOTE When ⌐ ⌙ is displayed, the automatic self-test is completed. By pressing E key, calibration mode of operation is entered.
35a	Press E key on keyboard to advance to calibration step 1, as indicated by b1bbbb on display.

Table 5-30. Attenuator Calibration - Continued

Step	Procedure
36	Observe digital display indication, add the 80 db correction value recorded in step 32 to the digital display indication, and record the result in the 80 db position on the calibration label affixed to the Test Set. For example, if the digital display indicates 80.2 db, and the 80 db correction value is -0.4 db, record 79.8 in the 80 db position on the calibration label (80.2 + (-0.4) = 79.8).
37	Adjust 80 db potentiometer 1A1A3VR10 for a digital display indication equal to the value recorded in step 36.
38	Set ATTENUATION DB 0-80 switch to 70.
39	Observe digital display indication, add the 70 db correction value recorded in step 28 to the digital display indication, and record the result in the 70 db position on the calibration label.
40	Adjust 70 db potentiometer 1A1A3VR9 for a digital display indication equal to the value recorded in step 39.
41	Set ATTENUATION DB 0-80 switch to the 60 through 10 positions; and for each position, record the digital display indication in the corresponding position on the calibration label.

Table 5-31. Attenuator Potentiometer Adjustment

Step	Procedure
1	Remove Electronics Assembly 1A1, using procedure of table 5-4.
2	Using the procedures of table 5-1, perform steps 1, 2, 3, and 6.
	NOTE When [ ] is displayed, the automatic self-test is completed. By pressing E key, calibration mode of operation is entered.
2a	Press E key on the keyboard to advance to calibration step 1, as indicated by b1bbbb on display.
3	Set ATTENUATION DB 0-80 switch to the 10 position.
4	Adjust 10 db potentiometer 1A1A3VR3 for a digital display indication equal to the value entered in the 10 db position on the calibration label affixed to the Test Set.
5	Repeat steps 3 and 4 for the 20 through 80 positions of the ATTENUATION DB 0-80 switch, adjusting the 20 DB through 80 DB potentiometers as follows:

ATTENUATION 0-80 switch position	Adjust potentiometer 1A1A3
20	VR4 (20 DB)
30	VR5 (30 DB)
40	VR6 (40 DB)
50	VR7 (50 DB)
60	VR8 (60 DB)
70	VR9 (70 DB)
80	VR10 (80 DB)

Table 5-32. Range Calibration

Step	Procedure
1	Connect test equipment as shown in figure 5-11, and perform the following: On the Test Set, set MODE switch to RADAR PULSE, DISPLAY SELECT switch to PRF (HZ), and TRIGGER switch to IN POS. On pulse generator, select a positive going 7 volt pulse, 1 microsecond wide, as shown in figure 5-11. While observing Test Set digital display, adjust pulse generator prf for display between 5,000 and 10,000 Hz.
2	Enter a range of 250 yards as follows: Set DISPLAY SELECT switch to RANGE (YDS). Using the keyboard, enter 250. A flashing 1 will be displayed when the first key is pressed. NOTE The entered value may be cleared at this time by pressing the CE (clear entry) key. Press E (enter) key. The flashing 1 will remain until the Test Set accepts the entered value.
3	Enter a range rate of -100 knots as follows: Set DISPLAY SELECT switch to RANGE RATE (KNS). Using keyboard, enter 100 then press +/- key. A flashing 1 will be displayed when the first key is pressed. NOTE The entered value may be cleared at this time by pressing the CE (clear entry) key. Press E (enter) key. The flashing 1 will remain until the Test Set accepts the entered value.
4	Adjust RANGE potentiometer 1A1A3VR11 until the delay between the positive edges of the channel A and B pulses, as observed on oscilloscope, is as close as possible to 1.525 microsecond. The channel B waveform moves in steps of 0.061 microsecond.
5	Disconnect test equipment.

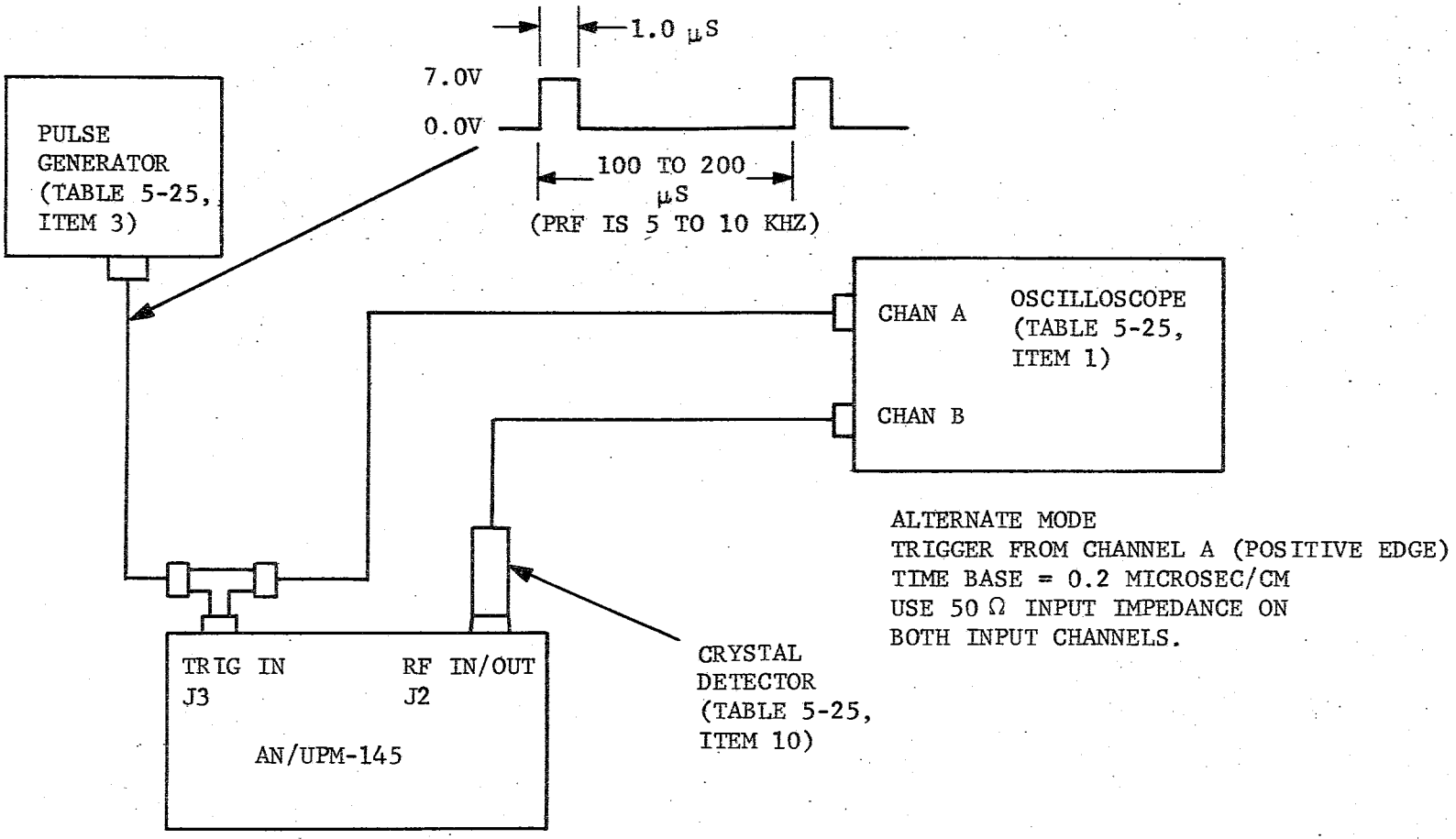


Figure 5-11. Range Calibration Test Equipment Setup

Table 5-33. Reference D/A Calibration

Step	Procedure
1	Remove Electronics Assembly 1A1, using the procedures of table 5-4.
2	Using the procedures of table 5-1, perform steps 1, 2, 3, and 6.
	NOTE When ⌊ ⌋ is displayed, the automatic self-test is completed. By pressing E key, calibration mode of operation is entered.
2a	Press E key on the keyboard to advance to calibration step 2 as indicated by b2bbbb on display.
3	Connect DVM (table 5-25, item 2) to D/A REF test point 1A1A3TP52 and connect DVM ground level to chassis ground.
4	While observing DVM, adjust D/A REF potentiometer 1A1A3VR2 for a -10.20 (plus or minus 0.02) vdc indication on DVM.
5	Disconnect DVM.

Table 5-34. Gunn Oscillator Voltage Regulator Adjustment

Step	Procedure
1	Remove Electronics Assembly 1A1, using the procedures of table 5-4.
2	Connect DVM (table 5-25, item 2) to test point 1A1A5A1TP1 on Gunn Oscillator Regulator 1A1A5A1. Connect DVM return lead to standoff 1A1A5A1E3 or E4 or E6.
3	Adjust potentiometer 1A1A5A1VR1 until DVM indication is equal to the voltage listed on the label affixed to Gunn Oscillator 1A1A5Y1.
4	Disconnect DVM.

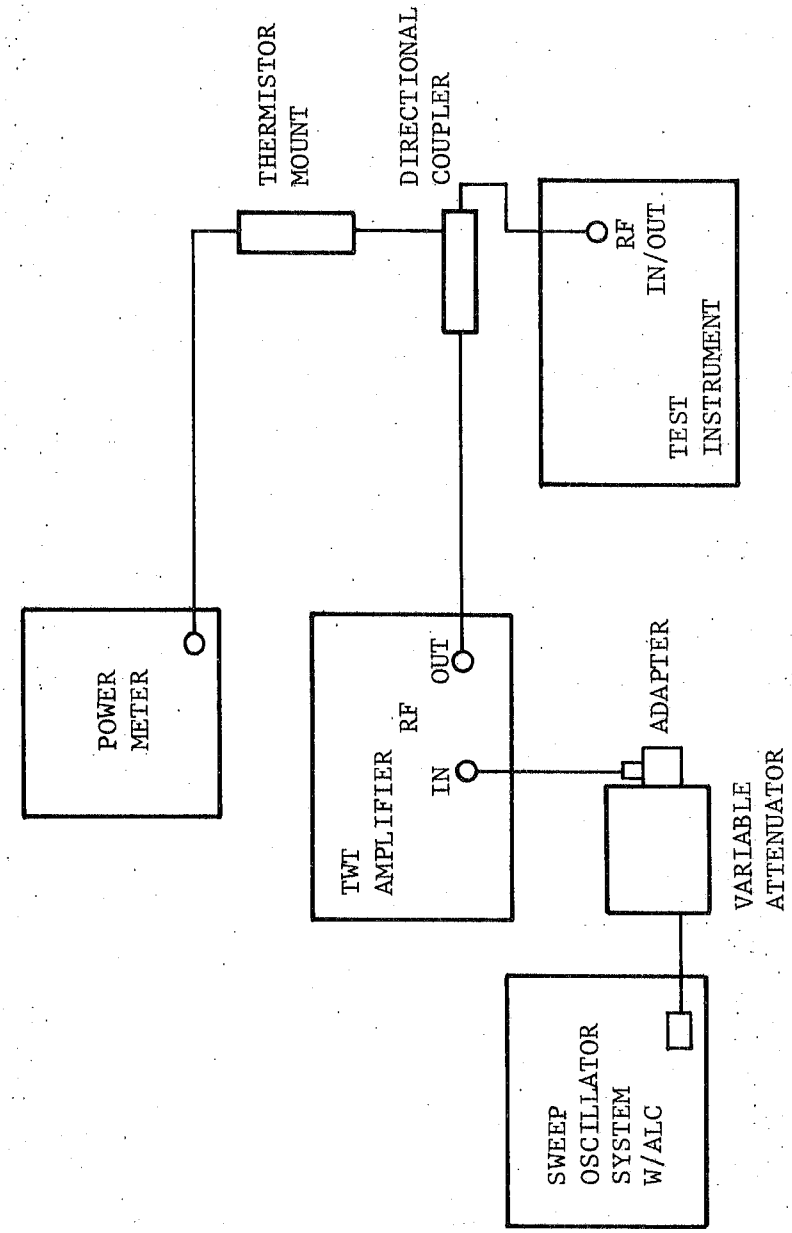


Figure 5-10. Power Calibration Test Equipment Setup

Table 5-30. Attenuator Calibration

Step	Procedure
	NOTE The Power Measurement Calibration procedure of table 5-29 must be performed prior to this procedure.
1	Insure that Electronics Assembly 1A1 is installed in case. It is not necessary to install all screws.
2	Set MODE switch to SIG GEN CW.
3	Set DISPLAY SELECT switch to FREQ (MHZ).
4	Set FREQ 8.4 TO 10.0 GHZ COARSE control for a digital display indication of 8,400 (plus or minus 20.0) MHz.
5	Using thermistor mount (table 5-25, item 9), connect power meter (table 5-25, item 8) to Test Set RF IN/OUT connector J2.
6	Set DISPLAY SELECT switch to RF SIG PWR (DBM).
7	Set ATTENUATION DB 0-80 switch to 0.
8	Set ATTENUATION DB FINE potentiometer for a power meter indication of 0.0 (plus or minus 0.05) dbm at 8,400 MHz.
9	Record exact Test Set display.
10	Repeat steps 8 and 9 for frequencies of 9,200 and 10,000 MHz.
11	Set Test Set output level to minimum and disconnect power meter.
12	Connect Test Set to Attenuator Calibrator (table 5-25, item 12).
13	Set Test Set DISPLAY SELECT to FREQ (MHZ) and adjust FREQ COARSE and FINE controls for a display of 8,400 MHz.
14	Set Test Set DISPLAY SELECT to RF SIG PWR (DBM) and adjust ATTENUATION DB and FINE controls for display recorded in step 9.
15	Detect and capture the Test Set RF signal with the Attenuator Calibrator.
16	Adjust Attenuator Calibrator STANDARD ATTENUATOR for null on Amplitude Balance Meter. Record STANDARD ATTENUATOR setting.
17	Set ATTENUATOR DB FINE potentiometer for a Test Set display of -5.0 (plus or minus 0.1) dbm.

Table 5-30. Attenuator Calibration - Continued

Step	Procedure
18	Adjust the Attenuator Calibrator for an increase of 15.0 (plus or minus 0.05) db of attenuation.
19	Set ATTENUATOR DB 0-80 switch to 10.
20	Set ATTENUATOR DB FINE potentiometer for a null on Standard Attenuator AMPLITUDE BALANCE meter. Record Test Set display.
21	Step the ATTENUATOR DB 0-80 switch to each decade, adjusting the STANDARD ATTENUATOR for an increase of 10 (plus or minus 0.05) dbm at each Test Set decade. Adjust ATTENUATOR DB FINE potentiometer to null the Standard Attenuator AMPLITUDE BALANCE meter at each step. Record Test Set display at each decade.
22	Repeat steps 12 through 20 at a frequency of 10,000 (plus or minus 20.0) MHz.
23	Repeat steps 12 through 20 at a frequency of 9,200 (plus or minus 20.0) MHz.
24	Calculate the correction factor as shown below for each decade at the three frequencies. [(nominal value in dbm) + (worse case error)] - (most positive Test Set display) = correction factor where: nominal value in dbm = power at J2 worse case error = $\frac{\text{(most positive error)} - \text{(most negative error)}}{2}$ most positive error = (most positive Test Set display) - (nominal value) most negative error = (least positive Test Set display) - (nominal value)
25	Disconnect Test Set from Attenuator Calibrator. Remove Electronics Assembly 1A1 from case.
26	Using the procedures of table 5-1, perform steps 1, 2, 3, and 6.

Table 5-30. Attenuator Calibration - Continued

Step	Procedure
	NOTE When [ ] is displayed, the automatic self-test is completed. By pressing E key, calibration mode of operation is entered.
27	Press E key on the keyboard to advance to calibration step 1, as indicated by +1bXXX on display.
	NOTE Display has an assumed negative value.
28	Using the calculated correction factors, adjust the 10 db through 80 db potentiometer as follows:

ATTENUATION DB 0-80 switch position	Adjust potentiometer 1A1A3	Test Set digital display indication
10	VR3	Displayed value plus correction factor.
20	VR4	Displayed value plus correction factor.
30	VR5	Displayed value plus correction factor.
40	VR6	Displayed value plus correction factor.
50	VR7	Displayed value plus correction factor.
60	VR8	Displayed value plus correction factor.
70	VR9	Displayed value plus correction factor.
80	VR10	Displayed value plus correction factor.

29	After adjustment, replace Electronics Assembly 1A1 in case and verify that displayed values have not changed.

Table 5-31. Range Calibration

Step	Procedure
1	Connect test equipment as shown in figure 5-11, and perform the following: On the Test Set, set MODE switch to RADAR PULSE, DISPLAY SELECT switch to PRF (HZ), and TRIGGER switch to IN POS. On pulse generator, select a positive going 7 volt pulse, 1 microsecond wide, as shown in figure 5-11. While observing Test Set digital display, adjust pulse generator prf for display between 5,000 and 10,000 Hz.
2	Enter a range of 250 yards as follows: Set DISPLAY SELECT switch to RANGE (YDS). Using the keyboard, enter 250. A flashing 1 will be displayed when the first key is pressed. NOTE The entered value may be cleared at this time by pressing the CE (clear entry) key. Press E (enter) key. The flashing 1 will remain until the Test Set accepts the entered value.
3	Enter a range rate of -100 knots as follows: Set DISPLAY SELECT switch to RANGE RATE (KNS). Using keyboard, enter 100 then press +/- key. A flashing 1 will be displayed when the first key is pressed. NOTE The entered value may be cleared at this time by pressing the CE (clear entry) key. Press E (enter) key. The flashing 1 will remain until the Test Set accepts the entered value.
4	Adjust RANGE potentiometer 1A1A3VR11 until the delay between the positive edges of the channel A and B pulses, as observed on oscilloscope, is as close as possible to 1.525 microsecond. The channel B waveform moves in steps of 0.061 microsecond.
5	Disconnect test equipment.

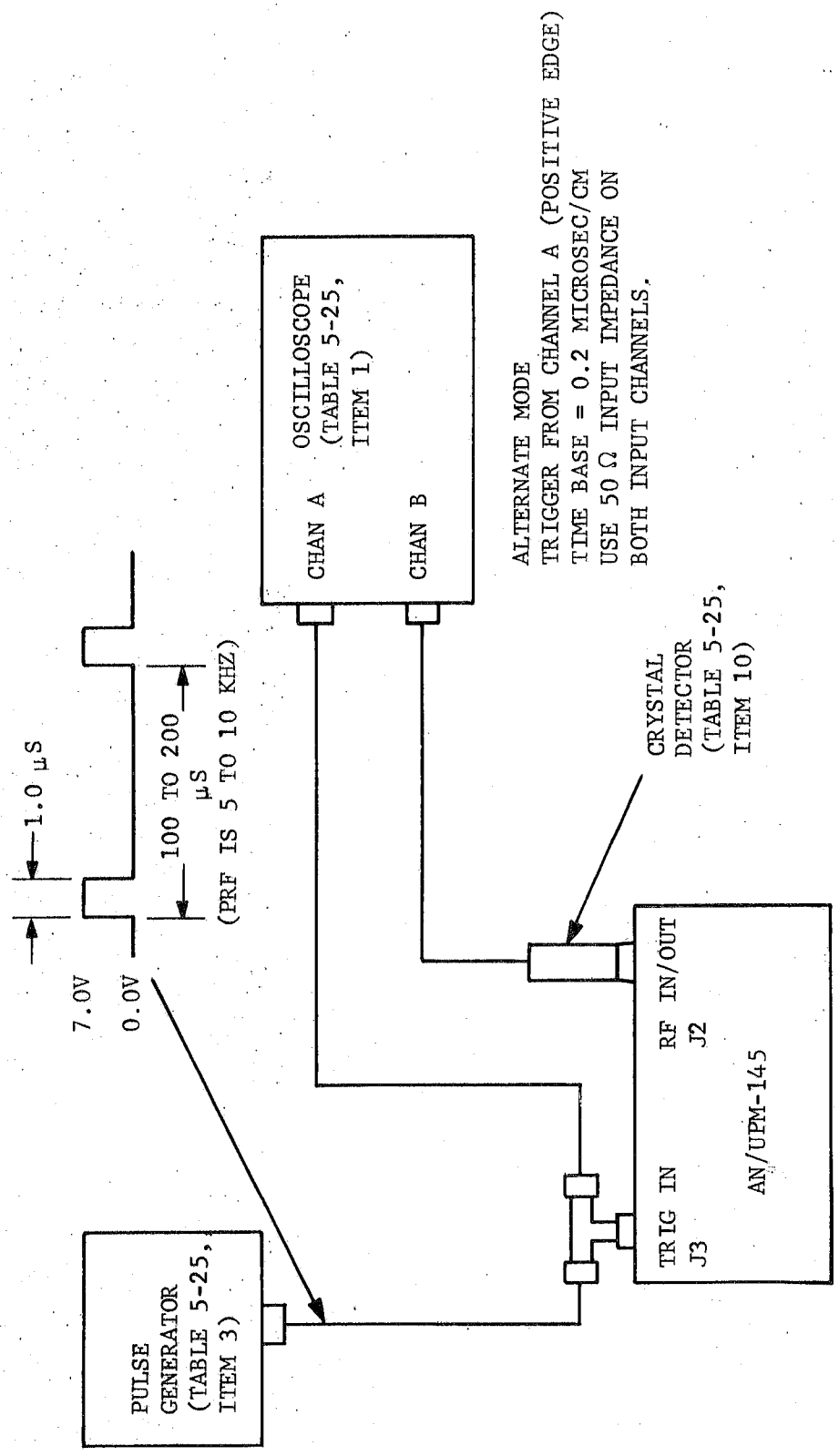


Figure 5-11. Range Calibration Test Equipment Setup

Table 5-32. Reference D/A Calibration

Step	Procedure
1	Remove Electronics Assembly 1A1, using the procedures of table 5-4.
2	Using the procedures of table 5-1, perform steps 1, 2, 3, and 6. NOTE When ⊏ ⊐ is displayed, the automatic self-test is completed. By pressing E key, calibration mode of operation is entered.
2a	Press E key on the keyboard to advance to calibration step 2 as indicated by b2bbbb on display.
3	Connect DVM (table 5-25, item 2) to D/A REF test point 1A1A3TP52 and connect DVM ground level to chassis ground.
4	While observing DVM, adjust D/A REF potentiometer 1A1A3VR2 for a 10.20 (plus or minus 0.02) vdc indication on DVM.
5	Disconnect DVM.

Table 5-33. Gunn Oscillator Voltage Regulator Adjustment

Step	Procedure
1	Remove Electronics Assembly 1A1, using the procedures of table 5-4.
2	Connect DVM (table 5-25, item 2) to test point 1A1A5A1TP1 on Gunn Oscillator Regulator 1A1A5A1. Connect DVM return lead to standoff 1A1A5A1E3 or E4 or E6.
3	Adjust potentiometer 1A1A5A1VR1 until DVM indication is equal to the voltage listed on the label affixed to Gunn Oscillator 1A1A5Y1.
4	Disconnect DVM.

SECTION VI

DIAGRAMS

6-1. GENERAL. This section contains the functional diagrams, schematic diagrams, and wire data lists necessary for maintenance of the Test Set. The functional diagrams are in support of the theory of operation of Section IV, and are arranged in the same order as described in the text. The functional diagrams are listed in table 6-1, Index of Diagrams. The wire data list for the Test Set wiring harness is provided in table 6-2.

Table 6-1. Index of Diagrams

Figure number	Diagram
6-1	Overall System Block Diagram
6-2	CPU and I/O Subsystem, Detailed Functional Diagram
6-3	Display Subsystem, Detailed Functional Diagram
6-4	RF Tune and Frequency Measurement Subsystem, Detailed Functional Diagram
6-5	Frequency Modulation Subsystem, Detailed Functional Diagram
6-6	Target Generation Subsystem, Detailed Functional Diagram
6-7	Power Measurements Subsystem, Detailed Functional Diagram
6-8	Measurements Subsystem, Detailed Functional Diagram
6-9	Power Distribution Subsystem, Detailed Functional Diagram
6-10	System Interconnection Block Diagram
6-11	Front Panel Interface 1A1A1 (58139-40020) Schematic Diagram
6-12	Digital Assembly 1A1A2 (58139-40015) Schematic Diagram
6-13	Microwave Interface 1A1A3 (58139-40010) Schematic Diagram
6-14	Microwave Assembly 1A1A4 (58139-40060) Schematic Diagram
6-15	RF Oscillator 1A1A5 (58139-40030) Schematic Diagram

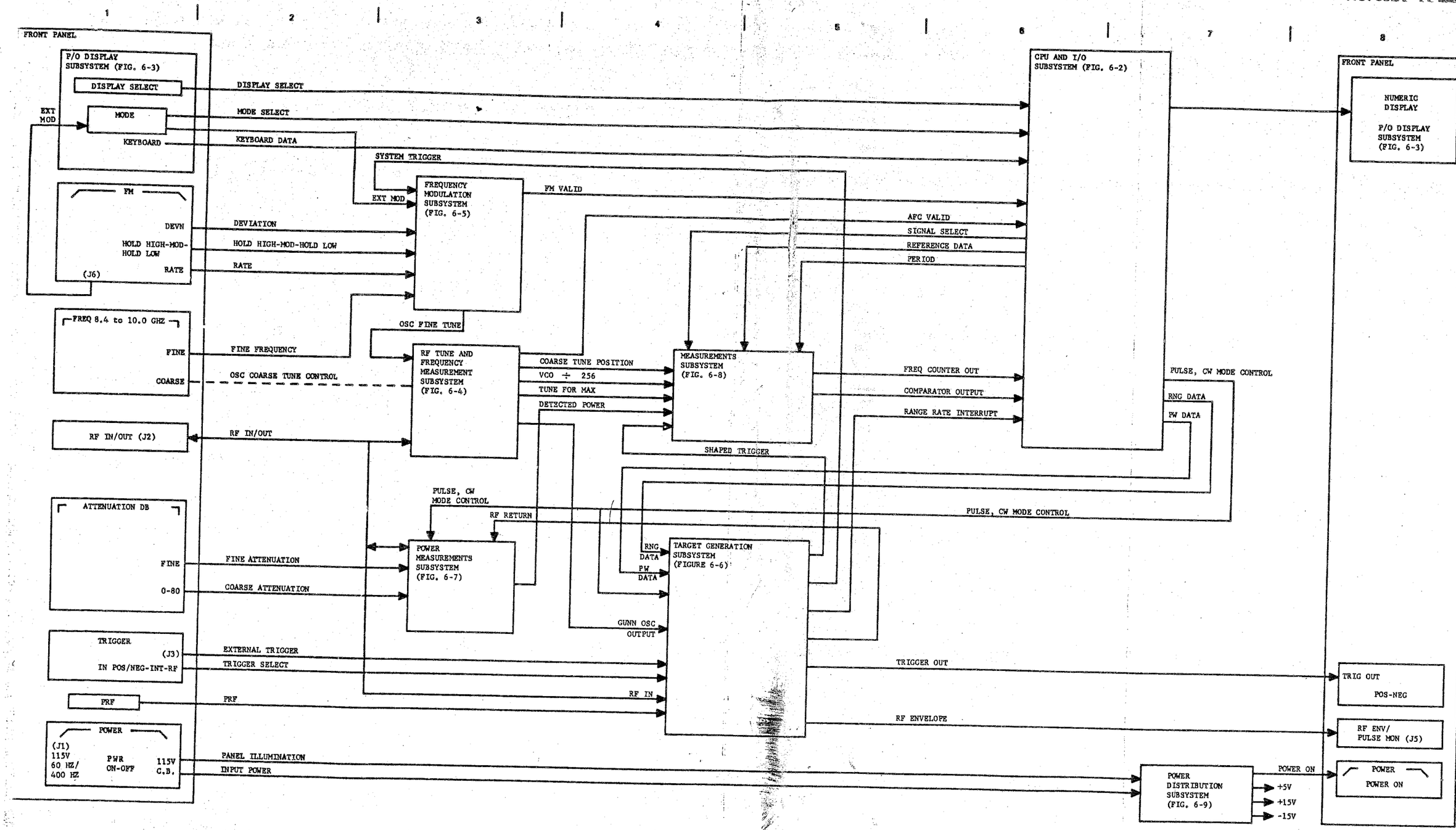


Figure 6-1. Overall System Block Diagram

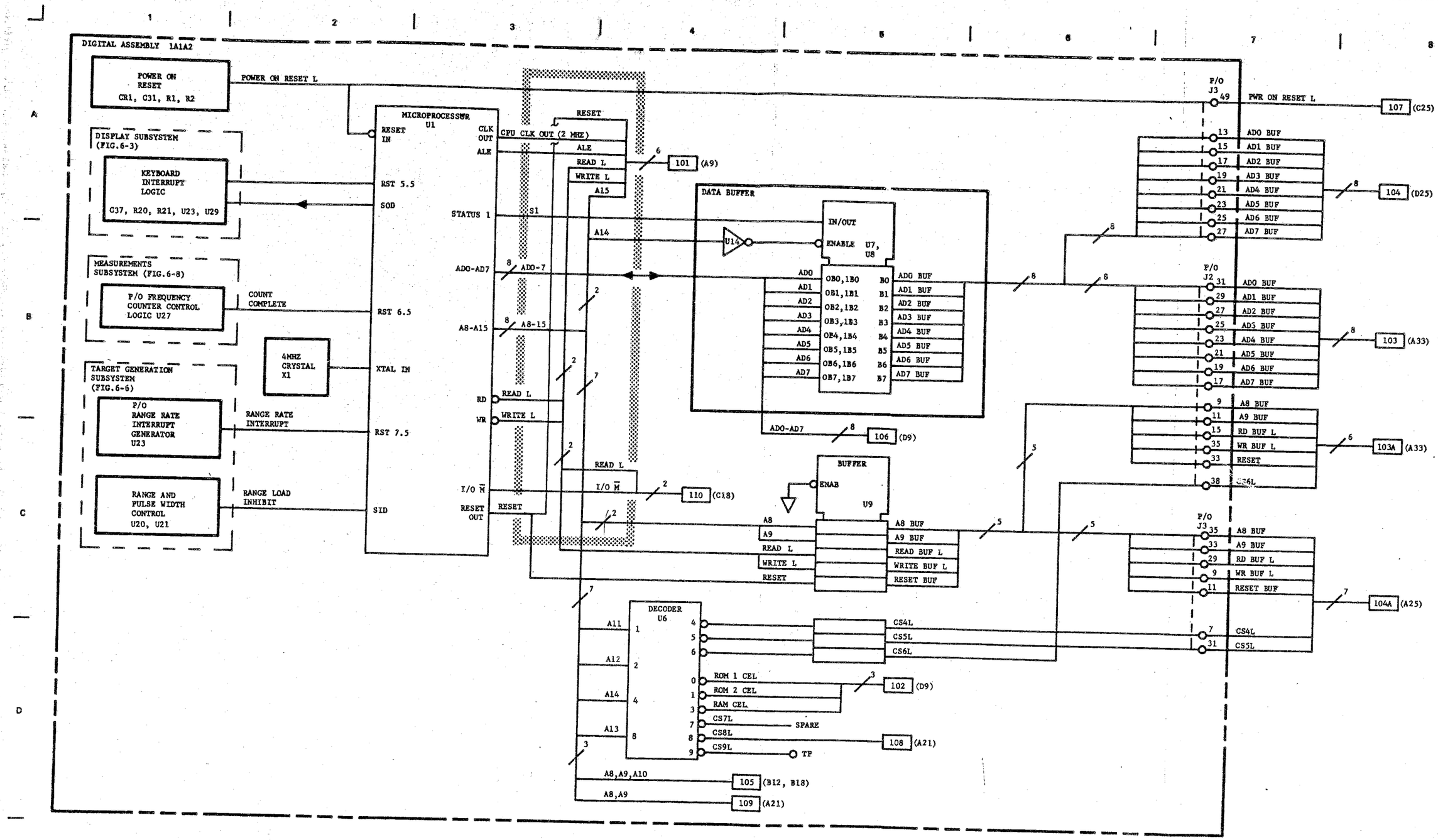


Figure 6-2. CPU and I/O Subsystem, Detailed Functional Diagram (Sheet 1 of 5)

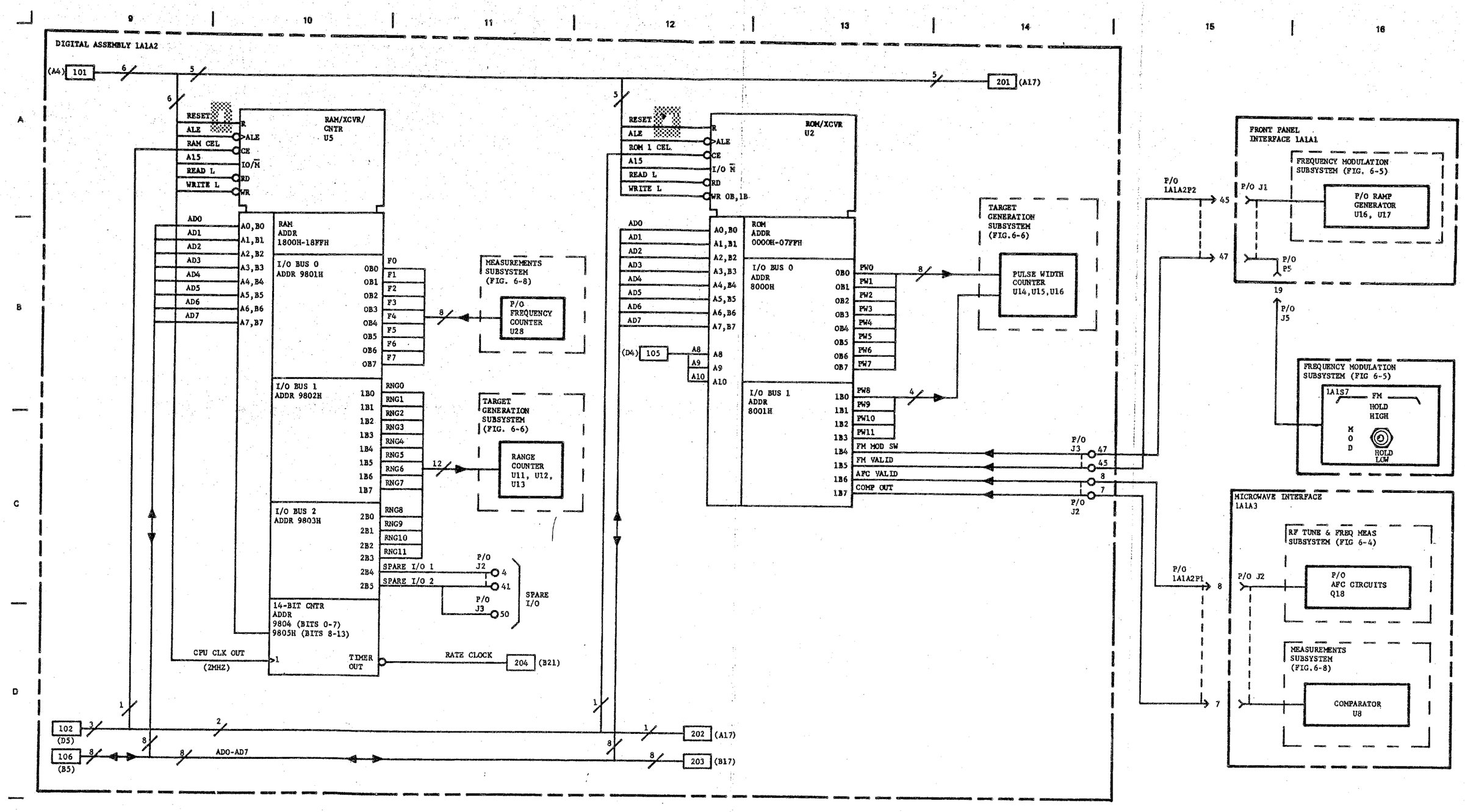


Figure 6-2. CPU and I/O Subsystem, Detailed Functional Diagram (Sheet 2 of 5)

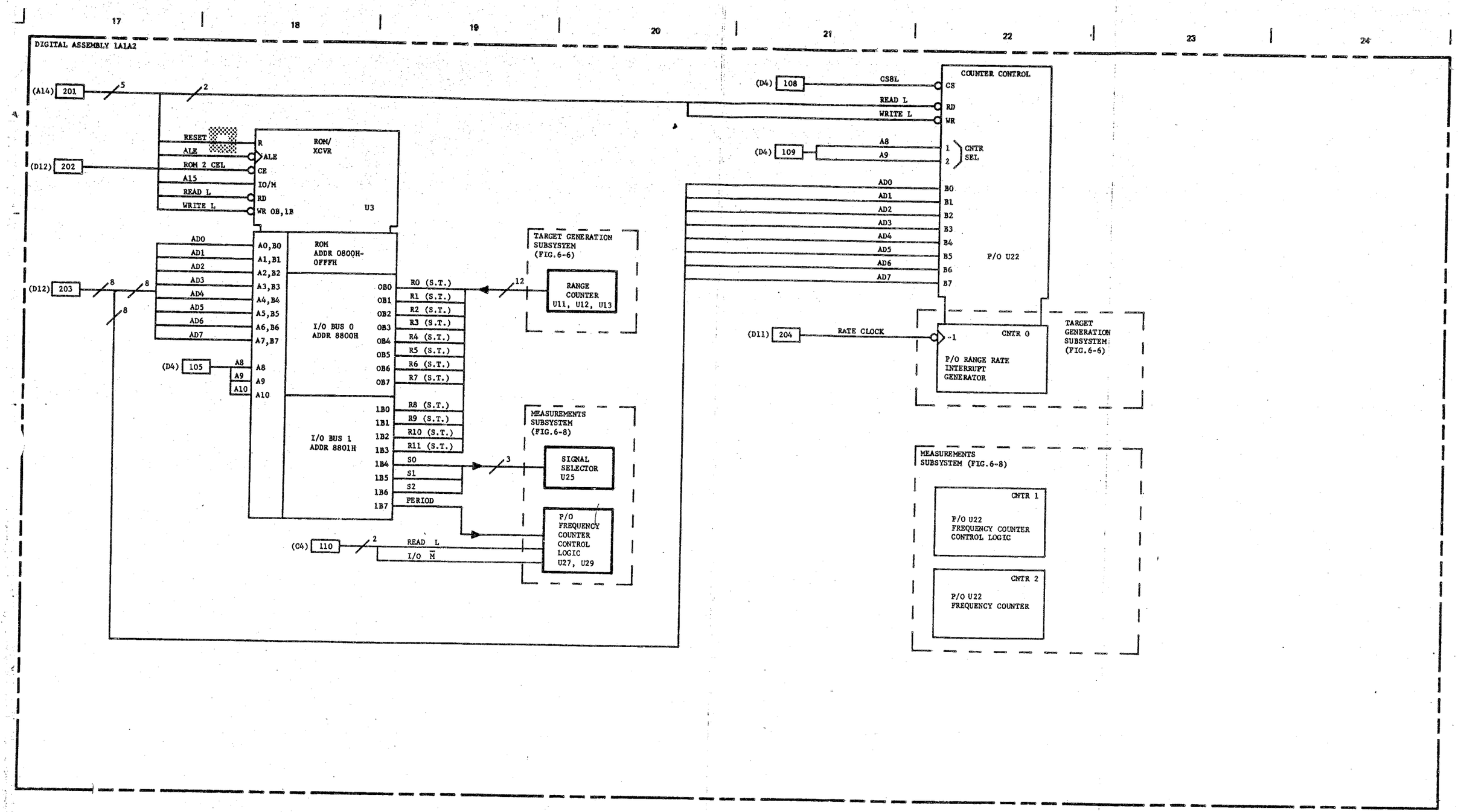


Figure 6-2. CPU and I/O Subsystem, Detailed Functional Diagram (Sheet 3 of 5)

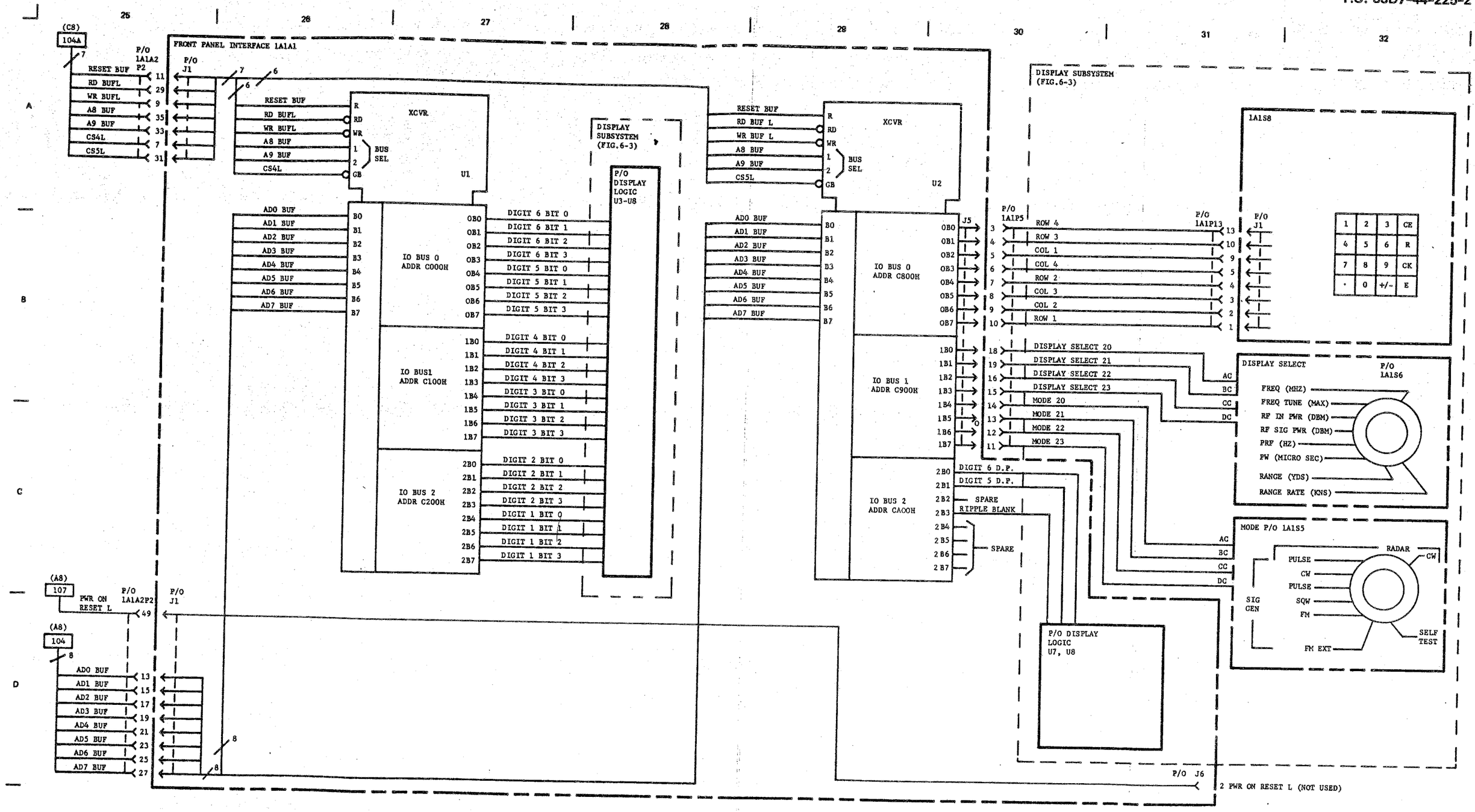


Figure 6-2. CPU and I/O Subsystem, Detailed Functional Diagram (Sheet 4 of 5)

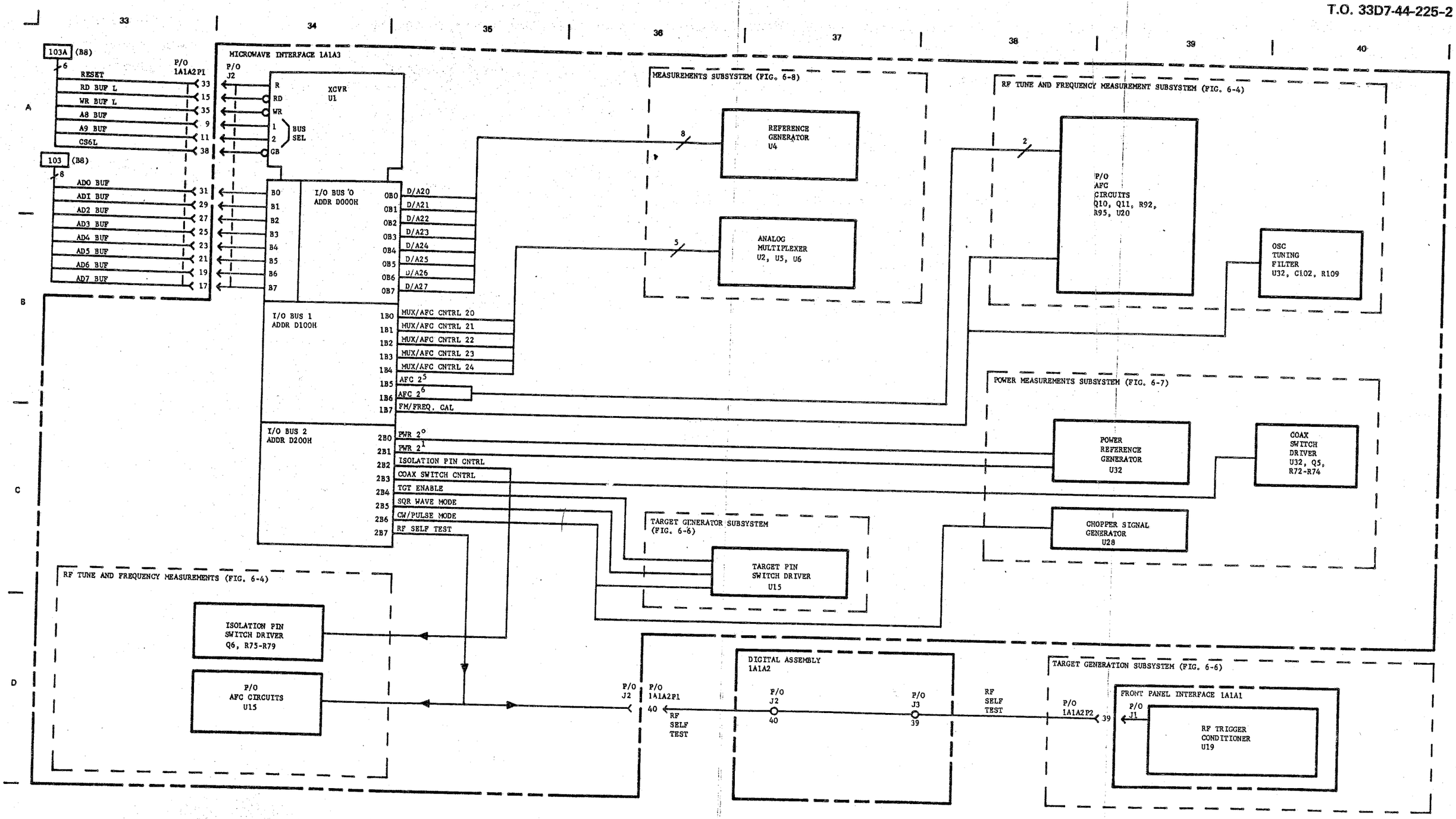


Figure 6-2. CPU and I/O Subsystem, Detailed Functional Diagram (Sheet 5 of 5)

S8 TRUTH TABLE

	OUTPUT							
	L	H	G	E	D	CJ	BK	A
0	0	1	1	1	1	1	0	1
1	1	1	0	1	1	1	1	0
2	1	1	1	1	1	1	0	0
3	1	1	1	1	1	0	1	0
4	1	1	0	1	0	1	1	1
5	1	1	1	1	0	1	0	1
6	1	1	1	1	0	0	1	1
7	1	0	0	1	1	1	1	1
8	1	0	1	1	1	1	0	1
9	1	0	1	1	1	0	1	1
.	0	1	0	1	1	1	1	1
+/-	0	1	1	1	1	0	1	1
E	0	1	1	0	1	1	1	1
CK	1	0	1	0	1	1	1	1
CE	1	1	1	0	1	1	1	0
R	1	1	1	0	0	1	1	1
	4	3	2	1	40	39	38	37

PINS ON U2

S6 TRUTH TABLE

POSITION	OUTPUT BIT 0	1	2	3
FREQ (MHZ)	0	0	0	0
FREQ TUNE (MAX)	1	0	0	0
RF IN PWR (DBM)	0	1	0	0
RF SIG PWR(DBM)	1	1	0	0
PRF (HZ)	0	0	1	0
PW (MICROSEC)	1	0	1	0
RANGE (YDS)	0	1	1	0
RANGE RATE (KNS)	1	1	1	0
	18	19	20	21

PINS ON U2

S5 TRUTH TABLE

POSITION	OUTPUT BIT 0	1	2	3
RADAR CW	0	0	0	0
RADAR PULSE	1	0	0	0
SIG GEN CW	0	1	0	0
SIG GEN PULSE	1	1	0	0
SIG GEN SQW	0	0	1	0
SIG GEN FM	1	0	1	0
SIG GEN FM EXT	0	1	1	0
SELF TEST	1	1	1	0
	22	23	24	25

PINS ON U2

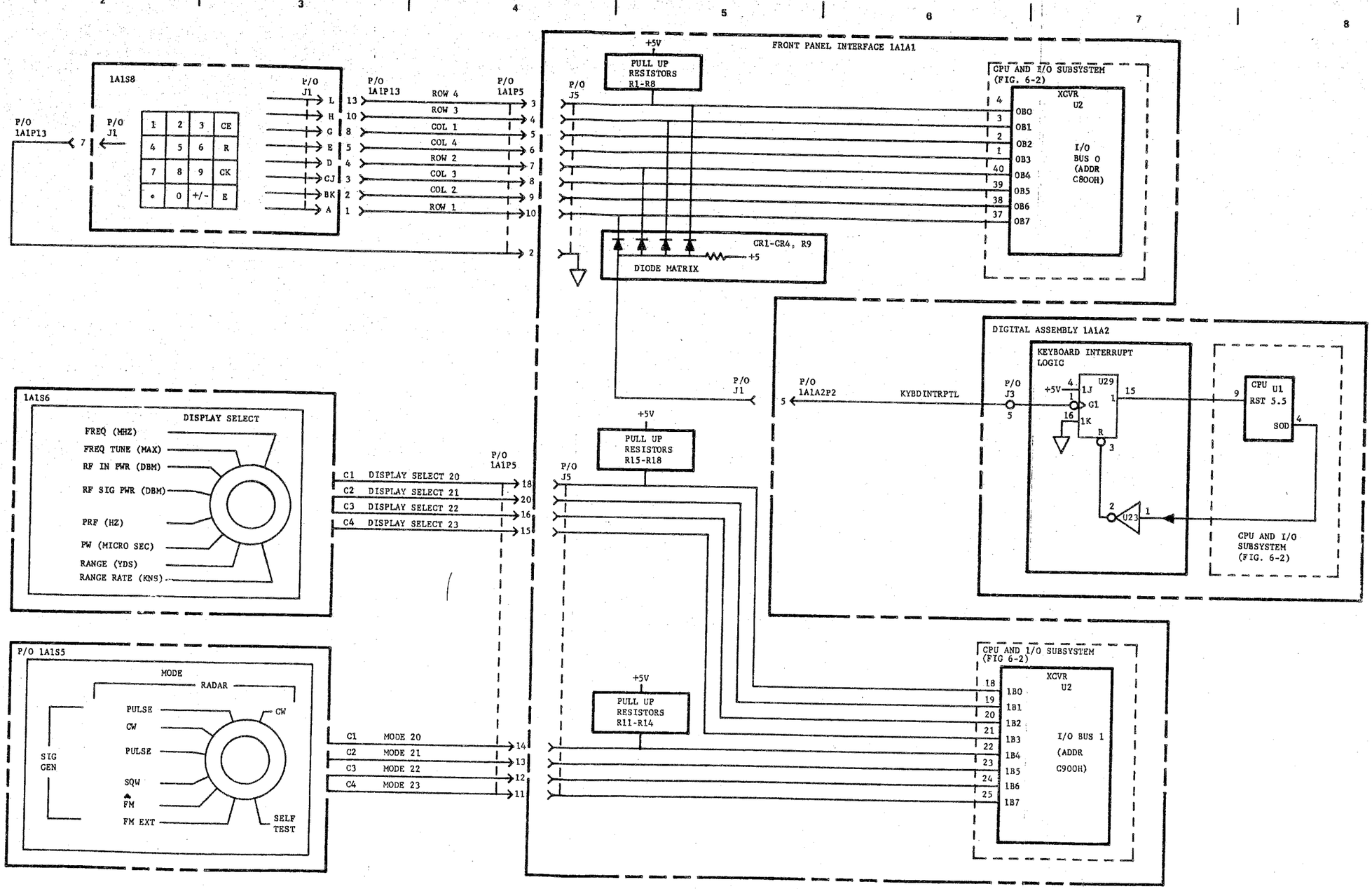


Figure 6-3. Display Subsystem, Detailed Functional Diagram (Sheet 1 of 2)

FRONT PANEL INTERFACE 1A1A1

CPU AND I/O SUBSYSTEM

XCVR U2
I/O BUS 2
(ADDR C400H)
2B0 DIGIT 6 D.P.
2B1 DIGIT 5 D.P.
2B3 RIPPLE BLANK

XCVR U1
I/O BUS 0
(ADDR C000H)
0B0 DIGIT 6 BIT 0
0B1 DIGIT 6 BIT 1
0B2 DIGIT 6 BIT 2
0B3 DIGIT 6 BIT 3
0B4 DIGIT 5 BIT 0
0B5 DIGIT 5 BIT 1
0B6 DIGIT 5 BIT 2
0B7 DIGIT 5 BIT 3

XCVR U1
I/O BUS 1
(ADDR C100H)
1B0 DIGIT 4 BIT 0
1B1 DIGIT 4 BIT 1
1B2 DIGIT 4 BIT 2
1B3 DIGIT 4 BIT 3
1B4 DIGIT 3 BIT 0
1B5 DIGIT 3 BIT 1
1B6 DIGIT 3 BIT 2
1B7 DIGIT 3 BIT 3

XCVR U1
I/O BUS 2
(ADDR C200H)
2B0 DIGIT 2 BIT 0
2B1 DIGIT 2 BIT 1
2B2 DIGIT 2 BIT 2
2B3 DIGIT 2 BIT 3
2B4 DIGIT 1 BIT 0
2B5 DIGIT 1 BIT 1
2B6 DIGIT 1 BIT 2 (SIGN BIT 0)
2B7 DIGIT 1 BIT 3 (SIGN BIT 1)

DISPLAY LOGIC

U8 4# U8 2# U8 6# U8 8# U8 10# U8 12#

U9 3 U9 6 U9 8 U9 11

X → Y DSPL DRVR U7 (RBI, 1, 2, 4, 8, LT, BI/RBO; A B C D E F G)
X → Y DSPL DRVR U6
X → Y DSPL DRVR U5
X → Y DSPL DRVR U4
X → Y DSPL DRVR U3

BIAS RESISTORS R118, R119
BIAS RESISTORS R116, R117
BIAS RESISTORS R109 THROUGH R115
BIAS RESISTORS R102 THROUGH R108
BIAS RESISTORS R95 THROUGH R101
BIAS RESISTORS R88 THROUGH R94, R121
BIAS RESISTORS R81 THROUGH R87, R120

DS1 +1
DS2
DS3 8
DS4 8
DS5 X 8
DS6 X 8

Figure 6-3. Display Subsystem, Detailed Functional Diagram (Sheet 2 of 2)

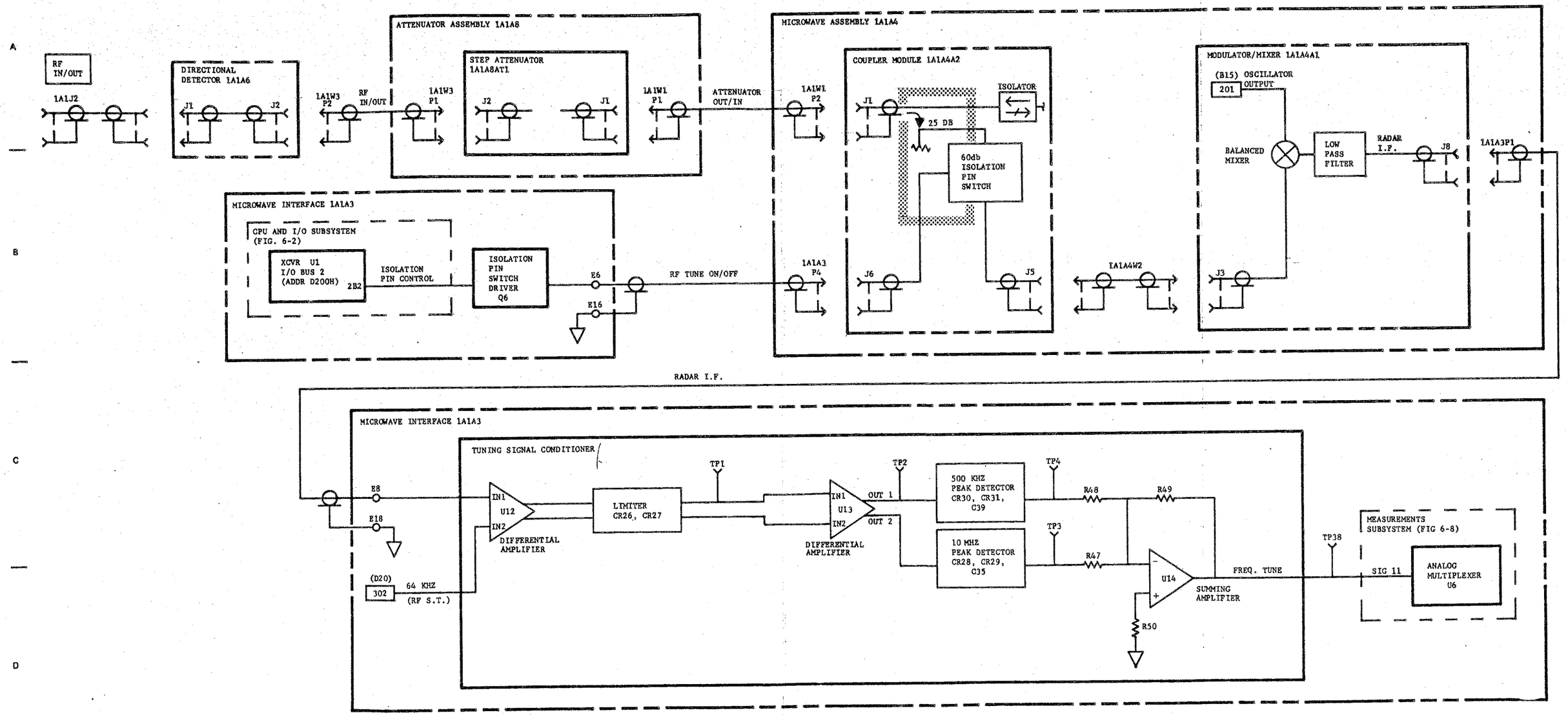


Figure 6-4. RF Tune and Frequency Measurement Subsystem, Detailed Functional Diagram (Sheet 1 of 3)

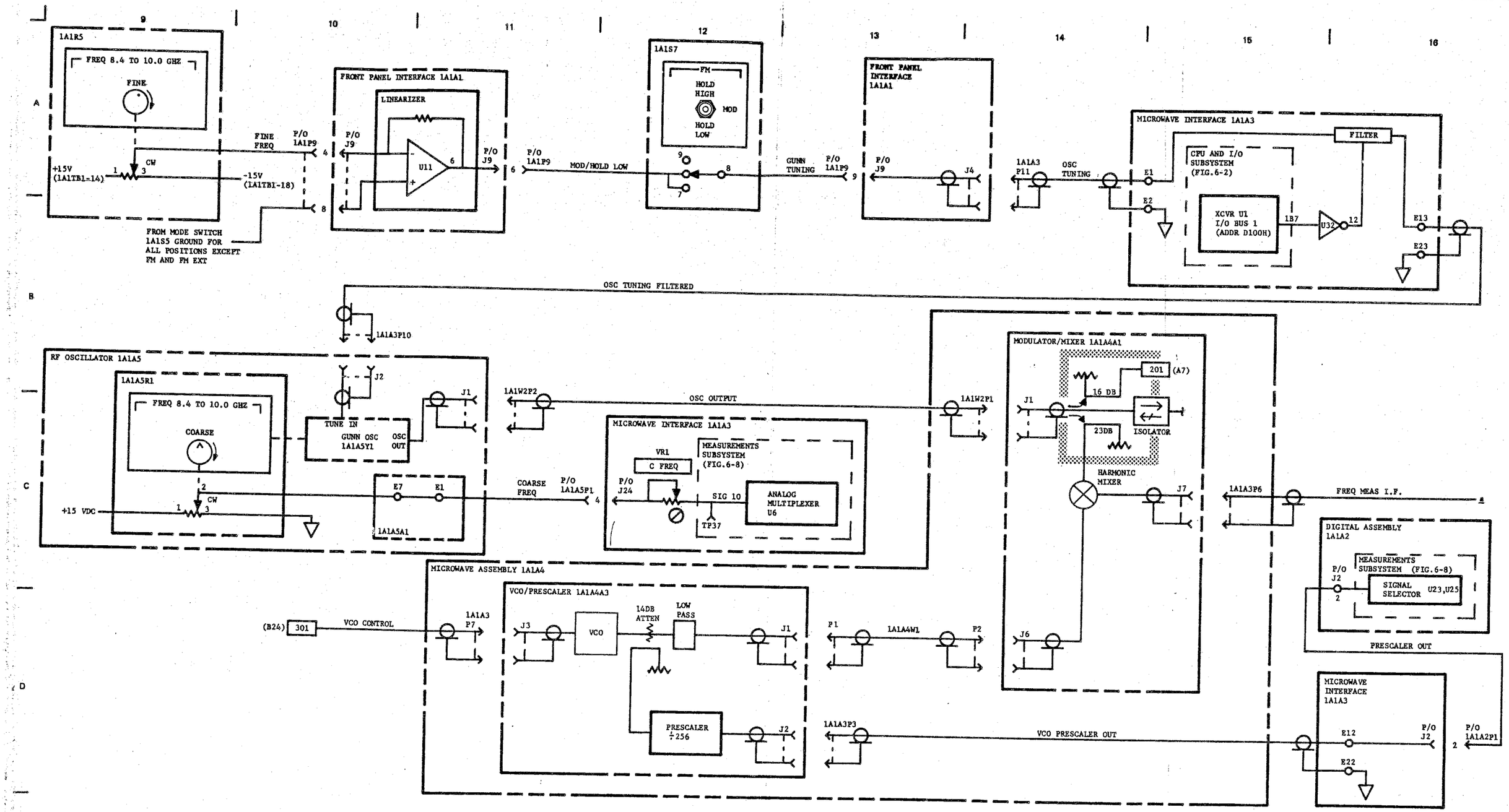


Figure 6-4. RF Tune and Frequency Measurement Subsystem, Detailed Functional Diagram (Sheet 2 of 3)

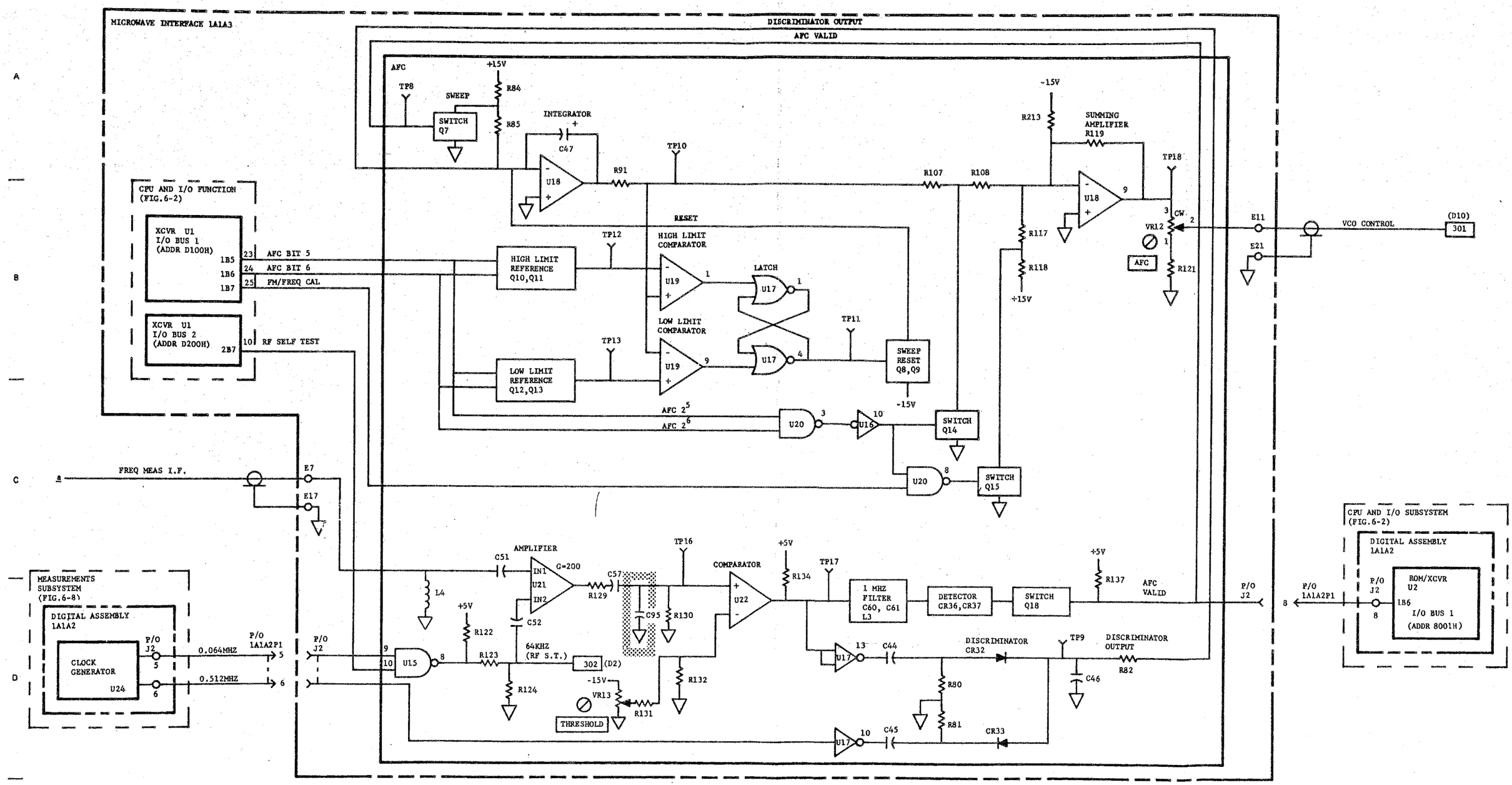


Figure 6-4. RF Tune and Frequency Measurement Subsystem, Detailed Functional Diagram (Sheet 3 of 3)

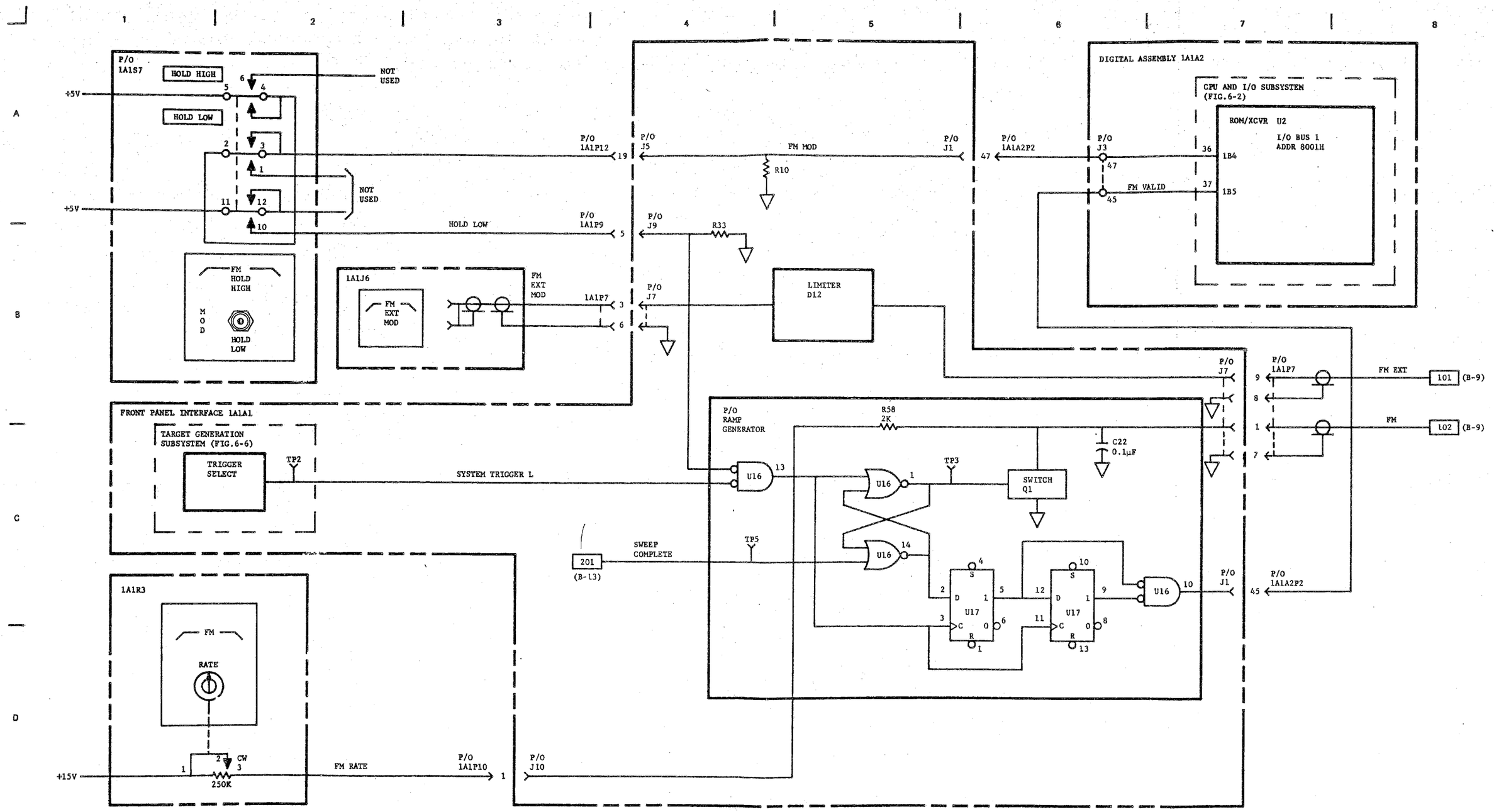


Figure 6-5. Frequency Modulation Subsystem, Detailed Functional Diagram (Sheet 1 of 2)

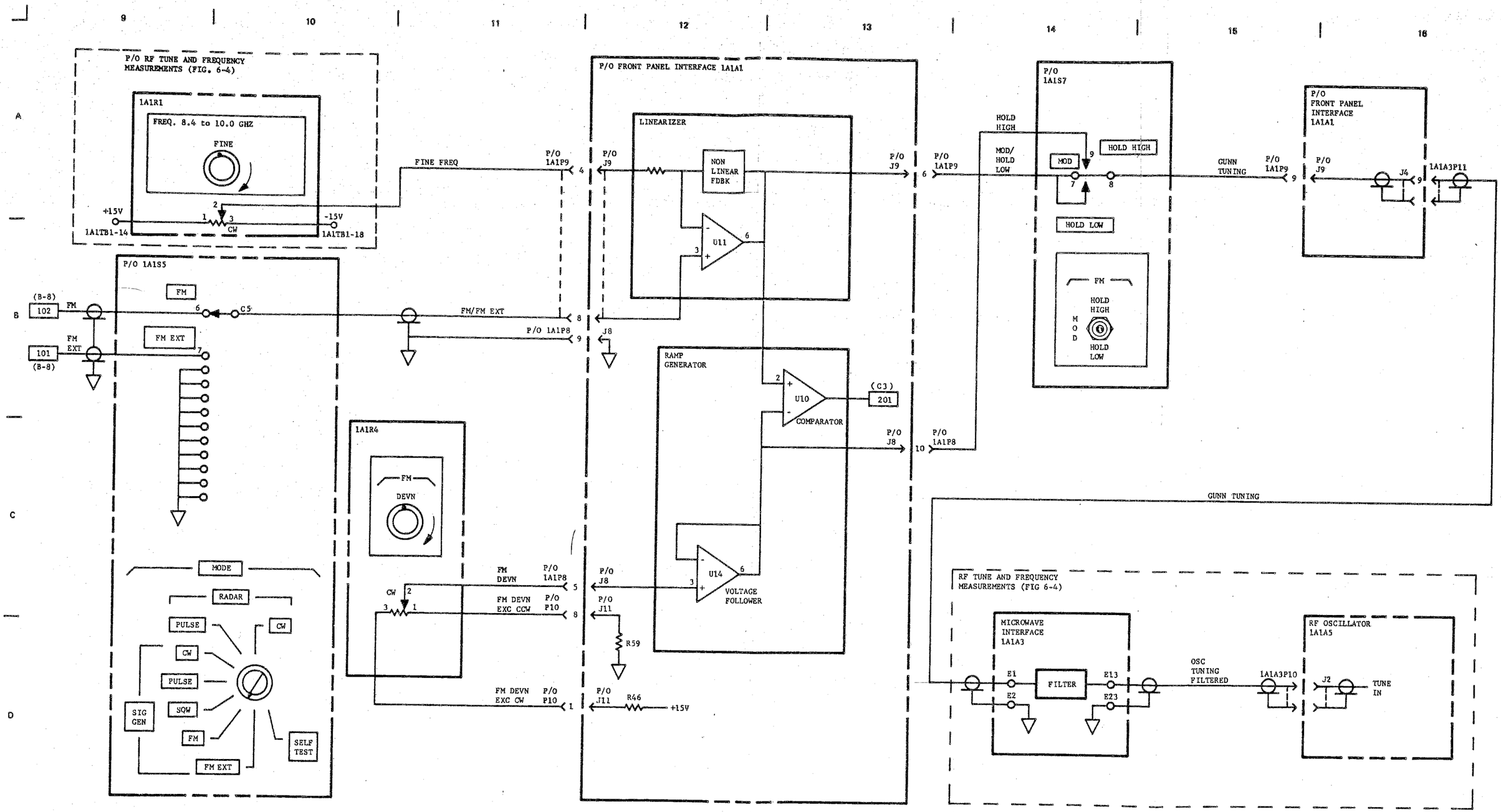


Figure 6-5. Frequency Modulation Subsystem, Detailed Functional Diagram (Sheet 2 of 2)

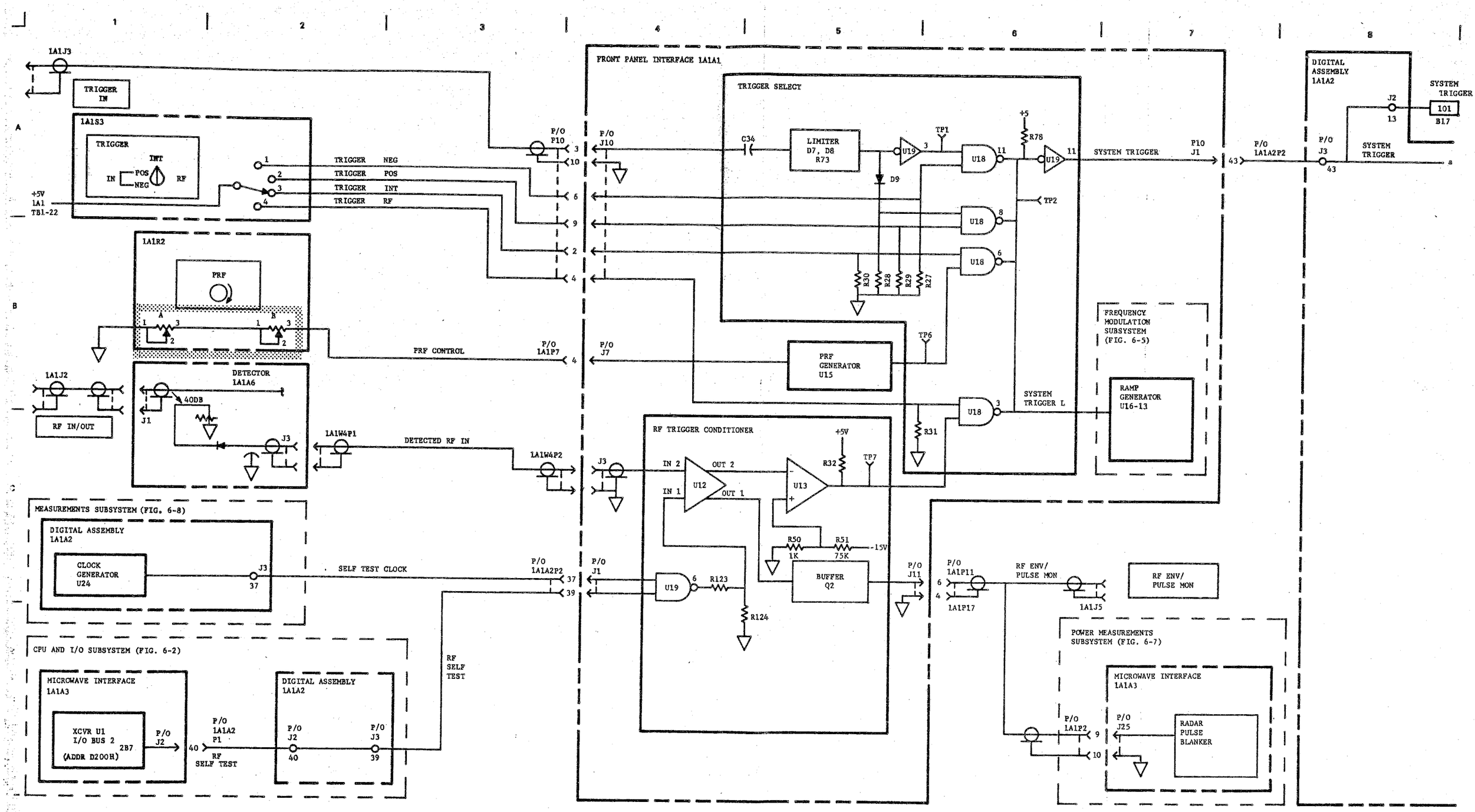


Figure 6-6. Target Generation Subsystem, Detailed Functional Diagram (Sheet 1 of 3)

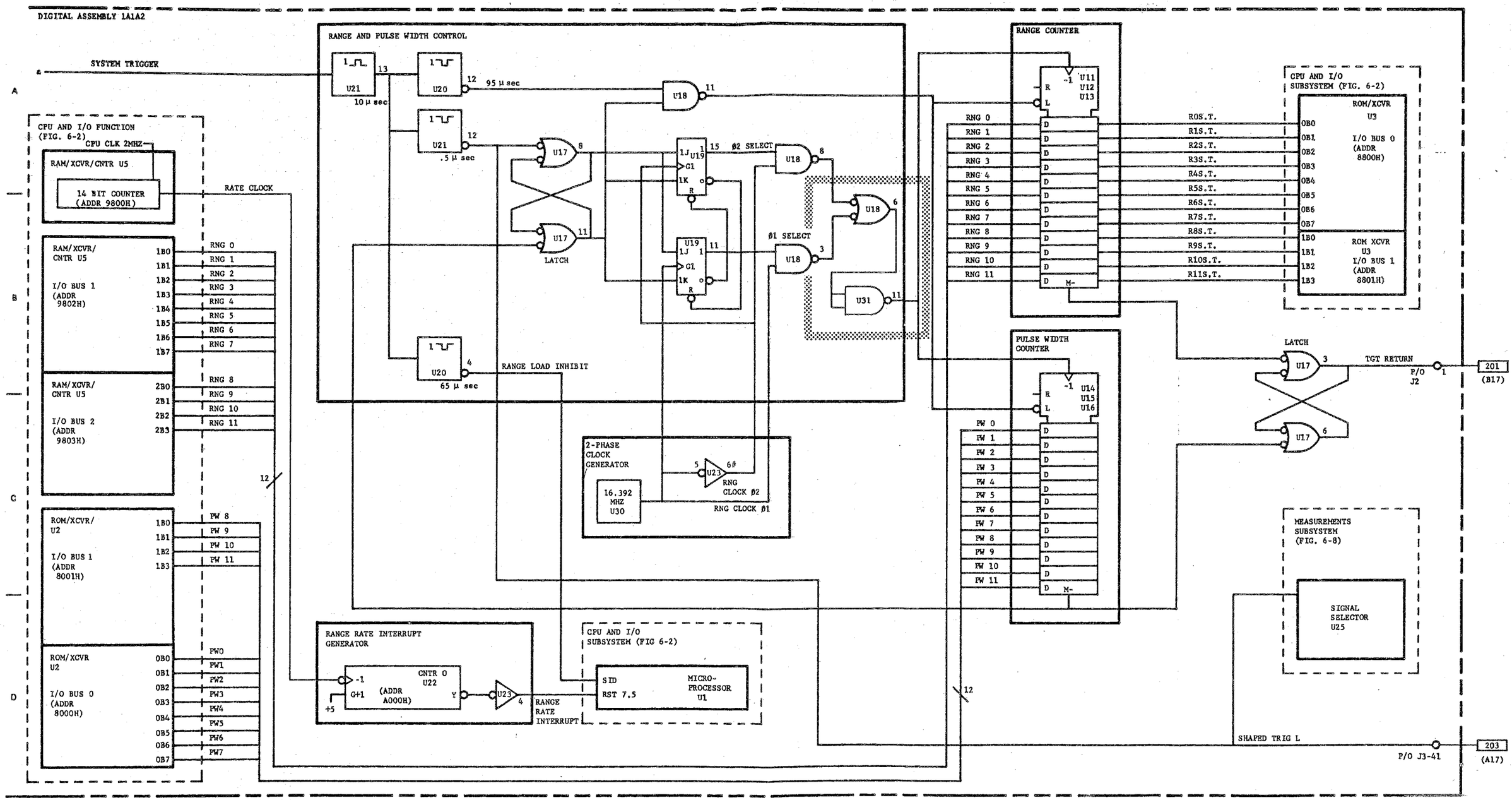


Figure 6-6. Target Generation Subsystem, Detailed Functional Block Diagram (Sheet 2 of 3)

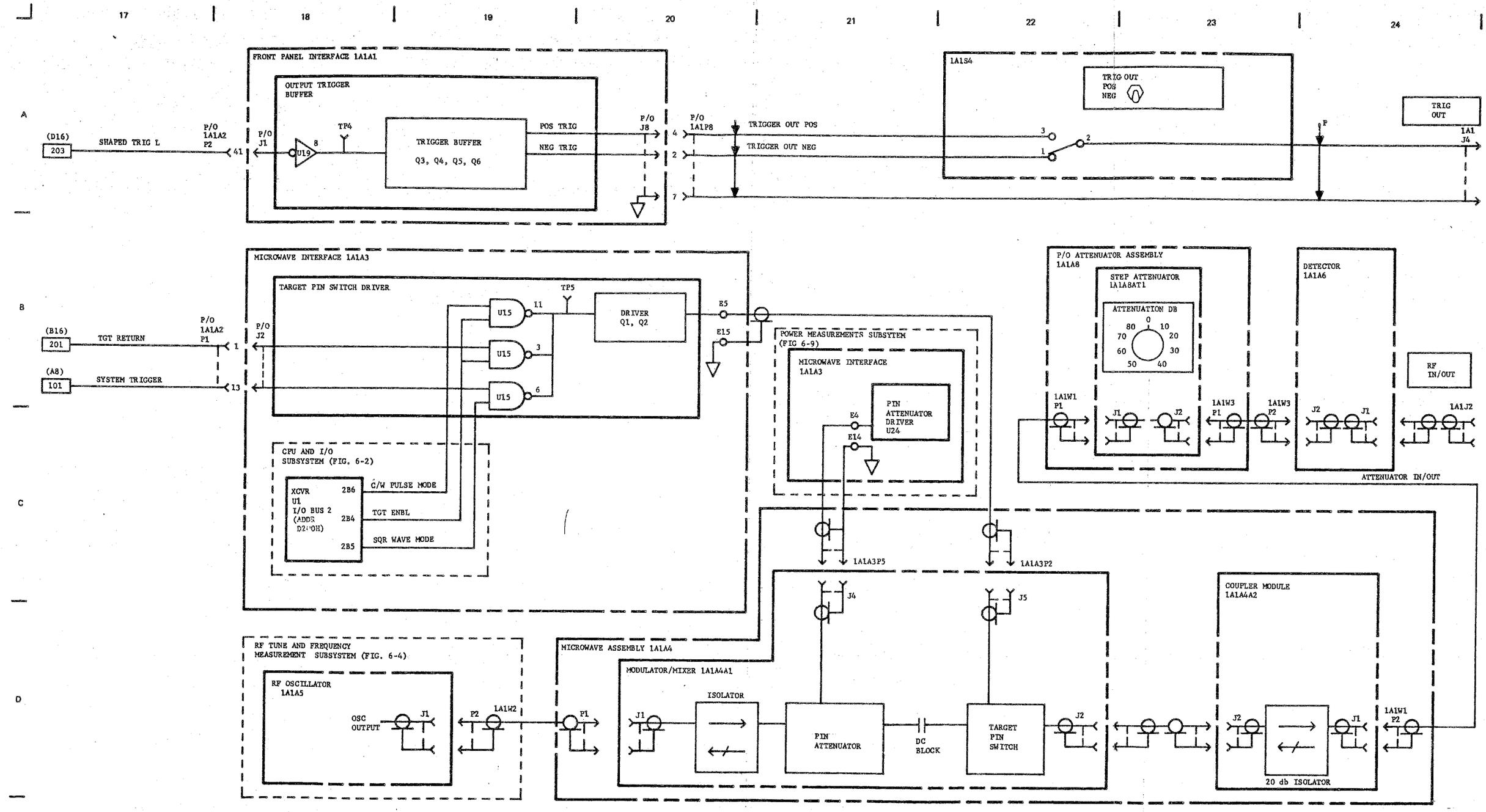


Figure 6-6. Target Generation Subsystem, Detailed Functional Diagram (Sheet 3 of 3)

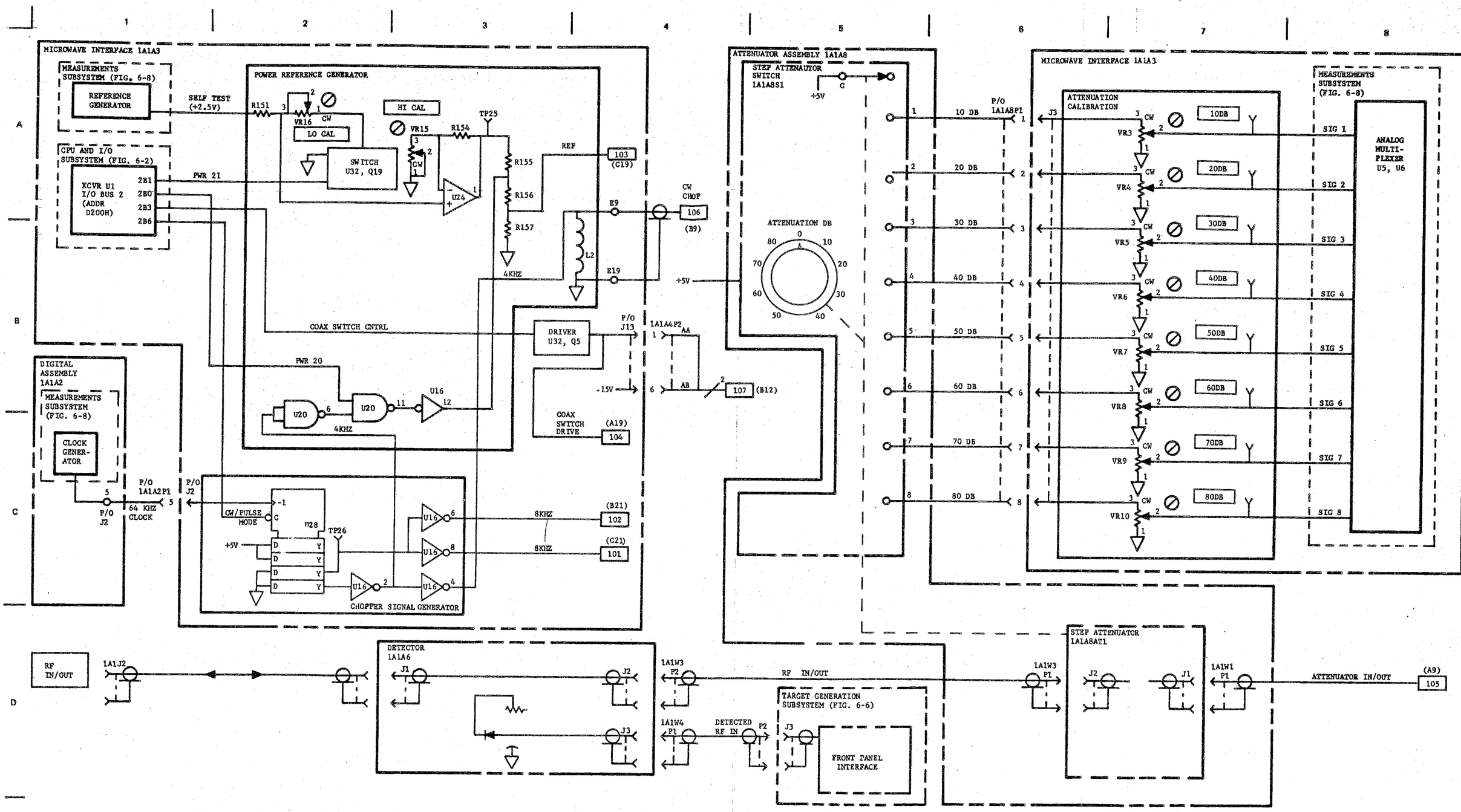


Figure 6-7. Power Measurements Subsystem, Detailed Functional Block Diagram (Sheet 1 of 3)

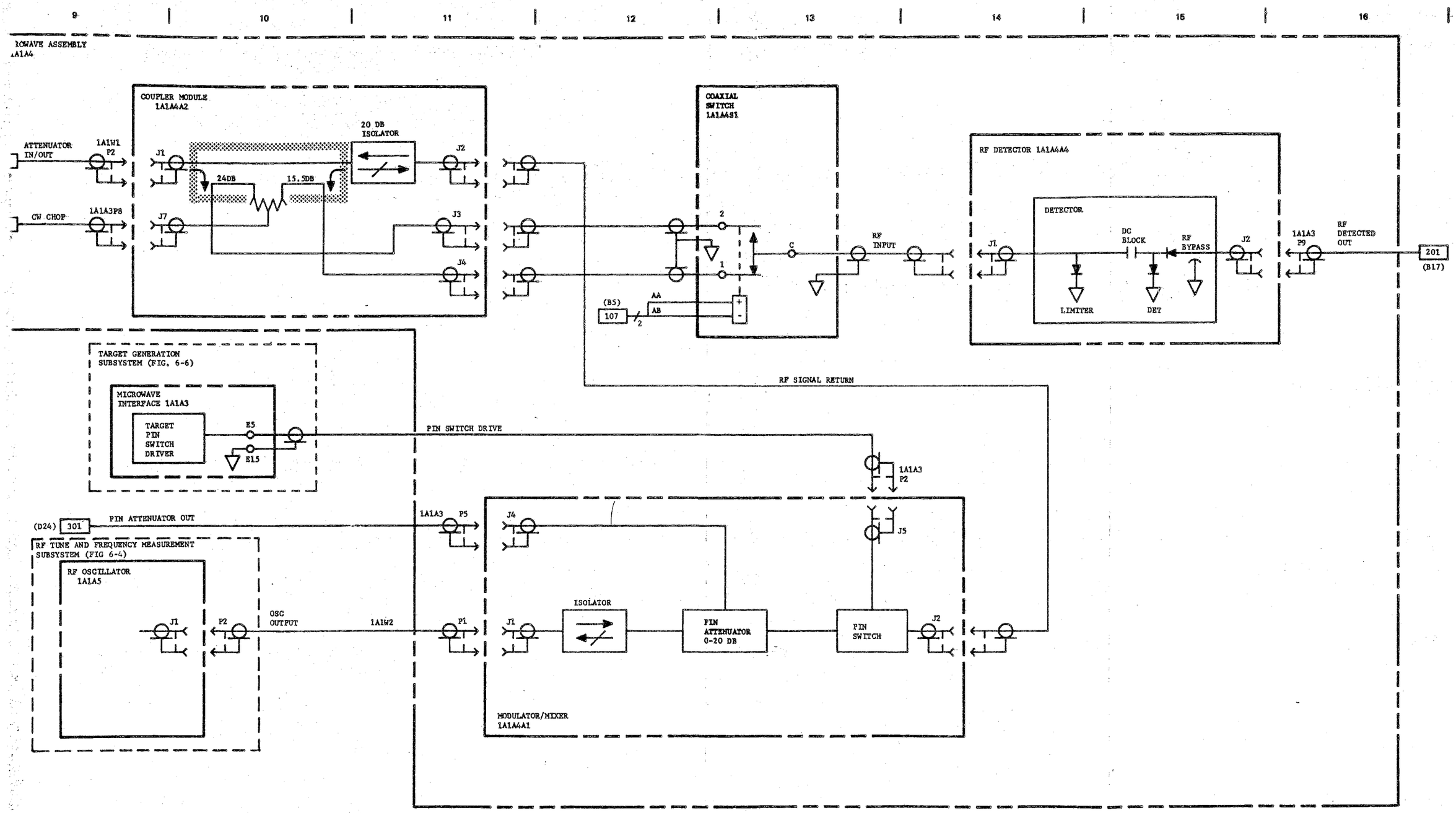


Figure 6-7. Power Measurements Subsystem, Detailed Functional Block Diagram (Sheet 2 of 3)

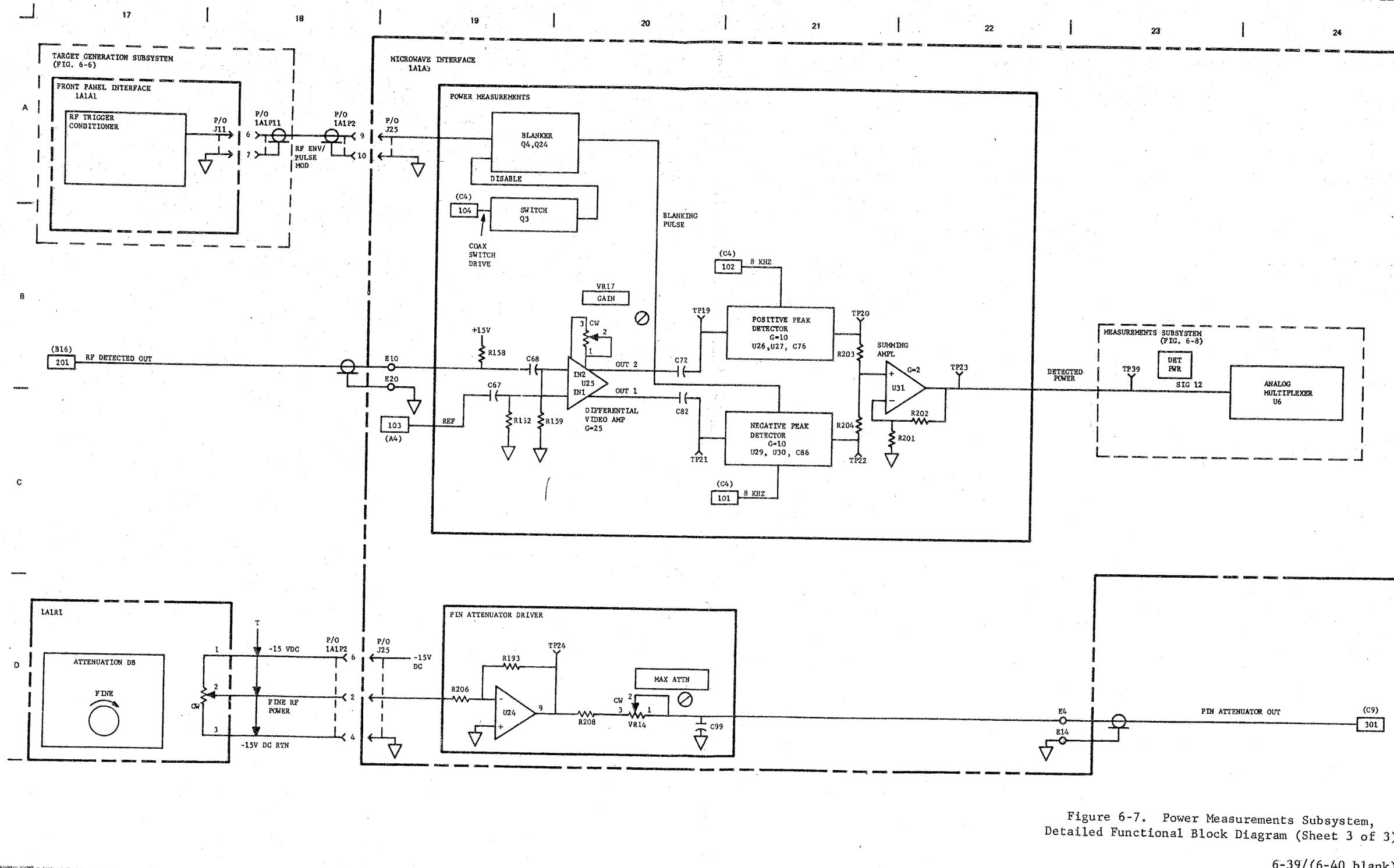


Figure 6-7. Power Measurements Subsystem, Detailed Functional Block Diagram (Sheet 3 of 3)

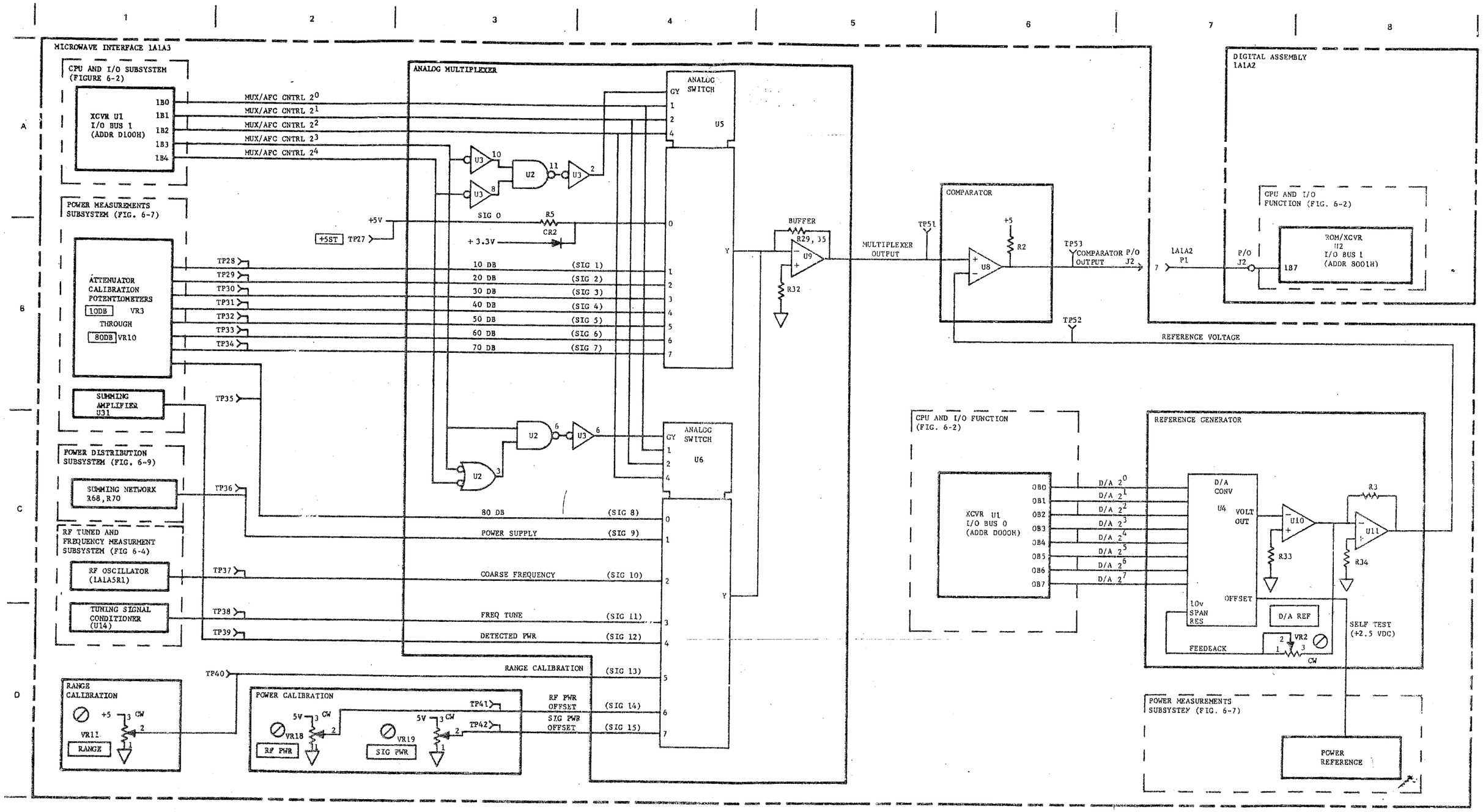


Figure 6-8. Measurements Subsystem, Detailed Functional Block Diagram (Sheet 1 of 2)

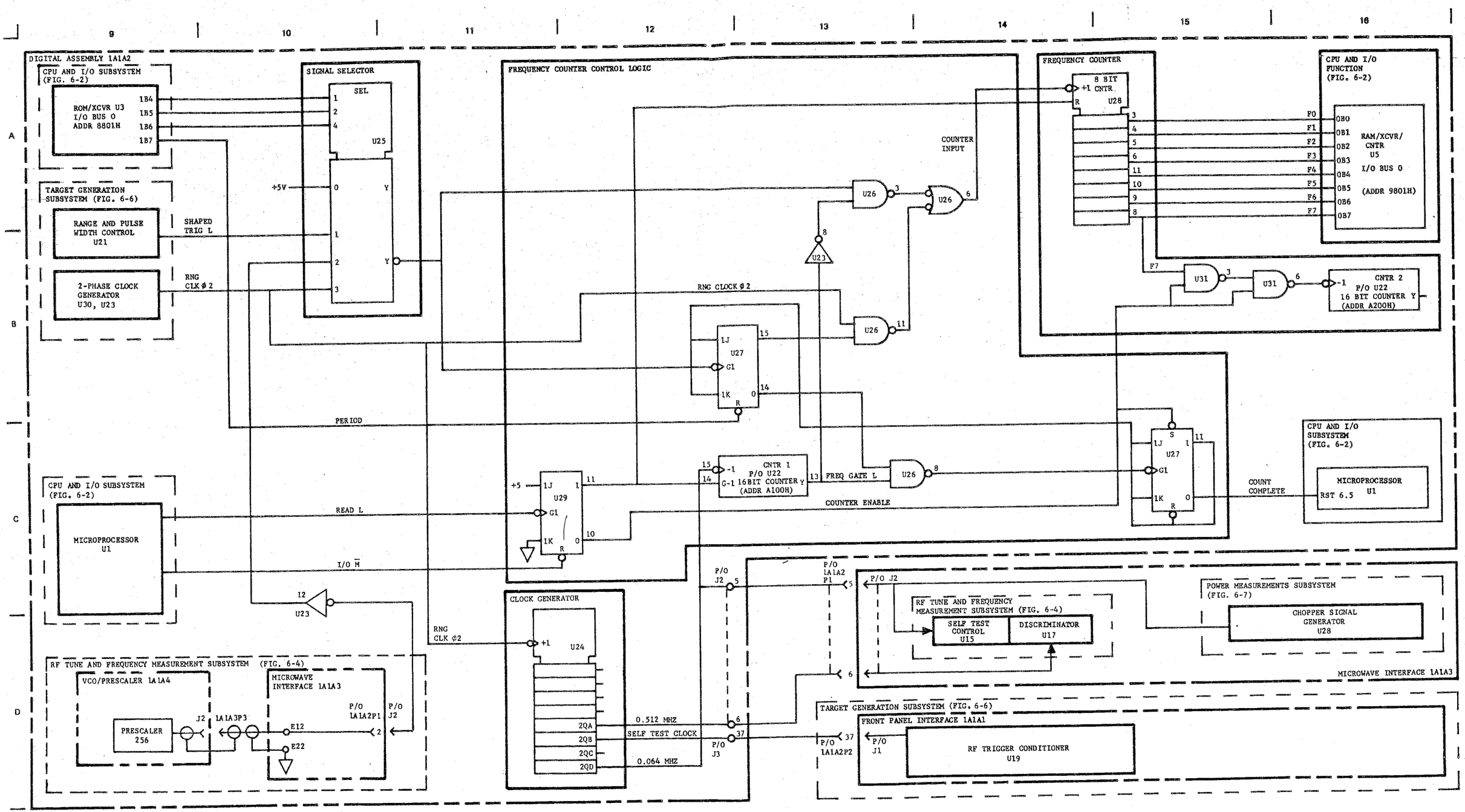


Figure 6-8. Measurements Subsystem, Detailed Functional Block Diagram (Sheet 2 of 2)

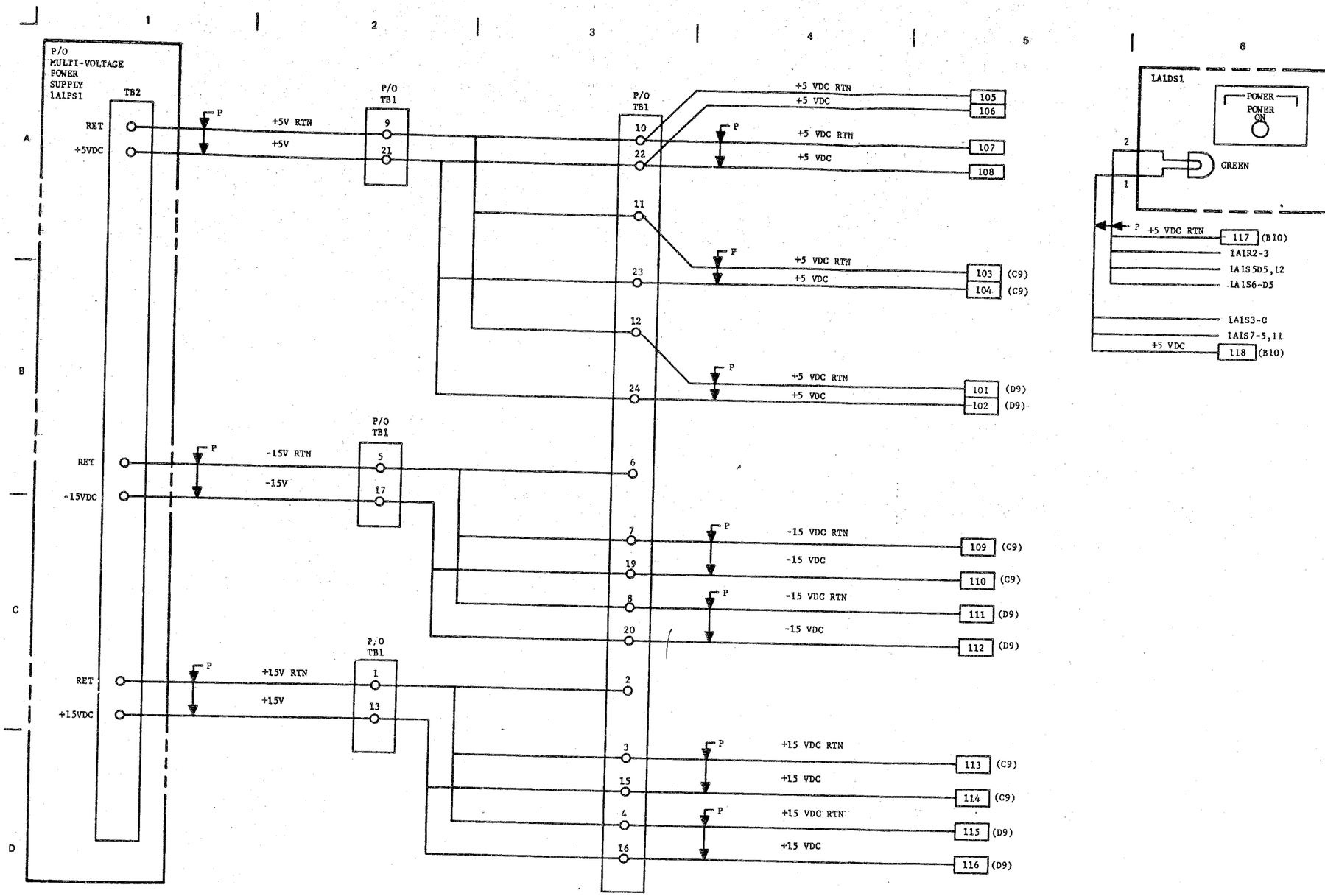


Figure 6-9. Power Distribution Subsystem, Detailed Functional Diagram (Sheet 1 of 2)

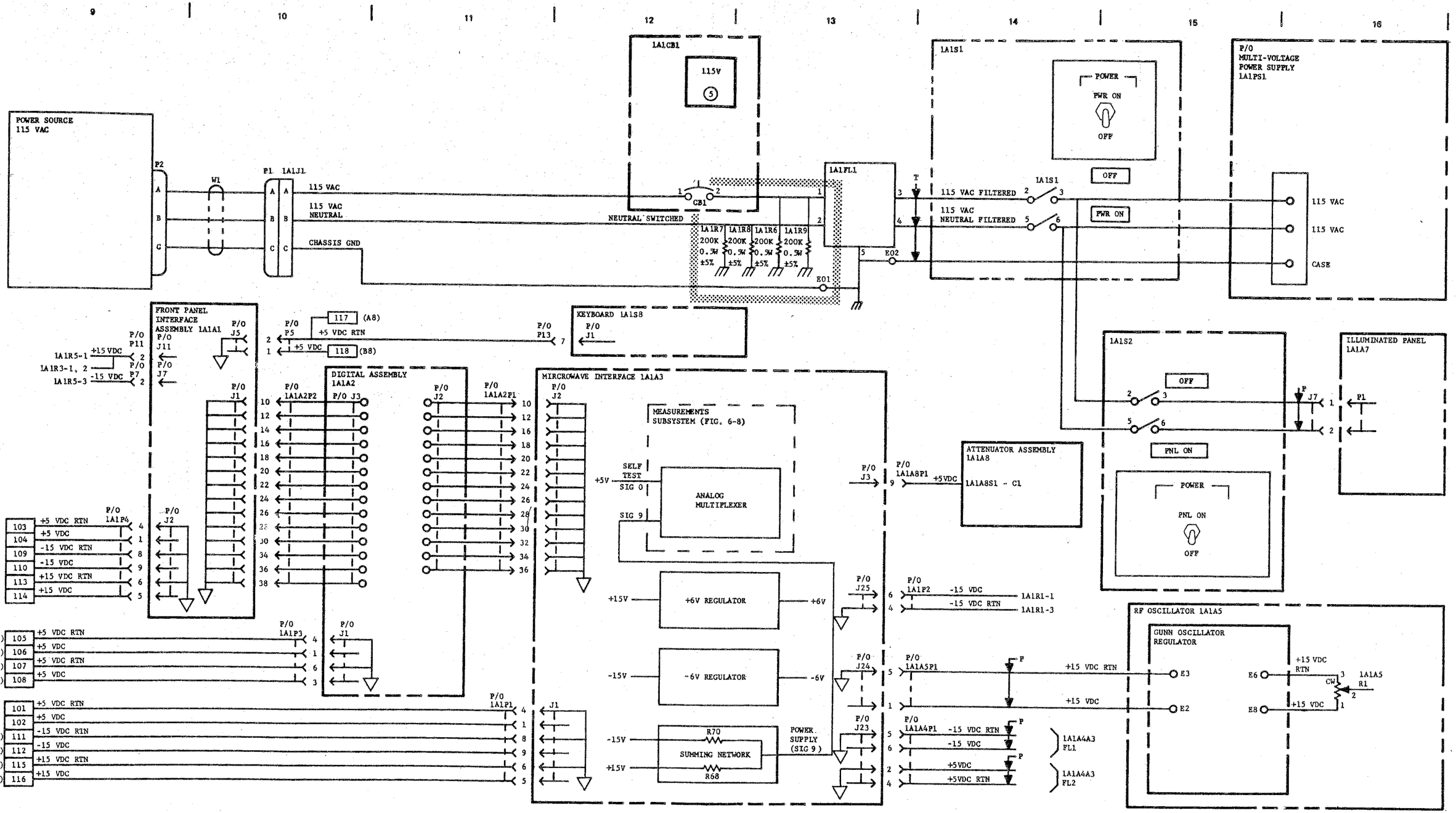


Figure 6-9. Power Distribution Subsystem, Detailed Functional Diagram (Sheet 2 of 2)

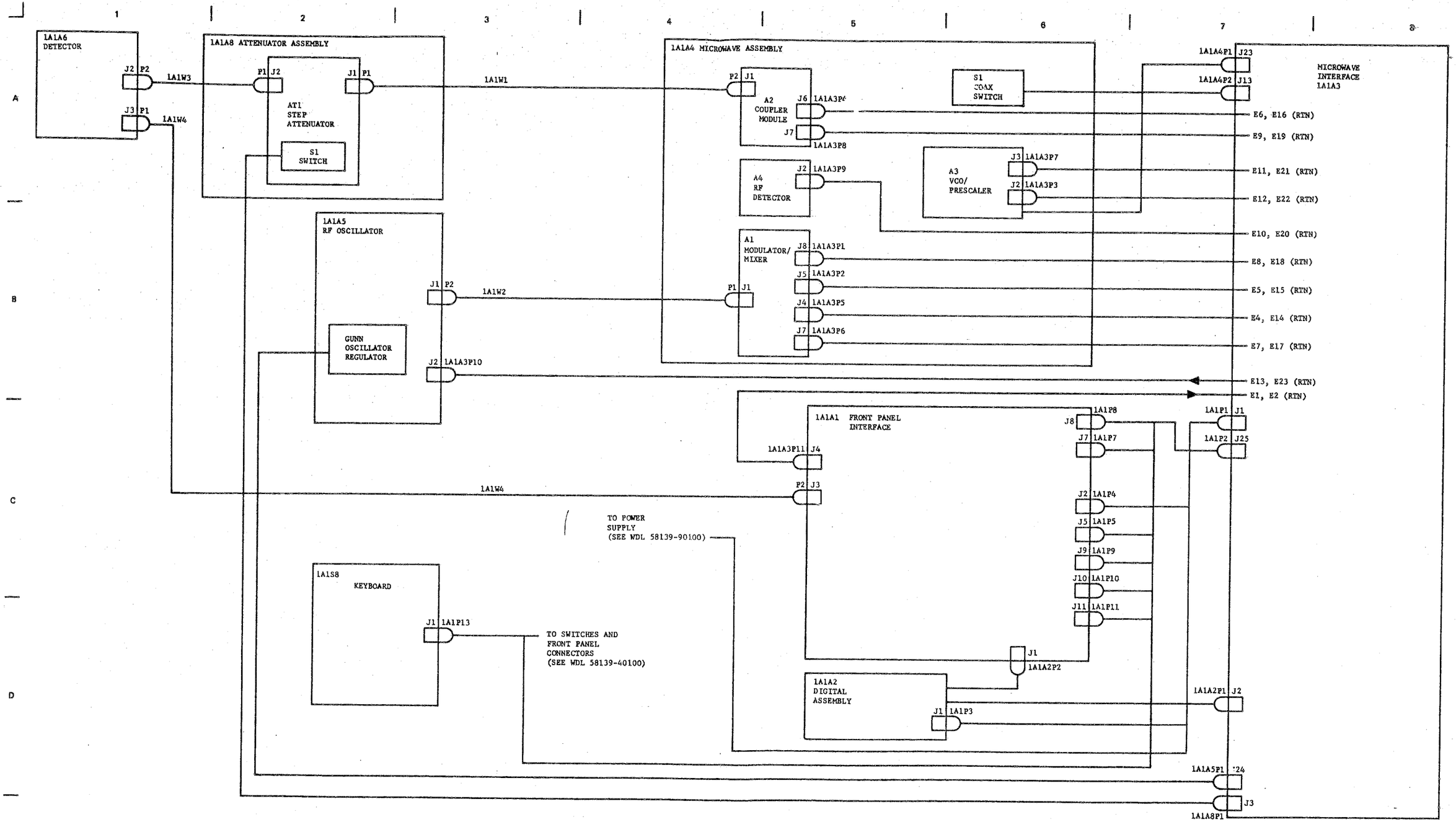
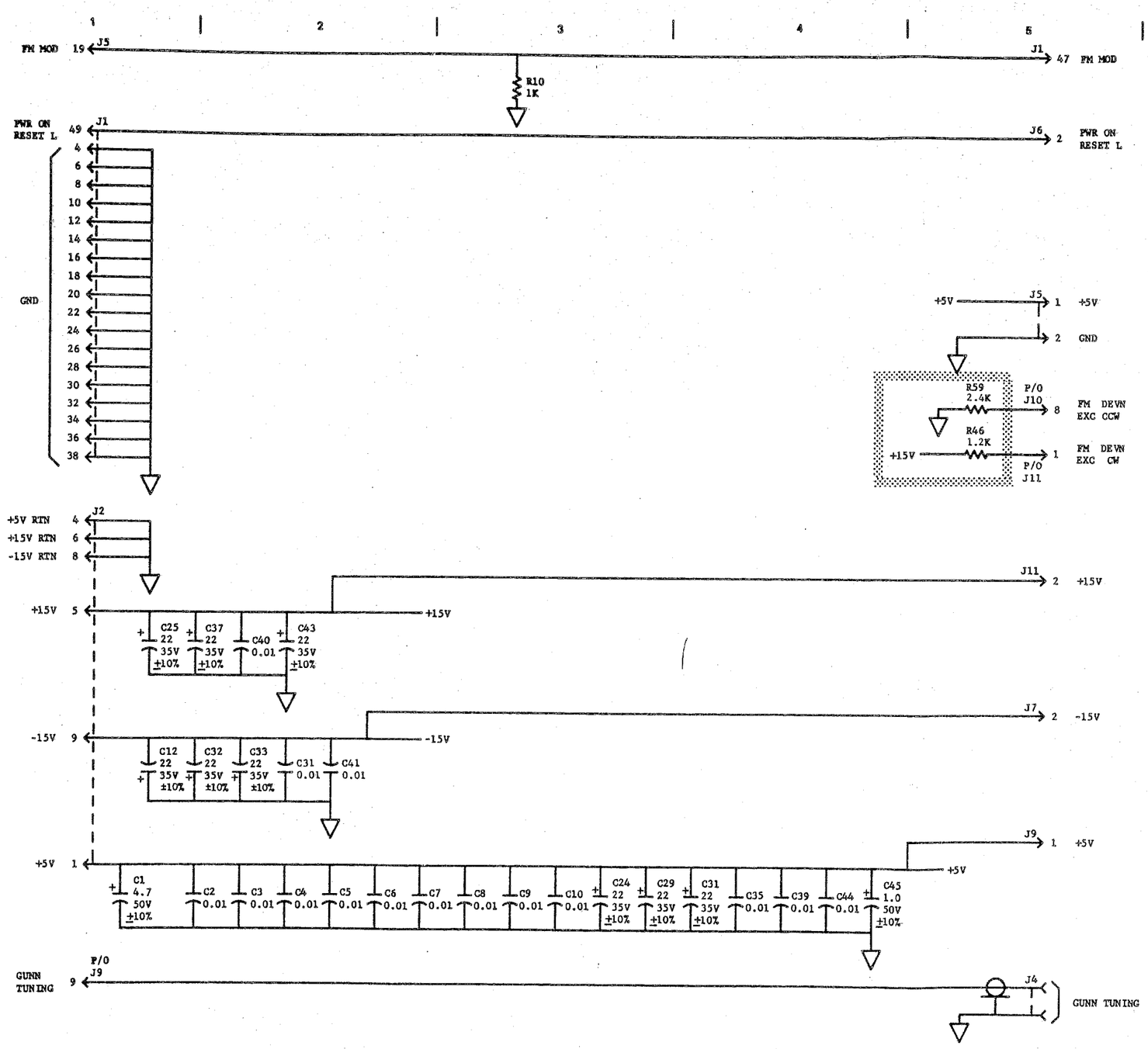


Figure 6-10. System Interconnection Block Diagram



NOTE:

UNLESS OTHERWISE SPECIFIED:

# INDICATES OPEN COLLECTOR OUTPUT
ALL RESISTANCES ARE IN OHMS, 1/4 WATT, ±5%
ALL CAPACITANCES ARE IN MICROFARADS

ALL CAPACITANCE TOLERANCES ARE ±20%, 500 VDC
ALL VOLTAGES ARE DC.

REF DES	TYPE	GND PIN NO.	+5V PIN NO.	+15V PIN NO.	-15V PIN NO.
U1 U2	8255A	7	26	-	-
U3 U4 U5 U6 U7	5447	8	16	-	-
U8 U9 U16 U17 U18 U19	5416 5400 5402 54LS74 5403 5400	7	14	-	-
U10 U13	LM111H	1	8	-	4
U11	LM118H	-	7	-	4
U12	733 DMBQ	10	-	-	5
U14	741H	-	-	7	4
U15	XR2207	10	-	1	-

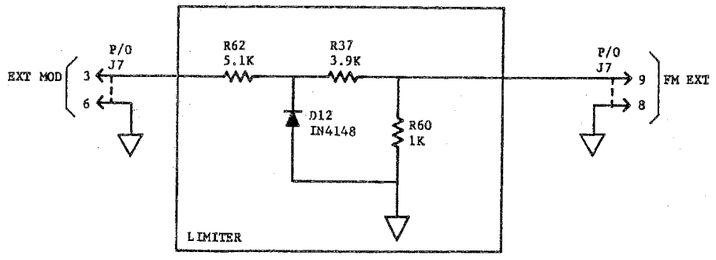


Figure 6-11. Front Panel Interface 1A1A1 (58139-40020) Schematic Diagram (Sheet 1 of 5)

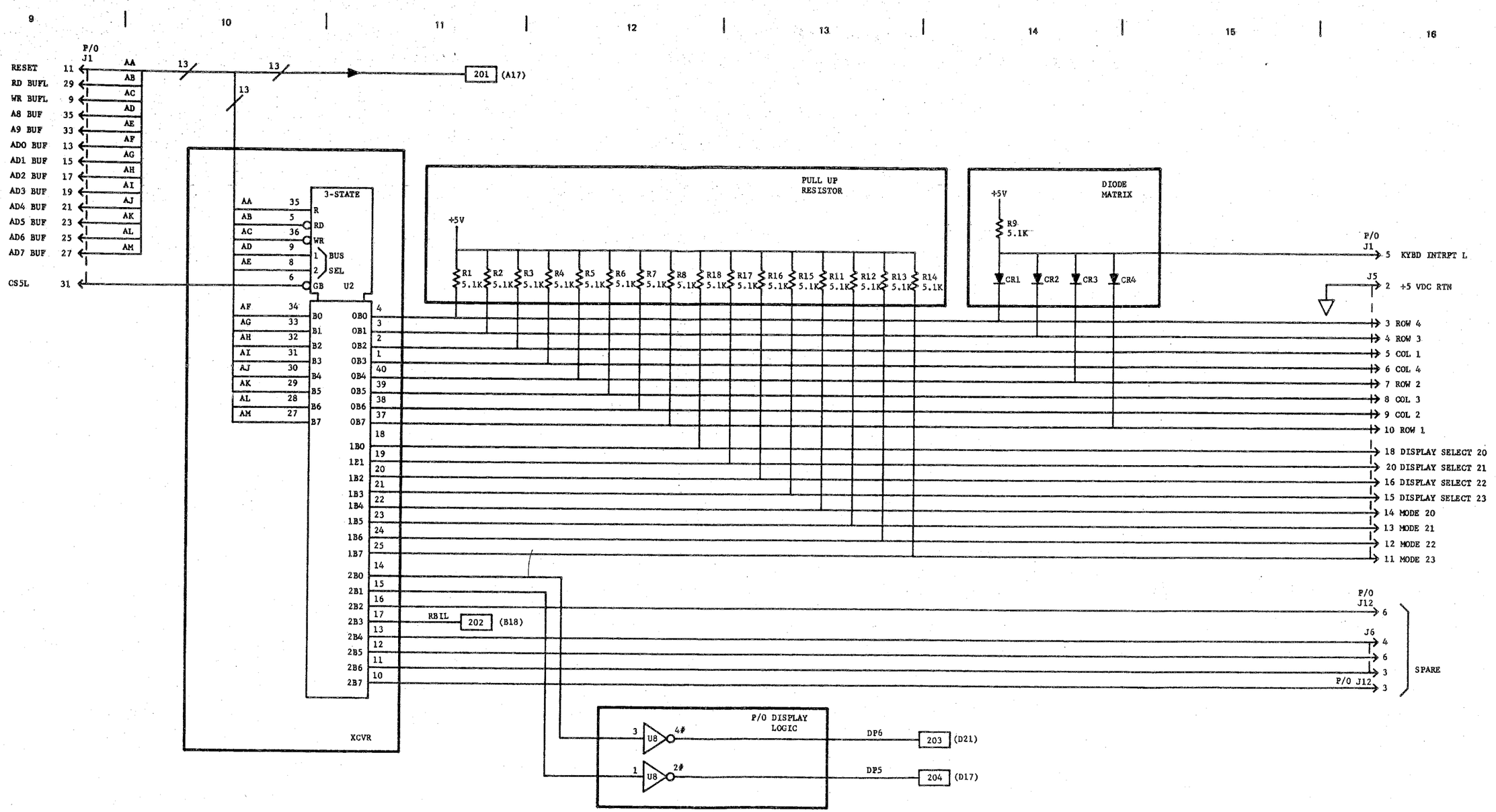


Figure 6-11. Front Panel Interface 1A1A1 (58139-40020) Schematic Diagram (Sheet 2 of 5)

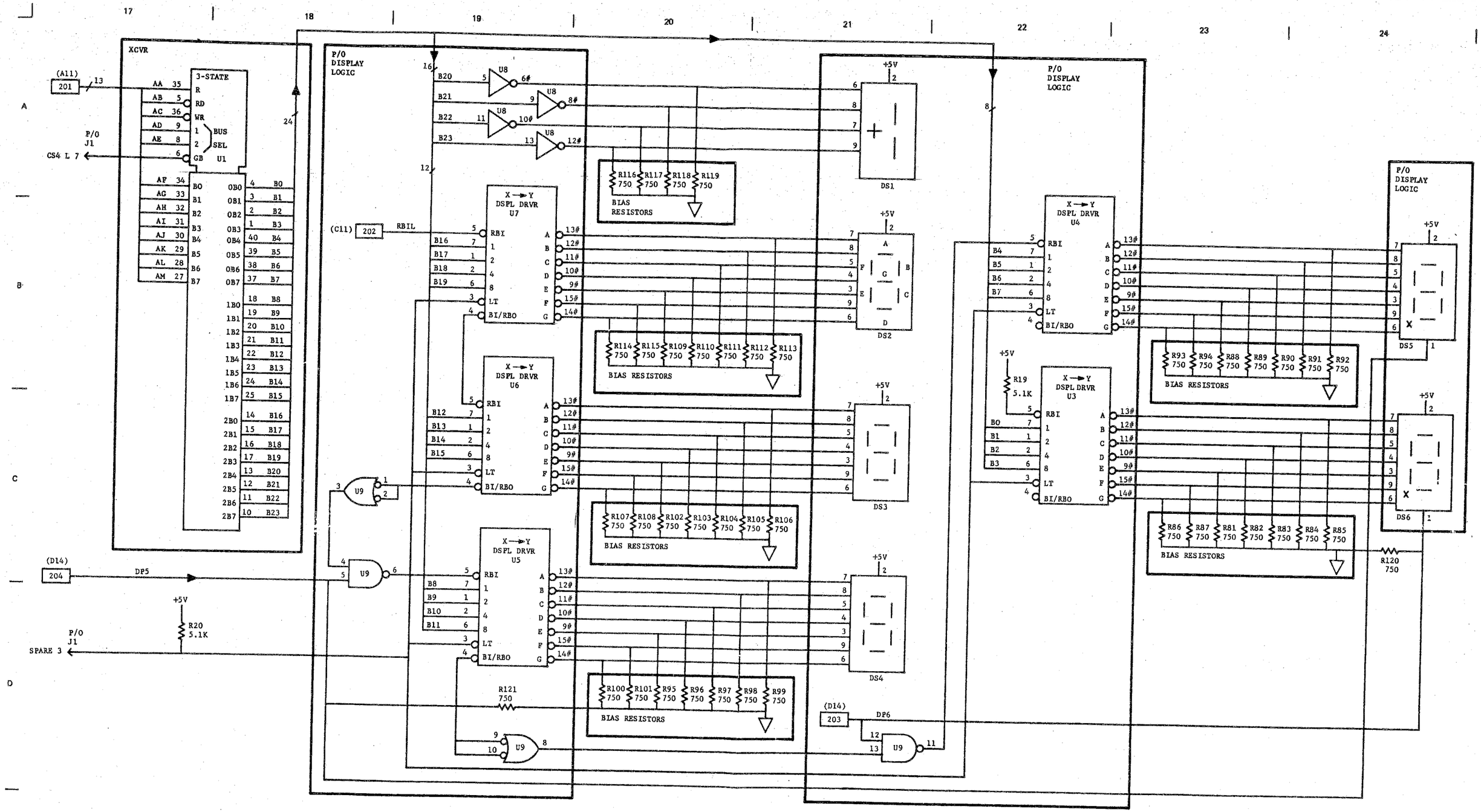
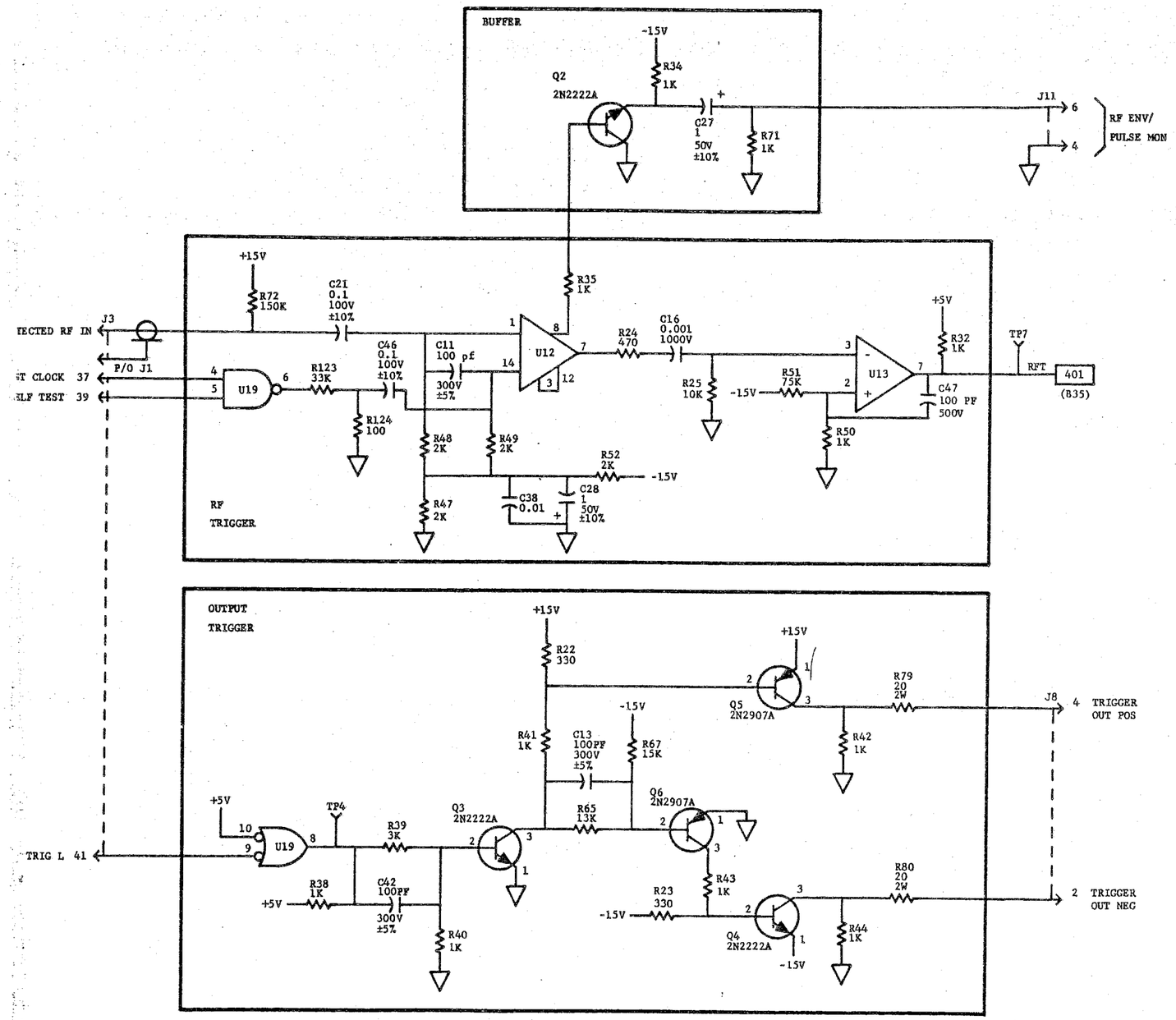


Figure 6-11. Front Panel Interface 1A1A1 (58139-40020) Schematic Diagram (Sheet 3 of 5)



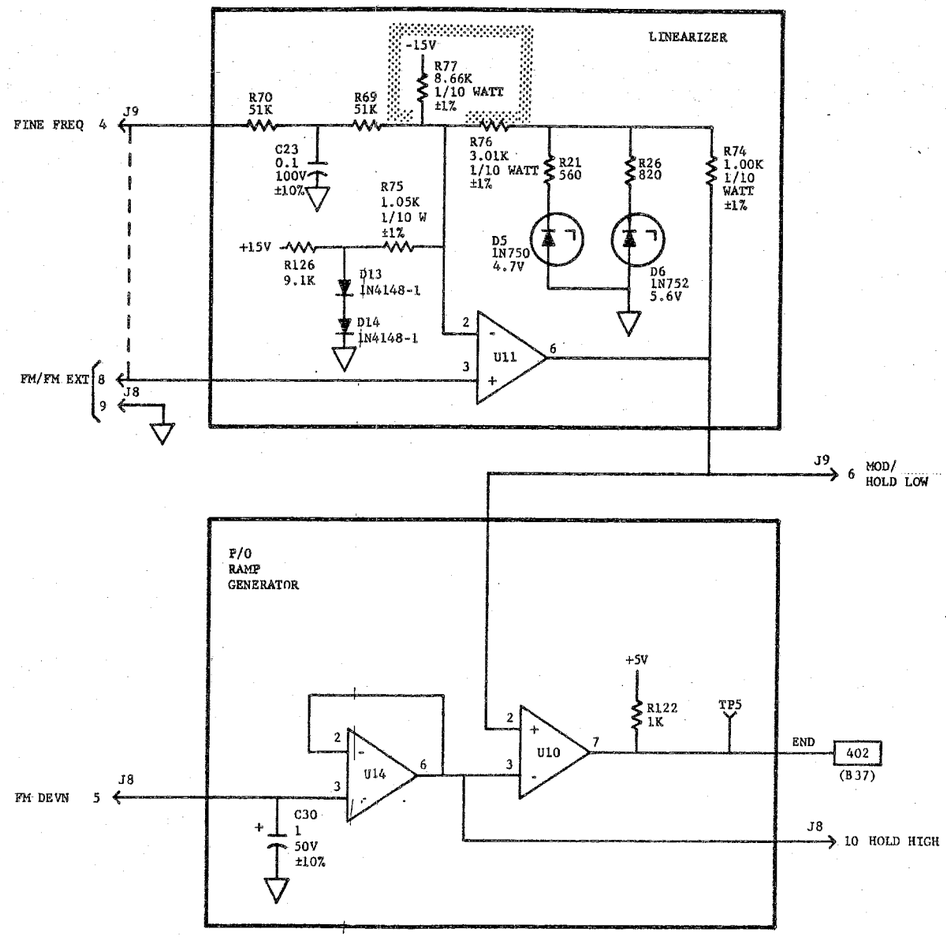


Figure 6-11. Front Panel Interface 1A1A1 (58139-40020) Schematic Diagram (Sheet 4 of 5)

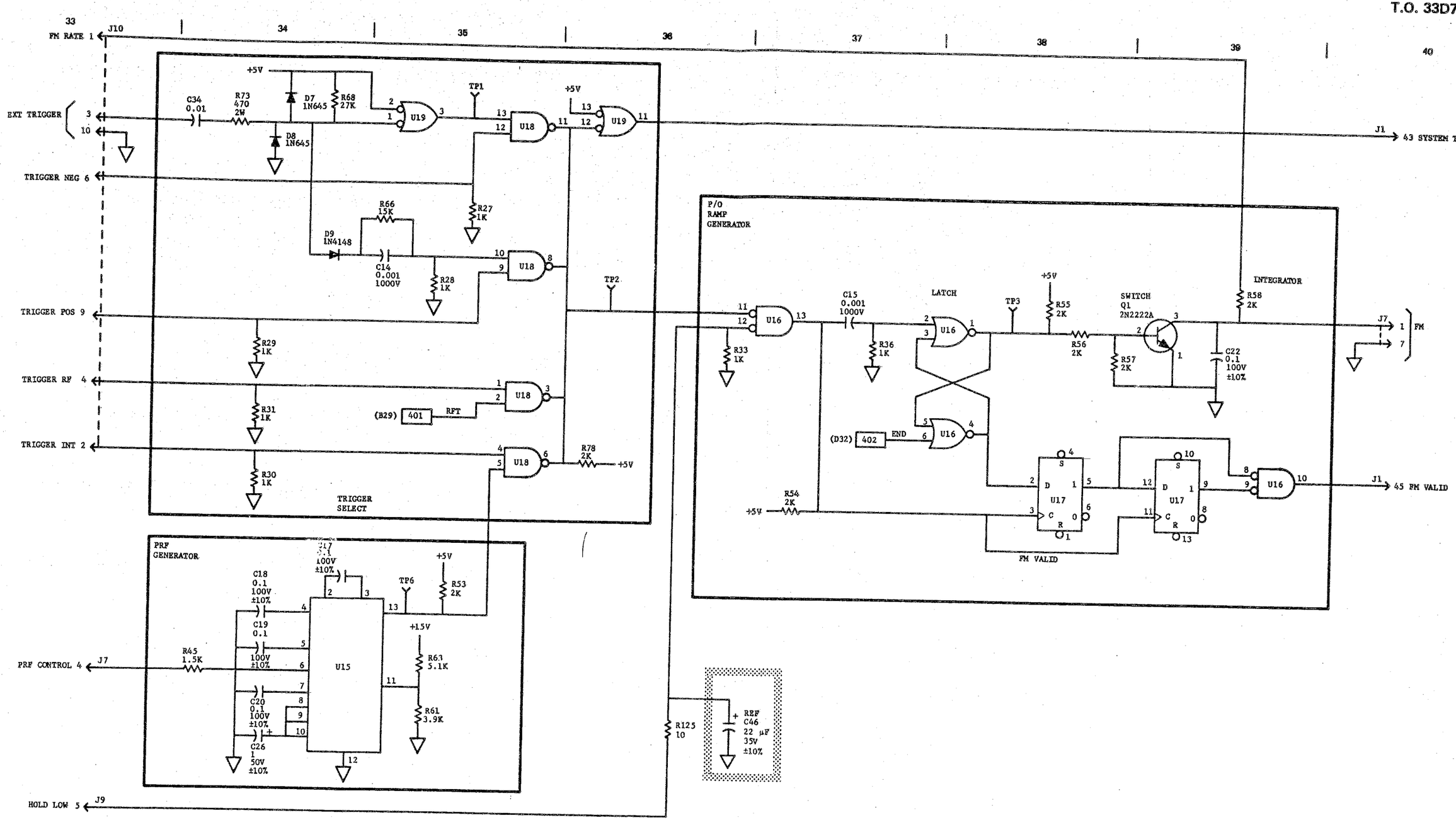
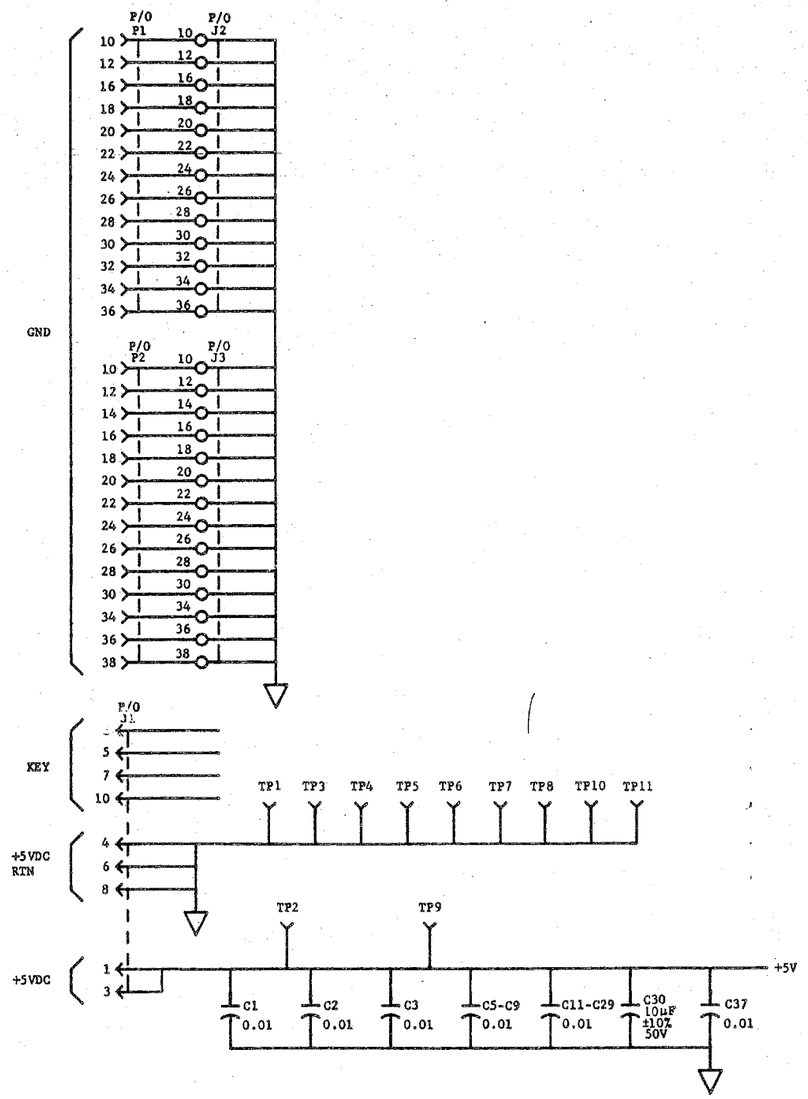


Figure 6-11. Front Panel Interface 1A1A1 (58139-40020) Schematic Diagram (Sheet 5 of 5)



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS, 1/4 W, ±5%
   ALL CAPACITANCES ARE IN MICROFARADS
   ALL CAPACITANCE TOLERANCES ARE ±20%, 500V
   ALL DIODES ARE 1N4148-1
   ALL VOLTAGES ARE DC
2.

REF DES	TYPE	SPEC	GND PIN	+5V PIN
U1	8085A	58133-90027	20	40
U2 U3	8755A or 8355	58139-90027	20	40
U5	8155	58139-90027	20	40
U6	54LS42	MIL-M-38510	7	16
U7 U8	8216	58139-90027	8	16
U9	54LS244	77057	10	20
U11 U12 U13 U14 U15 U16	54LS193	77057	8	16
U17	5400	77057	7	14
U18 U26 U31	54LS00	77057	7	14
U19 U27 U29	54LS76	77057	13	5
U20	54LS123	77057	8	16
U21	54LS221	77057	8	16
U22	8253	58139-90027	12	24
U23	54S04	MIL-M-38510	7	14
U24 U28	54LS393	MIL-M-38510	7	14
U25	54LS151	MIL-M-38510	8	16
X1	CR60 A/U-4MHZ	MIL-6-3098	-	-
U30	WB1, X-142, OR CO-231-1	58139-90030	-	-

NOTE:

THE 8755 A IS AN EPROM USED ON THE FIRST PRODUCTION UNITS. THE 8355 IS A ROM WHICH WILL BE USED ON FOLLOWING PRODUCTION UNITS.

Figure 6-12. Digital Assembly 1A1A2 (58139-40015) Schematic Diagram (Sheet 1 of 6)

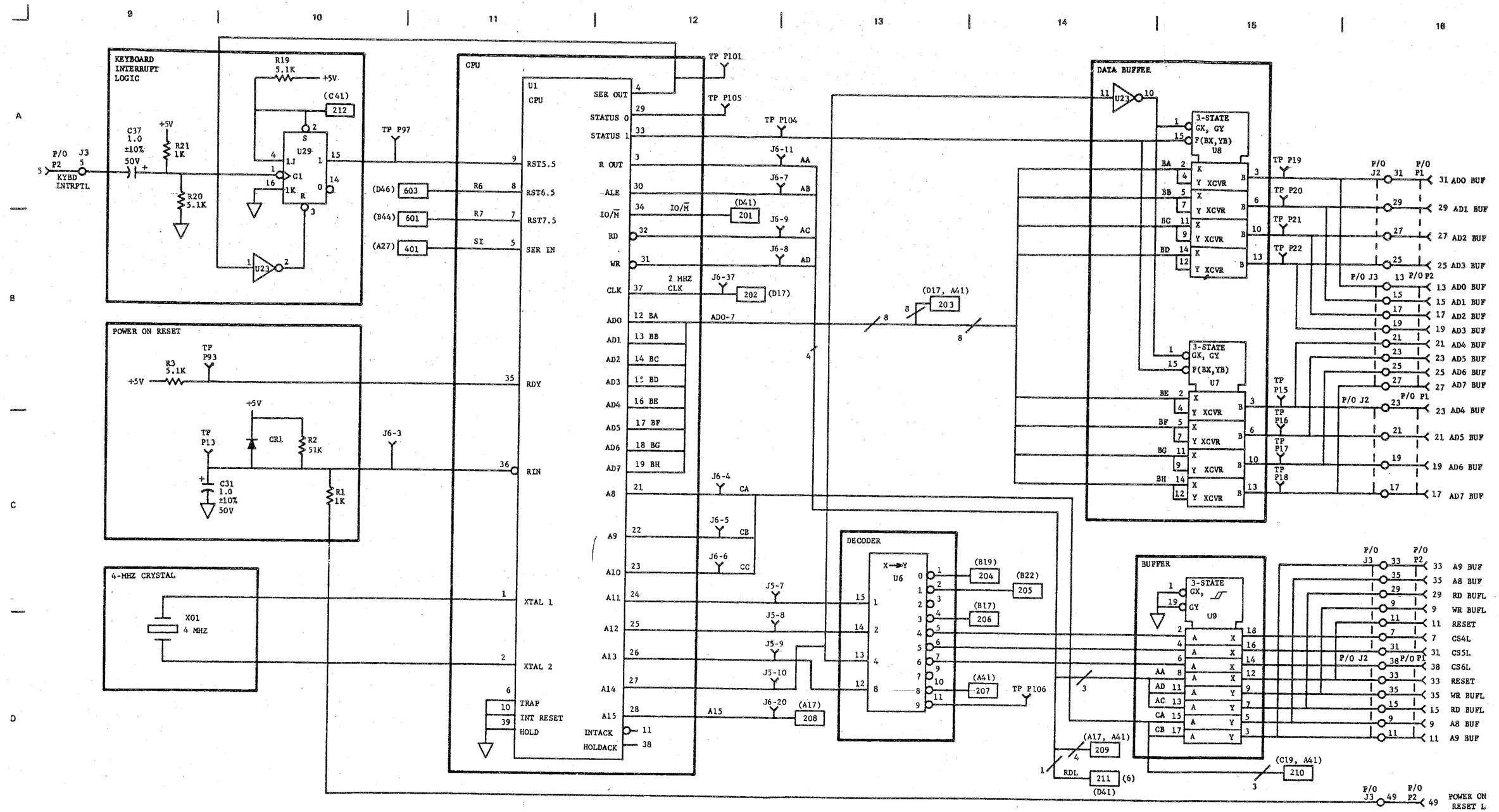


Figure 6-12. Digital Assembly 1A1A2 (58139-40015) Schematic Diagram (Sheet 2 of 6)

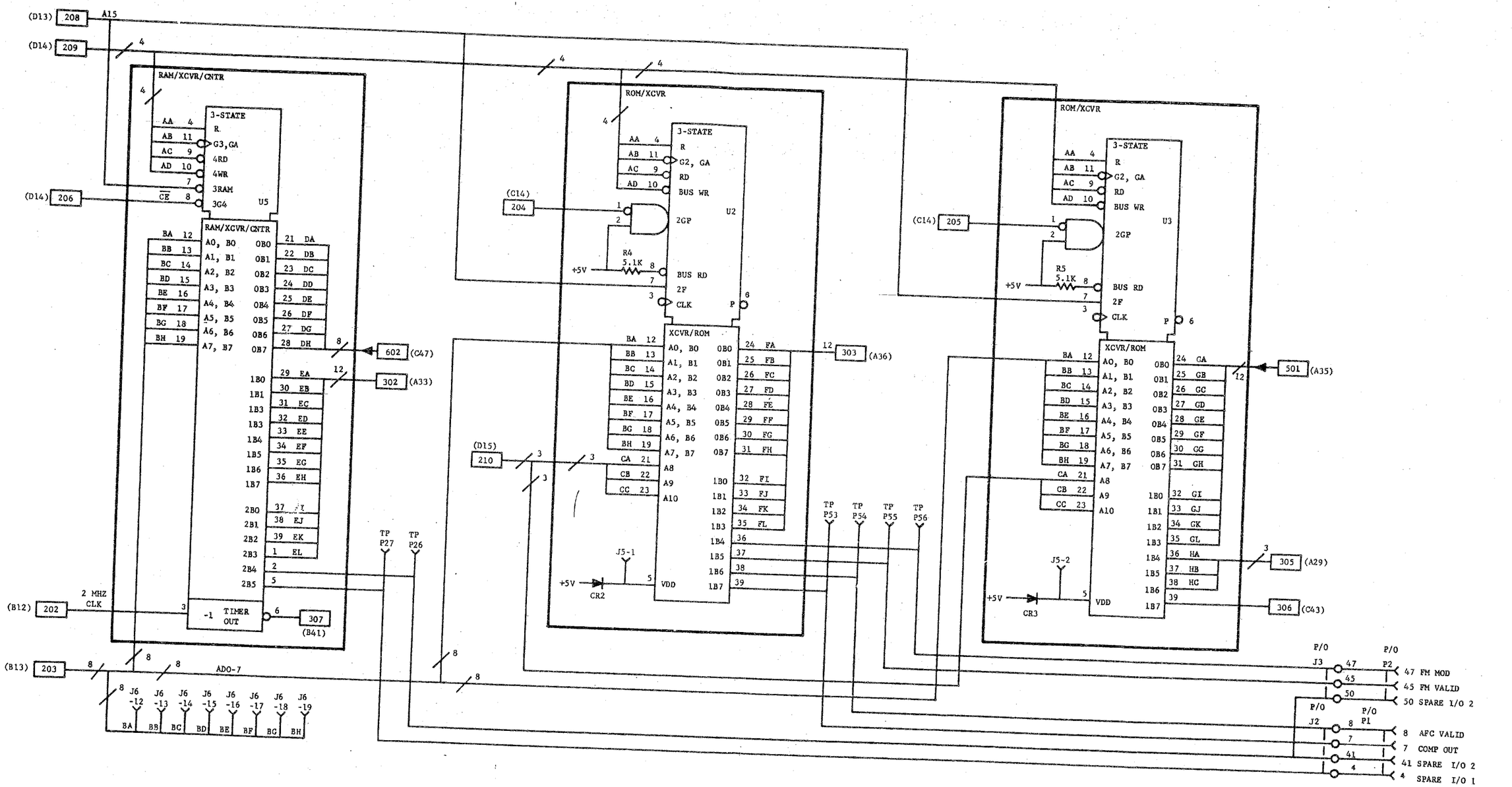


Figure 6-12. Digital Assembly 1A1A2 (58139-40015) Schematic Diagram (Sheet 3 of 6)

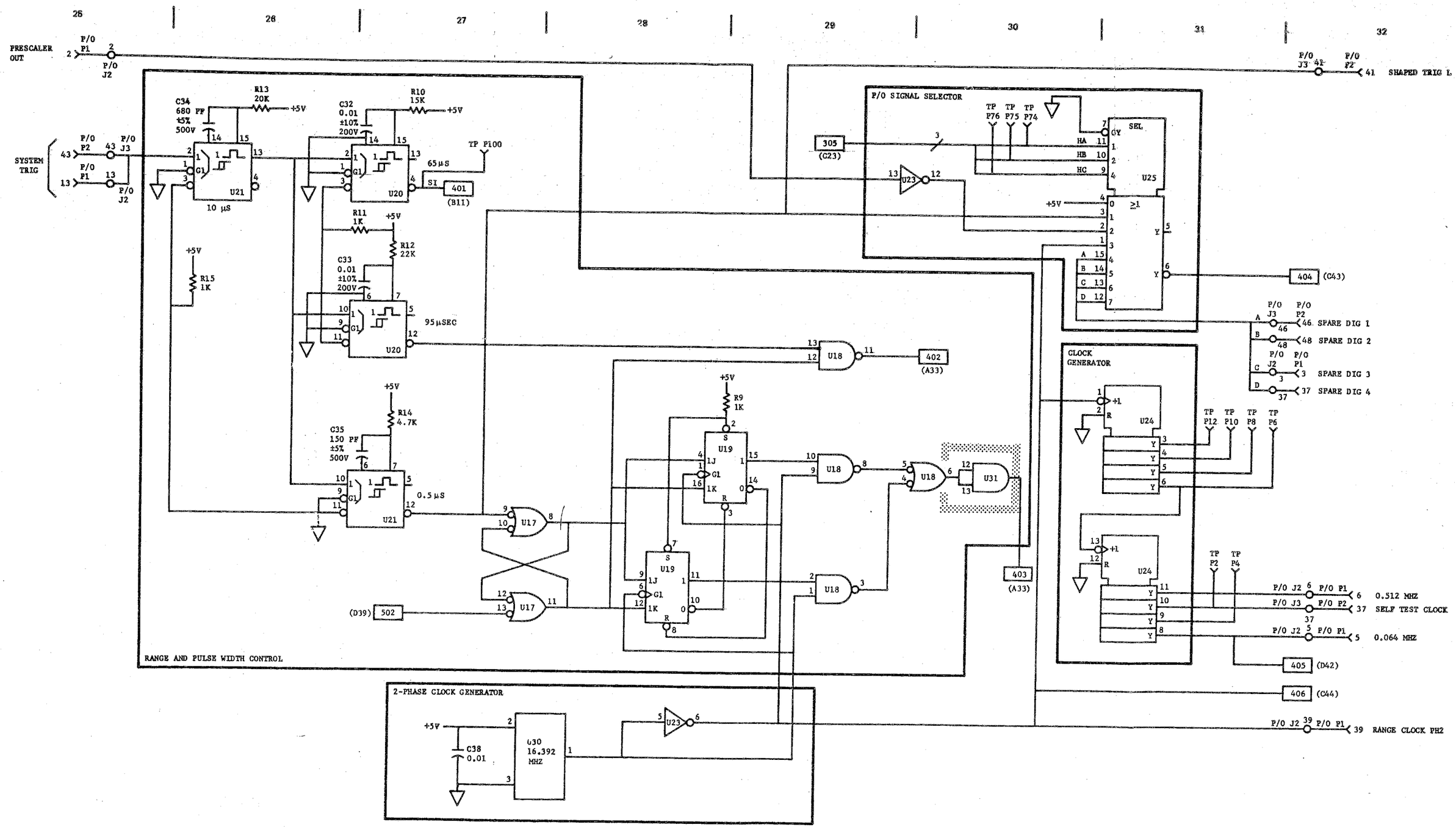


Figure 6-12. Digital Assembly 1A1A2 (58139-40015) Schematic Diagram (Sheet 4 of 6)

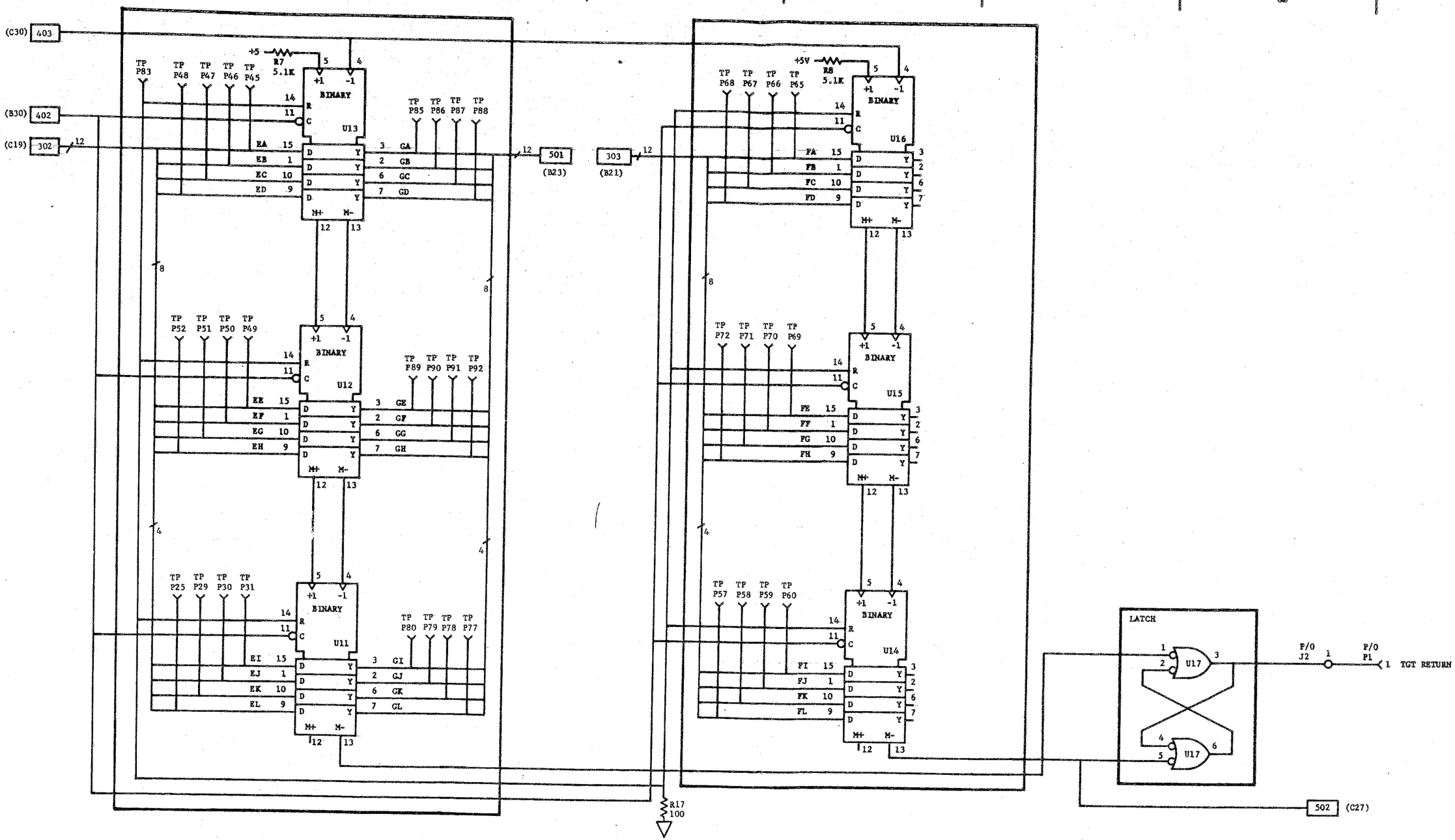


Figure 6-12. Digital Assembly 1A1A2 (58139-40015) Schematic Diagram (Sheet 5 of 6)

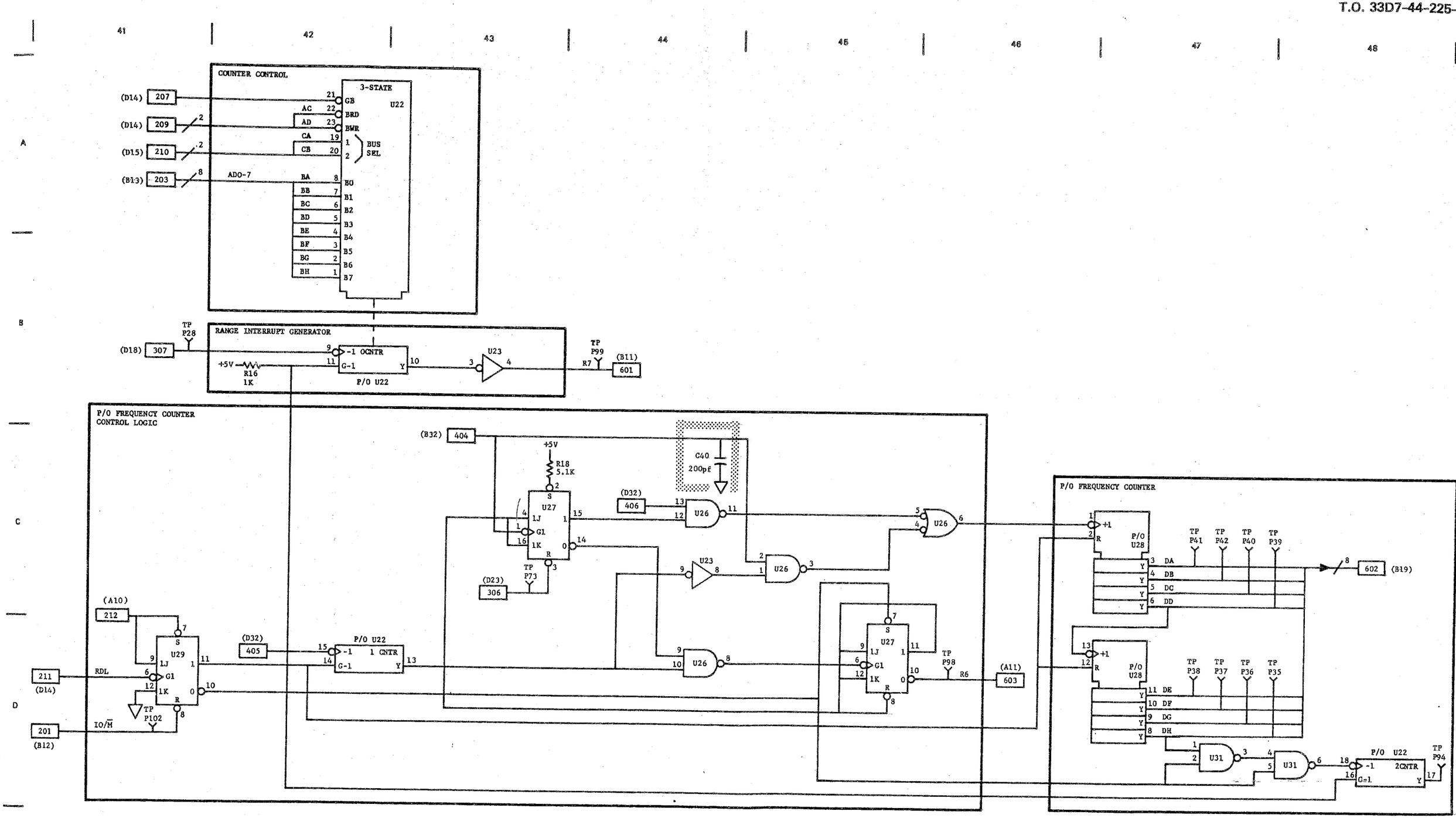
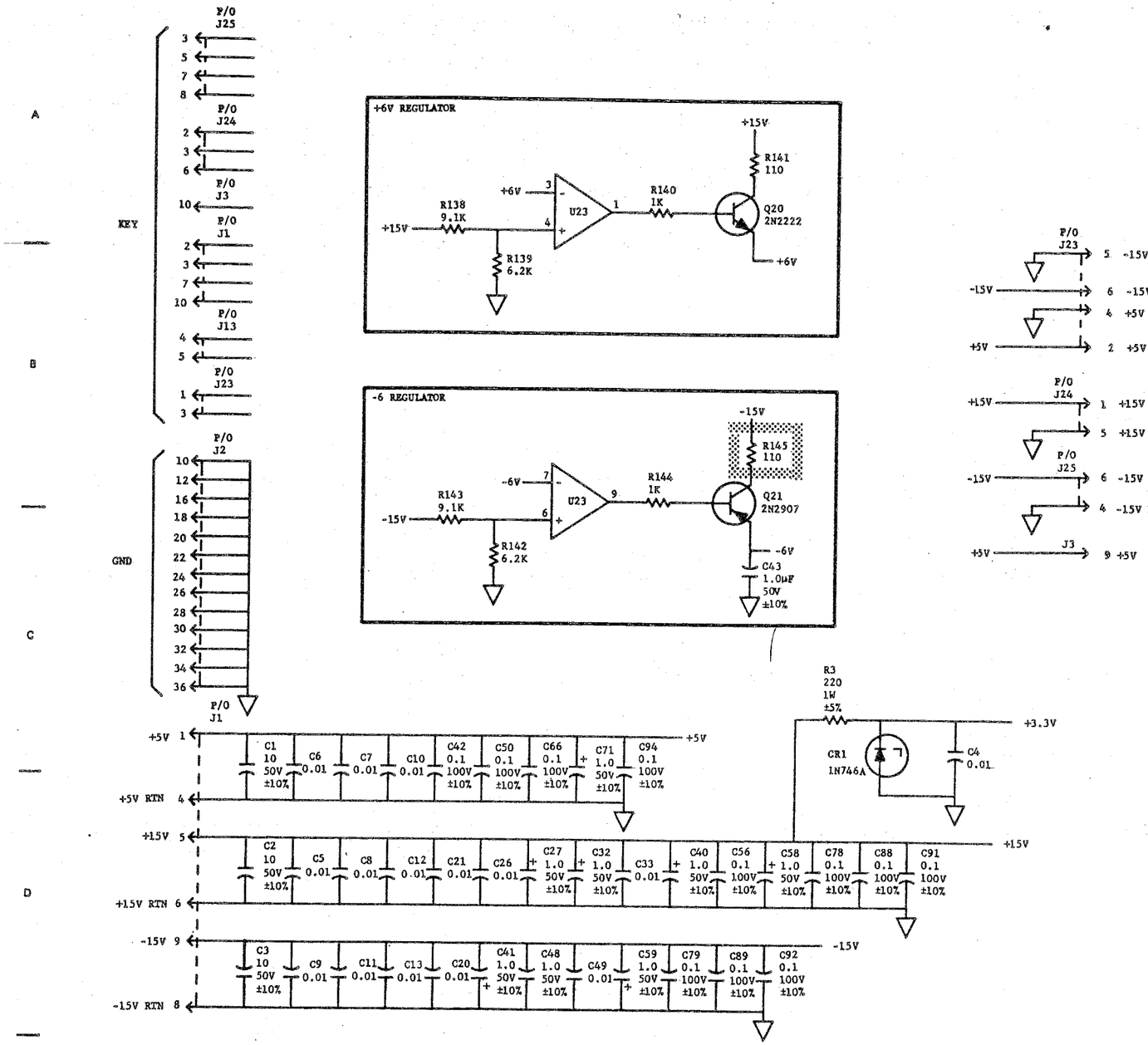


Figure 6-12. Digital Assembly 1A1A2 (58139-40015) Schematic Diagram (Sheet 6 of 6)



NOTES:

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTANCES ARE IN OHMS, 1/4W, ±5%
   ALL CAPACITANCES ARE IN MICROFARADS
   ALL CAPACITANCE TOLERANCES ARE 500V, ±20%
   ALL DIODES ARE IN458
   ALL VOLTAGES ARE DC

2.

REF DES.	TYPE	SPEC	GND PIN	+5V PIN	+15V PIN	-15V PIN	+V PIN	-V PIN
U1	D8255A		7	26	-	-	-	-
U2 U3	54LS14		7	14	-	-	-	-
U20	54LS00		7	14				
U4	AD561		1	14	-	3	-	-
U5 U6 U7	AM3705		-	4,	-	13	-	-
U8 U22	LM111		1	-	8	4	-	-
U9 U10 U11 U31	LM101A		-	-	7	4	-	-
U12 U13 U21 U25	733D		5	-	10	-	-	-
U14 U27 U30	LM108		-	-	7	4	-	-
U15	54LS03		7	14	-	-	-	-
U16 U32	5406		7	14	-	-	-	-
U17	54LS02		7	14	-	-	-	-
U18 U19 U23 U24	LM747		-	-	2, 8	5	-	-
U28	54LS193		8	16	-	-	-	-
U26 U29	LM160		5				8	4

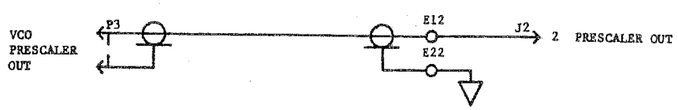


Figure 6-13. Microwave Interface 1A1A3 (58139-40010) Schematic Diagram (Sheet 1 of 7)

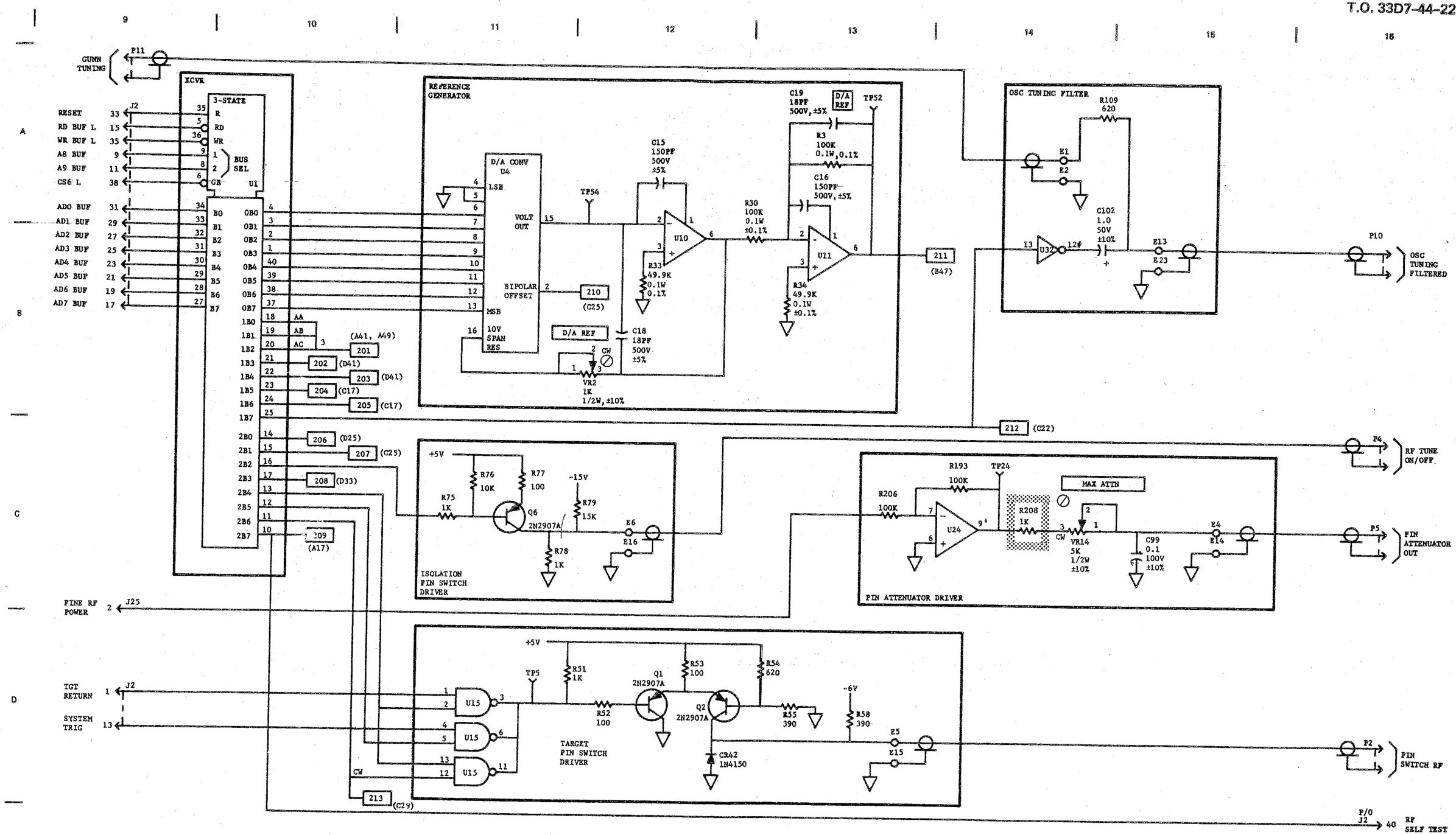


Figure 6-13. Microwave Interface 1A1A3 (58139-40010) Schematic Diagram (Sheet 2 of 7)

1 Nov 79
ch-3, dtd:
1 Feb 82

P/O ch-3, 1 Feb 82
TM

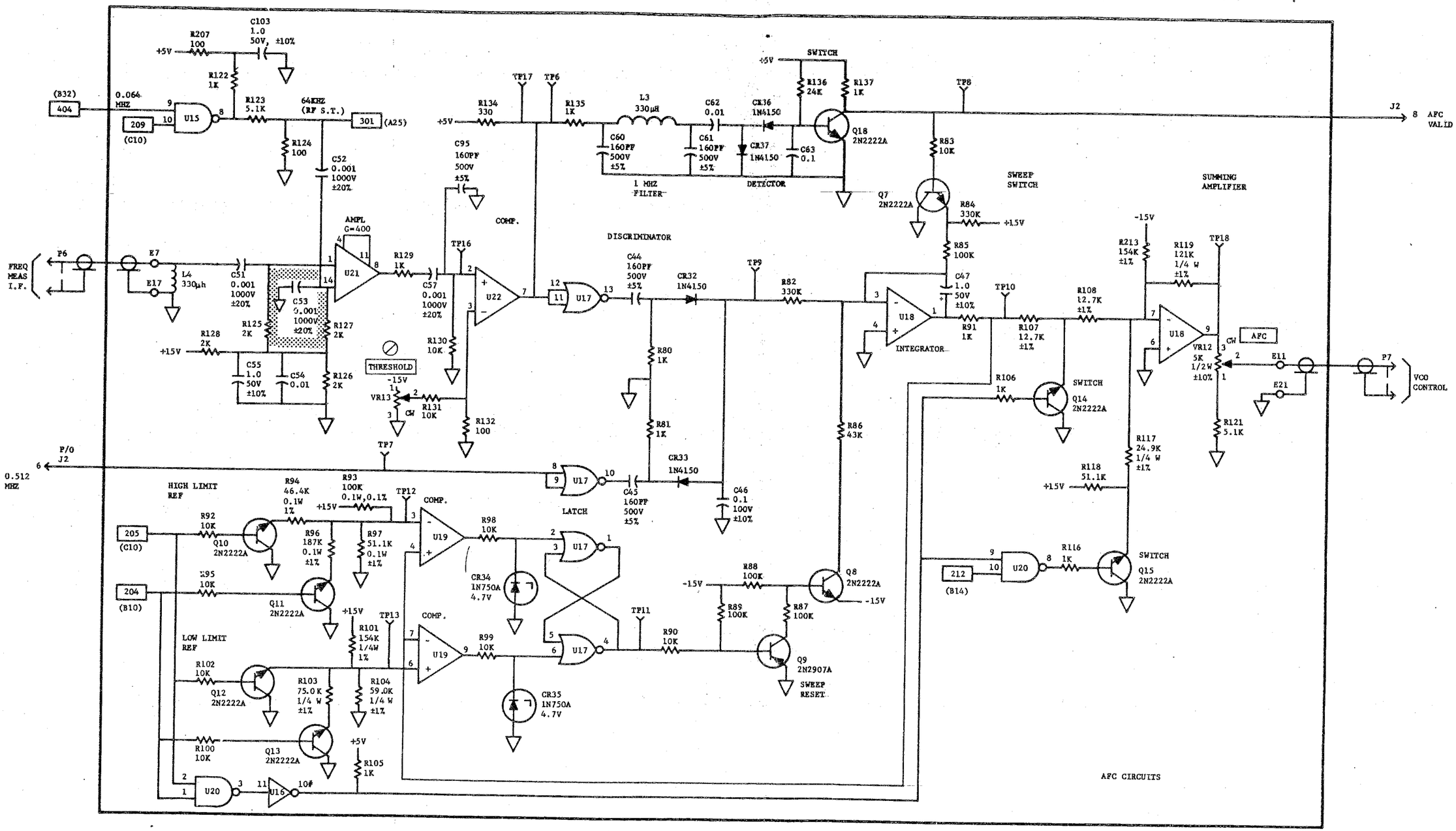


Figure 6-13. Microwave Interface 1A1A3 (58139-40010) Schematic Diagram (Sheet 3 of 7)

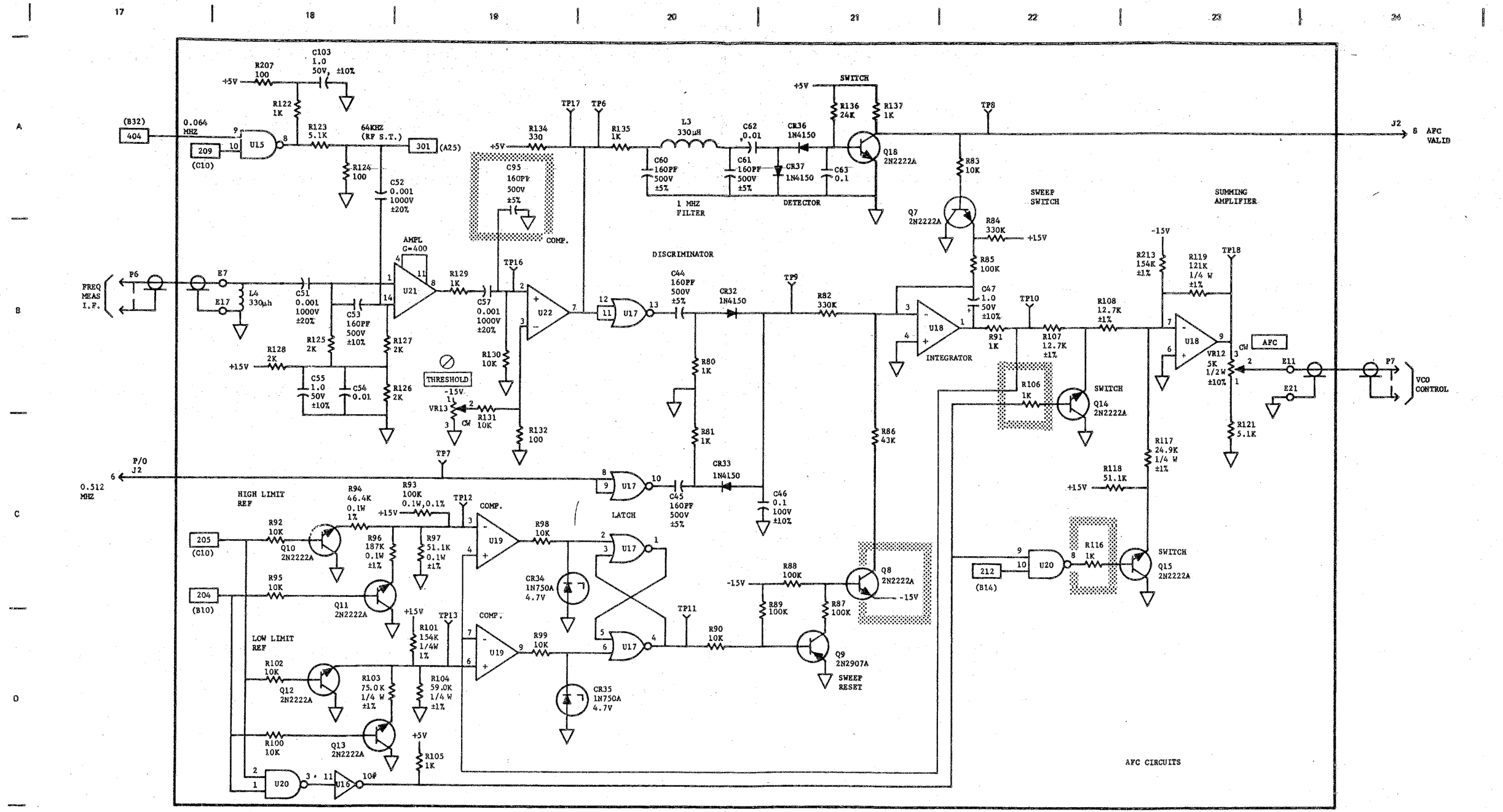


Figure 6-13. Microwave Interface 1A1A3 (58139-40010) Schematic Diagram (Sheet 3 of 7)

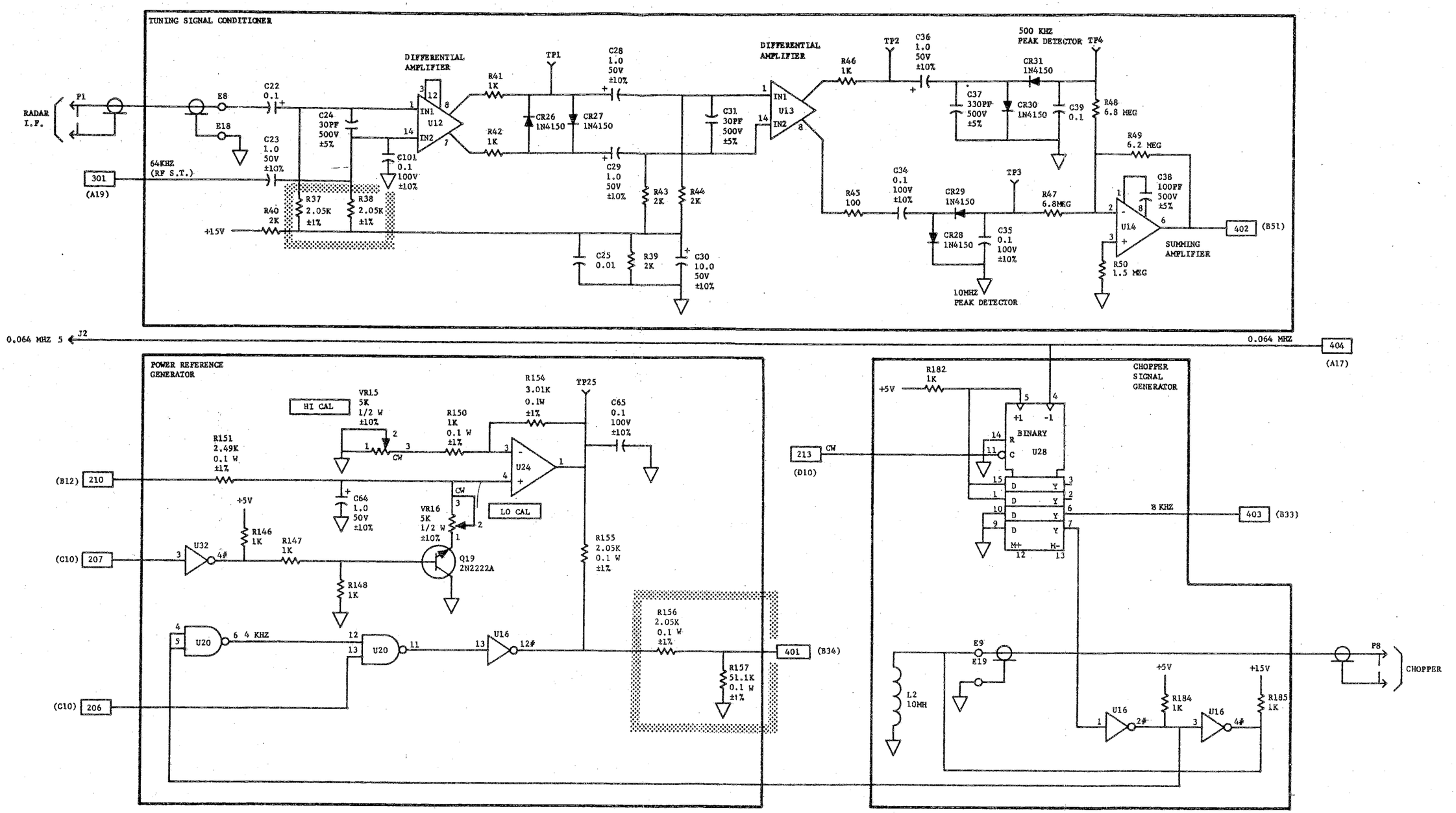


Figure 6-13. Microwave Interface 1A1A3 (58139-40010) Schematic Diagram (Sheet 4 of 7)

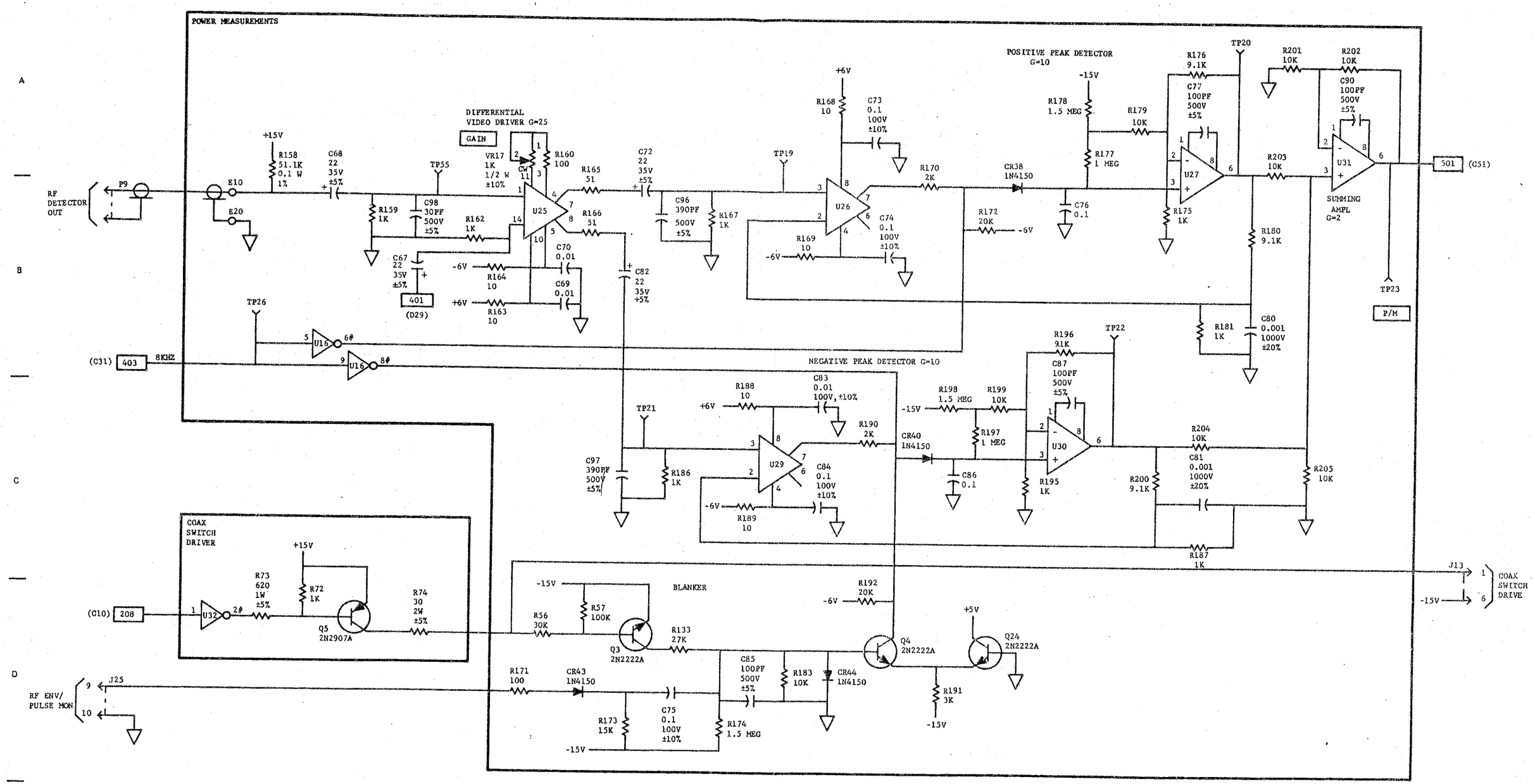


Figure 6-13. Microwave Interface 1A1A3 (58139-40010) Schematic Diagram (Sheet 5 of 7)

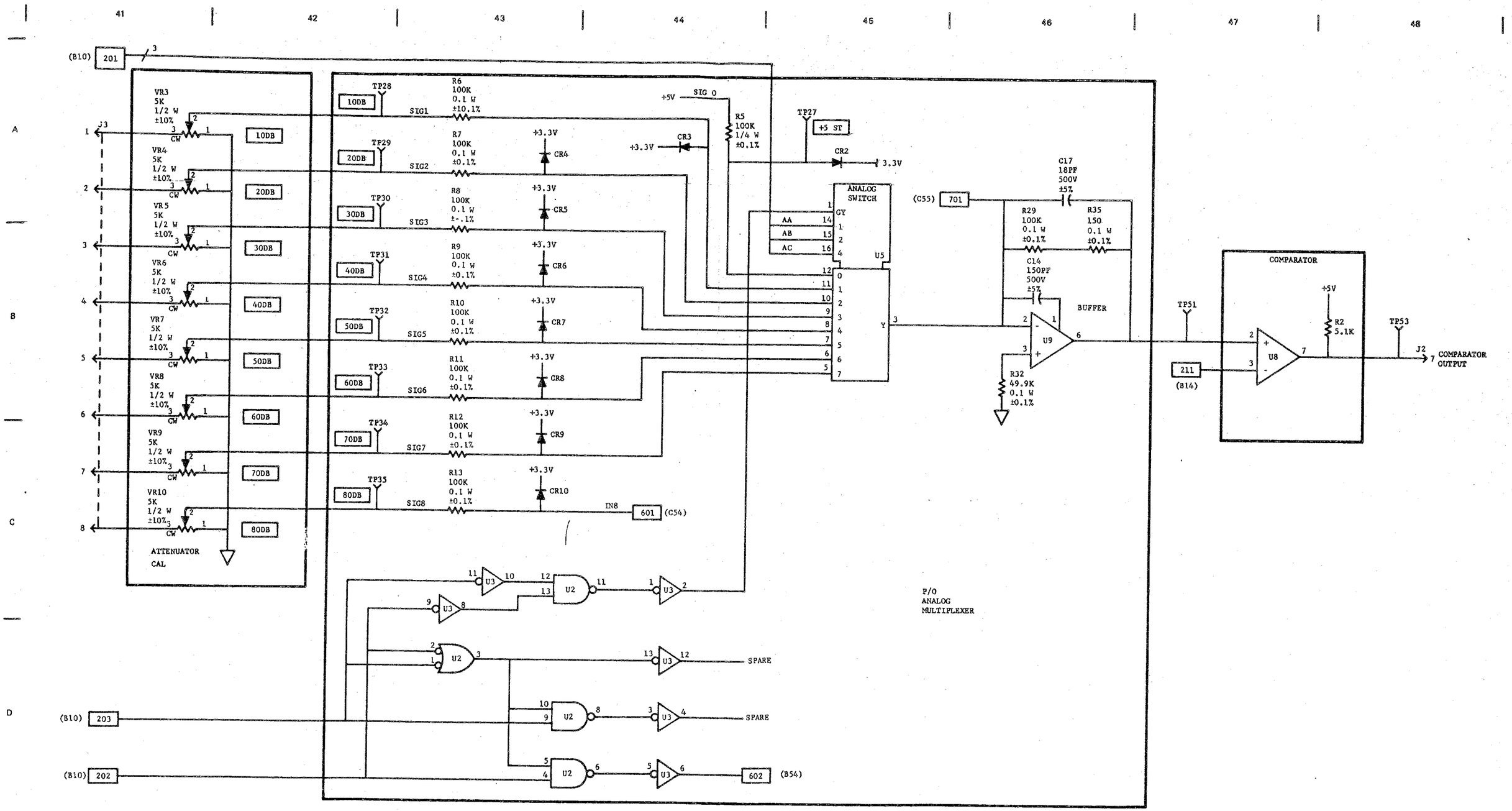


Figure 6-13. Microwave Interface 1A1A3 (58139-40010) Schematic Diagram (Sheet 6 of 7)

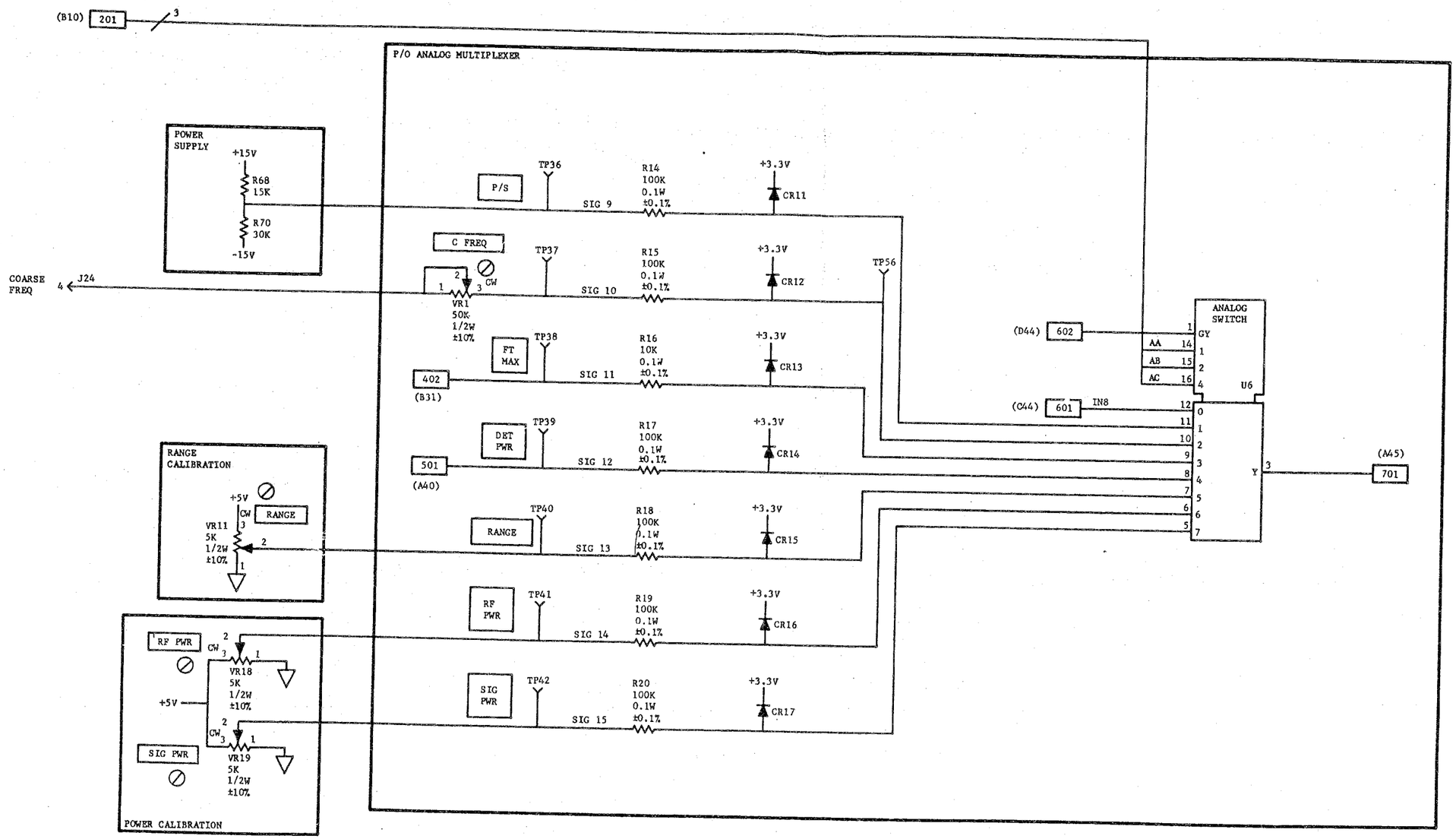


Figure 6-13. Microwave Interface 1A1A3 (58139-40010) Schematic Diagram (Sheet 7 of 7)

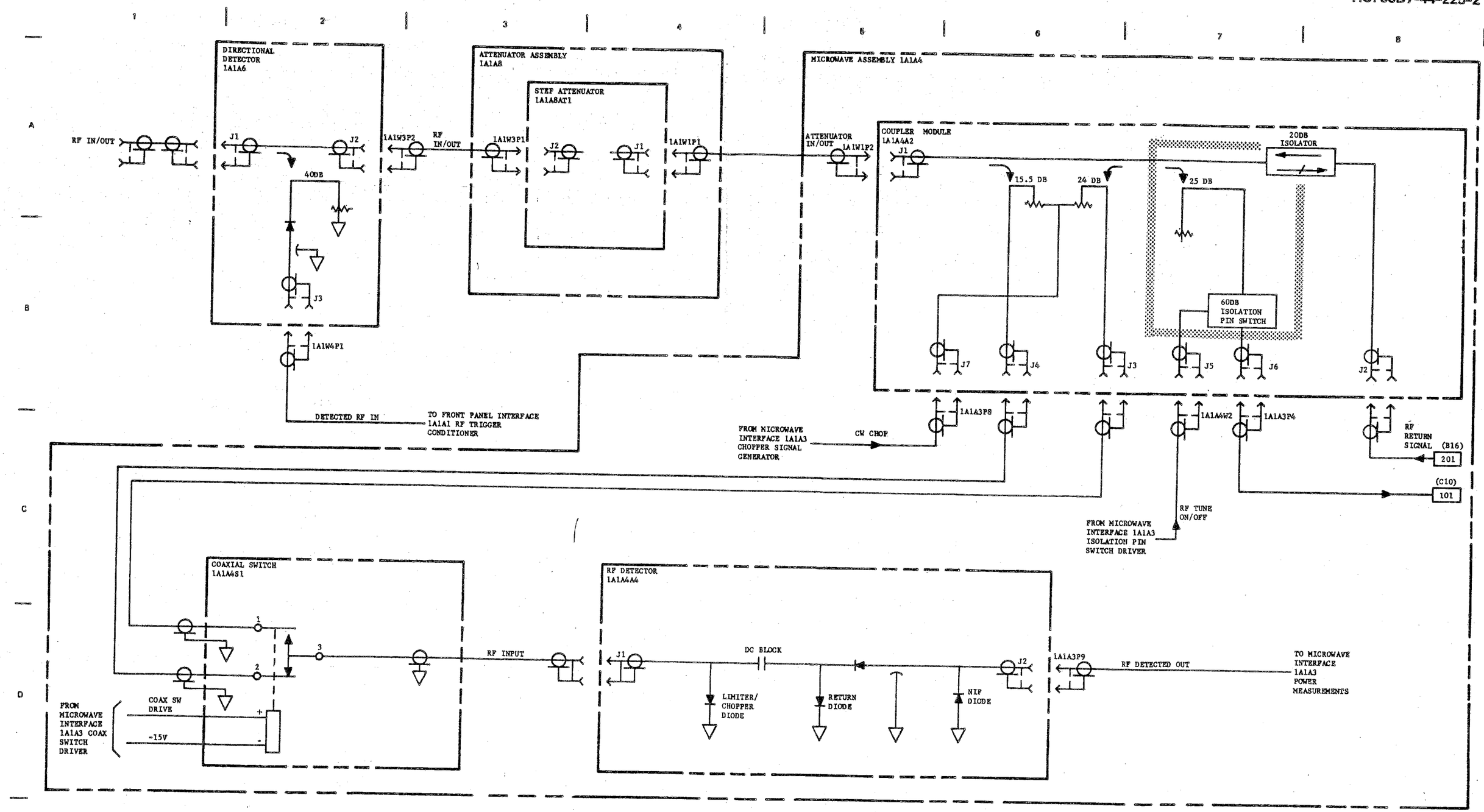


Figure 6-14. Microwave Assembly 1A1A4 (58139-40060) Schematic Diagram (Sheet 1 of 2)

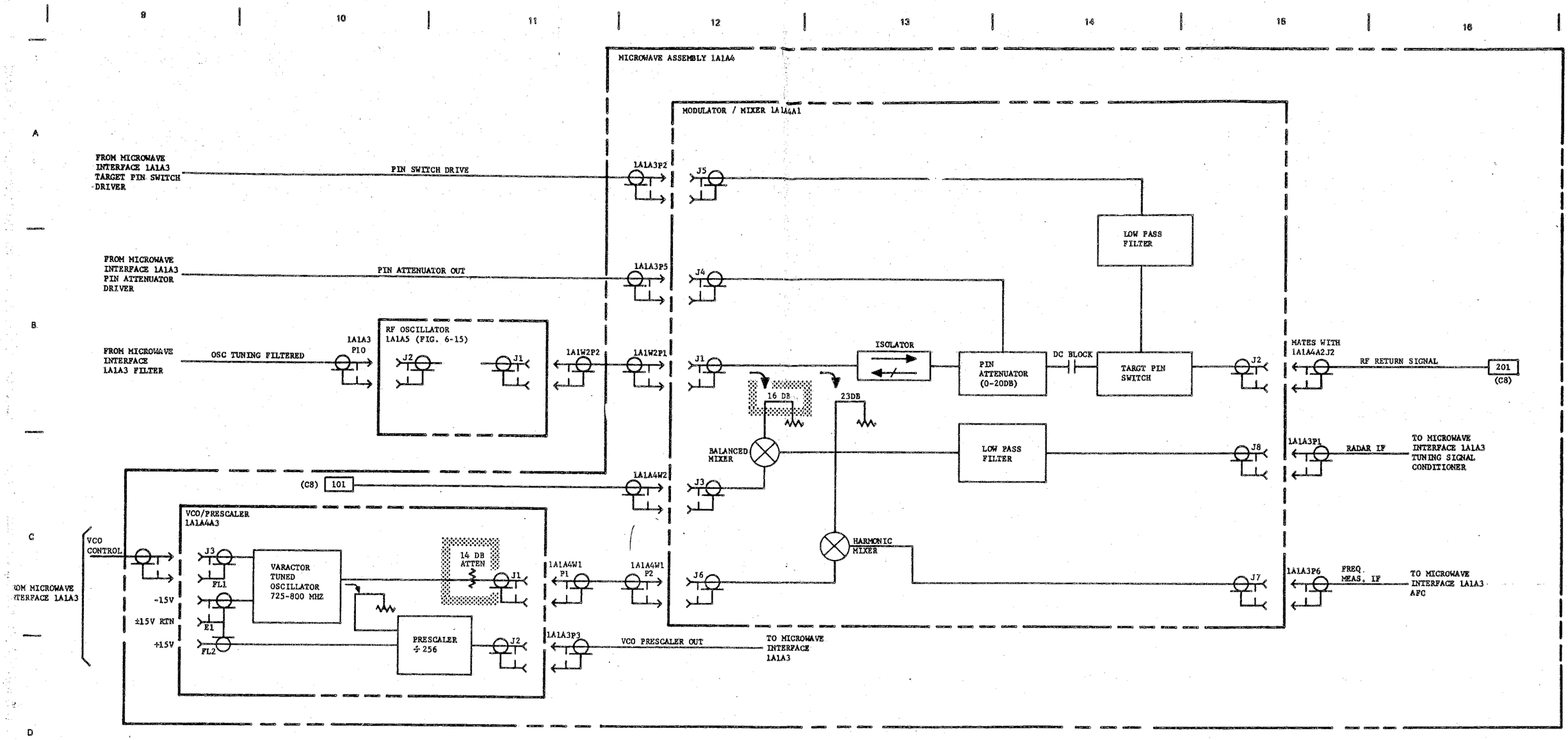
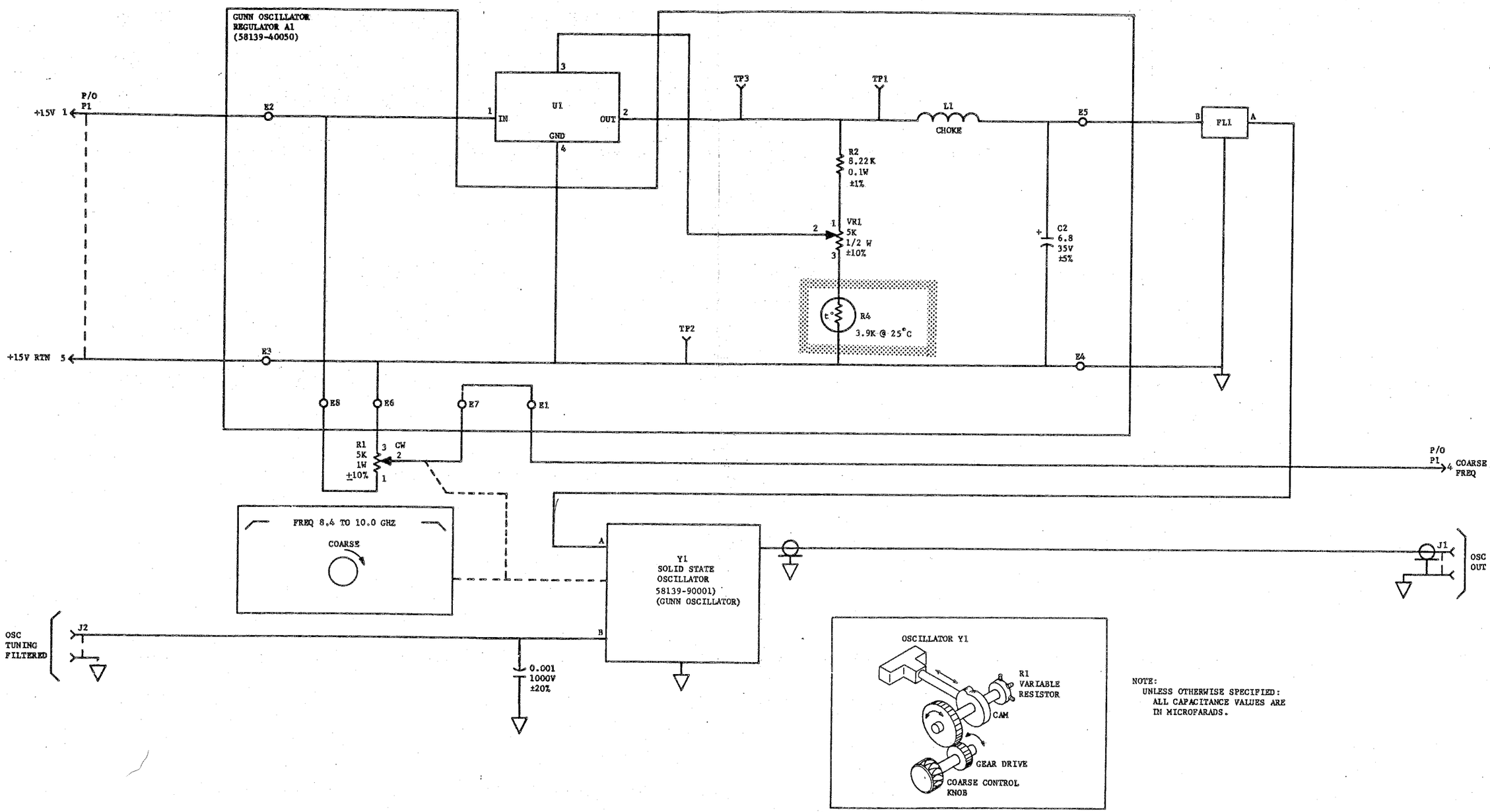


Figure 6-14. Microwave Assembly 1A1A4 (58139-40060) Schematic Diagram (Sheet 2 of 2)



NOTE:
UNLESS OTHERWISE SPECIFIED:
ALL CAPACITANCE VALUES ARE
IN MICROFARADS.

Figure 6-15. RF Oscillator 1A1A5 (58139-40030) Schematic Diagram

TABLE 6-2. TEST SET (58139-40010) WIRE DATA LIST

FROM	TO	COMMENTS
CB1-01	J01- A	115 VAC
CB1-02	FL1-01	115 VAC ON
DS1-01	S03- C	+5 VDC
DS1-02	S05D12	+5 VDC RET
E01	J01- C	CHASSIS GROUND
E02	PS1- CASE	CHASSIS GROUND
FL1-01	CB1-02	115 VAC ON
FL1-02	J01- B	115 VAC
FL1-03	S01-02	115 VAC FILTERED
FL1-04	S01-05	115 VAC FILTERED
J01- A	CB1-01	115 VAC
J01- B	FL1-02	115 VAC
J01- C	E01	CHASSIS GROUND
J03-01	P10-03	TRIGGER
J03-02	P10-10	TRIGGER SHIELD
J04-01	S04-02	TRIGGER OUT
J04-02	P08-07	TRIGGER OUT SHIELD
J05-01	P11-06	RF ENV/PULSE MON
J05-01	P02-09	RF ENV/PULSE MON
J05-02	P02-10	RF ENV/PULSE MON SHIELD
J05-02	P11-04	RF ENV/PULSE MON SHIELD
J06-01	P07-03	EXT MOD
J06-02	P07-06	EXT MOD SHIELD
J07-01	S02-03	115 VAC PANEL ON
J07-02	S02-06	115 VAC PANEL ON
PS1- +15 RET	TB1-01	+15 VDC RET
PS1- +5 VDC	TB1-21	+5 VDC
PS1- -15 VDC	TB1-17	-15 VDC
PS1-115 VAC	S01-03	115 VAC ON
PS1-CASE	E02	CHASSIS GROUND
PS1-115 VAC	S01-06	115 VAC ON
PS1- +15 VDC	TB1-13	+15 VDC
PS1- -15 RET	TB1-05	-15 VDC RET
PS1- +5 RET	TB1-09	+5 VDC RET
P01-01	TB1-24	+5 VDC
P01-04	TB1-12	+5 VDC RET
P01-05	TB1-16	+15 VDC
P01-06	TB1-04	+15 VDC RET
P01-08	TB1-08	-15 VDC RET
P01-09	TB1-20	-15 VDC

TABLE 6-2. TEST SET (58139-40010) WIRE DATA LIST - Continued

FROM	TO	COMMENTS
P02-02	R01-02	FINE RF POWER
P02-04	R01-03	-15 VDC RET
P02-06	R01-01	-15 VDC
P02-09	J05-01	ENV/PULSE MON
P02-10	J05-02	ENV/PULSE MON SHIELD
P03-01	TB1-22	+5 VDC
P03-03	TB1-22	+5 VDC
P03-04	TB1-10	+5 VDC RET
P03-06	TB1-10	+5 VDC RET
P04-01	TB1-23	+5 VDC
P04-04	TB1-11	+5 VDC RET
P04-05	TB1-15	+15 VDC
P04-06	TB1-03	+15 VDC RET
P04-08	TB1-07	-15 VDC RET
P04-09	TB1-19	-15 VDC
P05-01	S07-05	+5 VDC
P05-02	S06D05	+5 VDC RET
P05-03	P13-13	ROW 4
P05-04	P13-10	ROW 3
P05-05	P13-09	COL 1
P05-06	P13-05	COL 4
P05-07	P13-04	ROW 2
P05-08	P13-03	COL 3
P05-09	P13-02	COL 2
P05-10	P13-01	ROW 1
P05-11	S05D C	MODE 23
P05-12	S05C C	MODE 22
P05-13	S05B C	MODE 21
P05-14	S05A C	MODE 20
P05-15	S06D C	DISPLAY SELECT 23
P05-16	S06C C	DISPLAY SELECT 22
P05-18	S06A C	DISPLAY SELECT 20
P05-19	S07-03	MOD
P05-20	S06B C	DISPLAY SELECT 21
P07-01	S05E07	FM
P07-02	R05-03	-15 VDC
P07-03	J06-01	EXT MOD
P07-04	R02B03	PRF CONTROL
P07-06	J06-02	EXT MOD SHIELD
P07-07	S05E08	FM SHIELD
P07-08	S05E05	FM EXT SHIELD

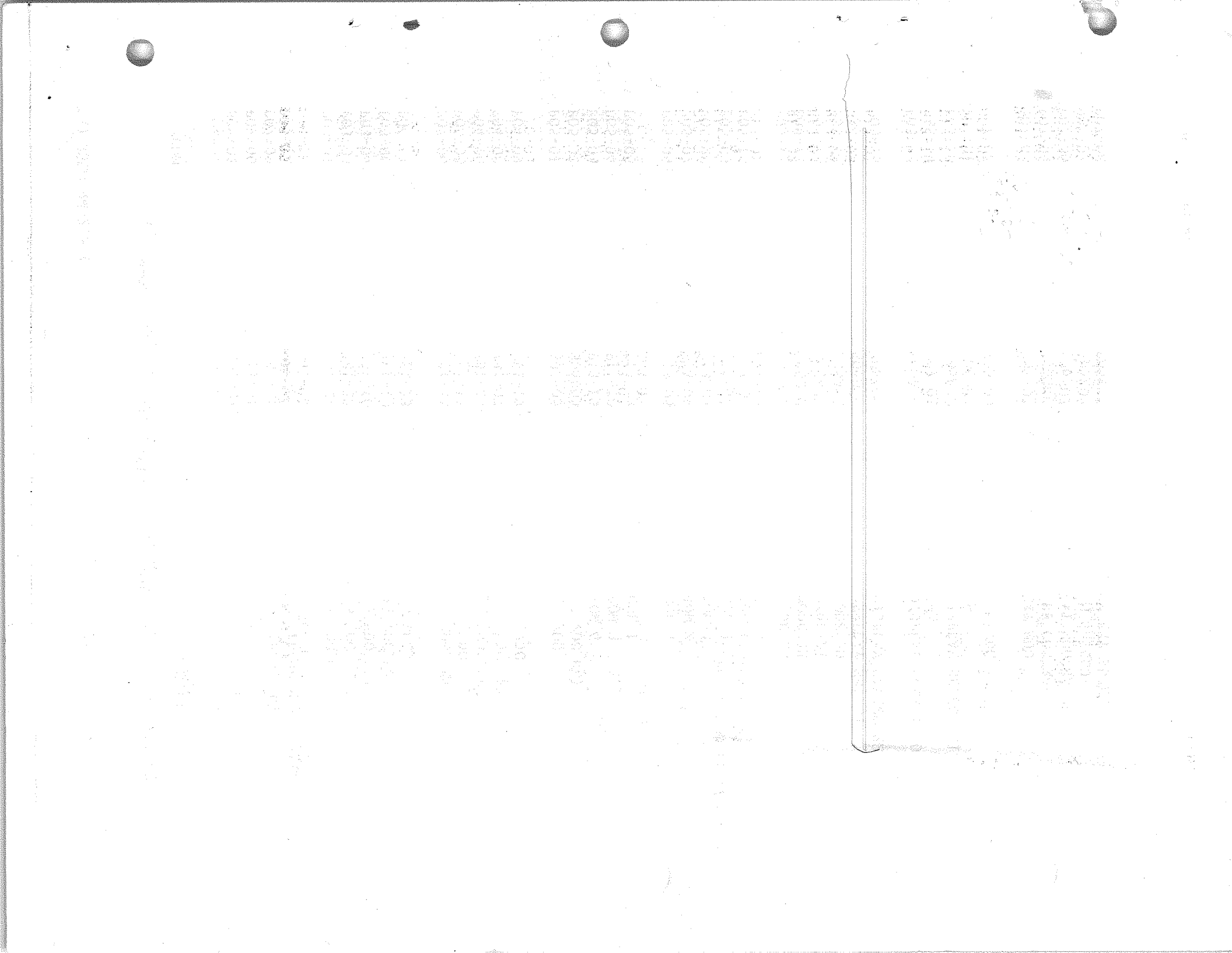


TABLE 6-2. TEST SET (58139-40010) WIRE DATA LIST - Continued

FROM	TO	COMMENTS
P07-09	S05E06	FM EXT
P08-02	S04-01	TRIGGER OUT NEG
P08-04	S04-03	TRIGGER OUT POS
P08-05	R04-02	FM DEVN
P08-07	J04-02	TRIGGER OUT SHIELD
P08-09	S05E12	FM/FM EXT SHIELD
P08-10	S07-09	HOLD HIGH
P09-04	R05-02	FINE FREQ
P09-05	S07-10	HOLD LOW
P09-06	S07-07	MOD/HOLD LOW
P09-08	S05E C	FM/FM EXT
P09-09	S07-08	GUNN TUNING
P10-01	R03-03	FM RATE
P10-02	S03-03	TRIGGER INT
P10-03	J03-01	TRIGGER
P10-04	S03-04	TRIGGER RF
P10-06	S03-01	TRIGGER NEG
P10-08	R04-01	FM DEVN EXC CCW
P10-09	S03-02	TRIGGER POS
P10-10	J03-02	TRIGGER SHIELD
P11-01	R04-03	FM DEVN EXC CW
P11-02	R03-01	+15 VDC
P11-04	J05-02	RF ENV/PULSE MON SHIELD
P11-06	J05-01	RF ENV/PULSE MON
P13-01	P05-10	ROW 1
P13-02	P05-09	COL 2
P13-03	P05-08	COL 3
P13-04	P05-07	ROW 2
P13-05	P05-06	COL 4
P13-07	S06D12	+5 VDC RET
P13-09	P05-05	COL 1
P13-10	P05-04	ROW 3
P13-13	P05-03	ROW 4
R01-01	P02-06	-15 VDC
R01-02	P02-02	FINE RF POWER
R01-03	P02-04	-15 VDC RET
R02A01	R02A02	JUMPER
R02A01	S05D05	+5 VDC RET
R02A02	R02A01	JUMPER
R02A03	R02B02	JUMPER

TABLE 6-2. TEST SET (58139-40010) WIRE DATA LIST - Continued

FROM	TO	COMMENTS
S05D05	S06D05	+5 VDC RET
S05D12	DS1-02	+5 VDC RET
S05E C	P09-08	FM/FM EXT
S05E05	P07-08	FM EXT SHIELD
S05E06	P07-09	FM EXT
S05E07	P07-01	FM
S05E08	P07-07	FM SHIELD
S05E12	P08-09	FM/FM EXT SHIELD
S06A C	P05-18	DISPLAY SELECT 20
S06B C	P05-20	DISPLAY SELECT 21
S06C C	P05-16	DISPLAY SELECT 22
S06D C	P05-15	DISPLAY SELECT 23
S06D05	P05-02	+5 VDC RET
S06D05	S05D05	+5 VDC RET
S06D12	P13-07	+5 VDC RET
S07-02	S07-04	JUMPER
S07-03	P05-19	MOD
S07-04	R02B03	PRF CONTROL
S07-05	P05-01	+5 VDC
S07-05	S07-11	+5 VDC
S07-07	P09-06	MOD/HOLD LOW
S07-08	P09-09	GUNN TUNING
S07-09	P08-10	HOLD HIGH
S07-10	P09-05	HOLD LOW
S07-11	S03- C	+5 VDC
S07-11	S07-05	+5 VDC
S08- B	S08- K	JUMPER
S08- C	S08- J	JUMPER
S08- J	S08- C	JUMPER
S08- K	S08- B	JUMPER
TB1-01	PS1- +15 RET	+15 VDC RET
TB1-03	P04-06	+15 VDC RET
TB1-04	P01-06	+15 VDC RET
TB1-05	PS1- -15 RET	-15 VDC RET
TB1-07	P04-08	-15 VDC RET
TB1-08	P01-08	-15 VDC RET
TB1-09	PS1- +5 RET	+5 VDC RET
TB1-10	P03-04	+5 VDC RET
TB1-10	P03-06	+5 VDC RET
TB1-11	P04-04	+5 VDC RET

TABLE 6-2. TEST SET (58139-40010) WIRE DATA LIST -Continued

FROM	TO	COMMENTS
TB1-12	P01-04	+5 VDC RET
TB1-13	PS1- +15 VDC	+15 VDC
TB1-15	P04-05	+15 VDC
TB1-16	P01-05	+15 VDC
TB1-17	PS1- -15 VDC	-15 VDC
TB1-19	P04-09	-15 VDC
TB1-20	P01-09	-15 VDC
TB1-21	PS1- +5 VDC	+5 VDC
TB1-22	P03-01	+5 VDC
TB1-22	P03-03	+5 VDC
TB1-23	P04-01	+5 VDC
TB1-24	P01-01	+5 VDC

*U.S.GOVERNMENT PRINTING OFFICE: 1982-569-060/285. Region 4.

TECHNICAL MANUAL

ILLUSTRATED PARTS BREAKDOWN

TEST SET, RADAR, AN/UPM-145, 58139-40001

AAI Corporation
F33657-78-C-0394

This manual supersedes T.O. 33D7-44-225-4 dated 1 November 1979 and incorporates Change 1 dated 31 March 1980.

Published under authority of the Secretary of the Air Force.

LIST OF EFFECTIVE PAGES

INSERT LATEST CHANGED PAGES. DESTROY SUPERSEDED PAGES.

NOTE: The portion of the text affected by the changes is indicated by a vertical line in the outer margins of the page. Changes to illustrations are indicated by miniature pointing hands. Changes to wiring diagrams are indicated by shaded areas.

Dates of issue for original and changed pages are:

Original...0... 1 July 1980

TOTAL NUMBER OF PAGES IN THIS PUBLICATION IS 64 CONSISTING OF THE FOLLOWING:

Page No.	# Change No.	Page No.	# Change No.
Title	0		
A	0		
i	0		
ii Blank	0		
1-1 - 1-5	0		
1-6 Blank	0		
2-1 - 2-43	0		
2-44 Blank	0		
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4-1 - 4-4	0		

Zero in this column indicates an original page.

TABLE OF CONTENTS

SECTION I

INTRODUCTION

1-1. SCOPE. This manual lists, describes, and illustrates assemblies sub-assemblies, and detail parts for Test Set, Radar, AN/UPM-145, manufactured by AAI Corporation, Cockeysville, Maryland (Federal Supply Code 97384).

1-2. PURPOSE AND USE. The purpose of this Illustrated Parts Breakdown is to provide a list of items necessary for support of the Radar Test Set. This manual is for use in requisitioning, storing, issuing, and identifying parts. This manual consists of a table of contents, introduction, Maintenance Parts List, Numerical Index, and Reference Designation Index.

1-3. SECTION I. INTRODUCTION. The introduction provides instruction for the use of information contained in Sections II, III, and IV.

1-4. SECTION II. MAINTENANCE PARTS LIST. The Maintenance Parts List is an illustrated breakdown of the equipment in disassembly sequence. In general, the assemblies and parts installed at the time the end item was manufactured, are listed and identified in the manual. Interchangeable and substitute assemblies and parts, subsequently authorized by the Government, are not listed in this manual; such items are identified by information available through the Interchangeable and Substitute (I & S) Data Systems. Refer to T.O. 00-25-184. This list includes the figure and index number, part number, federal supply code for manufacturers, description, units per assembly, usable on code, and source, maintenance, and Parts List are presented in the following paragraphs.

a. Figure and Index Number. This column identifies the figure that illustrates each listed item, and the index number that identifies the item on the illustration. On multiple sheet illustrations, the sheet number follows the figure number, separated by a diagonal.

b. Part Number Column. The numbers in the part number column are either the contractors' assigned numbers, Government standard numbers (AN, MS, etc) or vendor part numbers.

c. Federal Supply Code for Manufacturers (FSCM) Column. This column lists the appropriate five-digit numerical FSCM, as published in the current issues of H4-1, H4-2, H4-3 Cataloging Handbooks, Federal Supply Code for Manufacturers, directly opposite each part, model, and type number listed in the part number column. The FSCM identifies the manufacturer or Government agency whose number appears in the part number column. A complete listing of code-to-names and addresses of manufacturers reflected within this manual are provided in paragraph 1-8.

d. Description. This column lists items within the equipment in disassembly sequence (where applicable). Descriptions include appropriate nomenclature to define the items. An indented arrangement, utilizing ledder points, shows the relationship between a part and that parts' next higher assembly. Attaching parts are listed immediately following and at the same indention as the item they attach. Attaching parts are indentified by the abbreviation "AP" immediately following the description.

e. Units Per Assembly. The quantity shown in this column reflects the total quantity of a part required by that part's next higher assembly. This quantity is not necessarily the total used for the complete equipment; for total items required per equipment, refer to the quantity-per-end item column of the Section III Numerical Index. The abbreviation AR is used to indicate usage "As Required" of a particular item.. The abbreviation REF is used to indicate that the quantity of an item used per assembly is listed in the next higher assembly of the Maintenance Parts List.

f. Usable On Code. This column presents an alphabetical code indicating specific usability of all parts, when different equipment configurations exist. Where no usable on code appears, the listed part is applicable to all equipment configurations covered by this manual.

g. Source Maintenance and Recoverability (SMR) Code Column. This column contains the five-digit Joint Military Services Uniform SMR codes assigned by the Government and furnished by the procuring activity. Definitions of these codes are available in T.O. 00-25-195.

1-5. SECTION III. NUMERICAL INDEX. The Numerical Index presented in Section III consists of an alphanumerical listing of all parts of this equipment. Included in this list are references to figure and index numbers of Section II, and quantity per end item.

a. Part Number Column. This column contains the manufacturer numbers of all parts in the equipment as covered in the Maintenance Parts List, Section II. The part numbers are in alphanumerical order as follows:

Part number arrangement begins on the extreme left position and continues to the right. The first position arrangement of the part number is as follows:

Letters A through N, P through Z, Numerals 0 Through 9

The second position arrangement and succeeding positions are as follows:

Space (blank column)
Diagonal (slant)
Point (period)
Dash (-)
Letters A through N, P through Z, Numerals 0 through 9

b. Figure and Index Number Column. This column identifies the figure that illustrates each listed item, and the index number(s) that identifies the item on the illustration.

c. Quantity Per End Item Column. This column contains the total units required per article. The total quantity appears on the same line as the part number regardless of the different figures and index numbers listed.

1-6. SECTION IV. REFERENCE DESIGNATION INDEX. The Reference Designation Index provides an alphanumerical listing of all reference designations assigned to items listed in the Maintenance Parts List. The full reference designation is used in listing all items. When the reference designation is known and the item description is desired, the item should be located in the Reference Designation Index presented in Section IV.

1-7. SYMBOLS AND ABBREVIATIONS

a. Symbols. The part number for decalcomanias, metalcals, and vinyl film markings is followed, flush right, by an asterisk (*) symbol. This symbol signifies "Requisition this marking in accordance with the requirements of AFR 6-4." The part number for Government Furnished Equipment is followed, flush right, by a number sign (#) symbol. All symbols are in accordance with MIL-M-38807.

b. Abbreviations. Abbreviations used within this manual conform with MIL-STD-12C.

1-8. MANUFACTURERS' CODES. Following is a list of Federal manufacturers' codes and names and addresses of vendors, arranged in numerical sequence of Federal Manufacturers' Codes. At the end of the list, in alphabetical sequence, are manufacturers' names and addresses to whom no code has been assigned.

00779 AMP INC
PO BOX 3608
HARRISBURG PA 17105

01295 TEXAS INSTRUMENTS INC
PO BOX 5012
13500 N CENTRAL EXPRESSWAY
DALLAS TX 75222

06540 AMATOM ELECTRONIC HARDWARE
DIV MITE CORP
446 BLAKE ST
NEW HAVEN CT 06515

06773 TIMBER-TOP INC
PO BOX 517 HOPKINS RD
WATERTOWN CT 06795

07263 FAIRCHILD CAMERA &
INSTRUMENT CORP
SEMICONDUCTOR DIV
464 ELLIS ST
MOUNTAIN VIEW CA 94042

07418 SUNBANK ELECTRONICS INC
3110 NIMONA AVE
BURBANK CA 91504

07700 TECHNICAL WIRE PRODUCTS INC
129 DERMODY ST
CRANFORD NJ 07016

07886 NATIONAL RADIO CO INC
COMMERCIAL PRODUCTS DIV
89 WASHINGTON ST
MELROSE MA 02176

08524 DEUTSH FASTENER CORP
PO BOX 92925
7001 W IMPERIAL HWY
LOS ANGELES CA 90045

12881 METEX CORP
970 DURHAM RD
EDISON NJ 08817

13103 THERMALLOY CO INC
PO BOX 34829
2021 W VALLEY VIEW LA
DALLAS TX 75234

18565 CHOMERICS INC
77 DRAGON COURT
WOBURN MA 01801

22526 BERG ELECTRONICS INC
YOUK EXPRESSWAY
NEW CUMBERLAND PA 17070

24355 ANALOG DEVICES INC
PO BOX 280
NORWOOD MA 02062

27014 NATIONAL SEMICONDUCTOR CORP
2900 SEMICONDUCTOR DR
SANTA CLARA CA 95051

29440 BERG INC
499 OCEAN AVE
EAST ROCKAWAY LI NY 11518

31918 IEE/SCHADOW INC
8081 WALLACE RD
EDEN PRAIRIE MN 55343

32559 BIVAR INC
1617 E EDINGER AVE
SANTA ANA CA 92705

34649 INTEL CORP
3065 BOWERS AVE
SANTA CLARA CA 95051

51829 CR INDUSTRIES
CHICAGO RAWHIDE MFG CO
MACON COUNTY INDUSTRIAL PK
HWY 64 W BYPASS
FRANKLIN, NC 28734

52063 EXAR INTEGRATED SYSTEMS
750 PALOMAR AVE
SUNNYVALE CA 94086

72619 MASON BOX CO
521 MOUNT HOPE ST
ATTLEBORO FALL MA 02763

79409 WOODHEAD DANIEL CO
3411 WOODHEAD DR
NORTHBROOK IL 60062

81349 MILITARY SPECIFICATIONS
PROMULGATED BY MILITARY
DEPARTMENTS/AGENCIES UNDER
AUTHORITY OF DEFENSE
STANDARDIZATION MANUAL
4120 3-M

81831 FILTRON CO INC
6 AERIAL WAY
SYOSSET NY 11791

83330 HERMAN H SMITH INC
812 SNEDIKER AVE
BROOKLYN NY 11207

95077 SOLITRON/MICROWAVE
PO BOX 278
PORT SALERNO FL 33492

95987 WECKESSER CO INC
4444 WEST IRVING PARK RD
CHICAGO IL 60641

96906 MILITARY SPECIFICATIONS
PROMULGATED BY MILITARY
DEPARTMENTS/AGENCIES UNDER
AUTHORITY OF DEFENSE
STANDARDIZATION MANUAL
4120 3-M

97384 AAI CORP
COCKEYSVILLE MD 21030

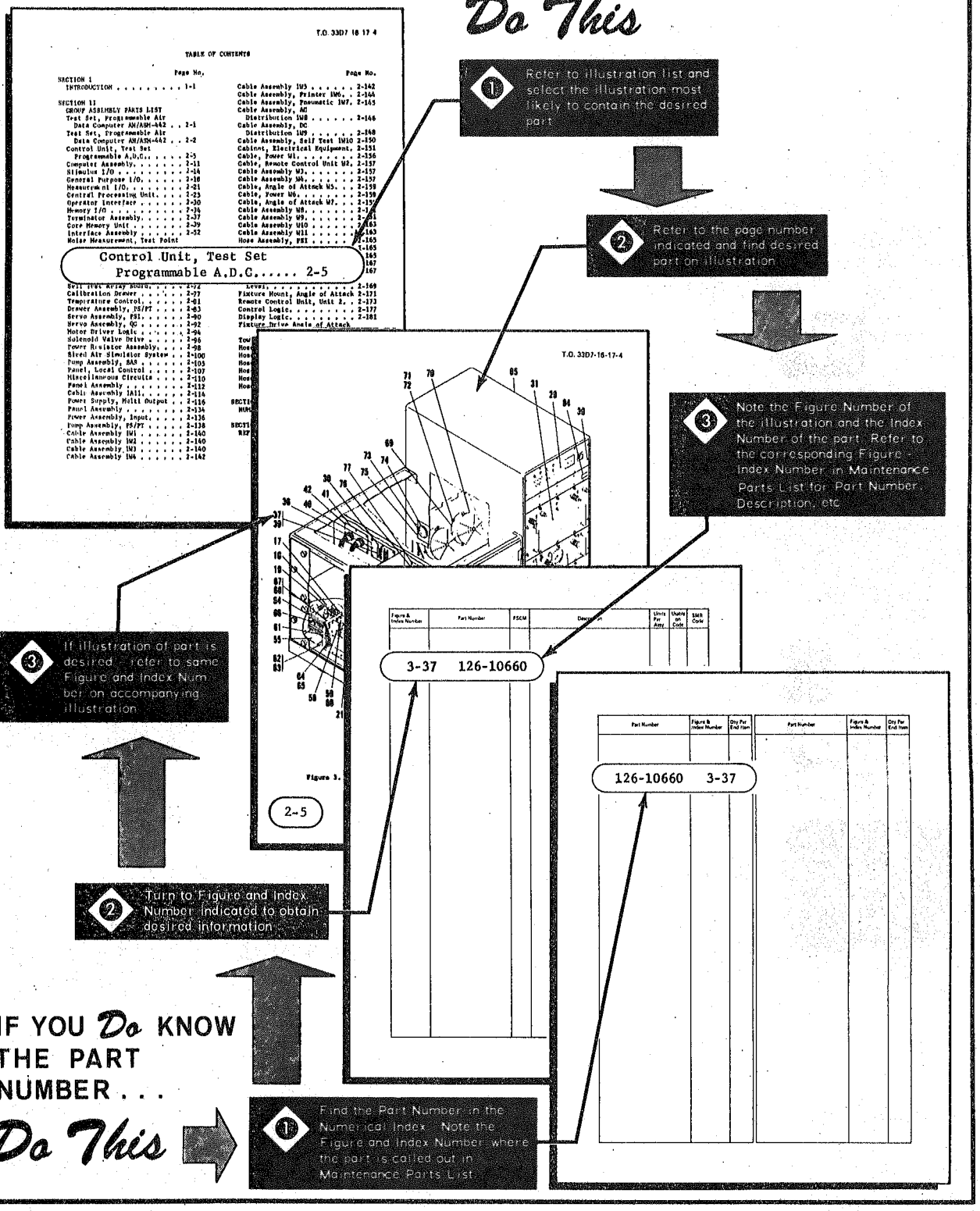
98159 RUBBER TECK INC
PO BOX 389
19115 HAMILTON AVE
GARDENA CA 90247

1-9. HOW TO USE THE PARTS BREAKDOWN. Instructions on how to use the Illustrated Parts Breakdown when the part number is not known and when the part number is known are provided on the following page.

HOW TO USE THE ILLUSTRATED PARTS BREAKDOWN

IF YOU *Don't* KNOW THE PART NUMBER...

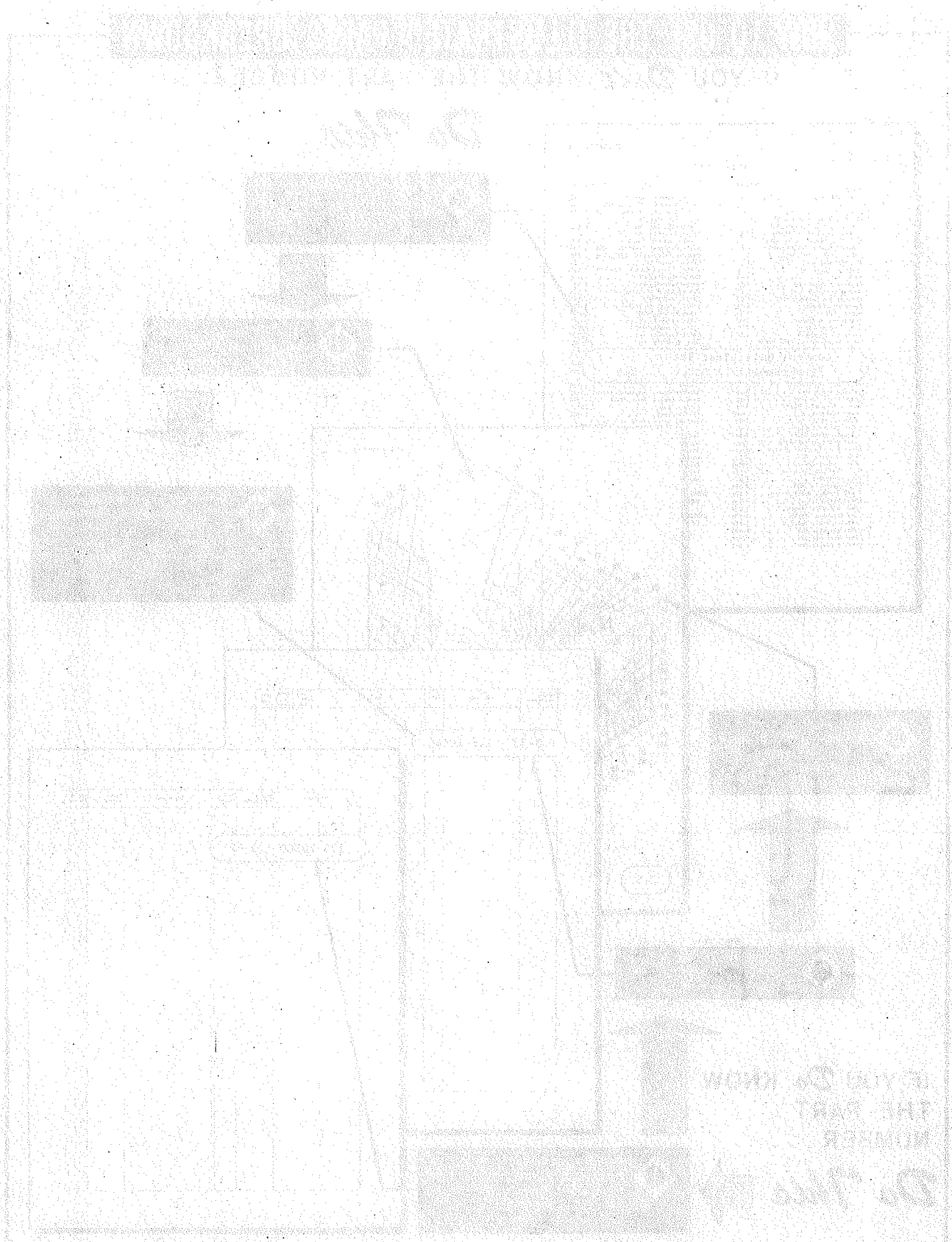
Do This



IF YOU *Do* KNOW THE PART NUMBER . . .

Do This

1. Find the Part Number in the Numerical Index. Note the Figure and Index Number where the part is called out in Maintenance Parts List



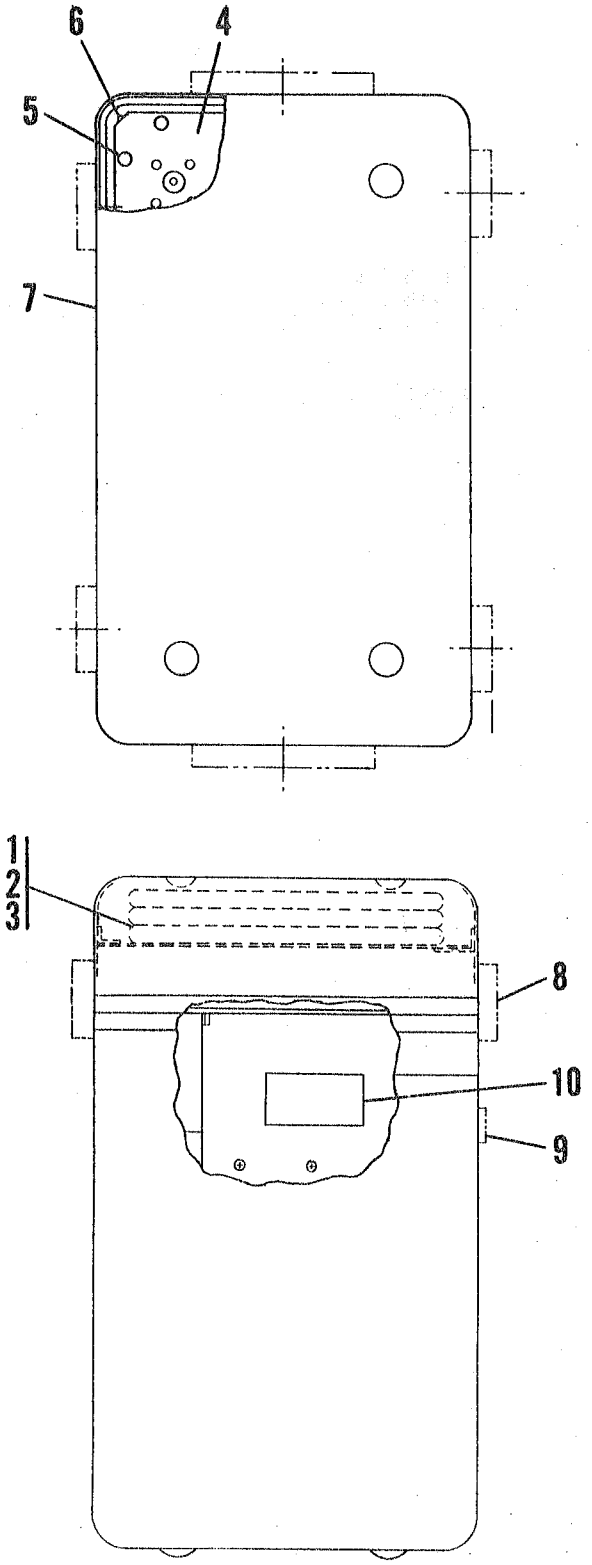


Figure 1. Test Set, Radar AN/UPM-145

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
1 -	58139-40001	97384	TEST SET, RADAR, AN/UPM-145.....	1		
-1	58139-40035	97384	.CABLE, SPECIAL PURPOSE, ELECTRICAL (POWER) SEE FIG 2 FOR DETAILS	1		AFFFF
-2	58139-40040	97384	.CABLE, SPECIAL PURPOSE, ELECTRICAL (RF) SEE FIG 3 FOR DETAILS	1		AFFFF
-3	58139-40045	97384	.CABLE, SPECIAL PURPOSE, ELECTRICAL (BNC) SEE FIG 4 FOR DETAILS	1		AFFFF
-4	58139-40005	97384	.TEST SET ELECTRONICS ASSEMBLY SEE FIG 5 FOR DETAILS	1		ADDDD
-5	MS51958-64	96906	.SCREW (AP).....	18		PAFZZ
	MS15795-808	96906	.WASHER (AP).....	18		PAFZZ
-6	58139-40019	97384	.GASKET.....	1		PAFZZ
-7	58139-90010	97384	.COMBINATION CASE (SOURCE CONTROL.. FROM PART NUMBER M17146 MFD BY 54215)	1		PBFFF
-8	B1900-656	82240	..LATCH.....	4		PAFZZ
-9	MH6-611	54215	..VALVE, PRESSURE RELIEF.....	1		PAFZZ
-10	58139-40082	97384	.PLATE, WARRANTY.....	1		

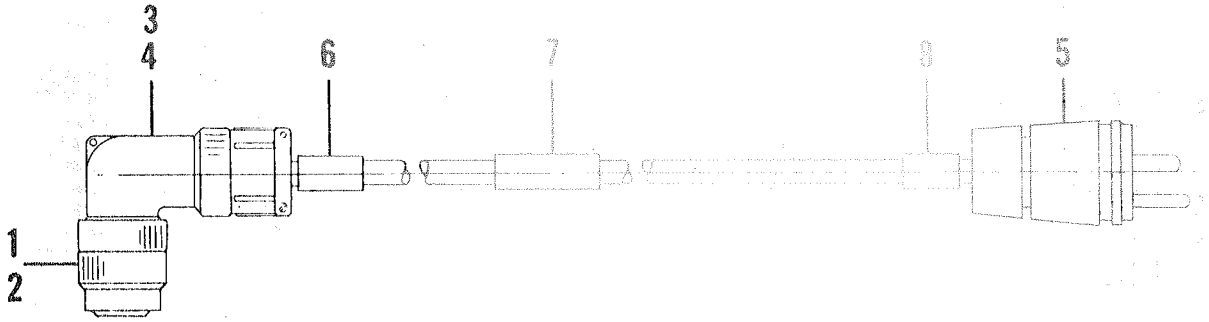


Figure 2. Cable, Special Purpose Electrical (Power)

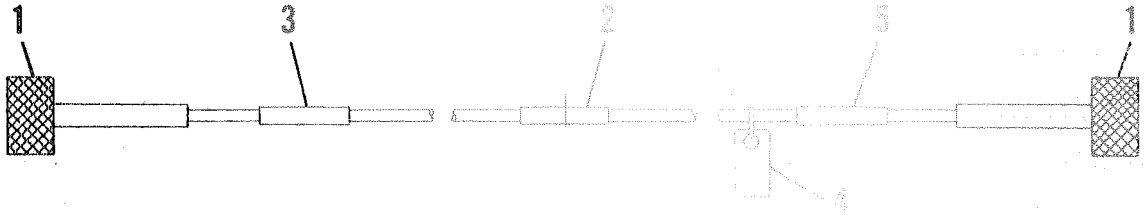


Figure 3. Cable, Special Purpose Electrical (RF)

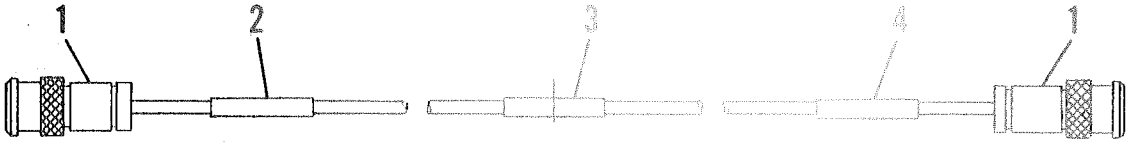
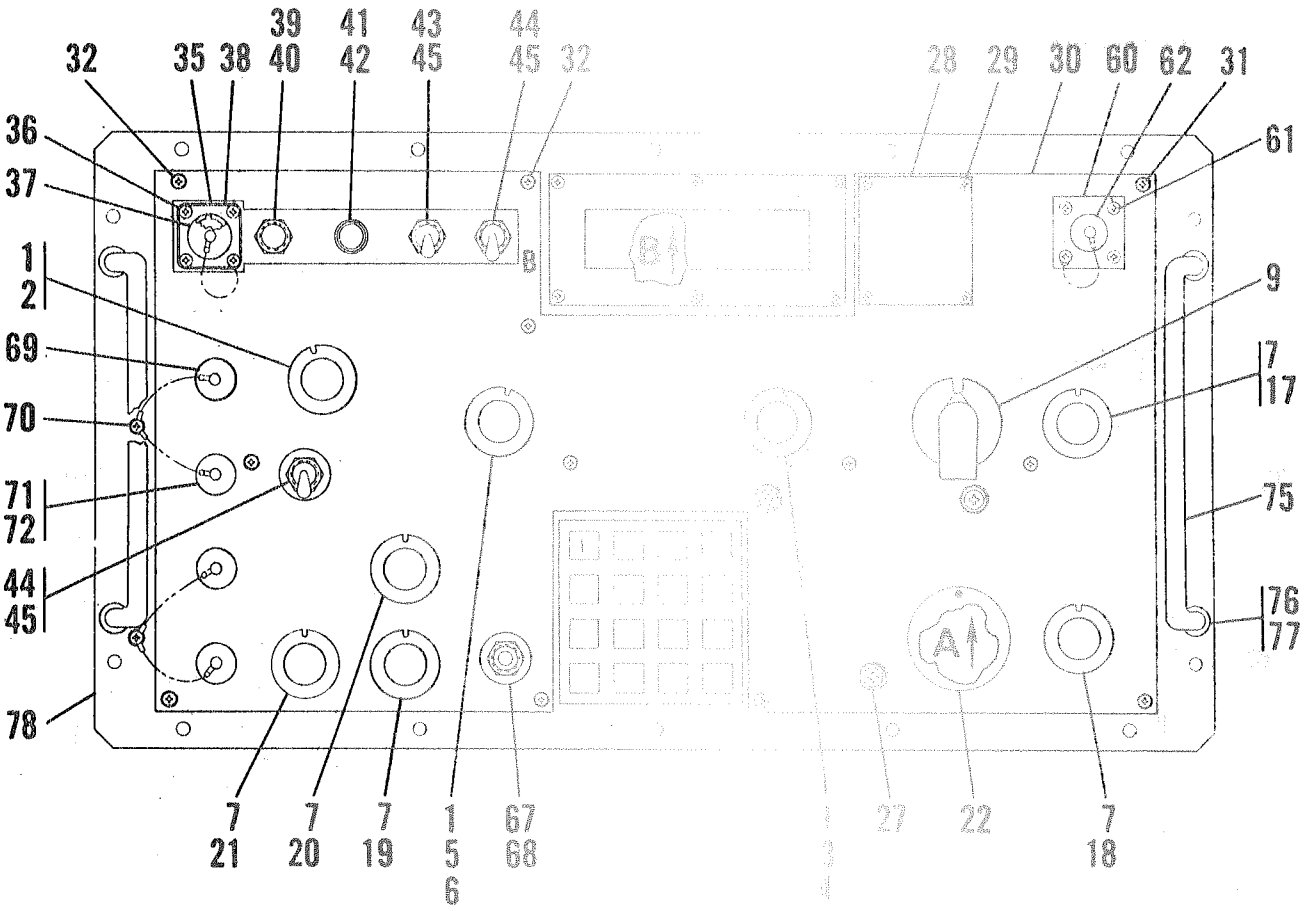


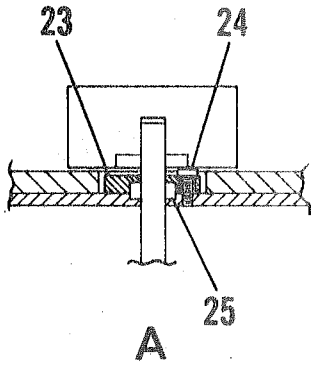
Figure 4. Cable, Special Purpose Electrical (BNC)

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
2 -	58139-40035	97384	CABLE, SPECIAL PURPOSE, ELECTRICAL. (POWER) SEE FIG 1 FOR NHA	REF		AFFFF
-1	MS3476L12-3S	96906	.CONNECTOR	1		PAFZZ
-2	M39029-5-16-16	81349	.CONTACT	3		XBFZZ
-3	M85049/8-7W	81349	.ADAPTER	1		PAFZZ
-4	NAS1745-3	80205	.BUTT SPLICE	3		PAZZN
-5	14W47	79409	.CONNECTOR, PLUG	1		PAFZZ
-6	58139-40035-1	97384	.MARKER, CABLE	1		MFFZZ
-7	58139-40035-2	97384	.MARKER, CABLE	1		MFFZZ
-8	58139-40035-3	97384	.MARKER, CABLE	1		MFFZZ
	M16878-1-20BLK	81349	.WIRE	AR		XBFZZ
	M16878-1-22BLK	81349	.WIRE	AR		XBFZZ

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
3 -	58139-40040	97384	CABLE, SPECIAL PURPOSE, ELECTRICAL. (RF) SEE FIG 1 FOR NHA	REF		AFFFF
-1	M39012/01-0005	81349	.CONNECTOR	2		PAFZZ
-2	58139-40040-1	97384	.MARKER, CABLE	1		MFFZZ
-3	58139-40040-2	97384	.MARKER, CABLE	1		MFFZZ
-4	58139-40043	97384	.TAG	1		XBFZZ
-5	58139-40040-3	97384	.MARKER, CABLE	1		MFFZZ
	M17-075-RG214	81349	.WIRE	AR		XBFZZ

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
4 -	58139-40045	97384	CABLE, SPECIAL PURPOSE, ELECTRICAL. (BNC) SEE FIG 1 FOR NHA	REF		AFFFF
-1	M39012/16-0001	96906	.CONNECTOR, PLUG	2		PAFZZ
-2	58139-40045-2	97384	.MARKER, CABLE	1		MFFZZ
-3	58139-40045-1	97384	.MARKER, CABLE	1		MFFZZ
-4	58139-40045-3	97384	.MARKER, CABLE	1		MFFZZ
	M17/028-RG58C/U	81349	.CABLE	AR		





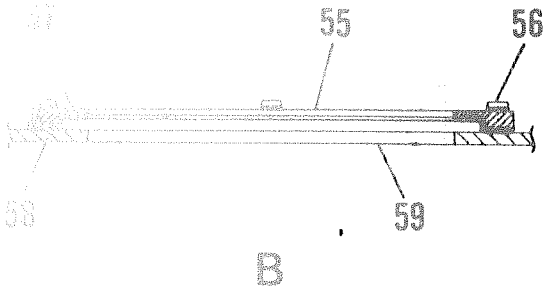


Figure 5. Test Set, Electronics Assembly (Sheet 1 of 6)

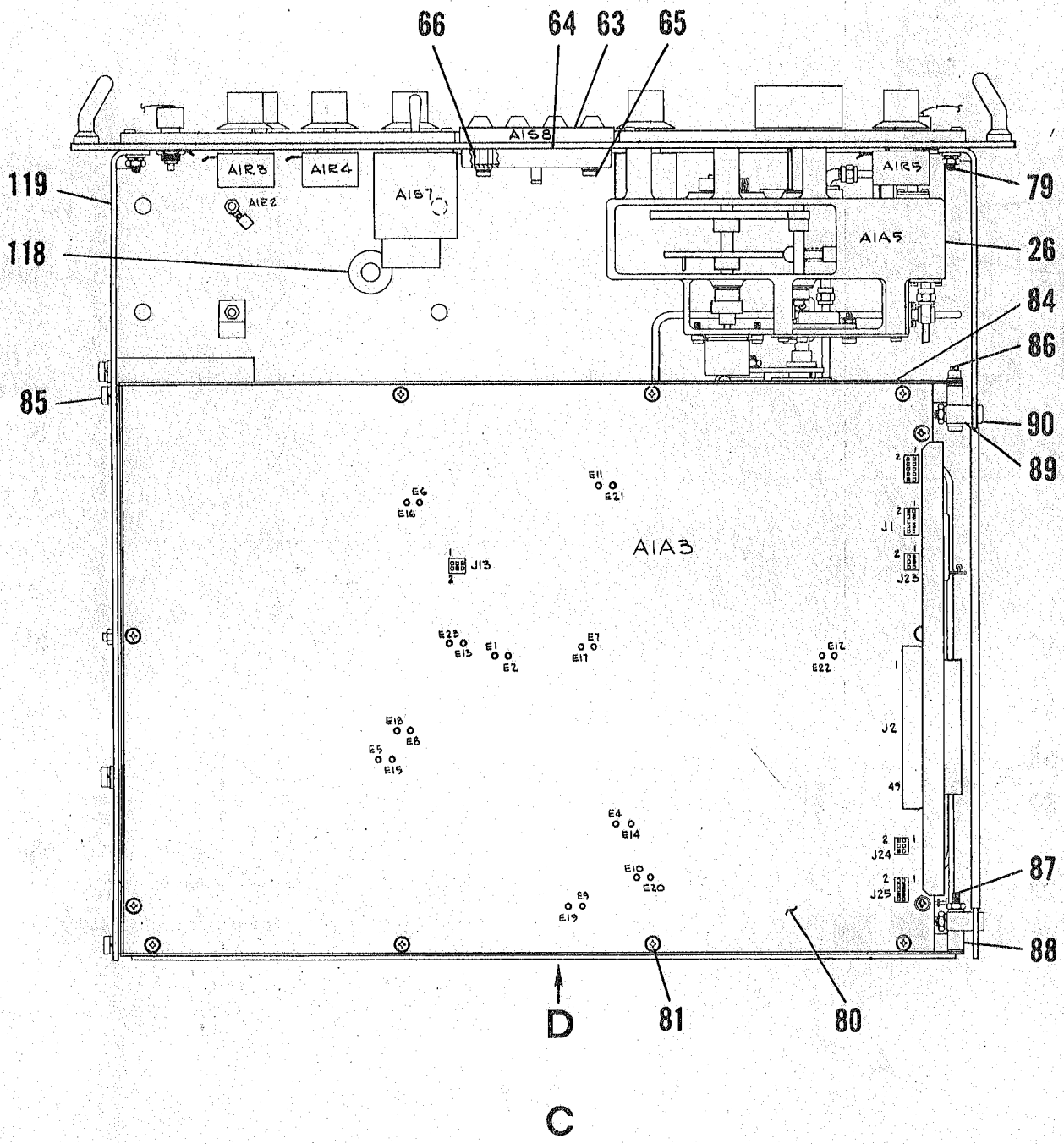
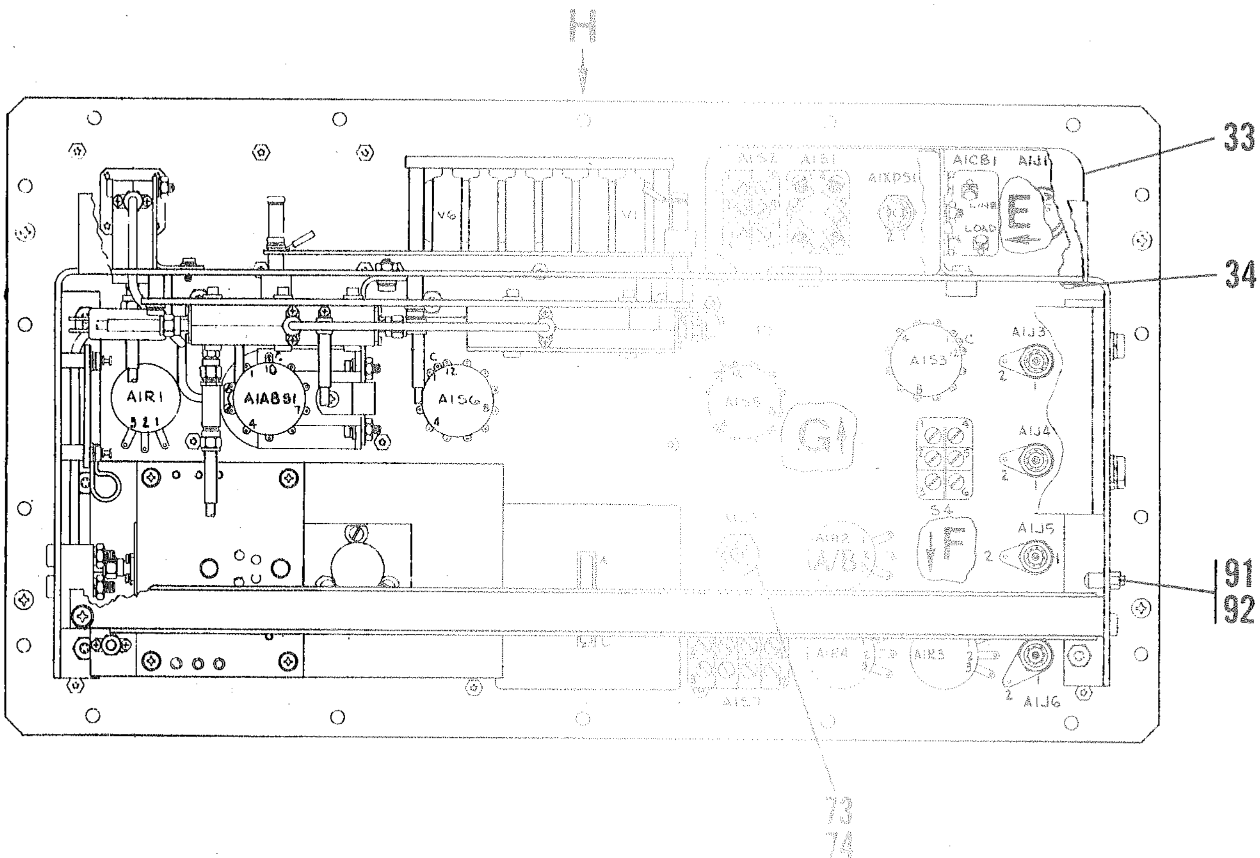


Figure 5. Test Set, Electronics Assembly (Sheet 2 of 6)



D

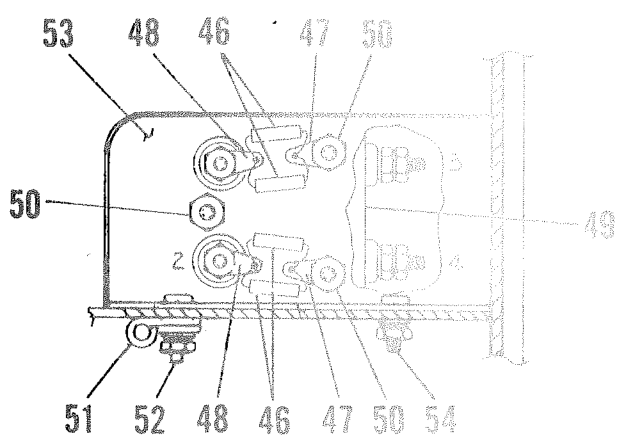


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Figure 5. Test Set, Electronics Assembly (Sheet 3 of 6)

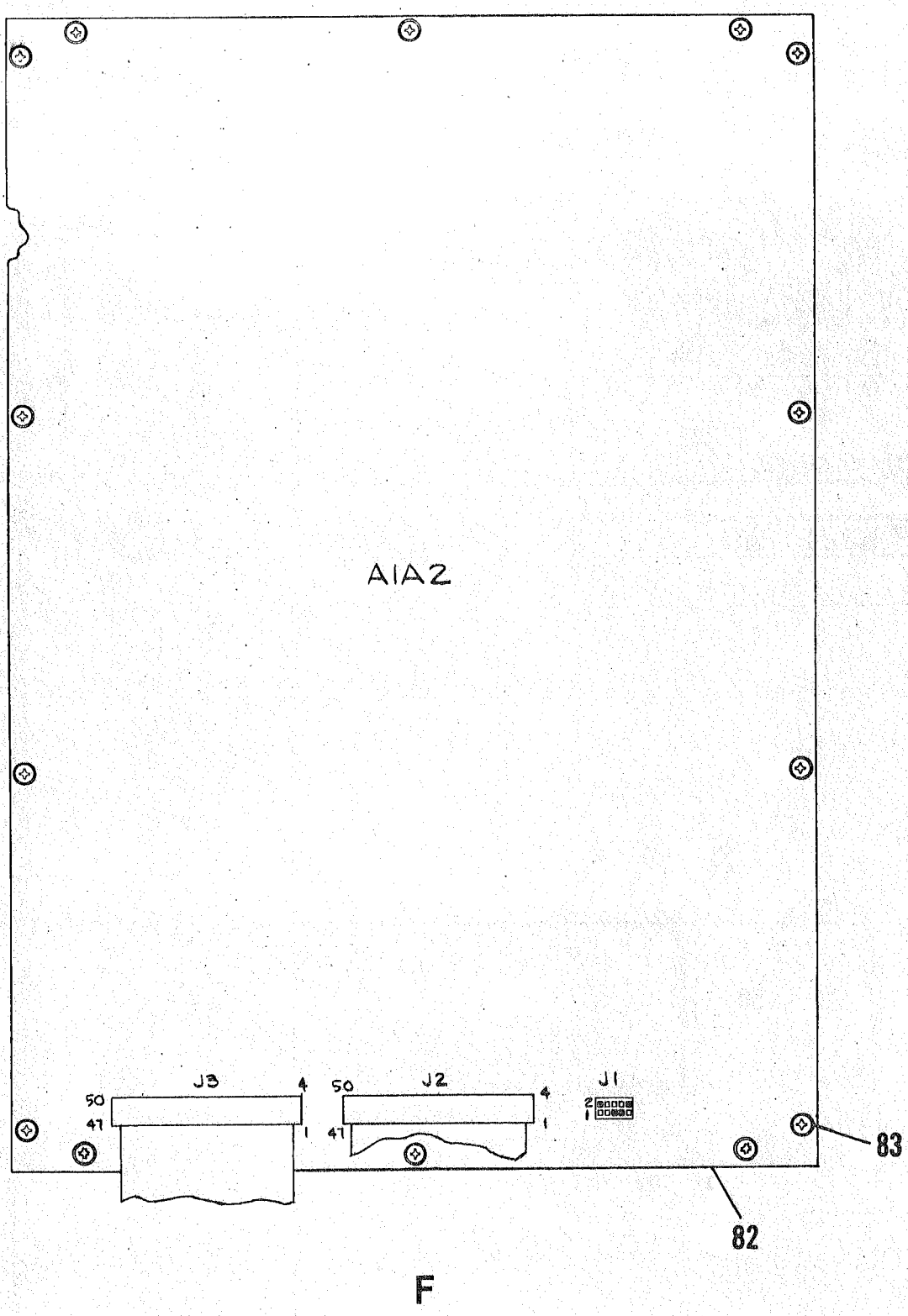


Figure 5. Test Set, Electronics Assembly (Sheet 4 of 6)

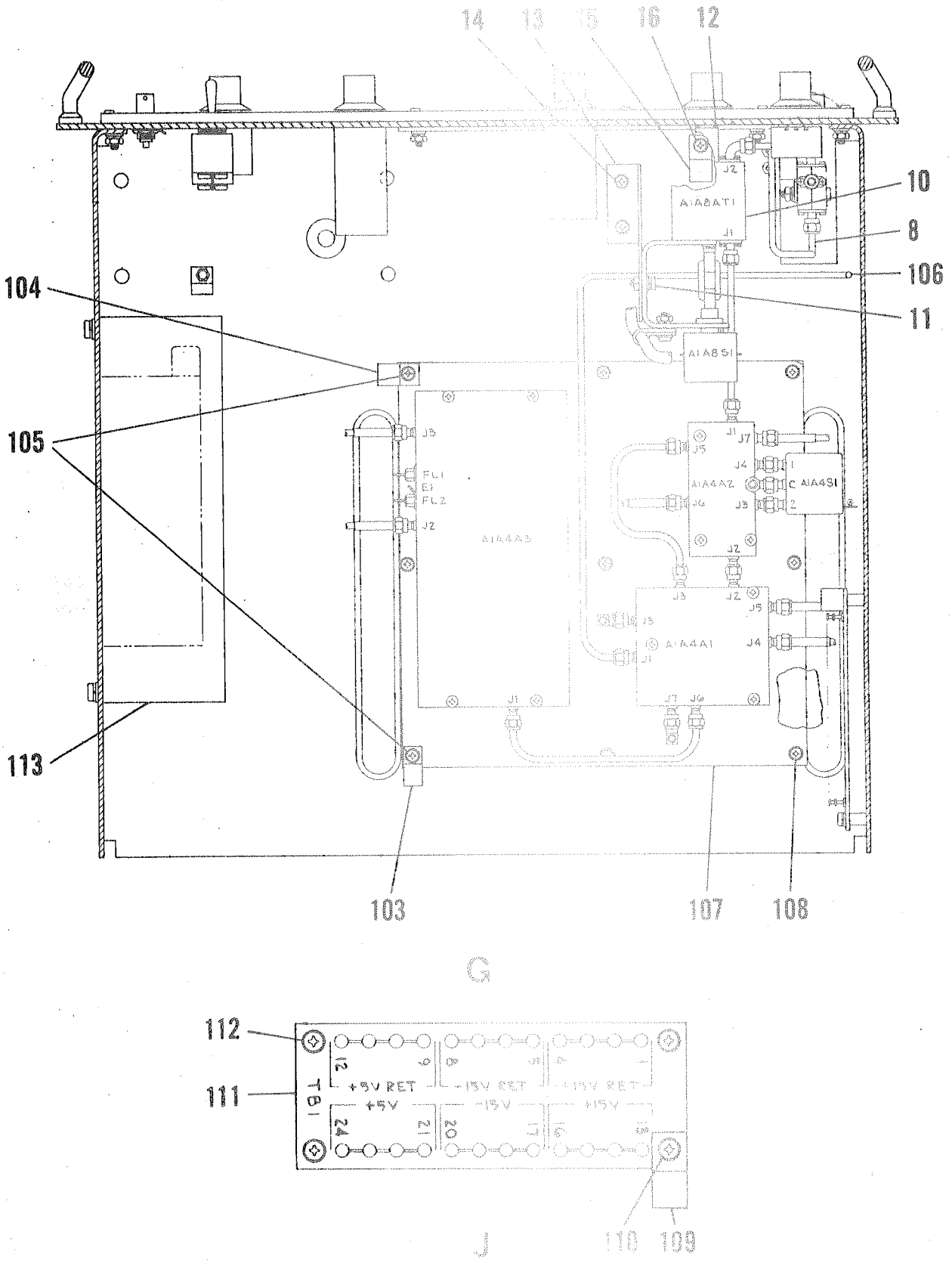


Figure 5. Test Set, Electronics Assembly (Sheet 5 of 6)

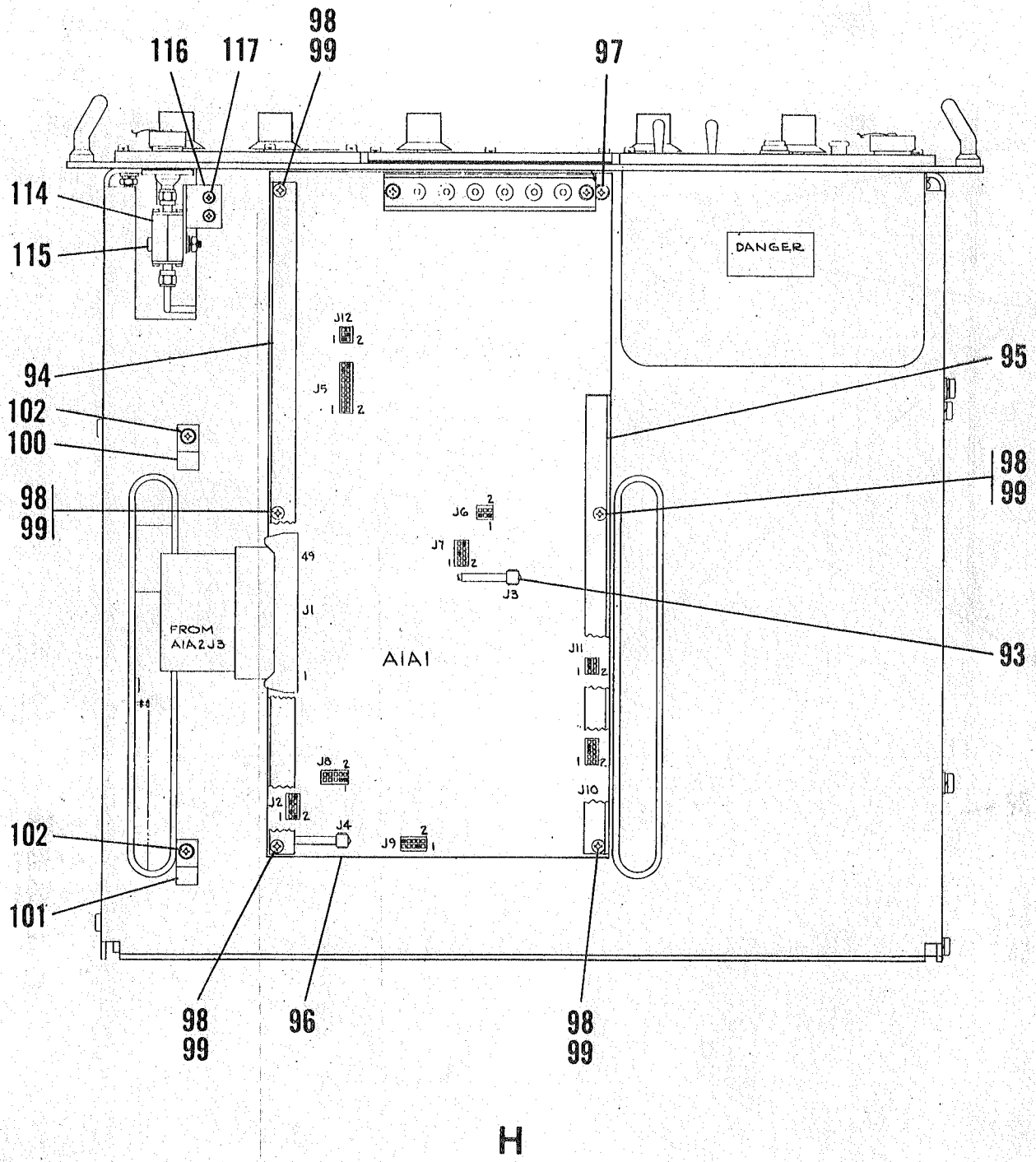


Figure 5. Test Set, Electronics Assembly (Sheet 6 of 6)

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
5 -	58139-40005	97384	TEST SET, ELECTRONICS ASSEMBLY SEE FIG 1 FOR NHA	REF		ADDDD
/ 1-1	MS91528-1H4B	96906	.KNOB	3		PAFZZ
/ 1-2	M3786/4-5004	81349	.SWITCH, ROTARY	1		PAFZZ
	58139-40070	97384	.SWITCH ASSEMBLY	1		AFFFF
/ 1-3	1199C	83330	..NUT, PLAIN (AP)	1		XBFZZ
/ 1-4	M3786/4-5077	81349	..SWITCH, ROTARY	1		PAFZZ
	58139-40075	97384	.SWITCH ASSEMBLY	1		AFFFF
/ 1-5	1199C	83330	..NUT, PLAIN (AP)	1		XBFZZ
/ 1-6	M3786/4-5099	81349	..SWITCH, ROTARY	1		PAFZZ
/ 1-7	MS91528-1H2B	96906	.KNOB	5		PAFZZ
/ 5-8	58139-90009-5	97384	.CABLE ASSEMBLY (SOURCE CONTROLLED. FROM PART NUMBER 58139-90009-5 MFD BY 98291)	1		PAFZZ
/ 1-9	58139-40078	97384	.KNOB (ALTERED FROM PART NUMBER MS91528-1B4B MFD BY 81349)	1		
/ 5-10	58139-40055	97384	.ATTENUATOR ASSEMBLY SEE FIG 6 FOR DETAILS	1		AFFFF
/ 5-11	MS51957-30	96906	.SCREW, MACHINE (AP)	2		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP)	2		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP)	2		PAFZZ
	MS35649-264	96906	.NUT, PLAIN (AP)	2		PAFZZ
/ 5-12	84-30200	07700	.O RING	1		XBFZZ
/ 5-13	58139-40068	97384	.BRACKET	1		MFFZZ
/ 5-14	MS51957-29	96906	.SCREW, MACHINE (AP)	2		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP)	2		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP)	2		PAFZZ
	MS35649-264	96906	.NUT, PLAIN (AP)	2		PAFZZ
/ 5-15	MS25281-R5	96906	.CLAMP, LOOP	1		PAFZZ
/ 5-16	MS51957-26	96906	.SCREW, MACHINE (AP)	1		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP)	1		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP)	1		PAFZZ
/ 1-17	RV4SAYSD103A	81349	.RESISTOR, VARIABLE	1		PAFZZ
/ 1-18	RV4SAYSD254A	81349	.RESISTOR, VARIABLE	1		PAFZZ
/ 1-19	RV4SAYSD103C	81349	.RESISTOR, VARIABLE	1		PAFZZ
/ 1-20	58139-90032	97384	.POTENTIOMETER, DUAL AAI SPEC CONT. DWG 58139-90032 R2A/8	1		PAFZZ
/ 1-21	RV4SAYSD254C	81349	.RESISTOR, VARIABLE	1		PAFZZ
/ 1-22	MS91528-4C2B	96906	.KNOB	1		PAFZZ
/ 1-23	58139-40018	97384	.COVER	1		MFFZZ
/ 1-24	MS51957-15	96906	.SCREW, MACHINE (AP)	3		PAFZZ
/ 1-25	2450	51829	.SEAL BUSHING	1		PAFZZ
/ 2-26	58139-40030	97384	.RF OSCILLATOR ASSEMBLY SEE FIG 7 FOR DETAILS	1		AFFFF
/ 1-27	MS51957-43B	96906	.SCREW, MACHINE (AP)	3		PAFZZ
	MS35338-137	96906	.WASHER, LOCK (AP)	3		PAFZZ
/ 1-28	58139-40047	97384	.NAMEPLATE	1		XBFZZ
/ 1-29	MS51957-17	96906	.SCREW, MACHINE (AP)	4		PAFZZ
	MS35338-135	96906	.WASHER, LOCK (AP)	4		PAFZZ
/ 1-30	58139-90011	97384	.PANEL, ILLUMINATED (SOURCE CONTROLLED FROM PART NUMBER 58139-90011 MFD BY 72914)	1		PBFBZ
/ 1-31	MS51957-17B	96906	.SCREW, MACHINE (AP)	10		PAFZZ
/ 1-32	MS51957-15B	96906	.SCREW, MACHINE (AP)	2		PAFZZ
	MS15795-803B	96906	.WASHER, FLAT (AP)	12		PAFZZ
	MS35338-135	96906	.WASHER, LOCK (AP)	12		PAFZZ
/ 3-33	58139-40072	97384	.ENCLOSURE	1		MFFZZ
/ 3-34	MS51957-28	96906	.SCREW, MACHINE (AP)	4		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP)	4		PAFZZ
	070231-2	97384	..LABEL DANGER HIGH VOLTAGE	1		MFFZZ
/ 1-35	MS3470L12-3P	81349	.CONNECTOR	1		PAFZZ
/ 1-36	MS51957-17	96906	.SCREW, MACHINE (AP)	4		PAFZZ
	MS35338-135	96906	.WASHER, LOCK (AP)	4		PAFZZ
	MS35649-244	96906	.NUT, PLAIN (AP)	4		PAFZZ
/ 1-37	MS3181-12CW	96906	.COVER	1		PAFZZ
/ 1-38	08-0301-0126	12881	.GASKET	1		PAFZZ
/ 1-39	MS24510-5	96906	.CIRCUIT BREAKER	1		PAFZZ
/ 1-40	MS25196-1	96906	.SEAL, BUSHING	1		PAFZZ

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
5/ 1-41	MS25237-328	96906	.LAMP, INCANDESCENT	1		PAFZZ
/ 1-42	134-8430-0332-203	72619	.LIGHT, INDICATOR	1		PAFZZ
/ 1-43	MS25307-222	96906	.SWITCH, TOGGLE	1		PAFZZ
/ 1-44	MS24524-23	96906	.SWITCH, TOGGLE	2		PAFZZ
/ 1-45	MS25196-1	96906	.SEAL, BUSHING	3		PAFZZ
/ 3-46	RCR20G204JS	81349	.RESISTOR	4		PAFZZ
/ 3-47	MS77070-3	96906	.TERMINAL, LUG	2		PAFZZ
/ 3-48	MS77070-2	96906	.TERMINAL, LUG	2		PAFZZ
/ 3-49	SP-205	97384	.FILTER, RFI AAI SPEC CONT DWG 58139-90024	1		PAFZZ
/ 3-50	MS35649-284	96906	.NUT, PLAIN (AP)	3		PAFZZ
	MS35338-137	96906	.WASHER, LOCK (AP)	3		PAFZZ
	MS15795-807	96906	.WASHER, FLAT (AP)	3		PAFZZ
/ 3-51	MS25281-R2	96906	.CLAMP, LOOP	1		PAFZZ
/ 3-52	MS51957-31	96906	.SCREW, MACHINE (AP)	1		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP)	1		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP)	1		PAFZZ
	MS35649-264	96906	.NUT, PLAIN (AP)	1		PAFZZ
/ 3-53	58139-40048	97384	.BRACKET	1		MFFZZ
/ 3-54	MS51957-30	96906	.SCREW, MACHINE (AP)	1		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP)	1		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP)	1		PAFZZ
	MS35649-264	96906	.NUT, PLAIN (AP)	1		PAFZZ
/ 1-55	58139-40028	97384	.FRAME	1		XBFZZ
/ 1-56	MS51957-17B	96906	.SCREW, MACHINE (AP)	6		PAFZZ
	MS35338-135	96906	.WASHER, LOCK (AP)	6		PAFZZ
/ 1-57	58139-40026	97384	.GASKET	1		PAFZZ
/ 1-58	58139-40027	97384	.GASKET	1		PAFZZ
/ 1-59	58139-90023	97384	.WINDOW (SOURCE CONTROL FROM PART NUMBER 58139-90023 MFD BY 07700)	1		PAFZZ
/ 1-60	1132-6002	97384	.CONNECTOR, RECEPTACLE AAI SPEC CONT DWG 58139-90004	1		PAFZZ
/ 1-61	MS51957-15B	96906	.SCREW, MACHINE (AP)	4		PAFZZ
	MS35338-135	96906	.WASHER, LOCK (AP)	4		PAFZZ
/ 1-62	M39012-25-0011	81349	.COVER	1		PAFZZ
/ 2-63	EM22438	97384	.KEYBOARD (SOURCE CONTROLLED FROM PART NUMBER 58139-90028 MFD BY 91929)	1		PAFZZ
/ 2-64	58139-40064	97384	.COVER	1		MFFZZ
/ 2-65	MS51957-26	96906	.SCREW, MACHINE	2		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP)	2		PAFZZ
	MS15795-805	96906	.WASHER, FLAT	2		PAFZZ
/ 2-66	8391-SS-0632-7	06540	.SPACER	2		XBFZZ
/ 1-67	MS27406-3	96906	.SWITCH, TOGGLE	1		PAFZZ
/ 1-68	MS25196-1	96906	.SEAL, BUSHING	1		PAFZZ
/ 1-69	M39012-25-0006	81349	.COVER	4		PAFZZ
/ 1-70	MS51957-15B	96906	.SCREW, MACHINE (AP)	2		PAFZZ
	MS15795-8038	96906	.WASHER, FLAT (AP)	2		PAFZZ
/ 1-71	M39012/21-0001	81349	.CONNECTOR, RECEPTACLE	4		PAFZZ
/ 1-72	1497	83330	.LUG,SOLDER	4		PAFZZ
/ 3-73	MS90335-5	96906	.CONNECTOR, RECEPTACLE	1		PAFZZ
/ 3-74	84-30203	07700	.O RING	1		PAFZZ
/ 1-75	13227-A-0832-2	06540	.HANDLE	2		XBFZZ
/ 1-76	16022-A-2	06540	.FERRULE	4		PAFZZ
/ 1-77	MS24693-C50	96906	.SCREW, MACHINE (AP)	4		PAFZZ
/ 1-78	58139-40002	97384	.PANEL	1		AFFFF
/ 2-79	MS24693-C51	96906	.SCREW, MACHINE (AP)	9		PAFZZ
	MS15795-807	96906	.WASHER, FLAT (AP)	9		PAFZZ
	MS35338-137	96906	.WASHER, LOCK (AP)	9		PAFZZ
	MS35649-284	96906	.NUT, PLAIN (AP)	9		PAFZZ
/ 2-80	58139-40010	97384	.CIRCUIT CARD ASSEMBLY, MICROWAVE INTERFACE SEE FIGURE 10 FOR DETAILS	1		PAFFD
/ 2-81	MS51957-28	96906	.SCREW, MACHINE (AP)	14		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP)	14		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP)	14		PAFZZ
/ 4-82	58139-40015	97384	.CIRCUIT CARD ASSEMBLY, DIGITAL SEE FIGURE 11 FOR DETAILS	1		PAFFD

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
5/ 4-83	MS51957-26	96906	.SCREW, MACHINE (AP).....	14		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP).....	14		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP).....	14		PAFZZ
/ 2-84	58139-40073	97384	.FRAME ASSEMBLY.....	1		XBFZZ
/ 2-85	MS51957-41	96906	.SCREW, MACHINE (AP).....	2		PAFZZ
	MS35338-137	96906	.WASHER, LOCK (AP).....	2		PAFZZ
/ 2-86	MS51957-50	96906	.SCREW, MACHINE (AP).....	1		PAFZZ
/ 2-87	MS24693-C56	96906	.SCREW, MACHINE (AP).....	1		PAFZZ
	MS15795-807	96906	.WASHER, FLAT (AP).....	4		PAFZZ
	MS21042L08	96906	.NUT, SELF-LOCKING (AP).....	2		PAFZZ
/ 2-88	58139-40076	97384	.SPACER.....	2		PAFZZ
/ 2-89	58139-40013	97384	.PLATE.....	2		XBFZZ
/ 2-90	MS51957-48	96906	.SCREW, MACHINE (AP).....	2		PAFZZ
	MS35338-137	96906	.WASHER, LOCK (AP).....	2		PAFZZ
	MS35649-284	96906	.NUT, PLAIN (AP).....	2		PAFZZ
/ 3-91	070109-3-88	97384	.SPACER, SLEEVE ROUND 97384.....	1		PAFZZ
/ 3-92	MS51957-30	96906	.SCREW, MACHINE (AP).....	1		PAFZZ
	MS35649-264	96906	.NUT, PLAIN (AP).....	1		PAFZZ
/ 6-93	58139-40025-1	97384	.CABLE ASSEMBLY SEE FIG 8 FOR..... DETAILS	1		PAFZZ
/ 6-94	58139-40081-1	97384	.ANGLE.....	1		PAFZZ
/ 6-95	58139-40081-2	97384	.ANGLE.....	1		PAFZZ
/ 6-96	58139-40020	97384	.CIRCUIT CARD ASSEMBLY, FRONT PANEL INTERFACE SEE FIGURE 12 FOR DETAILS	1		PAFFD
/ 6-97	MS51957-26	96906	.SCREW, MACHINE (AP).....	1		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP).....	1		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP).....	3		PAFZZ
/ 6-98	MS51957-35	96906	.SCREW, MACHINE (AP).....	5		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP).....	2		PAFZZ
/ 6-99	070109-3-308	97384	.SPACER.....	5		MFFZZ
/ 6-100	MS25281-R5	96906	.CLAMP, LOOP.....	1		PAFZZ
/ 6-101	MS25281-R3	96906	.CLAMP, LOOP.....	1		PAFZZ
/ 6-102	MS51957-28	96906	.SCREW, MACHINE (AP).....	2		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP).....	2		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP).....	2		PAFZZ
/ 5-103	MS25281-R3	96906	.CLAMP, LOOP.....	1		PAFZZ
/ 5-104	MS25281-R6	96906	.CLAMP, LOOP.....	1		PAFZZ
/ 5-105	MS51957-30	96906	.SCREW, MACHINE (AP).....	2		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP).....	2		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP).....	2		PAFZZ
/ 5-106	58139-90009-4	97384	.CABLE ASSEMBLY (SOURCE CONTROLLED. BY PART NO 58139-90009-4 MFD BY 98291)	1		PAFZZ
/ 5-107	58139-40060	97384	.MICROWAVE ASSEMBLY SEE FIG 9 FOR.. DETAILS	1		AFFFF
/ 5-108	MS51957-28	96906	.SCREW, MACHINE (AP).....	7		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP).....	7		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP).....	7		PAFZZ
/ 5-109	MS25281-R3	96906	.CLAMP, LOOP.....	1		PAFZZ
/ 5-110	MS51957-30	96906	.SCREW, MACHINE (AP).....	1		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP).....	1		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP).....	1		PAFZZ
/ 5-111	58139-40065	97384	.TERMINAL BOARD.....	1		PAFZZ
/ 5-112	MS51957-30	96906	.SCREW, MACHINE (AP).....	3		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP).....	3		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP).....	3		PAFZZ
/ 5-113	58139-90006	97384	.POWER SUPPLY, TRIPLE OUTPUT..... (SOURCE CONTROLLED FROM PART NUMBER PB3359 MFD BY 04942)	1		PAFZZ
/ 6-114	58139-90015	97384	.DIRECTIONAL DETECTOR (SOURCE..... CONTROLLED FROM PART NUMBER 40138-1 MFD BY 97384)	1		PAFZZ
/ 6-115	MS51957-34	96906	.SCREW, MACHINE (AP).....	2		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP).....	2		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP).....	2		PAFZZ
	MS35649-264	96906	.NUT, PLAIN (AP).....	2		PAFZZ
/ 6-116	58139-40008	97384	.BRACKET.....	1		MFFZZ

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
5/ 6-117	MS51957-15	96906	.SCREW, MACHINE (AP).....	2		PAFZZ
	MS15795-803	96906	.WASHER, FLAT (AP).....	2		PAFZZ
	MS35338-135	96906	.WASHER, LOCK (AP).....	2		PAFZZ
/ 2-118	MS35489-11	96906	.GROMMET, RUBBER.....	1		PAFZZ
/ 2-119	58139-40003	97384	.CHASSIS.....	1		AFFFF
	58139-40066-2	97384	.HOUSING, ELECTRICAL CONNECTOR.....	7		PAFZZ
	58139-40066-1	97384	.HOUSING, ELECTRICAL CONNECTOR.....	1		PAFZZ
	58139-40066-3	97384	.HOUSING, ELECTRICAL CONNECTOR.....	1		PAFZZ
	58139-40066-4	97384	..HOUSING, ELECTRICAL CONNECTOR....	1		PAFZZ
	58139-40066-5	97384	.HOUSING, ELECTRICAL CONNECTOR.....	1		PAFZZ
	87179-1	00779	.KEY INSERT.....	29		PAFZZ
	87165-1	00779	.CONTACT.....	91		PAFZZ
	58139-40005-1	97384	.MARKER, CABLE.....	1		MFFZZ
	58139-40005-2	97384	.MARKER, CABLE.....	1		MFFZZ
	58139-40005-3	97384	.MARKER, CABLE.....	1		MFFZZ
	58139-40005-4	97384	.MARKER, CABLE.....	1		MFFZZ
	58139-40005-6	97384	.MARKER, CABLE.....	1		MFFZZ
	58139-40005-7	97384	.MARKER, CABLE.....	1		MFFZZ
	58139-40005-8	97384	.MARKER, CABLE.....	1		MFFZZ
	58139-40005-9	97384	.MARKER, CABLE.....	1		MFFZZ
	58139-40005-10	97384	.MARKER, CABLE.....	1		MFFZZ
	58139-40005-12	97384	.MARKER, CABLE.....	1		MFFZZ
	58139-40005-13	97384	.MARKER, CABLE.....	1		MFFZZ
	PLTIM-CP	06383	.CABLE TIE.....	100		
	FS156	06383	.CABLE STRIP.....	2		

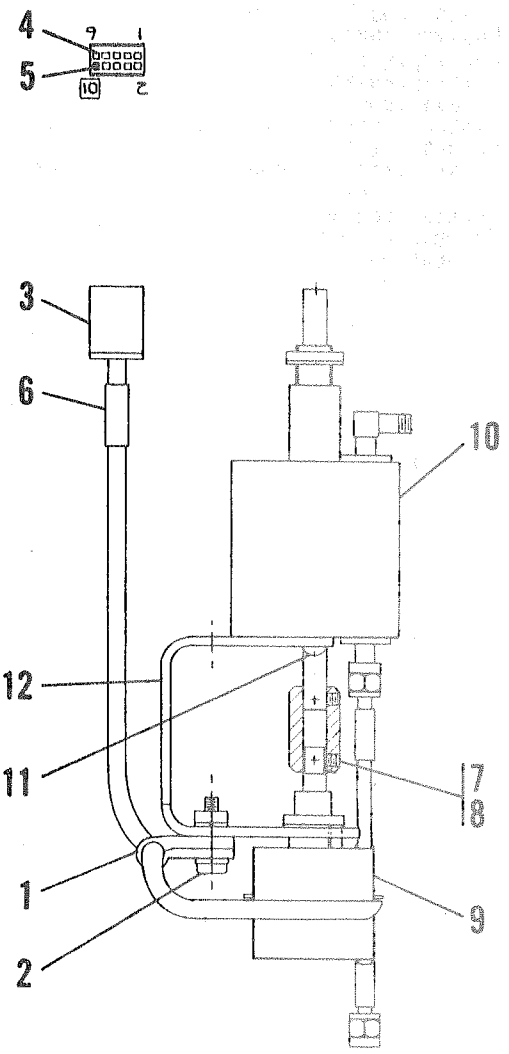


Figure 6. Attenuator Assembly

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
6 -	58139-40055	97384	ATTENUATOR ASSEMBLY SEE FIG 5 FOR.. NHA	REF		AFFFF
-1	MS25281-R4	96906	.CLAMP, LOOP.....	1		PAFZZ
-2	MS51957-30	96906	.SCREW, MACHINE (AP).....	1		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP).....	1		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP).....	1		PAFZZ
	MS35649-264	96906	.NUT, PLAIN (AP).....	1		PAFZZ
-3	58139-40066-2	97384	.HOUSING, CONNECTOR.....	1		PAFZZ
-4	87165-1	00779	.CONTACT, SPRING.....	9		PAFZZ
-5	87179-1	00779	.KEY INSERT.....	1		PAFZZ
-6	58139-40055-1	97384	.MARKER, CABLE.....	1		MFFZZ
-7	58139-40044	97384	.COUPLING.....	1		PAFZZ
-8	MS51963-20	96906	.SETSCREW (AP).....	4		PAFZZ
-9	M3786-4-3345	81349	.SWITCH.....	1		PAFZZ
-10	58139-90031	97384	.STEP ATTENUATOR AAI INTERFACE CONT DWG	1		PAFZZ
-11	MS51957-27	96906	.SCREW, MACHINE (AP).....	1		PAFZZ
	MS15795-805	96905	.WASHER, FLAT (AP).....	2		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP).....	2		PAFZZ
-12	58139-40009	97384	.BRACKET.....	1		XBFZZ

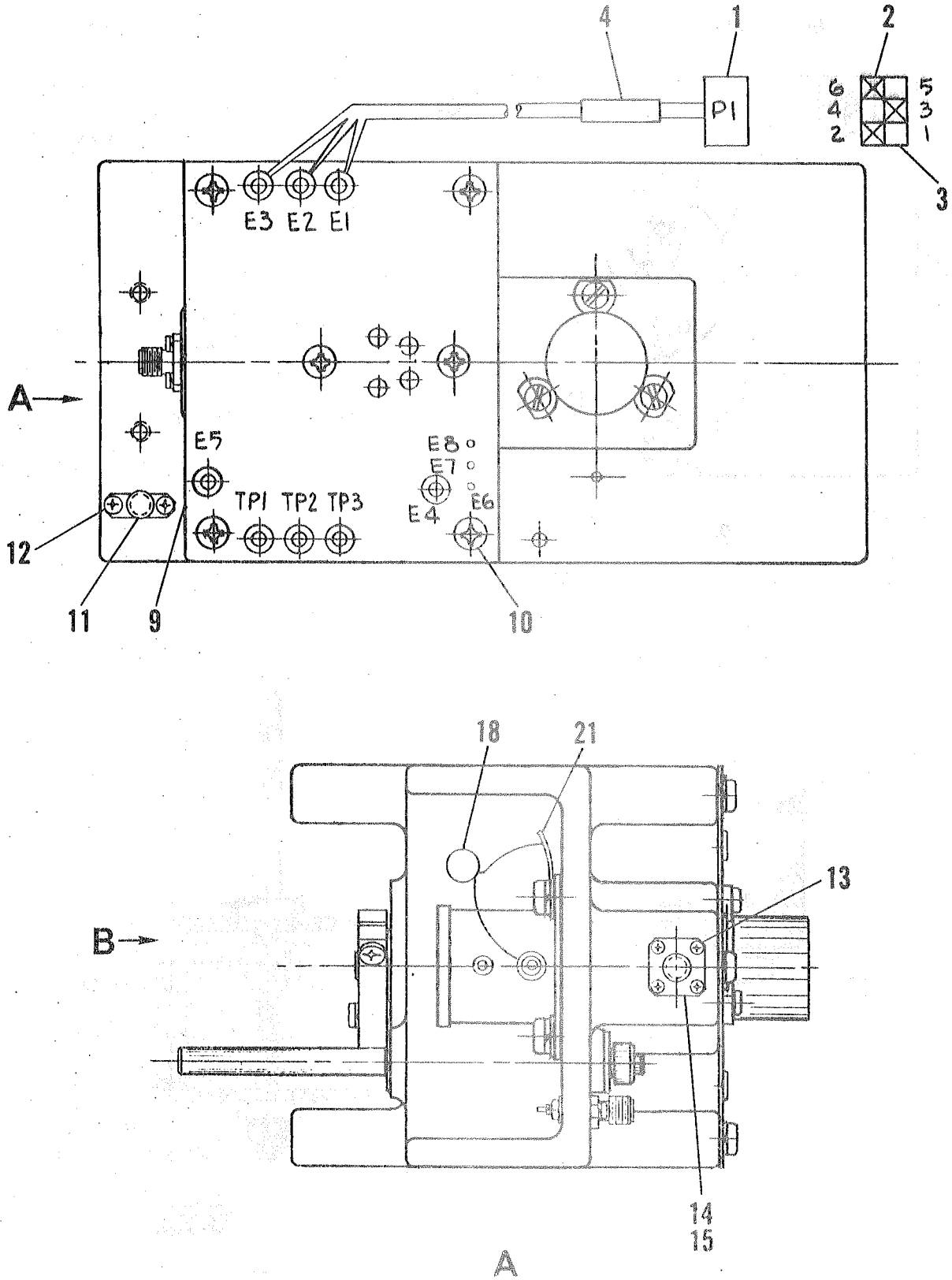
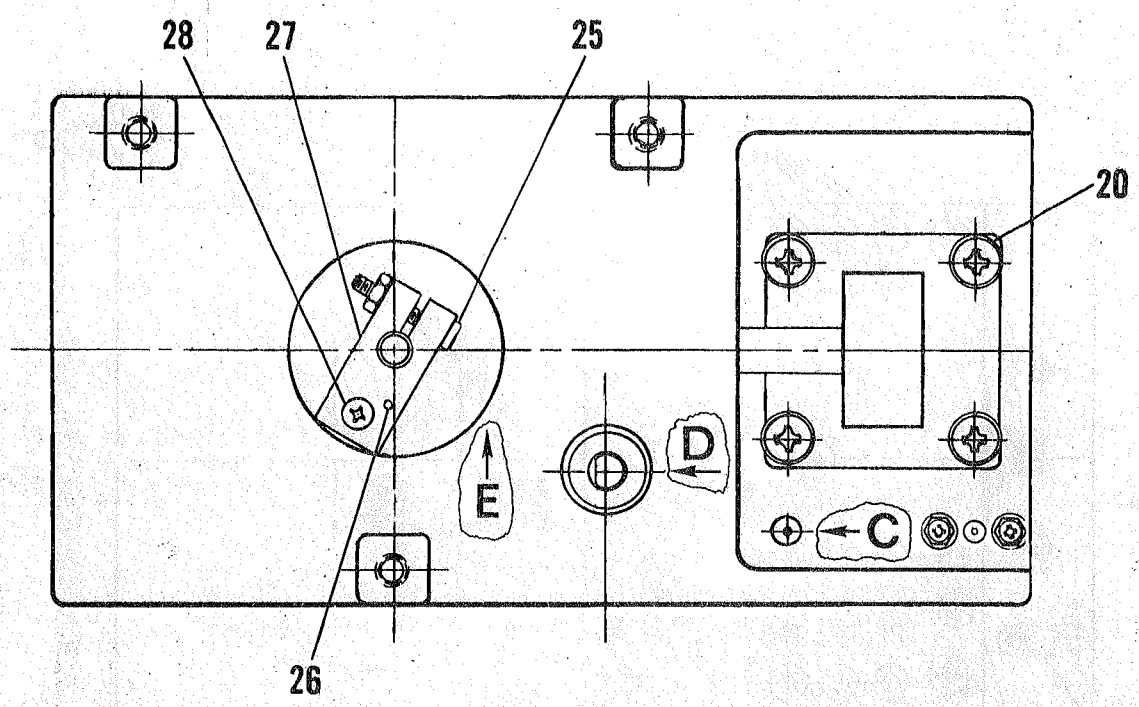
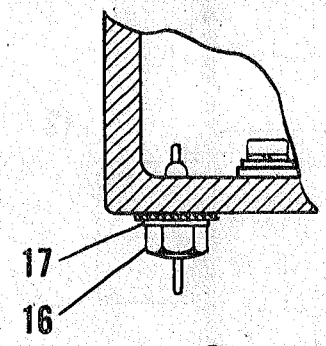


Figure 7. RF Oscillator Assembly (Sheet 1 of 3)



B



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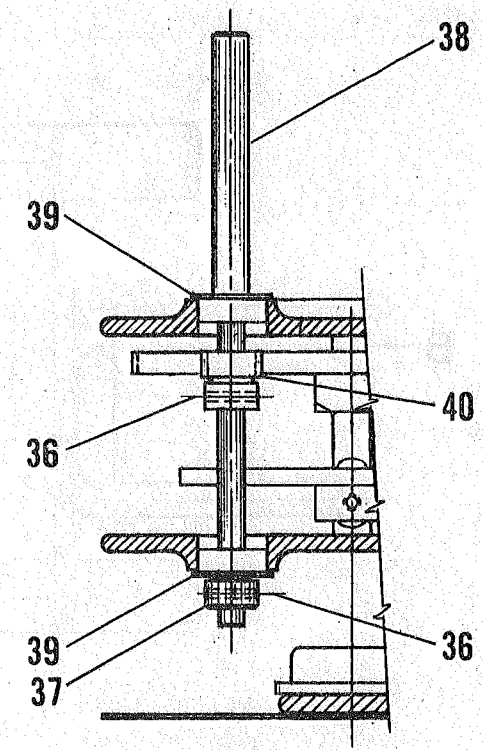

D

Figure 7. RF Oscillator Assembly (Sheet 2 of 3)

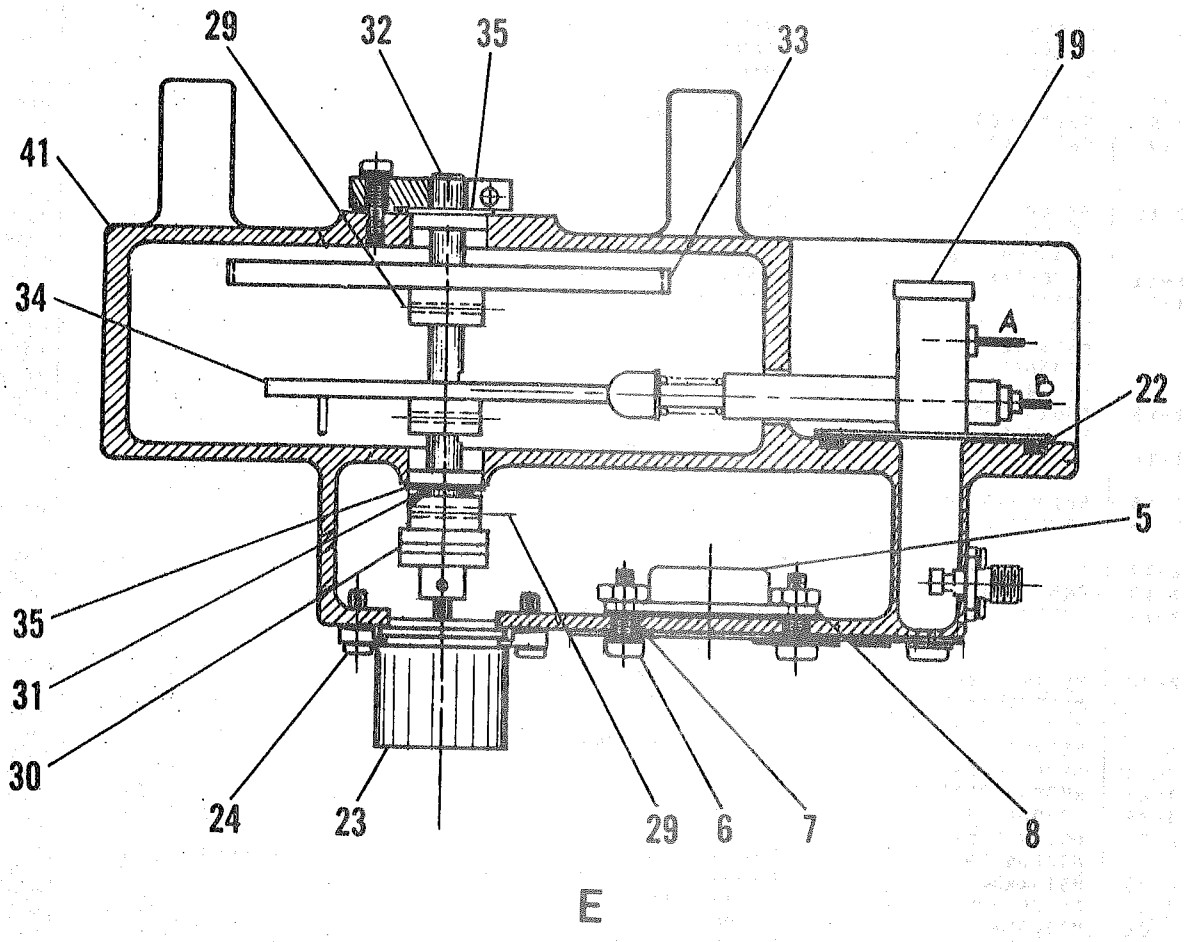

Figure 7. RF Oscillator Assembly (Sheet 3 of 3)

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
7 -	58139-40030	97384	RF OSCILLATOR ASSEMBLY SEE FIG 5... FOR NHA	REF		AFFFF
/ 1-1	58139-40066-1	97384	.HOUSING	1		PAFZZ
/ 1-2	87179-1	00779	.KEY INSERT	3		PAFZZ
/ 1-3	87165-1	00779	.CONTACT, SPRING	3		PAFZZ
/ 1-4	58139-40030-1	97384	.MARKER, CABLE	1		MFFZZ
/ 3-5	58139-90005-6	97384	.MICROCIRCUIT (SOURCE CONTROLLED... FROM PART NUMBER UA78GKM/QB MFG BY 07263)	1		PAFZZ
/ 3-6	MS51957-17	96906	.SCREW, MACHINE (AP)	2		PAFZZ
	MS35649-244	96906	.NUT, PLAIN (AP)	2		PAFZZ
	MS35338-135	96906	.WASHER, LOCK (AP)	2		PAFZZ
/ 3-7	SP-2	95987	.BUSHING	2		PAFZZ
/ 3-8	58139-40029	97384	.INSULATOR	1		MFFZZ
/ 1-9	58139-40050	97384	.CIRCUIT CARD ASSEMBLY, GUN... OSCILLATOR REGULATOR SEE FIGURE 13 FOR DETAILS	1		PAFFF
/ 1-10	MS51957-30	96906	.SCREW, MACHINE (AP)	4		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP)	4		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP)	4		PAFZZ
/ 1-11	M39012/60-3002	96906	.CONNECTOR, PLUG	1		PAFZZ
/ 1-12	MS51957-7	96906	.SCREW, MACHINE (AP)	2		PAFZZ
	MS15795-802	96906	.WASHER, FLAT (AP)	2		PAFZZ
	MS35338-134	96906	.WASHER, LOCK (AP)	2		PAFZZ
	MS35649-224	96906	.NUT, PLAIN (AP)	2		PAFZZ
	58139-40059	97384	.CONNECTOR ASSEMBLY J1	1		PAFZZ
/ 1-13	MS51957-2	96906	.SCREW, MACHINE (AP)	4		PAFZZ
	MS35338-134	96906	.WASHER, LOCK (AP)	4		PAFZZ
/ 1-14	2052-1201	16179	..CONNECTOR AAI SPEC CONT DWG... 58139-90025	1		PAFZZ
/ 1-15	58139-40059-2	97384	..SLEEVE	1		XA---
/ 2-16	859647-1	00779	.FILTER AAI SPEC CONT DWG... 58139-90029	1		PAFZZ
/ 2-17	MS15795-808	96906	.WASHER, FLAT (AP)	1		PAFZZ
/ 1-18	CK60AW102M	81349	.CAP, FXD, CERAMIC	1		PAFZZ
/ 3-19	58139-90001	97384	.SOLID STATE OSCILLATOR (SOURCE... CONTROLLED FROM PART NUMBER C-2120V MFD BY 33173)	1		PAFZZ
/ 2-20	MS51957-28	96906	.SCREW, MACHINE (AP)	4		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP)	4		PAFZZ
	MS35338-136	96906	.WASHER, LOCK (AP)	8		PAFZZ
/ 1-21	MS77070-2	96906	.TERMINAL, LUG	1		PAFZZ
/ 3-22	MS90064-13	96906	.SEAL	1		PAFZZ
/ 3-23	RR0900A2H7G502	81349	.RESISTOR, VARIABLE	1		PAFZZ
/ 3-24	106064-337	06773	.SYNCLAMP	3		PAFZZ
/ 2-25	MS51957-19	96906	.SCREW, MACHINE	1		PAFZZ
	MS21042L04	96906	.NUT, SELF-LKG	1		PAFZZ
/ 2-26	MS171436	96906	.PIN, SPRING	1		PAFZZ
/ 2-27	58139-40033	97384	.BRAKE	1		PAFZZ
/ 2-28	MS51957-17	96906	.SCREW, MACHINE (AP)	1		PAFZZ
	MS15795-803	96906	.WASHER, FLAT (AP)	2		PAFZZ
	MS35338-135	96906	.WASHER, LOCK (AP)	1		PAFZZ
/ 3-29	MS171436	96906	.PIN, SPRING	2		PAFZZ
/ 3-30	CO3-110	29440	.COUPLING	1		PAFZZ
/ 3-31	SS2-31	29440	.SPACER	1		PAFZZ
/ 3-32	58139-40071	97384	.SHAFT	1		PAFZZ
/ 3-33	P64A28-192	29440	.GEAR, SPUR	1		AFFFF
/ 3-34	58139-40036	97384	.CAM	2		PAFZZ
/ 3-35	B2-11-S	29440	.BEARING, BALL	2		PAFZZ
/ 2-36	MS171434	96906	.PIN, SPRING	1		PAFZZ
/ 2-37	CS-5	29440	.COLLAR	1		PAFZZ
/ 2-38	58139-40034	97384	.SHAFT	2		PAFZZ
/ 2-39	B2-6-S	29440	.BEARING, BALL	1		PAFZZ
/ 2-40	P64A21-24	29440	.GEAR, SPUR	1		XBFFF
/ 3-41	58139-40032	97384	.HOUSING, MACHINED			

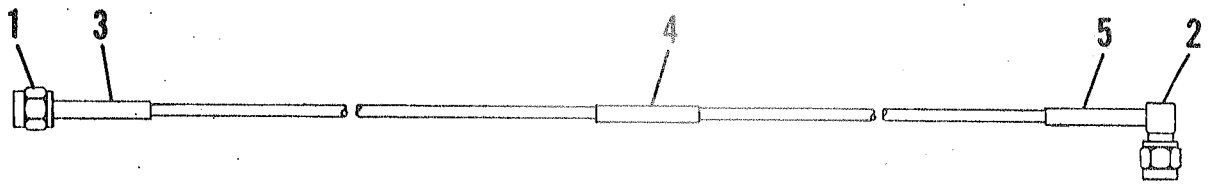

Figure 8. Cable Assembly

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
8 -	58139-40025-1	97384	CABLE ASSEMBLY SEE FIG 5 FOR NHA...	REF		PAFZZ
-1	M39012/55-3026	81349	.CONNECTOR, PLUG.....	1		XA---
-2	M39012/56-3026	81349	.CONNECTOR, PLUG.....	1		XA---
-3	58139-40025-3	97384	.MARKER, CABLE.....	1		MFFZZ
-4	58139-40025-4	97384	.MARKER, CABLE.....	1		MFFZZ
-5	58139-40025-5	97384	.MARKER, CABLE.....	1		MFFZZ

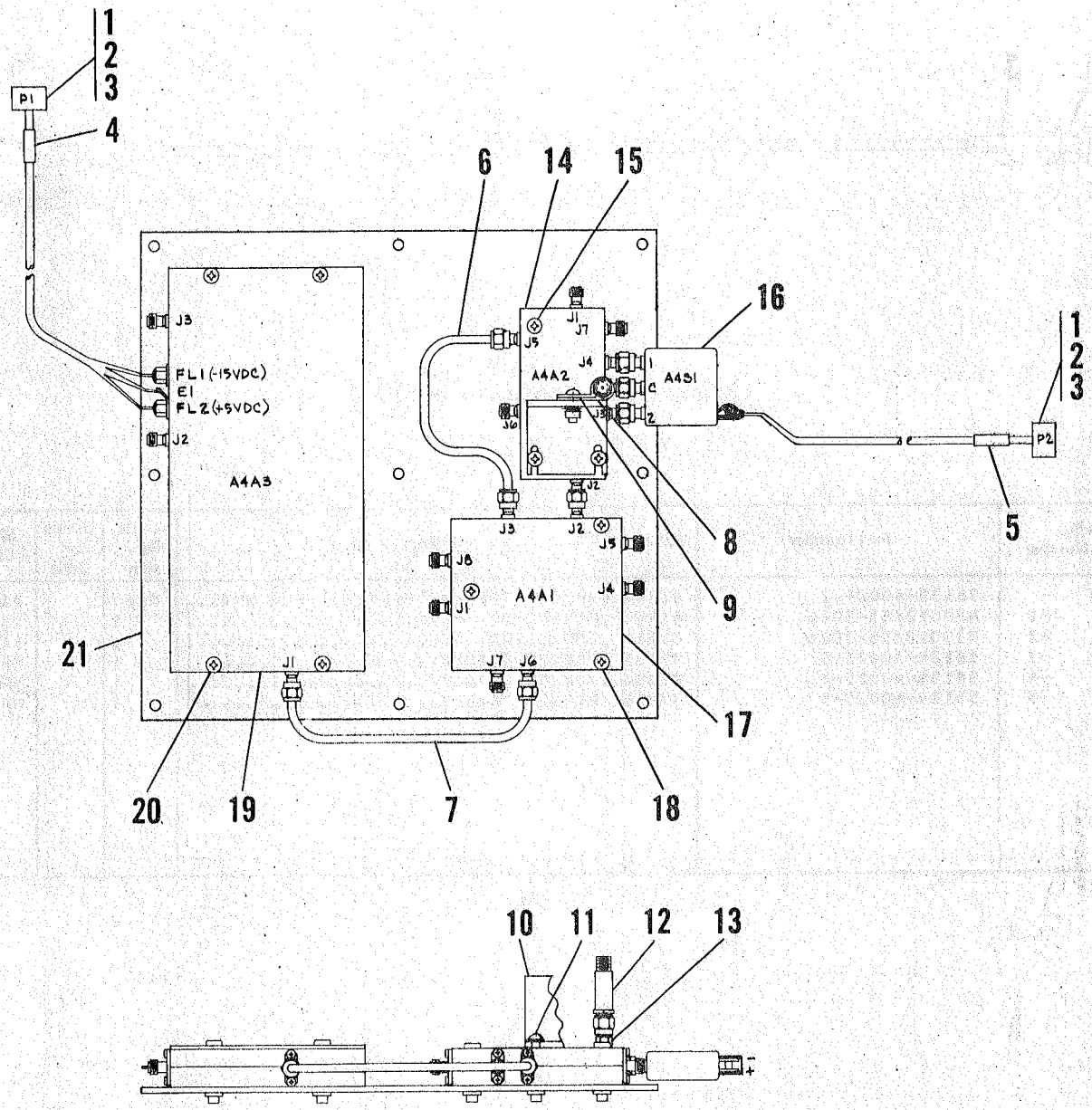

Figure 9. Microwave Assembly

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
9 -	58139-40060	97384	MICROWAVE ASSEMBLY SEE FIG 5 FOR... NHA	REF		AFFFF
-1	58139-40066-1	97384	.HOUSING.....	1		PAFZZ
-2	87165-1	00779	.CONTACT, SPRING.....	8		PAFZZ
-3	87179-1	00779	.KEY INSERT.....	4		PAFZZ
-4	58139-40060-1	97384	.MARKER, CABLE.....	1		MFFZZ
-5	58139-40060-2	97384	.MARKER, CABLE.....	1		MFFZZ
-6	58139-90009-2	97384	.CABLE ASSEMBLY (SOURCE CONTROLLED. FROM PART NUMBER 58139-90009-2 MFD BY 98291)	1		PAFZZ
-7	58139-90009-1	97384	.CABLE ASSEMBLY (SOURCE CONTROLLED. FROM PART NUMBER 58139-90009-1 MFD BY 98291)	1		PAFZZ
-8	MS25281-R5	96906	.CLAMP, LOOP.....	1		PAFZZ
-9	MS51957-46	96906	.SCREW, MACHINE (AP).....	1		PAFZZ
	MS15795-807	96906	.WASHER, FLAT (AP).....	1		PAFZZ
	MS35338-137	96906	.WASHER, LOCK (AP).....	1		PAFZZ
	MS35649-284	96906	.NUT (AP).....	1		PAFZZ
-10	58139-40074	97384	.BRACKET.....	1		XBFZZ
-11	MS51957-35	96906	.SCREW, MACHINE (AP).....	2		PAFZZ
	MS15795-805	96906	.WASHER, FLAT (AP).....	2		PAFZZ
-12	58139-90007	97384	.R F DETECTOR (SOURCE CONTROLLED... FROM PART NUMBER 58139-90007 MFD BY 96341)	1		PAFZZ
-13	58139-90016	97384	.RIGHT ANGLE ADAPTER (SOURCE..... CONTROLLED FROM PART NUMBER 58139-90016 MFD BY 16733)	1		PAFZZ
-14	58139-90013	97384	.COUPLER MODULE (SOURCE CONTROLLED. FROM PART NUMBER 40138-2 MFD BY 97384)	1		PAFZZ
-15	MS51957-34	96906	.SCREW, MACHINE (AP).....	3		PAFZZ
-16	58139-90003	97384	.COAXIAL SWITCH (SOURCE CONTROLLED. FROM PART NUMBER RSM-2-D MFD BY 54487)	1		PAFZZ
-17	58139-90012	97384	.MODULATOR MIXER (SOURCE CONTROLLED FROM PART NUMBER 40138-3 MFD BY 97384)	1		PAFZZ
-18	MS51957-34	96906	.SCREW, MACHINE (AP).....	3		PAFZZ
-19	58139-90014	97384	.VCO PRESCALER (SOURCE CONTROLLED.. FROM PART NUMBER 40138-4 MFD BY 97384)	1		PAFZZ
-20	MS51957-34	96906	.SCREW, MACHINE (AP).....	4		PAFZZ
-21	58139-40061	97384	.CHASSIS.....	1		XBFFF

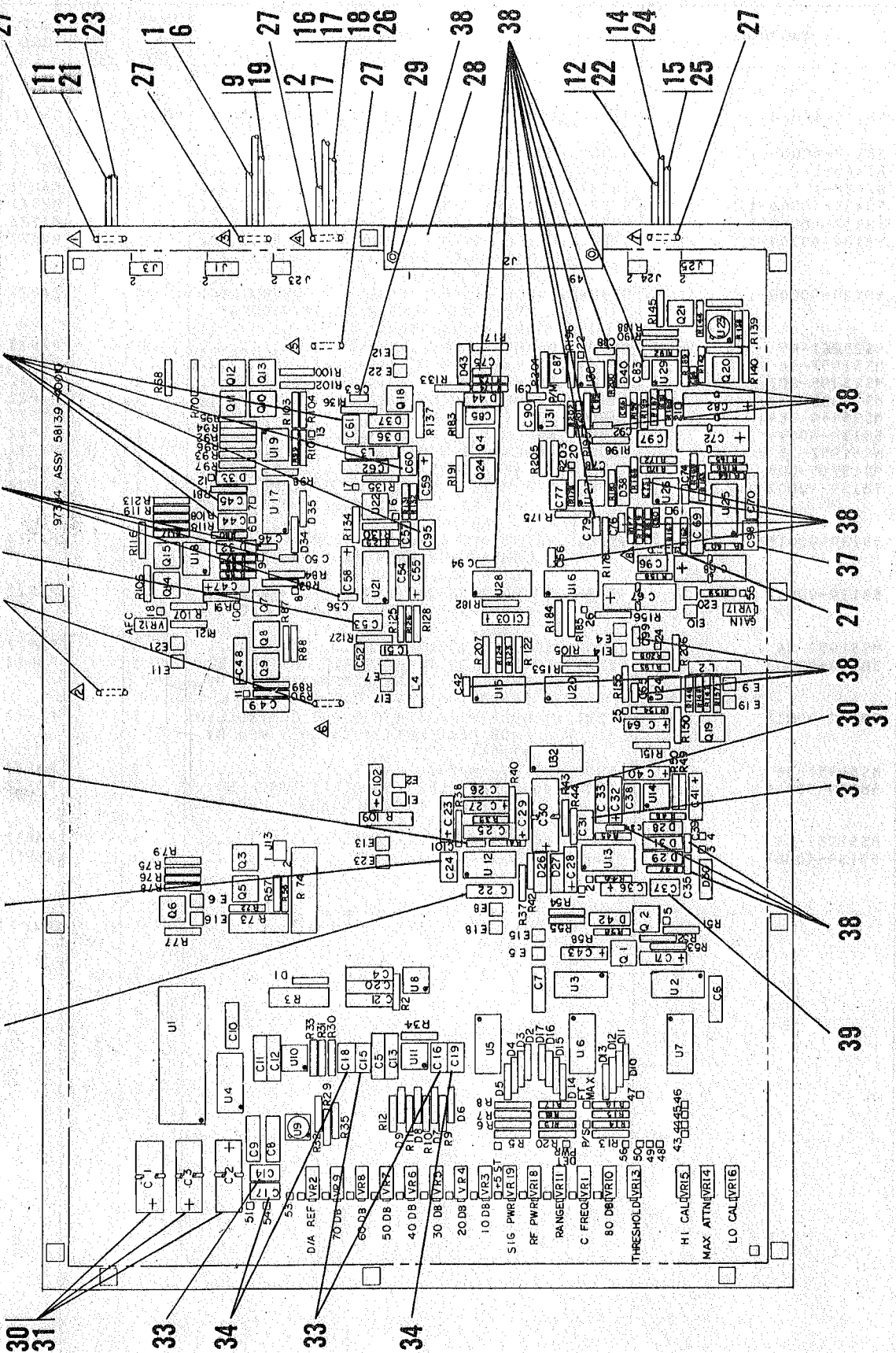

Figure 10. Circuit Card Assembly, Microwave Interface (Sheet 1 of 7)

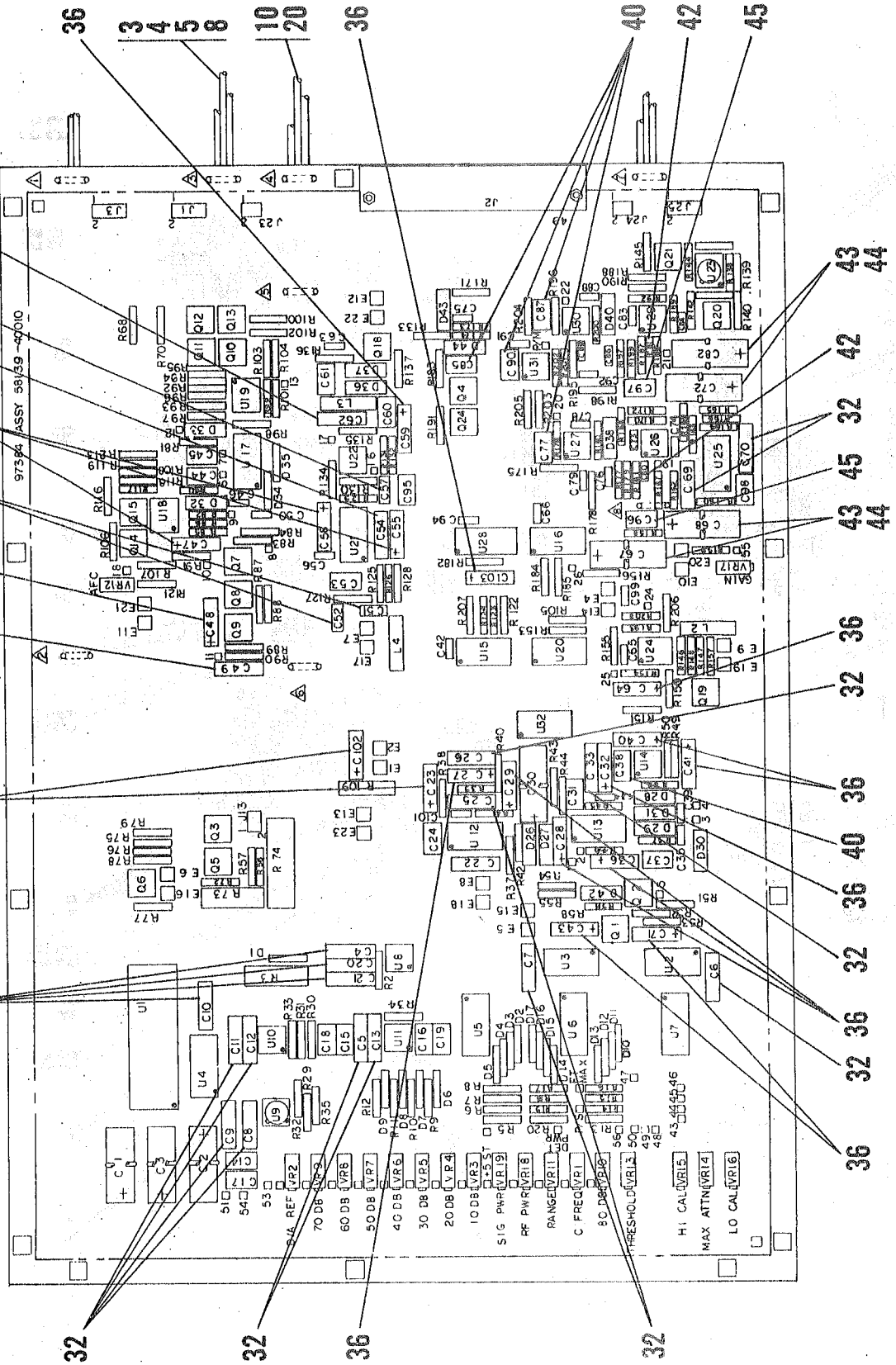

Figure 10. Circuit Card Assembly, Microwave Interface (Sheet 2 of 7)

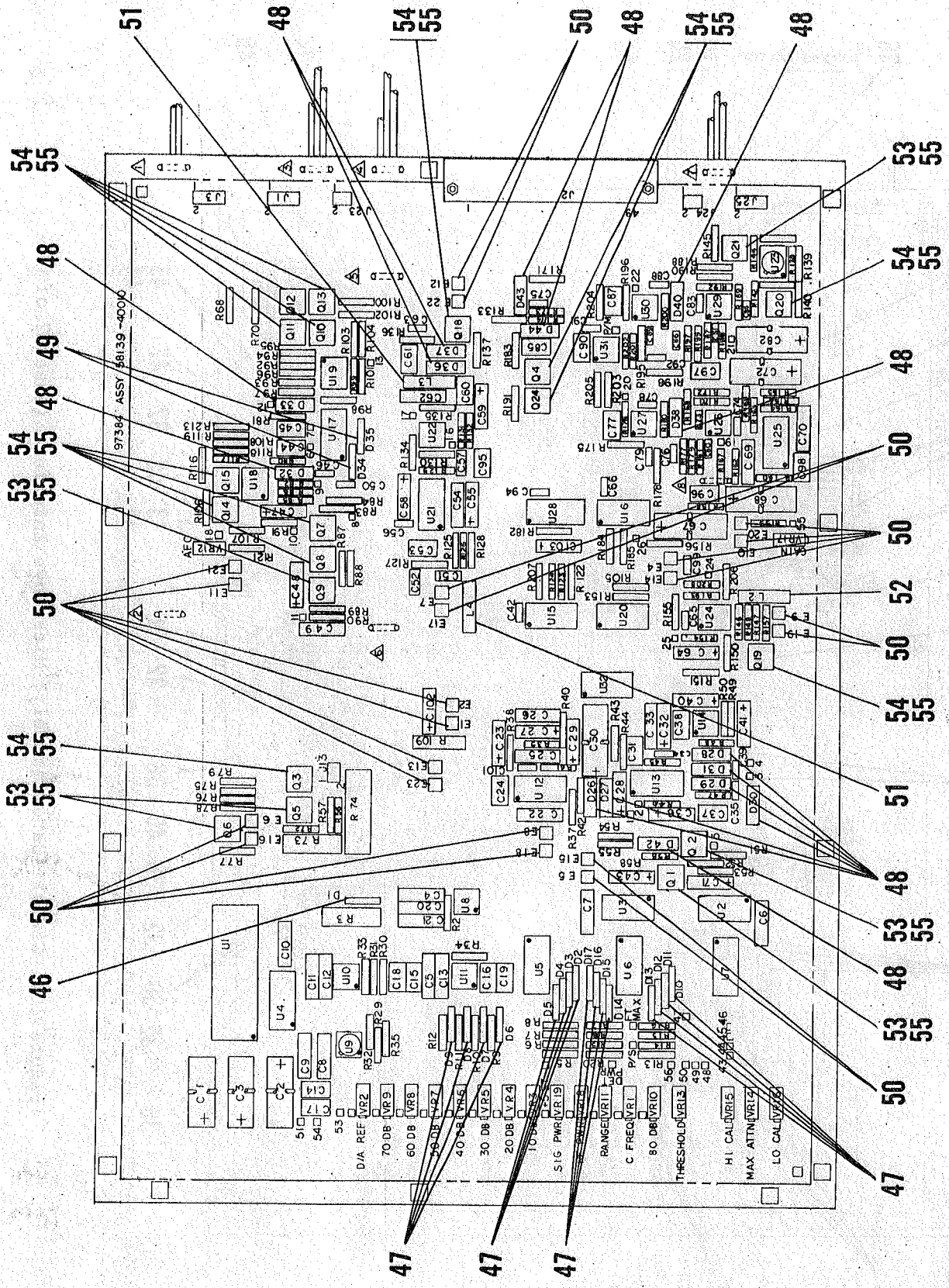

Figure 10. Circuit Card Assembly, Microwave Interface (Sheet 3 of 7)

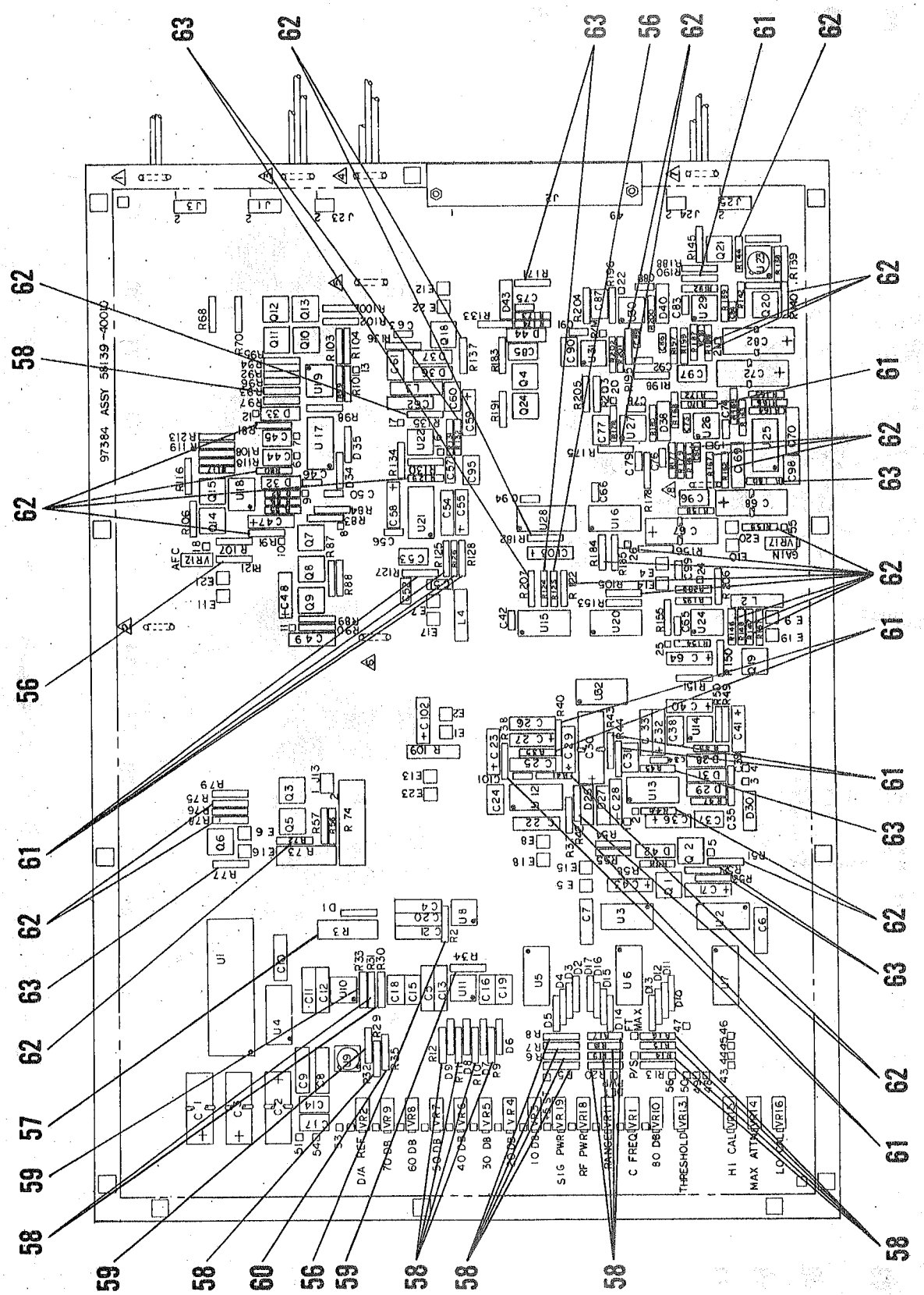

Figure 10. Circuit Card Assembly, Microwave Interface (Sheet 4 of 7)

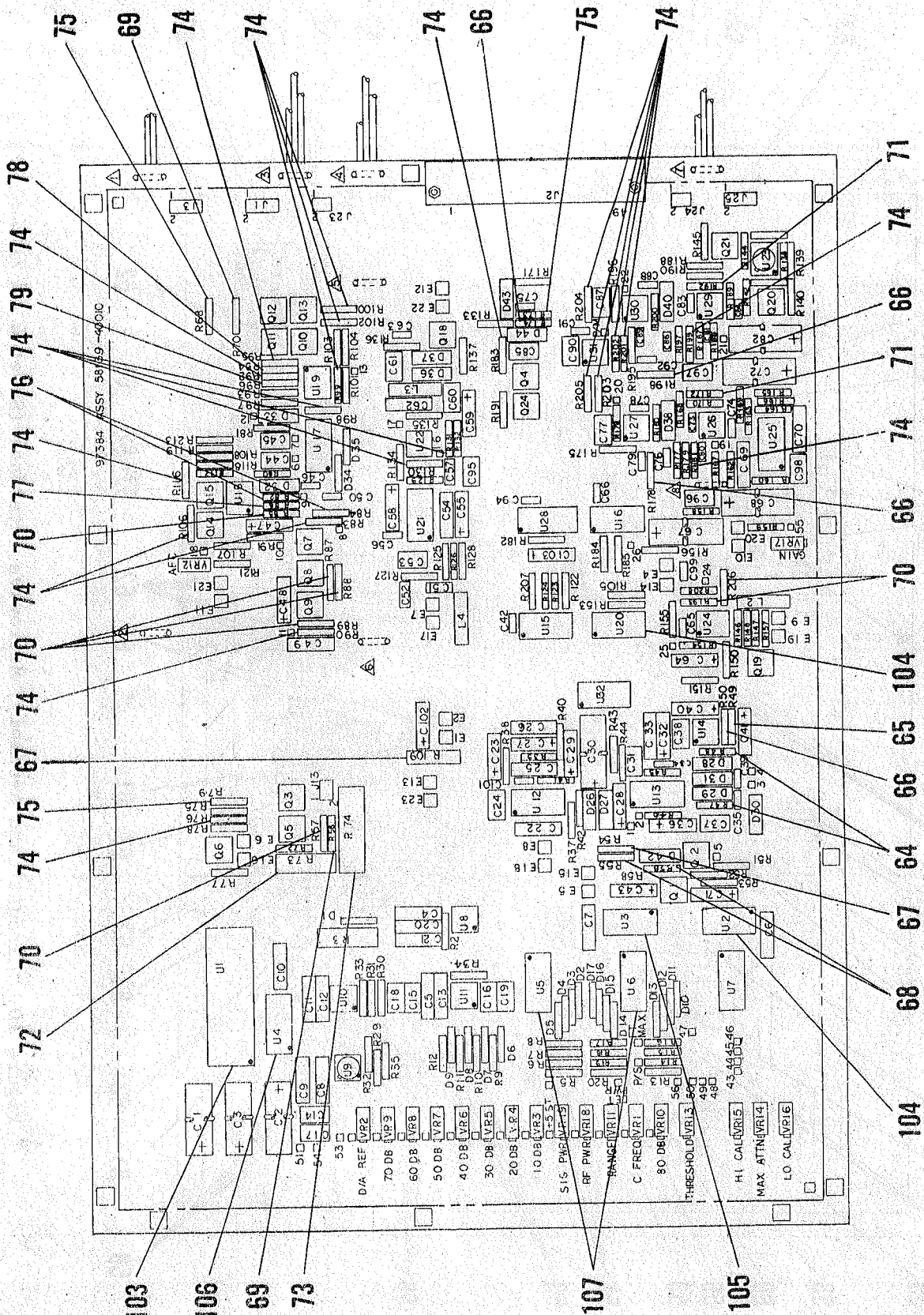

Figure 10. Circuit Card Assembly, Microwave Interface (Sheet 5 of 7)

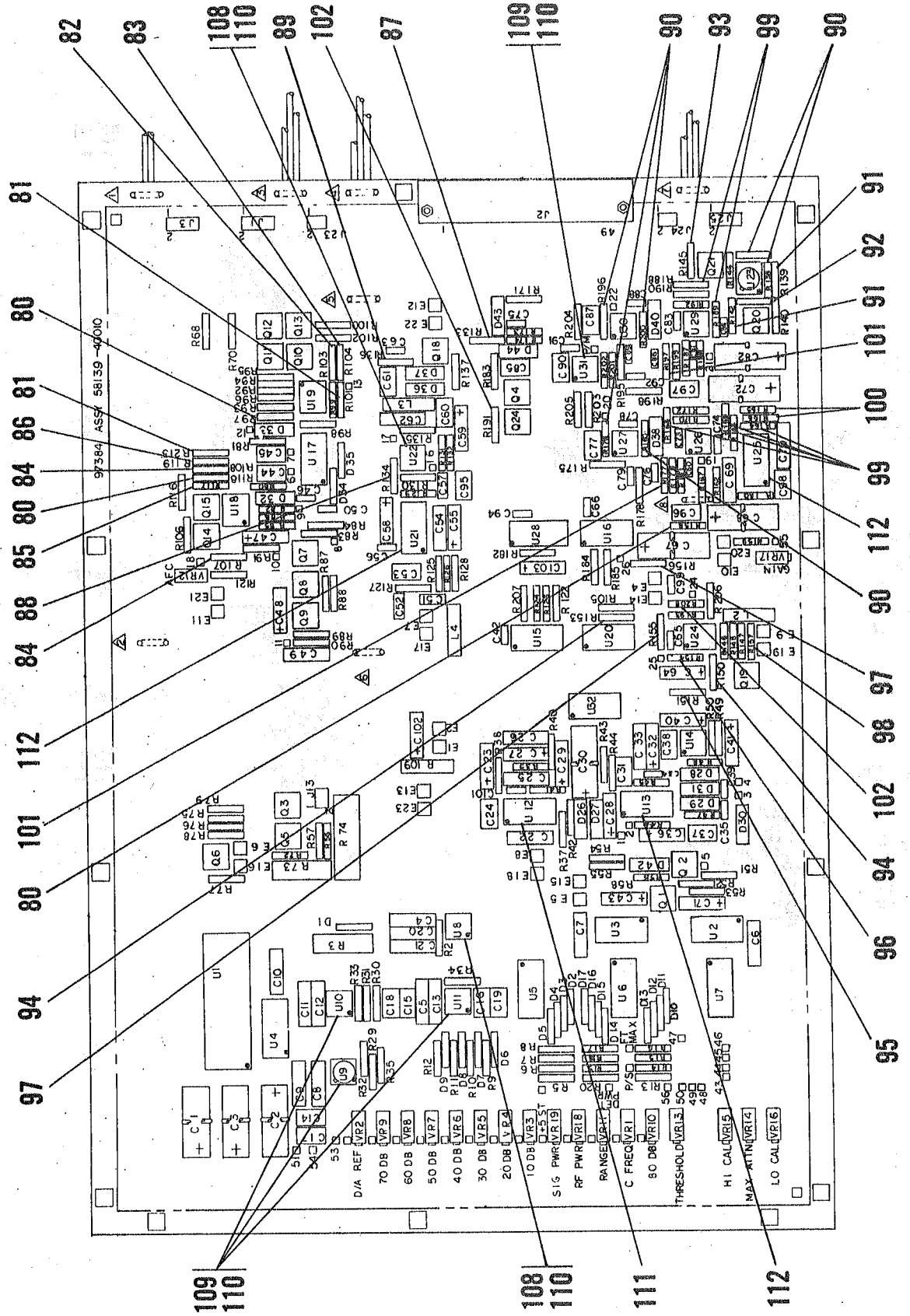

Figure 10. Circuit Card Assembly, Microwave Interface (Sheet 6 of 7)

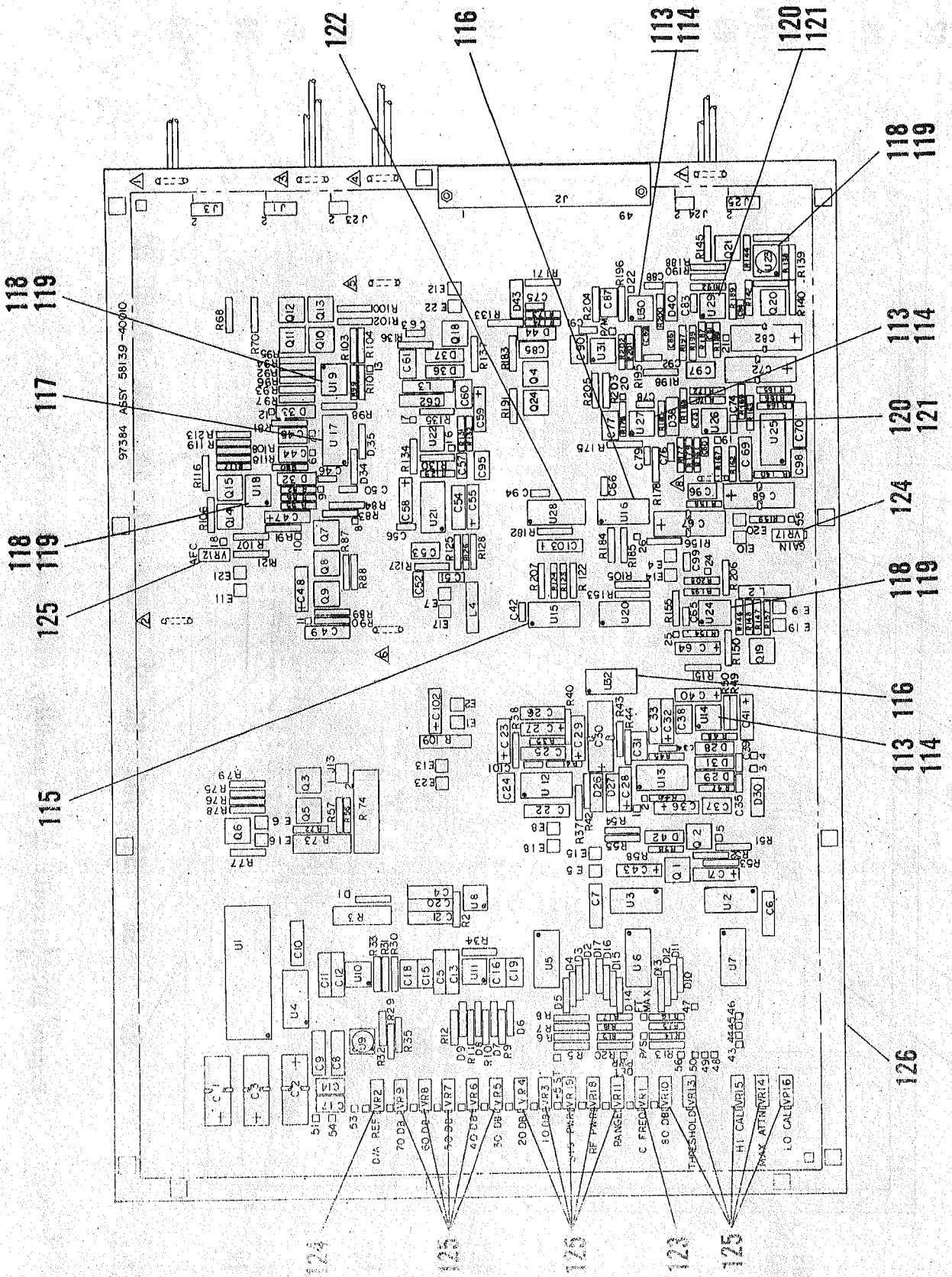

Figure 10. Circuit Card Assembly, Microwave Interface (Sheet 7 of 7)

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
10 -	58139-40010	97384	CIRCUIT CARD ASSEMBLY, MICROWAVE... INTERFACE SEE FIG 5 FOR NHA	REF		PAFFD
/ 1-1	58139-40053-1	97384	.CABLE ASSEMBLY.....	1		PAFZZ
/ 1-2	58139-40053-2	97384	.CABLE ASSEMBLY.....	1		PAFZZ
/ 2-3	58139-40053-3	97384	.CABLE ASSEMBLY.....	1		PAFZZ
/ 2-4	329413	00779	..SPLICE USED ON -1, -2, AND -3.... ASSEMBLY	1		XA---
/ 2-5	M39012/56-3026	81349	..CONNECTOR, PLUG USED ON -1, -2,.. AND -3 ASSEMBLY	1		XA---
/ 1-6	58139-40053-11	97384	..MARKER, CABLE USED ON -1 ASSEMBLY	1		XA---
/ 1-7	58139-40053-12	97384	..MARKER, CABLE USED ON -2 ASSEMBLY	1		XA---
/ 2-8	58139-40053-13	97384	..MARKER, CABLE USED ON -3 ASSEMBLY	1		XA---
/ 1-9	58139-40054-1	97384	.CABLE ASSEMBLY.....	1		PAFZZ
/ 2-10	58139-40054-2	97384	.CABLE ASSEMBLY.....	1		PAFZZ
/ 1-11	58139-40054-3	97384	.CABLE ASSEMBLY.....	1		PAFZZ
/ 1-12	58139-40054-4	97384	.CABLE ASSEMBLY.....	1		PAFZZ
/ 1-13	58139-40054-5	97384	.CABLE ASSEMBLY.....	1		PAFZZ
/ 1-14	58139-40054-6	97384	.CABLE ASSEMBLY.....	1		PAFZZ
/ 1-15	58139-40054-7	97384	.CABLE ASSEMBLY.....	1		PAFZZ
/ 1-16	58139-40054-8	97384	.CABLE ASSEMBLY.....	1		PAFZZ
/ 1-17	329413	00779	..SPLICE USED ON -1 THROUGH -8..... ASSEMBLY	1		XA---
/ 1-18	M39012/55-3026	81349	..CONNECTOR, PLUG USED ON -1..... THROUGH -8 ASSEMBLY P2 THROUGH P5, P7 THROUGH P9, P10	1		XA---
/ 1-19	58139-40054-11	97384	..MARKER, CABLE USED ON -1 ASSEMBLY	1		XA---
/ 2-20	58139-40054-12	97384	..MARKER, CABLE USED ON -2 ASSEMBLY	1		XA---
/ 1-21	58139-40054-13	97384	..MARKER, CABLE USED ON -3 ASSEMBLY	1		XA---
/ 1-22	58139-40054-14	97384	..MARKER, CABLE USED ON -4 ASSEMBLY	1		XA---
/ 1-23	58139-40054-15	97384	..MARKER, CABLE USED ON -5 ASSEMBLY	1		XA---
/ 1-24	58139-40054-16	97384	..MARKER, CABLE USED ON -6 ASSEMBLY	1		XA---
/ 1-25	58139-40054-17	97384	..MARKER, CABLE USED ON -7 ASSEMBLY	1		XA---
/ 1-26	58139-40054-18	97384	..MARKER, CABLE USED ON -8 ASSEMBLY	1		XA---
/ 1-27	2829-75-2	98159	.STRAP.....	8		PAFZZ
/ 1-28	58139-90019	97384	.HEADER, CONNECTOR (SOURCE..... CONTROLLED FROM PART NO 65823-093 MFD BY 22526)	1		PAFZZ
/ 1-29	MS51957-6	96906	.SCREW, MACHINE (AP).....	2		PAFZZ
	MS35649-224	96906	.NUT, PLAIN (AP).....	2		PAFZZ
/ 1-30	M39003/01-2614	81349	.CAPACITOR.....	4		PAFZZ
/ 1-31	2829-75-2	98159	.STRAP.....	4		PAFZZ
/ 2-32	CK63AW103M	81349	.CAPACITOR.....	20		PAFZZ
/ 1-33	CMR05F151JODP	81349	.CAPACITOR.....	3		PAFZZ
/ 1-34	CMR05C180JODP	81349	.CAPACITOR.....	3		PAFZZ
/ 1-35	M39003/01-2560	81349	.CAPACITOR.....	1		PAFZZ
/ 2-36	M39003/01-2596	81349	.CAPACITOR.....	18		PAFZZ
/ 1-37	CMR05E300JODP	81349	.CAPACITOR.....	3		PAFZZ
/ 1-38	M39014/02-1310	81349	.CAPACITOR.....	26		PAFZZ
/ 1-39	CMR05F331JODP	81349	.CAPACITOR.....	1		PAFZZ
/ 2-40	CMR05F101JODP	81349	.CAPACITOR.....	5		PAFZZ
/ 1-41	CMR05F161JODP	81349	.CAPACITOR.....	6		PAFZZ
/ 2-42	CK60AW102M	81349	.CAPACITOR.....	5		PAFZZ
/ 2-43	M39003/01-2546	81349	.CAPACITOR.....	4		PAFZZ
/ 2-44	2829-75-2	98159	.STRAP.....	4		PAFZZ
/ 2-45	CMR05F391JODP	81349	.CAPACITOR.....	2		PAFZZ
/ 3-46	JANTX1N746A	81349	.SEMICONDUCTOR DEVICE.....	1		PAFZZ
/ 3-47	JAN1N458	81349	.SEMICONDUCTOR DEVICE.....	16		PAFZZ
/ 3-48	JANTX1N4150-1	81349	.SEMICONDUCTOR DEVICE.....	15		PAFZZ
/ 3-49	JANTX1N750A	81349	.SEMICONDUCTOR DEVICE.....	2		PAFZZ
/ 3-50	SE16XC01	81349	.TERMINAL.....	22		PAFZZ
/ 3-51	MS75089-17	96906	.COIL, RF.....	2		PAFZZ
/ 3-52	MS75089-35	96906	.COIL, RF.....	1		PAFZZ
/ 3-53	JANTX2N2907A	81349	.TRANSISTOR.....	6		PAFZZ
/ 3-54	JANTX2N2222A	81349	.TRANSISTOR.....	14		PAFZZ
/ 3-55	7717-44-DAP	13103	.TRANSIPAD.....	20		PAFZZ
/ 4-56	RCR07G512JS	81349	.RESISTOR.....	3		PAFZZ
/ 4-57	RCR32G221JS	81349	.RESISTOR.....	1		PAFZZ
/ 4-58	RNC55J10038M	81349	.RESISTOR.....	20		PAFZZ

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
10/ 4-59	RNC55J4992BM	81349	.RESISTOR	3		PAFZZ
/ 4-60	RNC55J1500BM	81349	.RESISTOR	1		PAFZZ
/ 4-61	RCR07G202JS	81349	.RESISTOR	12		PAFZZ
/ 4-62	RCR07G102JS	81349	.RESISTOR	31		PAFZZ
/ 4-63	RCR07G101JS	81349	.RESISTOR	9		PAFZZ
/ 5-64	RCR07G685JS	81349	.RESISTOR	2		PAFZZ
/ 5-65	RCR07G625JS	81349	.RESISTOR	1		PAFZZ
/ 5-66	RCR07G155JS	81349	.RESISTOR	4		PAFZZ
/ 5-67	RCR07G621JS	81349	.RESISTOR	2		PAFZZ
/ 5-68	RCR07G391JS	81349	.RESISTOR	2		PAFZZ
/ 5-69	RCR07G303JS	81349	.RESISTOR	2		PAFZZ
/ 5-70	RCR07G104JS	81349	.RESISTOR	7		PAFZZ
/ 5-71	RCR07G203JS	81349	.RESISTOR	2		PAFZZ
/ 5-72	RCR32G621JS	81349	.RESISTOR	1		PAFZZ
/ 5-73	RCR42G300JS	81349	.RESISTOR	1		PAFZZ
/ 5-74	RCR07G103JS	81349	.RESISTOR	21		PAFZZ
/ 5-75	RCR07G153JS	81349	.RESISTOR	3		PAFZZ
/ 5-76	RCR07G334JS	81349	.RESISTOR	2		PAFZZ
/ 5-77	RCR07G433JS	81349	.RESISTOR	1		PAFZZ
/ 5-78	RNC55J4642FM	81349	.RESISTOR	1		PAFZZ
/ 5-79	RNC55J1873FM	81349	.RESISTOR	1		PAFZZ
/ 6-80	RNC55J5112FM	81349	.RESISTOR	3		PAFZZ
/ 6-81	RNC55J1543FM	81349	.RESISTOR	2		PAFZZ
/ 6-82	RNC55J7502FM	81349	.RESISTOR	1		PAFZZ
/ 6-83	RNC55J5902FM	81349	.RESISTOR	1		PAFZZ
/ 6-84	RNC55J1272FM	81349	.RESISTOR	2		PAFZZ
/ 6-85	RNC55J2492FM	81349	.RESISTOR	1		PAFZZ
/ 6-86	RNC55J1213FM	81349	.RESISTOR	1		PAFZZ
/ 6-87	RCR07G273JS	81349	.RESISTOR	1		PAFZZ
/ 6-88	RCR07G331JS	81349	.RESISTOR	1		PAFZZ
/ 6-89	RCR07G243JS	81349	.RESISTOR	1		PAFZZ
/ 6-90	RCR07G912JS	81349	.RESISTOR	6		PAFZZ
/ 6-91	RCR07G622JS	81349	.RESISTOR	2		PAFZZ
/ 6-92	RCR07G111JS	81349	.RESISTOR	1		PAFZZ
/ 6-93	RCR07G181JS	81349	.RESISTOR	1		PAFZZ
/ 6-94	RNC55J1001FM	81349	.RESISTOR	2		PAFZZ
/ 6-95	RNC55J2491FM	81349	.RESISTOR	1		PAFZZ
/ 6-96	RNC55J3011FM	81349	.RESISTOR	1		PAFZZ
/ 6-97	RNC55J2051FM	81349	.RESISTOR	2		PAFZZ
/ 6-98	RNC55J51R1FM	81349	.RESISTOR	1		PAFZZ
/ 6-99	RCR07G100JS	81349	.RESISTOR	6		PAFZZ
/ 6-100	RCR07G510JS	81349	.RESISTOR	2		PAFZZ
/ 6-101	RCR07G105JS	81349	.RESISTOR	2		PAFZZ
/ 6-102	RCR07G302JS	81349	.RESISTOR	2		PAFZZ
/ 5-103	58139-90027-5	97384	.MICROCIRCUIT (SOURCE CONTROLLED... FROM PART NO ID8255A MFD BY 34649)	1		PAFZZ
/ 5-104	M38510/30001BCB	81349	.MICROCIRCUIT	2		PAFZZ
/ 5-105	M38510/31302BCB	81349	.MICROCIRCUIT	1		PAFZZ
/ 5-106	58139-90005-3	97384	.MICROCIRCUIT (SOURCE CONTROLLED... FROM PART NO AD561SD/883B MFD BY 12040)	1		PAFZZ
/ 5-107	58139-90005-4	97384	.MICROCIRCUIT (SOURCE CONTROLLED... FROM PART NO AM3705D/883B MFD BY 12040)	2		PAFZZ
/ 6-108	M38510/10304BGC	81349	.MICROCIRCUIT	2		PAFZZ
/ 6-109	M38510/10103BGC	81349	.MICROCIRCUIT	4		PAFZZ
/ 6-110	808-187	32559	.INSULATOR	6		PAFZZ
/ 6-111	58139-40083	97384	.MICROCIRCUIT	1		PAFZZ
/ 6-112	58139-90005-8	97384	.MICROCIRCUIT (SOURCE CONTROLLED... FROM PART NO 733DMQB MFD BY 34148)	3		PAFZZ
/ 7-113	M38510/10104BGC	81349	.MICROCIRCUIT	3		PAFZZ
/ 7-114	808-187	32559	.INSULATOR	3		PAFZZ
/ 7-115	M38510/30002BCB	81349	.MICROCIRCUIT	1		PAFZZ
/ 7-116	M38510/00801BCB	81349	.MICROCIRCUIT	2		PAFZZ
/ 7-117	M38510/30301BCB	81349	.MICROCIRCUIT	1		PAFZZ
/ 7-118	M38510/10102BIC	81349	.MICROCIRCUIT	4		PAFZZ

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
10/ 7-119	810-187	32559	.INSULATOR.....	4		PAFZZ
/ 7-120	58139-90005-5	97384	.MICROCIRCUIT (SOURCE CONTROLLED... FROM PART NO LM160H MFD BY 12040)	2		PAFZZ
/ 7-121	808-187	32559	.INSULATOR.....	2		PAFZZ
/ 7-122	M38510/31508BEB	81349	.MICROCIRCUIT.....	1		PAFZZ
/ 7-123	RJR24FX503M	81349	.RESISTOR,VARIABLE.....	1		PAFZZ
/ 7-124	RJR24FX102M	81349	.RESISTOR,VARIABLE.....	2		PAFZZ
/ 7-125	RJR24FX502M	81349	.RESISTOR,VARIABLE.....	16		PAFZZ
	86091-2	00779	.TERMINAL.....	33		PAFZZ
	75401-003	22526	.POST, WIRE WRAP.....	55		PAFZZ
/ 7-126	58139-40011	97384	.PRINTED WIRING BOARD.....	1		XA---

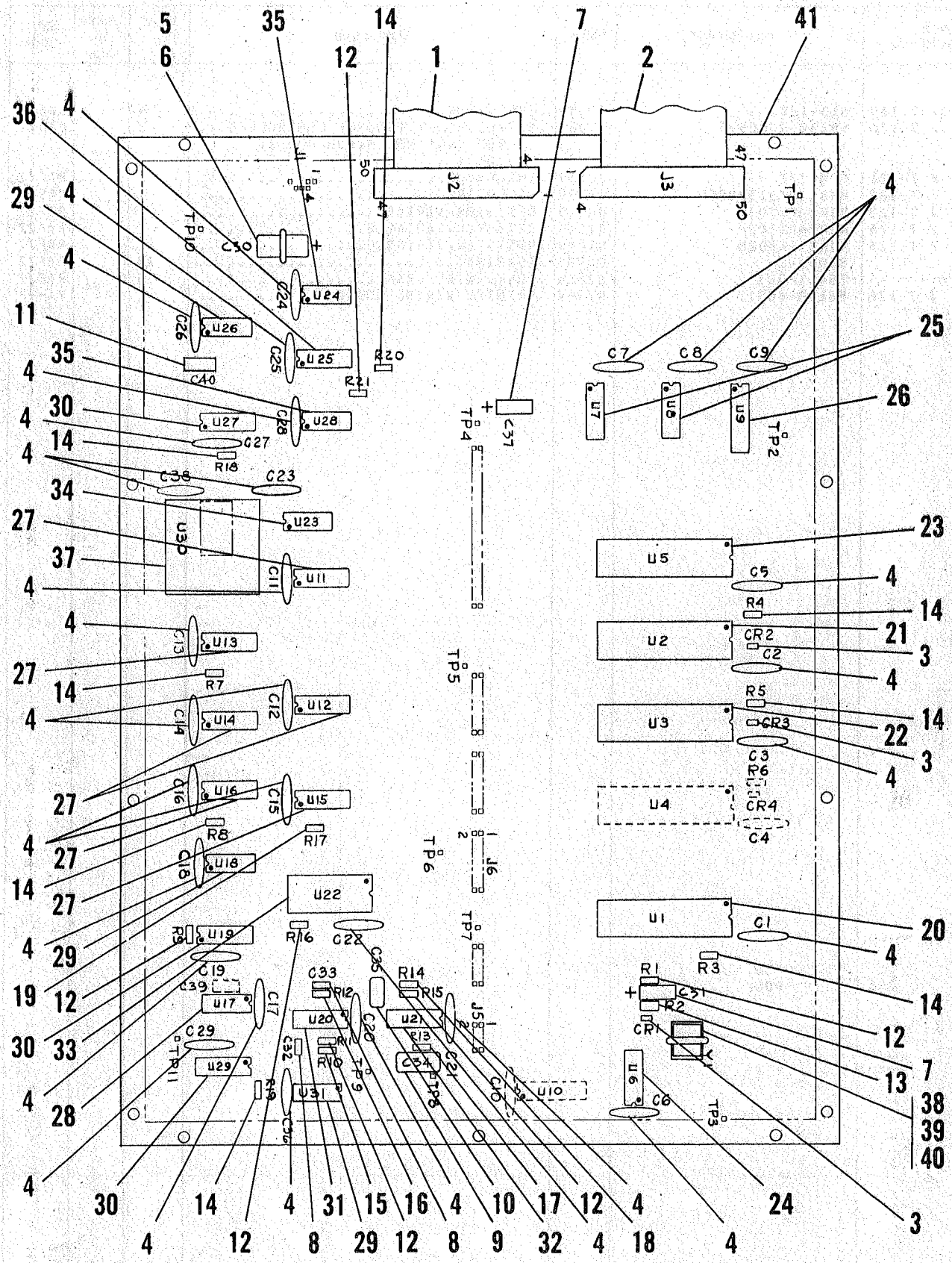

Figure 11. Circuit Card Assembly, Digital

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
11 -	58139-40015	97384	CIRCUIT CARD ASSEMBLY, DIGITAL SEE FIG 5 FOR NHA	REF		PAFFD
-1	58139-90020-1	97384	.CABLE ASSEMBLY (SOURCE CONTROLLED. FROM PART NO 58139-90020-1 MFD BY 22526)	1		PBFFF
-2	58139-90020-2	97384	.CABLE ASSEMBLY (SOURCE CONTROLLED. FROM PART NO 58139-90020-2 MFD BY 22526)	1		PBFFF
-3	JANTX1N4148-1	81349	.SEMICONDUCTOR DEVICE.....	3		PAFZZ
-4	CK63AW103M	81349	.CAPACITOR.....	29		PAFZZ
-5	M39003/01-2614	81349	.CAPACITOR.....	1		PAFZZ
-6	2829-75-2	98159	.STRAP.....	1		PAFZZ
-7	M39003/01-2596	81349	.CAPACITOR.....	2		PAFZZ
-8	M39014/02-1258	81349	.CAPACITOR.....	2		PAFZZ
-9	CMR06F681JDDP	81349	.CAPACITOR.....	1		PAFZZ
-10	CMR05F151JDDP	81349	.CAPACITOR.....	1		PAFZZ
-11	CMR05F101JDDP	81349	.CAPACITOR.....	1		PAFZZ
-12	RCR07G102JS	81349	.RESISTOR.....	6		PAFZZ
-13	RCR07G513JS	81349	.RESISTOR.....	1		PAFZZ
-14	RCR07G512JS	81349	.RESISTOR.....	8		PAFZZ
-15	RCR07G153JS	81349	.RESISTOR.....	1		PAFZZ
-16	RCR07G223JS	81349	.RESISTOR.....	1		PAFZZ
-17	RCR07G203JS	81349	.RESISTOR.....	1		PAFZZ
-18	RCR07G472JS	81349	.RESISTOR.....	1		PAFZZ
-19	RCR07G101JS	81349	.RESISTOR.....	1		PAFZZ
-20	58139-90027-1	97384	.MICROCIRCUIT (SOURCE CONTROLLED... FROM PART NO ID8085A MFD BY 34649)	1		PAFZZ
-21	58139-40057-1	97384	.MICROCIRCUIT.....	1		PAFZZ
-22	58139-40057-2	97384	.MICROCIRCUIT.....	1		PAFZZ
-23	58139-90027-2	97384	.MICROCIRCUIT (SOURCE CONTROLLED... FROM PART NO. ID8155 MFD BY 34649)	1		PAFZZ
-24	M38510/307038EB	81349	.MICROCIRCUIT.....	1		PAFZZ
-25	58139-90005-1	97384	.MICROCIRCUIT (SOURCE CONTROLLED... FROM PART NO. MD8216/8 MFD BY 34335)	2		PAFZZ
-26	7705701RB	14933	.MICROCIRCUIT.....	1		PAFZZ
-27	M38510/31508BEB	81349	.MICROCIRCUIT.....	6		PAFZZ
-28	M38510/00104BCB	81349	.MICROCIRCUIT.....	1		PAFZZ
-29	M38510/30001BCB	81349	.MICROCIRCUIT.....	3		PAFZZ
-30	M38510/30110BEB	81349	.MICROCIRCUIT.....	3		PAFZZ
-31	M38510/31401BEB	81349	.MICROCIRCUIT.....	1		PAFZZ
-32	M38510/31402BEB	81349	.MICROCIRCUIT.....	1		PAFZZ
-33	58139-90027-4	97384	.MICROCIRCUIT (SOURCE CONTROLLED... FROM PART NO ID8253 MFD BY 34649)	1		PAFZZ
-34	M38510/07003BCB	81349	.MICROCIRCUIT.....	1		PAFZZ
-35	58139-90005-2	97384	.MICROCIRCUIT (SOURCE CONTROLLED... FROM PART NO. SNJ54LS393J MFD BY 01295)	2		PAFZZ
-36	M38510/30901BEB	81349	.MICROCIRCUIT.....	1		PAFZZ
-37	58139-90030	97384	.OSCILLATOR, CRYSTAL CLOCK (SOURCE. CONTROLLED FROM PART NO. CO-231-1 MFD BY 27802)	1		PAFZZ
-38	CR60A/U-4.0000MHZ	81349	.CRYSTAL UNIT, QUARTZ.....	1		PAFZZ
-39	2829-75-2	98159	.STRAP.....	1		PAFZZ
-40	58139-40042	97384	.INSULATOR.....	1		MFFZZ
	86091-2	00779	.TERMINAL.....	142		PAFZZ
	75401-003	22526	.POST WIRE WRAP.....	11		PAFZZ
-41	58139-40016	97384	.PRINTED WIRING BOARD.....	1		XA---

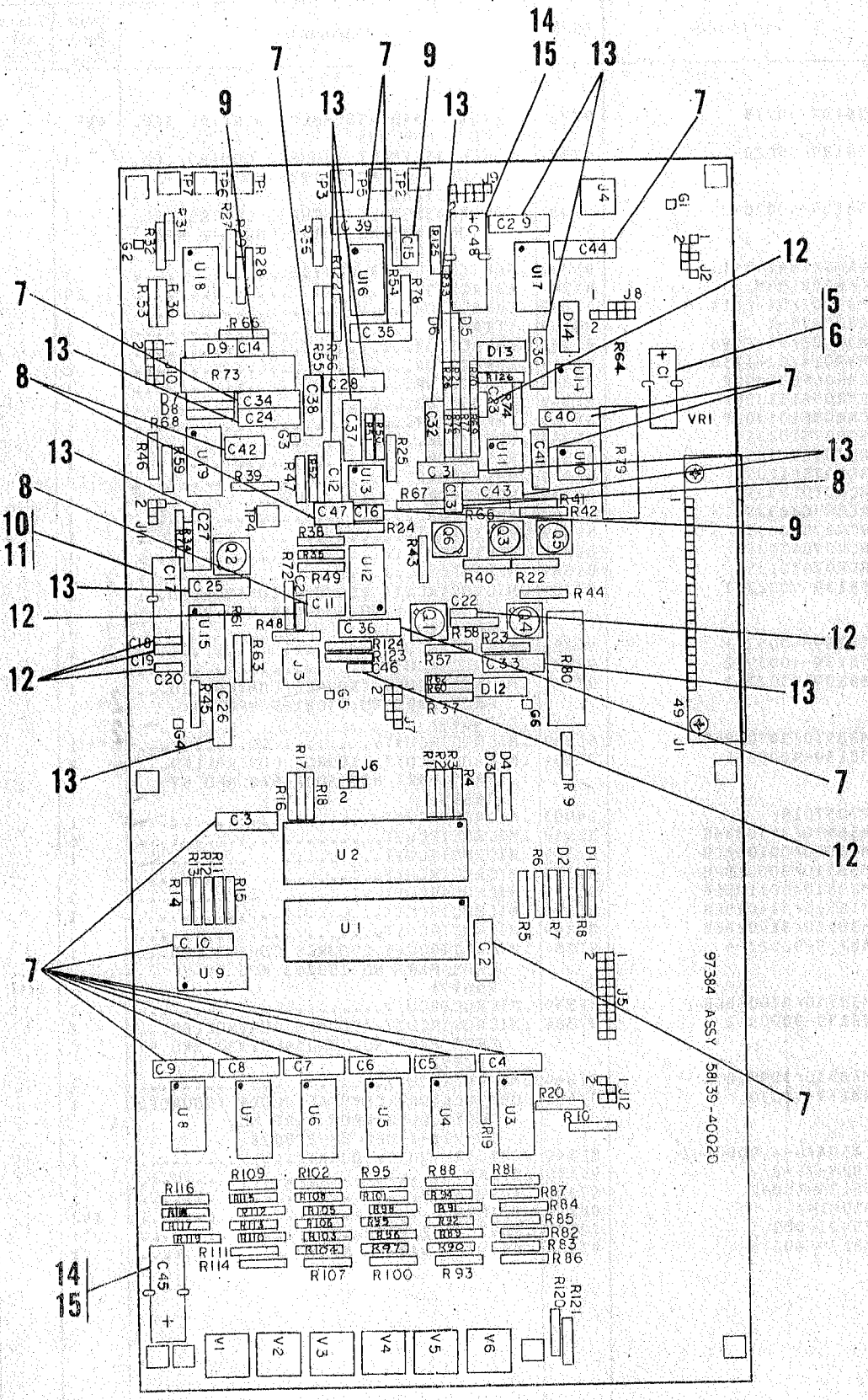

Figure 12. Circuit Card Assembly, Front Panel Interface (Sheet 1 of 4)

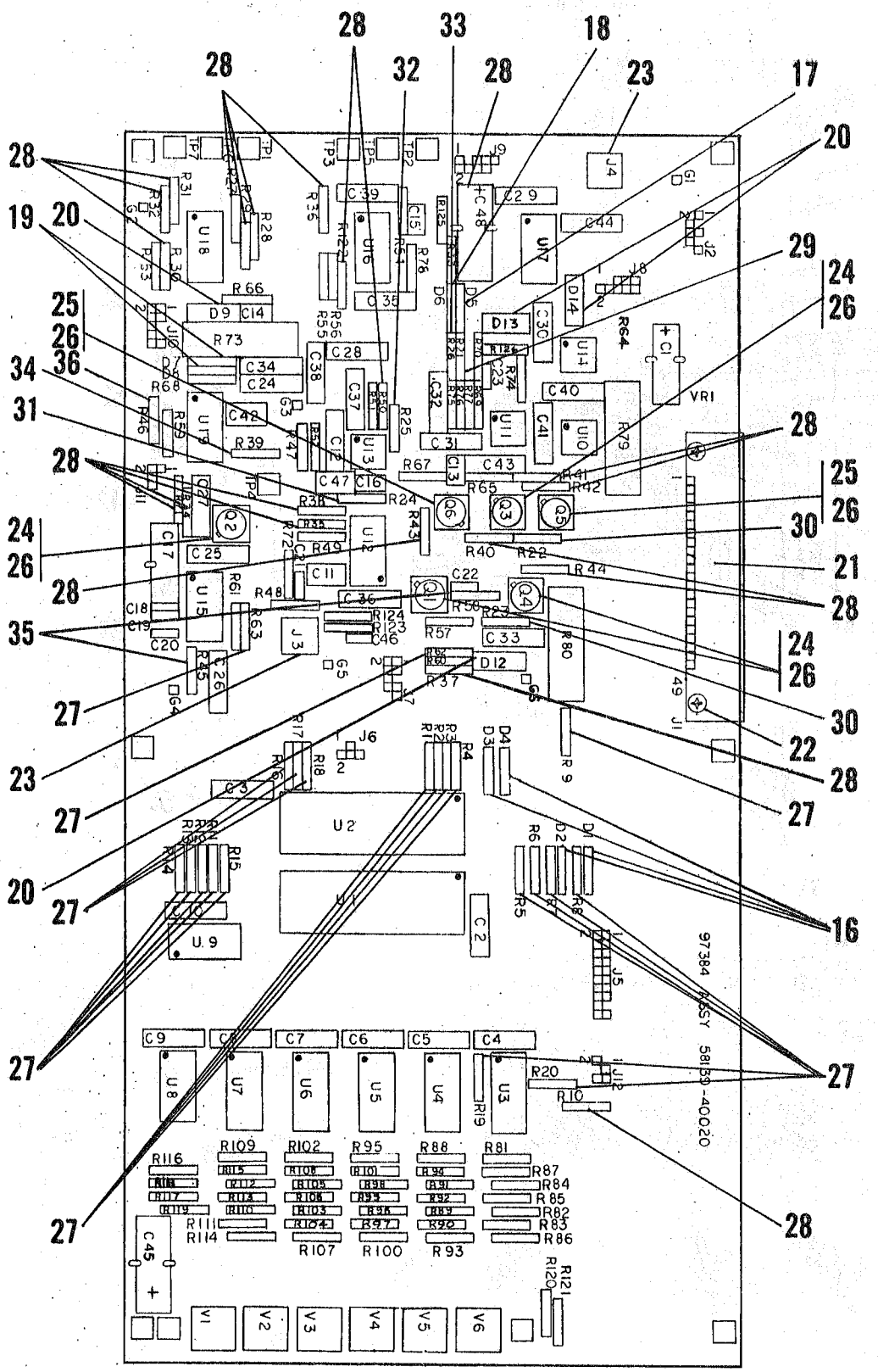

Figure 12. Circuit Card Assembly, Front Panel Interface (Sheet 2 of 4)

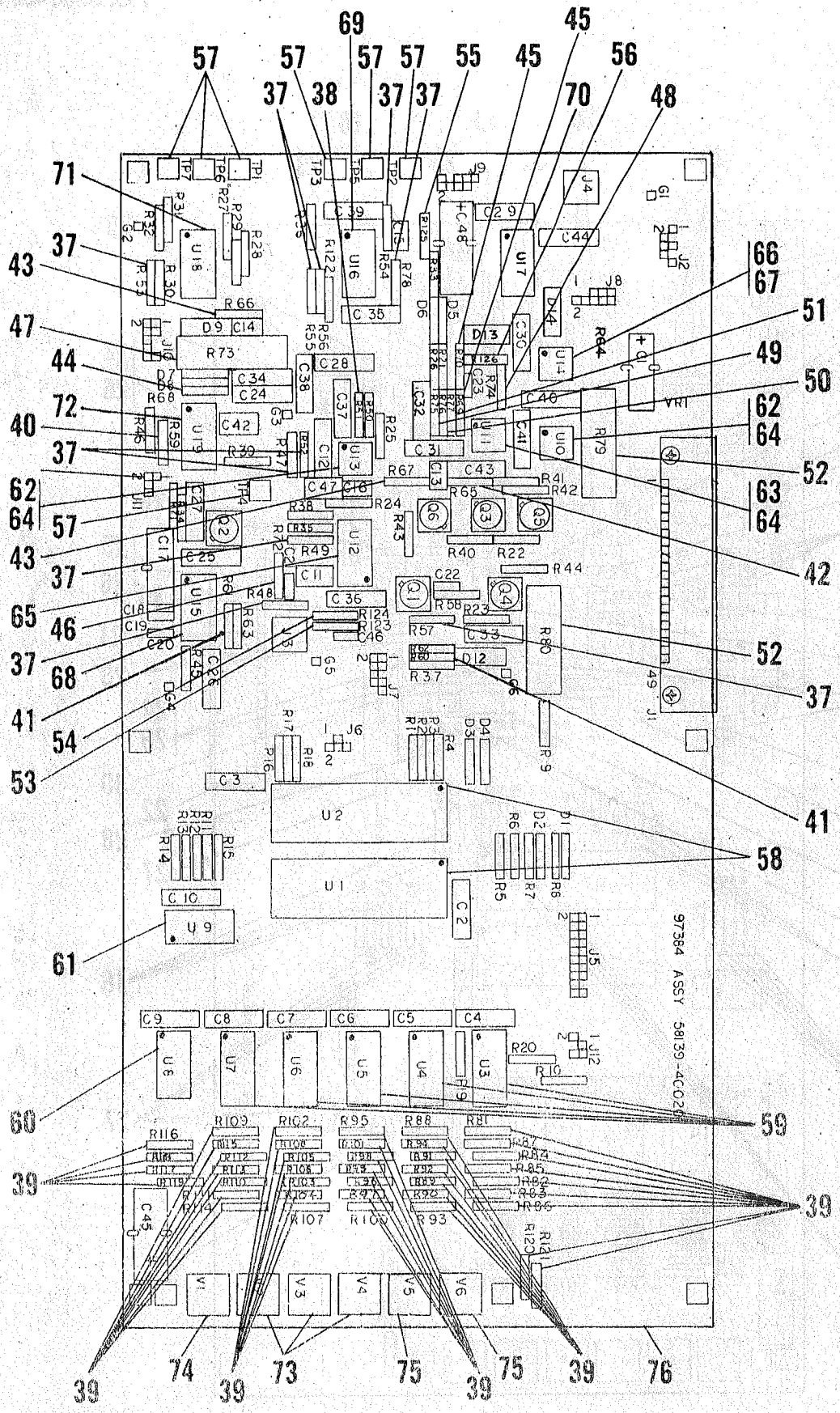

Figure 12. Circuuit Card Assembly, Front Panel Interface (Sheet 3 of 4)

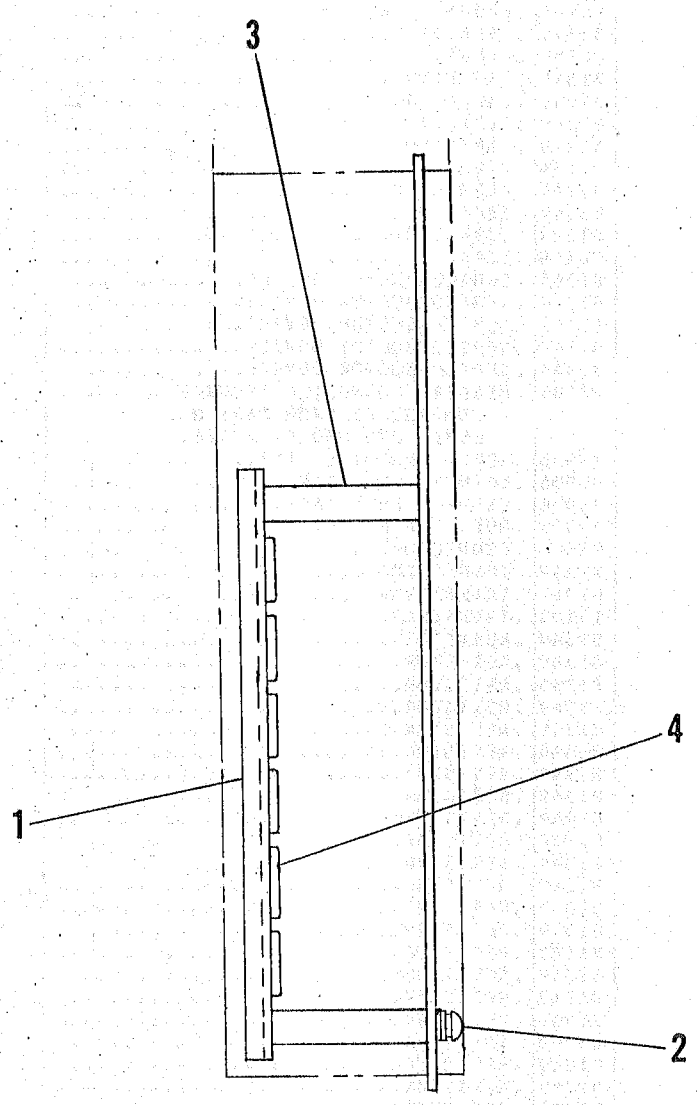

Figure 12. Circuit Card Assembly, Front Panel Interface (Sheet 4 of 4)

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
12 -	58139-40020	97384	CIRCUIT CARD ASSEMBLY, FRONT PANEL. INTERFACE SEE FIG 5 FOR NHA	REF		PAFFD
/ 4-1	58139-40024	97384	.CHANNEL	1		MFFZZ
/ 4-2	MS51957-27	96906	.SCREW, MACHINE	4		PAFZZ
	MS35338-136	96906	.WASHER, LOCK	4		PAFZZ
	MS15795-805	96906	.WASHER, FLAT	4		PAFZZ
	2515	83330	.WASHER, NYLON	2		PAFZZ
/ 4-3	58139-40023	97384	.POST, 6-32 UNC-2B THD X .25 MIN. DEEP (BOTH ENDS) 1-25 LG, .250 DIA	2		MFFZZ
/ 4-4	MS35489-1	96906	.GROMMET, RUBBER	6		PAFZZ
/ 1-5	M39003/01-2608	81349	.CAPACITOR	1		PAFZZ
/ 1-6	2829-75-2	98159	.STRAP	1		PAFZZ
/ 1-7	CK63AW103M	81349	.CAPACITOR	17		PAFZZ
/ 1-8	CMR05F101JODP	81349	.CAPACITOR	4		PAFZZ
/ 1-9	CK60AW102M	81349	.CAPACITOR	3		PAFZZ
/ 1-10	CFR06ANC104KM	81349	.CAPACITOR	1		PAFZZ
/ 1-11	2829-75-2	98159	.STRAP	1		PAFZZ
/ 1-12	M39014/02-1310	81349	.CAPACITOR	7		PAFZZ
/ 1-13	M39003/01-2596	81349	.CAPACITOR	13		PAFZZ
/ 1-14	M39003/01-2546	81349	.CAPACITOR	2		PAFZZ
/ 1-15	2829-75-2	98159	.STRAP	2		PAFZZ
/ 2-16	JAN1N277	81349	.SEMICONDUCTOR DEVICE	4		PAFZZ
/ 2-17	JANTX1N750A	81349	.SEMICONDUCTOR DEVICE	1		PAFZZ
/ 2-18	JANTX1N752A	81349	.SEMICONDUCTOR DEVICE	1		PAFZZ
/ 2-19	JANTX1N645-1	81349	.SEMICONDUCTOR DEVICE	2		PAFZZ
/ 2-20	JANTX1N4148-1	81349	.SEMICONDUCTOR DEVICE	4		PAFZZ
/ 2-21	58139-90019	97384	.HEADER, CONNECTOR (SOURCE CONTROLLED FROM PART NO. 65823-093 MFD BY 22526)	1		PAFZZ
/ 2-22	MS51957-6	96906	.SCREW, MACHINE (AP)	2		PAFZZ
	MS15795-802	96906	.WASHER, FLAT (AP)	2		PAFZZ
	MS35338-134	96906	.WASHER, LOCK (AP)	2		PAFZZ
	MS35649-224	96906	.NUT, PLAIN (AP)	2		PAFZZ
/ 2-23	M39012/93-3001	96906	.CONNECTOR	2		PAFZZ
/ 2-24	JANTX2N2222A	81349	.TRANSISTOR	4		PAFZZ
/ 2-25	JANTX2N2907A	81349	.TRANSISTOR	2		PAFZZ
/ 2-26	7717-44-DAP	13103	.TRANSIPAD	6		PAFZZ
/ 2-27	RCR07G512JS	81349	.RESISTOR	21		PAFZZ
/ 2-28	RCR07G102JS	81349	.RESISTOR	21		PAFZZ
/ 2-29	RCR07G561JS	81349	.RESISTOR	1		PAFZZ
/ 2-30	RCR07G331JS	81349	.RESISTOR	2		PAFZZ
/ 2-31	RCR07G471JS	81349	.RESISTOR	1		PAFZZ
/ 2-32	RCR07G103JS	81349	.RESISTOR	1		PAFZZ
/ 2-33	RCR07G821JS	81349	.RESISTOR	1		PAFZZ
/ 2-34	RCR07G302JS	81349	.RESISTOR	1		PAFZZ
/ 2-35	RCR07G152JS	81349	.RESISTOR	2		PAFZZ
/ 2-36	RCR07G122JS	81349	.RESISTOR	1		PAFZZ
/ 3-37	RCR07G202JS	81349	.RESISTOR	10		PAFZZ
/ 3-38	RCR07G753JS	81349	.RESISTOR	1		PAFZZ
/ 3-39	RCR07G751JS	81349	.RESISTOR	41		PAFZZ
/ 3-40	RCR07G242JS	81349	.RESISTOR	1		PAFZZ
/ 3-41	RCR07G392JS	81349	.RESISTOR	2		PAFZZ
/ 3-42	RCR07G133JS	81349	.RESISTOR	1		PAFZZ
/ 3-43	RCR07G153JS	81349	.RESISTOR	2		PAFZZ
/ 3-44	RCR07G273JS	81349	.RESISTOR	1		PAFZZ
/ 3-45	RCR07G513JS	81349	.RESISTOR	2		PAFZZ
/ 3-46	RCR07G154JS	81349	.RESISTOR	1		PAFZZ
/ 3-47	RCR42G471JS	81349	.RESISTOR	1		PAFZZ
/ 3-48	RNC55J1001FM	81349	.RESISTOR	1		PAFZZ
/ 3-49	RNC55J1051FM	81349	.RESISTOR	1		PAFZZ
/ 3-50	RNC55J3011FM	81349	.RESISTOR	1		PAFZZ
/ 3-51	RNC55J8661FM	81349	.RESISTOR	1		PAFZZ
/ 3-52	RCR42G200JS	81349	.RESISTOR	2		PAFZZ
/ 3-53	RCR07G333JS	81349	.RESISTOR	1		PAFZZ
/ 3-54	RCR07G101JS	81349	.RESISTOR	1		PAFZZ
/ 3-55	RCR07G100JS	81349	.RESISTOR	1		PAFZZ
/ 3-56	RCR07G912JS	81349	.RESISTOR	1		PAFZZ

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
12/ 3-57	M55155/29-6	81349	.TERMINAL.....	7		PAFZZ
/ 3-58	58139-90027-5	97384	.MICROCIRCUIT (SOURCE CONTROLLED... FROM PART NO ID8255A MFD BY 34649)	2		PAFZZ
/ 3-59	M38510/010078FB	81349	.MICROCIRCUIT.....	5		PAFZZ
/ 3-60	M38510/00802BCB	81349	.MICROCIRCUIT.....	1		PAFZZ
/ 3-61	M38510/001048CB	81349	.MICROCIRCUIT.....	1		PAFZZ
/ 3-62	M38510/10304BGC	81349	.MICROCIRCUIT.....	2		PAFZZ
/ 3-63	M38510/10107BGC	81349	.MICROCIRCUIT.....	1		PAFZZ
/ 3-64	808-187	32559	.INSULATOR.....	3		PAFZZ
/ 3-65	58139-90005-8	97384	.MICROCIRCUIT (SOURCE CONTROLLED... FROM PART NO 733DMQB MFD BY 34148)	1		PAFZZ
/ 3-66	M38510/10101BGC	81349	.MICROCIRCUIT.....	1		PAFZZ
/ 3-67	808-187	32559	.INSULATOR.....	1		PAFZZ
/ 3-68	58139-90005-7	97384	.MICROCIRCUIT (SOURCE CONTROLLED... FROM PART NO XR2207M MFD BY 52063)	1		PAFZZ
/ 3-69	M38510/303018CB	81349	.MICROCIRCUIT.....	1		PAFZZ
/ 3-70	M38510/30102BCB	81349	.MICROCIRCUIT.....	1		PAFZZ
/ 3-71	M38510/30002BCB	81349	.MICROCIRCUIT.....	1		PAFZZ
/ 3-72	M38510/300018CB	81349	.MICROCIRCUIT.....	1		PAFZZ
/ 3-73	DA2100V1	97384	.INCANDESCENT DISPLAY TUBE AAI SPEC CONT DWG 58139-90017-2	3		PAFZZ
/ 3-74	DA2120V1	97384	.INCANDESCENT DISPLAY TUBE AAI SPEC CONT DWG 58139-90017-3	1		PAFZZ
/ 3-75	DA2110V1	97384	.INCANDESCENT DISPLAY TUBE AAI SPEC CONT DWG 58139-90017-1	2		PAFZZ
	86091-2	00779	.TERMINAL.....	69		PAFZZ
/ 3-76	58139-40021	97384	.PRINTED WIRING BOARD.....	1		XA---

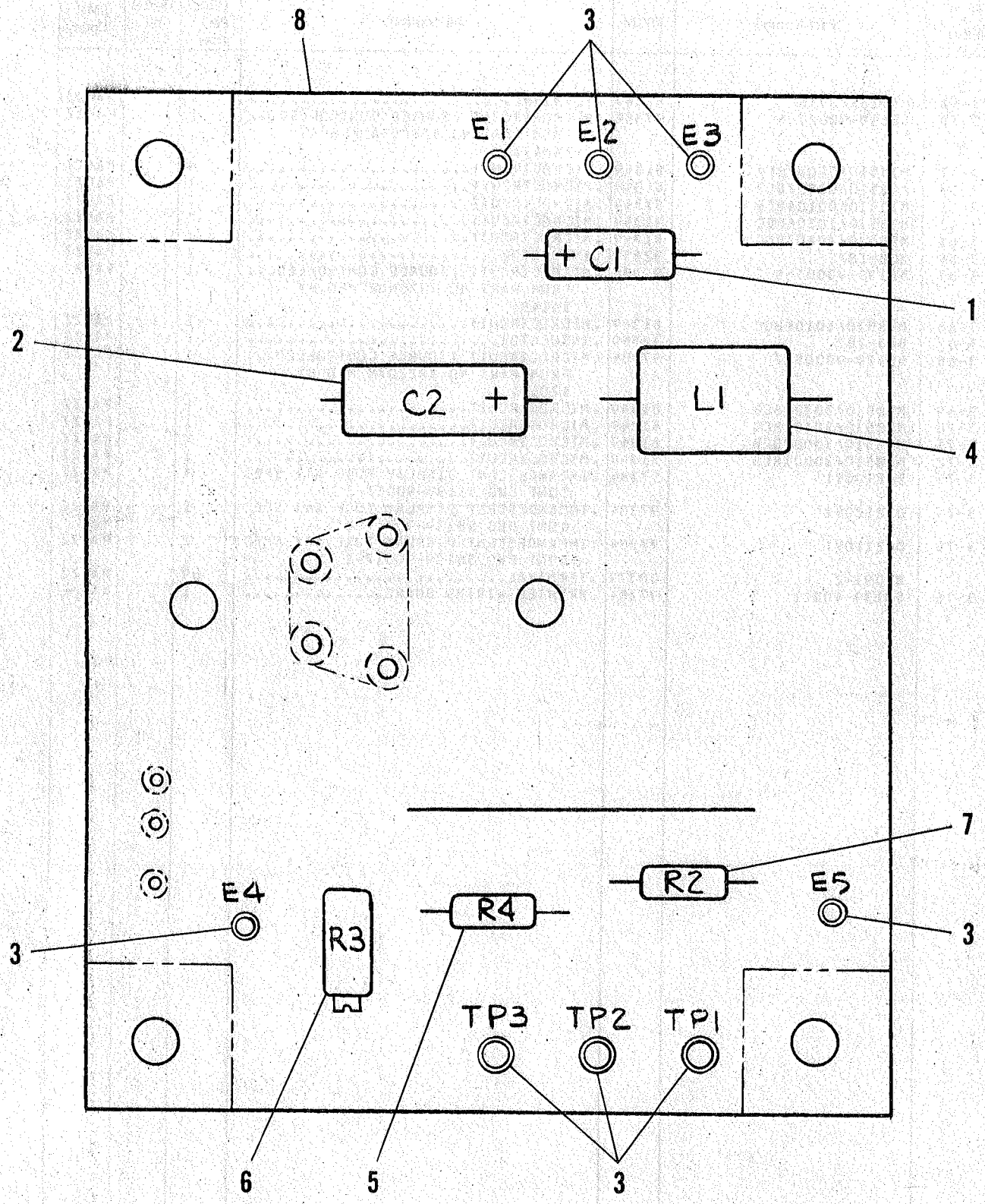

Figure 13. Circuit Card Assembly, Gun Oscillator Regulator

Figure & Index Number	Part Number	FSCM	Description	Units Per Assy	Usable on Code	SMR Code
13 -	58139-40050	97384	CIRCUIT CARD ASSEMBLY, GUN..... OSCILLATOR REGULATOR SEE FIG 7 FOR NHA	REF		PAFFF
-1	M39003/01-2596	81349	.CAPACITOR.....	1		PAFZZ
-2	M39003/01-2544	81349	.CAPACITOR.....	1		PAFZZ
-3	SE12XC04	81349	.TERMINAL.....	8		PAFZZ
-4	VK200-10/3B	02114	.CHOKE, RF.....	1		PAFZZ
-5	RTH42ES392J	81349	.THERMISTER.....	1		PAFZZ
-6	RJR24FX502M	81349	.RESISTOR, VARIABLE.....	1		PAFZZ
-7	RNC55J8221FM	81349	.RESISTOR.....	1		PAFZZ
-8	58139-40051	97384	PRINTED WIRING BOARD.....	1		XA---

SECTION III
NUMERICAL INDEX

Part Number	Figure & Index Number	Qty Per End Item
B1900-656	1-8	4
B2-11-S	7-35	2
B2-6-S	7-39	2
CFR06ANC104KM	12-10	
CK60AW102M	7-18	8
	10-42	
	12-9	
CK63AW103M	10-32	71
	11-4	
	12-7	
CMR05C180JDDP	10-34	3
CMR05E300JDDP	10-37	3
CMR05F101JDDP	10-40	9
	11-11	
	12-8	
CMR05F151JDDP	10-33	4
	11-10	
CMR05F161JDDP	10-41	5
CMR05F331JDDP	10-39	1
CMR05F391JDDP	10-45	2
CMR06F681JDDP	11-9	1
CR60A/U-4.0000MHZ	11-38	1
CS-5	7-37	1
CO3-11U	7-30	1
DA2100V1	12-73	3
DA2110V1	12-75	2
DA2120V1	12-74	1
EM22438	5-63	1
FS156	F 5-119	2
JANTX1N4148-1	11-3	5
	12-20	
JANTX1N4150-1	10-48	15
JANTX1N645-1	12-19	2
JANTX1N746A	10-46	1
JANTX1N750A	10-49	4
	12-17	
JANTX1N752A	12-18	1
JANTX2N2222A	10-54	17
	12-24	
JANTX2N2907A	10-53	9
	12-25	
JAN1N277	12-16	4
JAN1N458	10-47	15
MH6-611	1-9	1
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