WJ-861X RECEIVER

APPENDIX C

WJ-861X DIGITAL REFRESHED DISPLAY OPTION

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WARNING

This equipment utilizes voltages which are potentially dangerous and may be fatal if contacted. Exercise extreme caution when working with the equipment with any protective cover removed.

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DIGITAL REFRESHED DISPLAY (DRD) OPTION

C.1 GENERAL DESCRIPTION

The Type 796217-1 Digital Refreshed Display (DRD) option is operational in the Scan mode and provides a signal strength vs frequency plot of the frequency band being scanned. To utilize this option, the receiver must be equipped with the Signal Monitor option (SM) or an external display. As the receiver scans, the signal strength is sampled at 256 equally spaced points throughout the Scan and the signal strength data is stored in an on-board memory. The memory locations are then stepped through at a higher rate of speed by an on-board counter reading the stored data and supplying the display with the horizontal and vertical signals needed to generate the signal strength plot. The signal strength data is displayed in ascending frequency order, with the start frequency at the extreme left of the display and the stop frequency at the extreme right.

C.2 INSTALLATION

Most of the connections required by the DRD option are provided at the Option Slot 2 connector of the Digital I/O Motherboard (A5). Generally, installation consists of inserting the board into the slot and making one additional plug connection.

Installation is performed as follows:

1. Remove the top and bottom covers from the receiver.

2. Insert the Type 796217-1 Digital Refresh Display circuit board into Option Slot 2 on the Digital I/O Motherboard (A5). Orient the circuit board such that pin 1 of the board mates with pin 1 of Option Slot 2.

3. (Perform this step when the SM option is installed in the receiver.) From the underside of the receiver, remove plug P38 from J5 (on the Digital Motherboard) and install P38 to the pins of Option Slot 2. Orient the plug such that pin 2 of P38 mates with pin 4 of Option Slot 2 and pin 6 of P38 mates with Option Slot 2 pin 12.

4. If an external display is utilized, check the operating manual of the display unit to determine the polarity of the blanking pulse required (Z axis). The standard receiver chassis is wired to provide a negative blanking pulse. If a positive pulse is required, remove the wire-wrap connection from pin 21 of Option Slot 2 and instaN at pin 22.

C.3 CIRCUIT DESCRIPTION

C.3.1 FUNCTIONAL DESCRIPTION

When Scan is initiated, the microprocessor divides the Scan band into 256 equal segments and provides the signal strength data obtained in each segment to the DRD memory (U4 and U7). As the first segment is scanned, the signal strength data acquired is written into the DRD memory at address 0. The output of the DRD circuitry is then enabled and the memory is then stepped through at a rapid rate producing the first segment of the signal strength vs frequency trace. When the second segment of the frequency band is scanned, the DRD output is disabled and the signal strength data acquired during the second segment of the Scan is written into memory address 1. The DRD output is again enabled and the on-board counter again steps through the memory locations producing the first and second segments of the signal strength vs frequency trace. This sequence continues until the entire 256 segments have been scanned or until the Scan is halted, due to the acquisition of a signal greater than the programmed COR level or until the receiver is placed into the Scan continue mode of operation. At that time, the memory locations are continuously stepped through by the counter providing a continuous trace of the signals acquired up to that point. When the receiver is returned to the manual operating mode, the DRD output is disabled and the standard signal monitor trace is provided to the display (when the SM option is installed in the receiver).

C.3.2 DETAILED CIRCUIT DESCRIPTION

C.3.2.1 Type 796217-1, Digital Refreshed Display (DRD)

The option designation for this subassembly is DRD. Refer to **Figure C-1** for the Type 796217-1 Digital Refresh Display schematic diagram.

The Type 796217-1 Digital Refreshed Display is comprised of a 1024-byte memory (U10 and U11), a 12-bit binary counter (U12) and two Digital-to-Analog Converters to provide X axis (U14) and Y axis (U13) signals to the display unit. The remaining circuitry comprises the switching circuits to control the DRD operation, under the direction of the microprocessor. Integrated circuits U10 and U11 form the DRD random-access-memory, which is capable of storing up to 1024 8-bit data words. With the standard receiver software, only the first 256 memory locations are utilized providing a single output trace. When data is written into memory, address bus lines A0 through A7 are applied to the memory address inputs, via the switching circuit comprised of U7, U8 and U9. The R/W select input to the W (write enable) input of each memory chip, placing the memory into the write mode, is enabled via decoder U4. Data representing the strength of the acquired signal is then placed on the memory data input lines via octal buffer U1. After the signal data is stored in memory, the microprocessor causes the memory address inputs to be switched from the address bus to the on-board binary counter (U12). U12 then continuously steps through each of the memory locations recalling the data stored at each address. The outputs of U12 are also provided to the data inputs are of D/A converter U14, generating a linear voltage sawtooth that causes the display trace to track horizontally across the CRT face. Since the data recall and the horizontal trace are both synchronized to the outputs of U12, the signal data appears as a vertical deflection at the proper time relationship with the sweep. The output data from the memory is applied to D/A converter U13 producing an analog voltage that is proportional to the magnitude of the data byte. This analog voltage is then applied to the vertical circuitry of the display producing a vertical deflection that is proportional to the signal strength of the signal.

D/A converter U14 produces an output current sink at pin 1 that is capable of sinking from 0 mA, when the inputs at pins 4 through 11 are all at logic "0", to approximately 2 mA, when the inputs are all at logic "1." Each binary input between these two extremes produces a current change that is equal to 1/256 of the total current range. Potentiometer R10 provides a voltage reference for the current amplifier within U14. The output is converted to a voltage sawtooth that varies from -10 V to +10 V by U16B. Resistor R21 controls the offset at the output. Potentiometer R22 adjusts the offset controlling the horizontal placement of the CRT trace and potentiometer R10 adjusts the peak-to-peak output of the sawtooth adjusting the horizontal width of the trace. This output is applied, via U17, to the H output (connector pin 4) and to the EH output (pin 47), via the voltage divider formed by R16, R25 and R19. This voltage divider drops the output voltage to a 1 V peak-to-peak level to be compatible with an external display. The D/A converter and the output circuit comprised of U13 and U16A is identical to the circuitry of U14, except that this circuit produces short duration pulses that range from -.5 V, when the data inputs are all at logic "0", to +.5 V, when the data inputs are all at logic "1". Potentiometer R5 adjusts the vertical amplitude and R7 adjusts the vertical offset controlling the vertical placement of the CRT trace.

Binary counter U12 receives a 31.25 kHz signal from the microprocessor sub-assembly (CLK 5) and utilizes this clock to produce a continuous binary count of from 0 to 1023. The CA0 through CA7 outputs are utilized to step through the DRD memory and to produce a sawtooth output voltage, which drives the display trace. These outputs continuously count from 0 to 255, every 8 msec. The CA7 output of U12 is also utilized to produce a retrace blanking pulse every time the counter passes its maximum count of 255. Integrated circuit U15A is strobed on the 256th count providing a pulse to pin 22 as the +Z output. The inverted blanking pulse provided as a negative going pulse at the -Z output (pin 21).

Integrated circuit U4 decodes the logic levels of inputs A10 and R/W controlling the DRD inputs and outputs. This decoder is enabled when the OE input is "0" and the DBE clock is at "1", to enable the appropriate switching circuits. When A10 and R/W are "0", U4 enables U1 permitting data from the data bus to be written into memory. With A10 at "0" and R/W at "1", U1 is enabled placing data from the DRD memory on the data bus. This permits the microprocessor to read data from the DRD memory, as required. U4 enables control register U2 when the microprocessor is in the write mode (R/W="0") and A10 is at logic "1". A "0" transition at pin 11 of U4 causes the data present on the D0, D1 and D2 data bus lines to be latched at the Q outputs of U2. D0 enables (1) or disables (0) the DRD output and D1 enables (1) or disables (0) the standard signal monitor trace (when installed in the receiver). D2 is provided to enable U3A and U3B when the receiver software utilized contains the capability of a four trace display.

C.4 ALIGNMENT PROCEDURES

Alignment of the Type 796217-1 Digital Refreshed Display consists of setting the offset and gain of the DRD output circuits, as follow:

1. Remove the receiver top cover to provide access to the DRD adjustment potentiometers.

2. Set the receiver to scan between 20 and 30 MHz. Set the COR level to "--" providing a continuous Scan.

3. Connect the HP-8640B signal generator to the ANT 1 input and set the generator to produce a 25 MHz CW output. Adjust the output level to minimum.

4. Adjust R22, on the DRD subassembly centering the trace horizontally on the signal monitor CRT.

5. Adjust R10 until the trace just touches the scale markings at the extreme left and right of the CRT face.

6. Adjust the vertical position of the trace by rotating R7 until the trace is directly under the bottom line of the CRT scale.

7. Increase the signal generator output level until a signal pip, one division in amplitude, is present on the trace.

8. Increase the generator output level by 30 dB and adjust R5 for a pip amplitude of exactly four divisions.

9. If an external display is utilized, adjust R25 to obtain the desired sweep width on the CRT of the display.

C.5 PARTS LIST

C.5.1 TYPE 796217-1 DIGITAL REFRESHED DISPLAY

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
	Revision F				
C1	Capacitor, Electrolytic, Tantalum: 10 µF, 20%, 20 V	2	196D106X0020JE3	56289	
C2	Same as C1				
C3	Capacitor, Ceramic, Disc: .1 µF, 20%, 50 V	10	34475-1	14632	
C4	Capacitor, Ceramic, Disc: 2200 pF, 10%, 200 V	1	CK06BX222K	81349	
C5	Capacitor, Mica, Dipped: 47 pF, 2%, 500 V	1	CM04ED470G03	81349	
C6	Capacitor, Electrolytic, Tantalum: 47 µF, 20%, 20 V	3	196D476X0020PE4	56289	
C7	Same as C6				
C8	Same as C6				
C9 Thru C16	Same as C3				
C17	Not Used				
C18	Same as C3				
C19	Capacitor, Mica, Dipped: 470 pF, 2%, 500 V	1	DMLS-471G	72136	
CR1	Diode	2	5082-2811	28480	
CR2	Same as CR1				
R1	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/8 W	4	CF1/8-3.3 K/J	09021	
R2	Same as R1				
R3	Resistor, Fixed, Film: 2.2 kΩ, 5%, 1/8 W	1	CF1/8-2.2 K/J	09021	
R4	Resistor, Fixed, Film: 470Ω, 5%, 1/8 W	1	CF1/8-470 OHMS/J	09021	
R5	Resistor, Trimmer, Film: 10 kΩ, 10%, 1/2 W	2	62PAR10K	73138	
R6	Resistor, Fixed, Film: 33 kΩ, 5%, 1/8 W	2	CF1/8-33 K/J	09021	
R7	Resistor, Trimmer, Film: 200 kΩ, 10%, 1/2 W	2	62PAR200K	73138	
R8	Resistor, Fixed, Film: 560Ω, 5%, 1/4 W	1	CF1/4-560 OHMS/J	09021	
R9	Resistor, Fixed, Film: 2.4 kΩ, 5%, 1/4 W	1	CF1/4-2.4 K/J	09021	
R10	Same as R5				
R11	Resistor, Fixed, Film: 680Ω, 5%, 1/8 W	2	CF1/8-680 OHMS/J	09021	
R12	Resistor, Fixed, Film: 100Ω, 5%, 1/4 W	2	CF1/4-100 OHMS/J	09021	
R13	Resistor, Fixed, Film: 100 kΩ, 5%, 1/8 W	1	CF1/8-100 K/J	09021	
R14	Same as R11				
R15	Same as R12				
R16	Resistor, Fixed, Film: 8.2 kΩ, 5%, 1/8 W	2	CF1/8-8.2 K/J	09021	
R17	Resistor, Fixed, Film: 120 kΩ, 5%, 1/8 W	1	CF1/8-120 K/J	09021	
R18	Same as R16				
R19	Resistor, Fixed, Film: 150Ω, 5%, 1/8 W	1	CF1/8-150 OHMS/J	09021	
R20	Same as R1				
R21	Resistor, Fixed, Film: 22 kΩ, 5%, 1/8 W	1	CF1/8-22 K/J	09021	
R22	Same as R7				
R23	Same as R6				
R24	Resistor, Fixed, Film: 15 kΩ, 5%, 1/8 W	1	CF1/8-15K/J	09021	
R25	Resistor, Trimmer, Film: 500Ω, 10%, 1/2 W	1	62PAR500	73138	
R26	Same as R1				

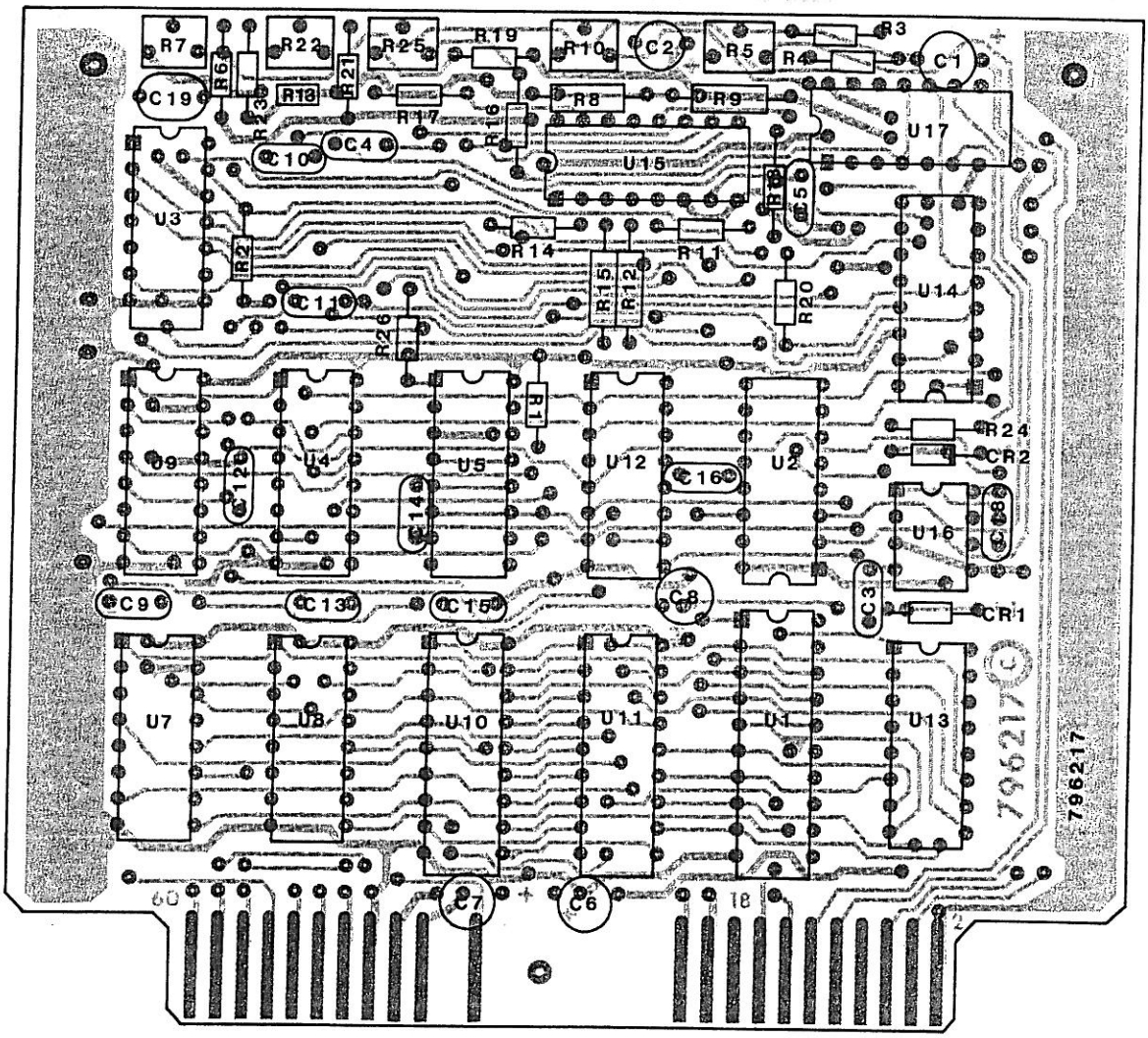

Figure C-1. Type 796217-1 Digital Refreshed Display (Option 2), Location of Components

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
U1	Integrated Circuit	1	MM74HCT245N	27014	
U2	Integrated Circuit	1	MM74C175N	27014	
U3	Integrated Circuit	1	SN74LS02N	01295	
U4	Integrated Circuit	1	SN74LS139N	01295	
U5	Integrated Circuit	1	SN74LS161AN	01295	
U6	Not Used				
U7	Integrated Circuit	3	SN74ALS157N	01295	
U8	Same as U7				
U9	Same as U7				
U10	Integrated Circuit	2	P2114AL4	34649	
U11	Same as U10				
U12	Integrated Circuit	1	CD4040BE	02735	
U13	Integrated Circuit	2	AD7524JN	24355	
U14	Same as U13				
U15	Integrated Circuit	1	SN74LS123N	01295	
U16	Integrated Circuit	1	MC1458N	18324	
U17	Integrated Circuit	1	DG302CJ	17856	